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(54) **Title**: ON-SILICON LOW-LOSS TRANSMISSION LINES AND MICROWAVE COMPONENTS

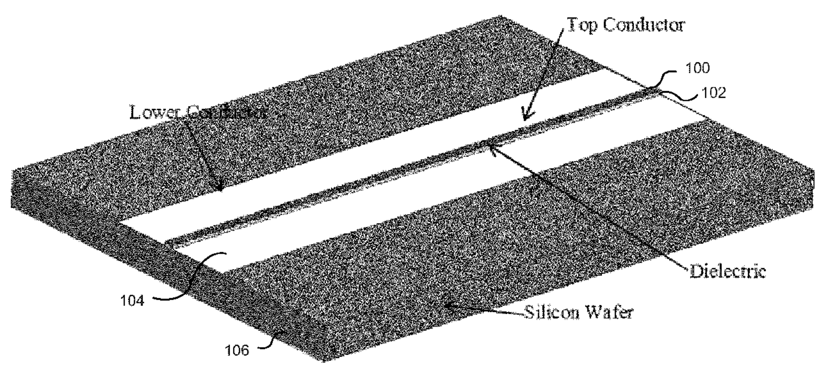


Figure 1

(57) **Abstract**: A method of passive microwave component construction is disclosed. A metal conductor is sputtered on a silicon wafer to form a ground plane. A photoresist dielectric film is applied on top of the metal conductor. Photolithography is performed to construct a substrate structure using the photoresist. A metal conductor is sputtered through mask onto the substrate structure to form a top conductor. A development process is performed to remove unexposed photoresist leaving exposed photoresist between the top conduct and ground plane. A passive microwave component is also disclosed having a metal conductor on a silicon wafer providing a ground plane. A substrate deposited on the metal conductor formed during photolithography using a photoresist; and a top metal conduct on the narrow film substrate.

WO 2015/149172 A1

ON-SILICON LOW-LOSS TRANSMISSION LINES AND MICROWAVE COMPONENTS

CROSS-REFERNCE TO RELATED APPLICATION

This application claims priority from United States Provisional Patent Application No. 61/972,711 filed March 31, 2014 the entirety of which is incorporated by reference for all purposes.

TECHNICAL FIELD

[0001] The present disclosure relates to passive microwave components and in particular to on silicon transmission lines and antennas.

BACKGROUND

[0002] The integration of passive microwave components such as transmission lines, inductors, capacitors, filters, and antennas is extremely important as they account for more than 75% of circuit elements in wireless transceivers. However, the low-resistivity (high-loss) silicon, which is a standard substrate for most radio frequency integrated circuits, has hindered quality of integrated passive microwave components.

[0003] Accordingly, there is a need for improved integrated passive microwave components.

SUMMARY

[0004] In accordance with an aspect of the present disclosure there is provided a method of passive microwave component construction. The method comprising sputtering metal conductor on a silicon wafer to form a ground plane; applying a photoresist dielectric film on top of the metal conductor; performing photolithography to construct a substrate structure using the photoresist; sputter a metal conductor through mask onto the substrate structure to form a top conductor; and performing a development process to remove unexposed photoresist leaving exposed photoresist between the top conduct and ground plane.

[0005] In accordance with another aspect the metal conducts is a conductive metal such as copper or aluminum.

[0006] In accordance with another aspect the photoresist creates a support structure.

[0007] In accordance with another aspect the development process utilizes a propylene glycol monomethyl ether acetate.

[0008] In accordance with another aspect the photoresist is selected from the group consisting of: SU-8 ($\varepsilon r = 3.2$), Polyimide ($\varepsilon r = 3.5$), benzocyclobutene or BCB ($\varepsilon r = 2.7$), and Silicon dioxide ($\varepsilon r = 3.9$).

[0009] In accordance with another aspect the photoresist is applied at approximately 25 μm thick film of a low permittivity polymer.

[0010] In accordance with another aspect the photoresist has a dielectric constant of 3.2.

[0011] In accordance with another aspect a transmission line width is created by the top conductor.

[0012] In accordance with another aspect the a characteristic impedance of a narrow film transmission line geometry is 50 Ω with w = 70 μm.

[0013] In accordance with another aspect the substrate width forms a narrow film transmission line is truncated to fit the 50 Ω microstrip line width.

[0014] In accordance with another aspect the dielectric posts are created by the substrate.

[0015] In accordance with another aspect the dielectric posts are periodically patterned along a transmission line.

[0016] In accordance with another aspect the posts are approximately 25 μm thick dielectric posts with dimensions of 100 μm × 70 μm.

[0017] In accordance with another aspect the posts are 200 μm far from each other.

[0018] In accordance with another aspect the posts are varied along a line width by approximately 0.3 mm.

[0019] In accordance with another aspect the method is for manufacturing a stepped impedance filter.

[0020] In accordance with another aspect the size of the posts are varied in size.

[0021] In accordance with another aspect the method is for manufacturing a microstrip patch antenna.

[0022] In accordance with another aspect the antenna is implemented on a 25 μm-thick dielectric film with dielectric constant of 3 and loss tangent of 0.03.

[0023] In accordance with another aspect the dielectric film is truncated to fit or be slightly smaller than the top conductor.

[0024] In accordance with another aspect narrow line posts are used in the structure where posts are space along the width of the top conductor and posts are spaced along transmission line.

[0025] In accordance with another aspect the structure is a silicon antenna using 25 μm tall narrow line posts.

[0026] In accordance with another aspect the structure is a microstrip patch antenna using square posts.

[0027] In accordance with another aspect the method further comprising repeatedly applying multiple layers and top conductive layers.

[0028] In accordance with another aspect further comprising removing the photoresist creates one or more air gaps between the top conduct and the ground plane.

[0029] In accordance with yet another aspect of the present disclosure there is provided a passive microwave component comprising a metal conductor on a silicon wafer providing a ground plane; a substrate deposited on the metal conductor formed during photolithography using a photoresist; and a top metal conduct on the narrow film substrate.

[0030] In accordance with yet another aspect the metal conducts is a conductive metal such as copper or aluminum.

[0031] In accordance with yet another aspect the photoresist creates a support structure.

[0032] In accordance with yet another aspect the development process utilizes a propylene glycol monomethyl ether acetate.

[0033] In accordance with yet another aspect the photoresist is selected from the group consisting of: SU-8 ($\varepsilon r = 3.2$), Polyimide ($\varepsilon r = 3.5$), benzocyclobutene or BCB ($\varepsilon r = 2.7$), and Silicon dioxide ($\varepsilon r = 3.9$).

[0034] In accordance with yet another aspect the photoresist is applied at approximately 25 μm thick film of a low permittivity polymer.

[0035] In accordance with yet another aspect the photoresist has a dielectric constant of 3.2.

[0036] In accordance with yet another aspect a transmission line width is created by the top conductor.

[0037] In accordance with yet another aspect a characteristic impedance of a narrow film transmission line geometry is 50 Ω with $w = 70$ μm.

[0038] In accordance with yet another aspect the substrate width forms a narrow film transmission line is truncated to fit the 50 Ω microstrip line width.

[0039] In accordance with yet another aspect dielectric posts are created by the substrate.

[0040] In accordance with yet another aspect dielectric posts are periodically patterned along a transmission line.

[0041] In accordance with yet another aspect the posts are approximately 25 μm thick dielectric posts with dimensions of 100 μm × 70 μm.

[0042] In accordance with yet another aspect the posts are 200 μm far from each other.

[0043] In accordance with yet another aspect the posts are varied along a line width by approximately 0.3 mm.

[0044] In accordance with yet another aspect the passive microwave component is for manufacturing a stepped impedance filter.

[0045] In accordance with yet another aspect the size of the posts are varied in size.

[0046] In accordance with yet another aspect the passive microwave component is a microstrip patch antenna.

[0047] In accordance with yet another aspect the antenna is implemented on a 25 μm-thick dielectric film with dielectric constant of 3 and loss tangent of 0.03.

[0048] In accordance with yet another aspect the dielectric film is truncated to fit or be slightly smaller than the top conductor.

[0049] In accordance with yet another aspect narrow line posts are used in the structure where posts are space along the width of the top conductor and posts are spaced along transmission line.

[0050] In accordance with yet another aspect the structure is a silicon antenna using 25 μm tall narrow line posts.

[0051] In accordance with yet another aspect the structure is a microstrip patch antenna using square posts.

[0052] In accordance with yet another aspect the structure comprises multiple substrate and conductive layers.

[0053] In accordance with yet another aspect one or more air gaps are created between the top conduct and the ground plane.

BRIEF DESCRIPTION OF THE DRAWINGS

[0054] Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the appended drawings, in which:

Figure 1 shows a narrow film on-silicon microstrip line;

Figure 2 shows a graph of characteristic impedance of the narrow film transmission line;

Figure 3 shows a graph of attenuation of the proposed transmission lines compared with the attenuation of conventional thin film microstrip line;

Figure 4 shows a representation of conventional on-silicon thin film microstrip line;

Figure 5 shows representation of on-silicon transmission line using 25 μm tall posts with dimensions of 100 μm by 70 μm where the distance between two adjacent posts is 200 μm;

Figure 6 shows representation of on-silicon stepped line using 25 μm tall posts;

Figure 7 shows representation of on-silicon stepped-impedance filter;

Figure 8 shows on-silicon conventional microstrip patch antenna;

Figure 9 shows graphs of (a) reflection coefficient and (b) gain of the on-silicon conventional patch antenna using 25 μm tall films;

Figure 10 shows radiation patterns of the on-silicon conventional antenna using 25 μm tall films at 60 GHz where (a) is the E-plane; (b) is the H-plane where the cross-polarization levels are less than -30 dB and therefore are not shown in the graphs;

Figure 11 shows on-silicon microstrip patch antenna using narrow and truncated films;

Figure 12 graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall narrow and truncated films;

Figure 13 shows radiation patterns of the on-silicon antenna using 25 μm tall narrow and truncated films where (a) is the E-plane; (b) is the H-plane where cross-polarization levels are less than -30 dB and therefore are not shown in the graphs;

Figure 14 shows on-silicon microstrip patch antenna using narrow line posts;

Figure 15 shows graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall narrow line posts;

Figure 16 shows radiation patterns of the on-silicon antenna using 25 μm tall narrow line posts where (a) is the E-plane; (b) is the H-plane where the cross-polarization levels are less than -30 dB and therefore are not shown in the graphs;

Figure 17 shows on-silicon microstrip patch antenna using square posts;

Figure 18 graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall square posts;

Figure 19 shows radiation patterns of the on-silicon antenna using 25 μm tall square posts where (a) is the E-plane; (b) is the H-plane where the cross-polarization levels are less than -20 dB and are shown in dot-dash lines;

Figure 20 shows on-silicon microstrip patch antenna using a multi-layer design for the top conductor;

Figure 21 shows a graph of gain of the on-silicon microstrip patch antenna using a multi-layer design for the top conductor;

Figure 22 illustrates a fabrication process; and

Figure 23 shows a method of fabricating a passive microwave component.

[0055] It will be noted that throughout the appended drawings, like features are identified by like reference numerals.

DETAILED DESCRIPTION

[0056] Embodiments are described below, by way of example only, with reference to Figs. 1-23.

[0057] A simple but very efficient approach is described to exploit dielectric narrow films and dielectric posts in realization of highly-efficient on-silicon microwave devices. In this approach the narrow thin film or dielectric posts of low-permittivity (usually polymers or photoresists) is applied on silicon substrate to achieve antennas and microwave devices.

[0058] High-performance on-silicon transmission lines, microwave components, and antennas are described and a method of manufacture. Narrow and thin dielectric substrate films with dimensions similar or smaller than the top conductors are used to increase the efficiency of components. In another design, the narrow film is truncated to make dielectric posts and further improve performance of the components. It is shown that multi-layer design for the top conductor can further increase the efficiency of the components. A microfabrication method is presented to realize these structures. The improvements introduced by these simple changes in the circuit are considerable, especially at millimetre wave frequencies where the losses associated with the substrate and conductors are significant. These simple designs not only introduce considerable improvements, but also can facilitate the integration and make the circuit more compact.

[0059] Fig. 1 shows an example of on-silicon transmission line 100 implemented on a narrow dielectric thin film layer 102. The lower metal conductor 104 acts as the ground plane on the silicon wafer 106, the narrow dielectric thin film 102 coated on the ground plane 104 is the substrate, and the upper metal conductor is used as the signal line. The characteristic impedance of this transmission line is shown in the graph in Fig. 2 as a function of transmission line width (w) when a 25 μm thick film of a low permittivity polymer with dielectric constant of 3.2 is considered. A wide range of characteristic impedances (10-100 Ω) is possible within a reasonable range of width (25-470 μm), facilitating implementation of passive microwave components. In specific, the characteristic impedance of the narrow film transmission line geometry is 50 Ω with w = 70 μm. Most of the materials compatible with microfabrication processes such as SU-8 (εr = 3.2), Polyimide (εr = 3.5), benzocyclobutene or BCB (εr = 2.7), and Silicon dioxide (εr = 3.9) have relatively similar low dielectric constants and therefore should achieve similar results.

[0060] The attenuation for the narrow film transmission line and the conventional thin film microstrip line (the structure 400 is shown in Fig. 4) are shown in graph in Fig. 3. In both cases, the substrate is 25 μm thick with dielectric constant of 3.2 and loss tangent of 0.015. The substrate width for the proposed narrow film transmission line is truncated to fit the 50 Ω microstrip line width (i.e., w = 70 μm). This line presents attenuation of 0.11 dB/mm at 30 GHz, which is 0.025 dB/mm (i.e., ~20%) less than that of the conventional thin film microstrip line. It should be noted that this improvement is achieved based on a change in structural design.

[0061] To decrease the attenuation associated with the on-silicon transmission line, another novel structure is shown in Fig. 5. The structure 500 consists of dielectric posts 502 (instead of narrow film) that are periodically patterned along the line 504 below transmission line 100. Depending on the dielectric material, width of the transmission line 100, thickness of the film, and other parameters, posts with different dimensions can be used. In this example, 25 μm thick dielectric posts with dimensions of 100 μm × 70 μm are considered. The posts 502 are 200 μm far from each other and supposed to have dielectric constant of 3.2 and loss tangent of 0.015 (similar to the previous case). The attenuation for this transmission line is also illustrated in Fig. 3. The improvement is significant, showing that the attenuation is less than 0.08 dB/mm at 30 GHz. This is 0.055 dB/mm less than that of the conventional thin film microstrip line, and 0.03 dB/mm less than that of the narrow film transmission line, corresponding to over 40% and 27% improvements.

[0062] Referring to Fig. 6, a slight nonlinear variation in attenuation is realized over the frequency band for the transmission line with dielectric posts 604. This is due to a variation in characteristic impedance of the line and it can be controlled by changing the transmission line width 602a and 602b along the transmission line path 602. An example is shown in Fig. 6 where the line width is periodically varied by 0.3 mm in structure 600. The result for this structure is also shown in Fig. 3. This can be also utilized to achieve stepped impedance filters when the difference between impedances is increased and the line 702 length 702a and 702b is varied as in structure 700 shown in Fig. 7 with the size of the respective posts 704a and 704b.

[0063] Using the same methodology other microwave passive components can be designed and implemented on the low-resistivity silicon wafer. For instance, microstrip patch antennas are designed at 60 GHz and their performance is compared with the conventional on-silicon patch antenna. All antennas are implemented on a 25 μm-thick dielectric film with dielectric constant of 3 and loss tangent of 0.03.

[0064] Fig. 8 shows the structure 800 of conventional on-silicon patch antenna 802 which is fed using microstrip line 804. The output results are shown in Figs. 9 and 10. Broadside radiation patterns and -2.5 dBi gain are achieved. Figure 9 shows graphs of (a) reflection coefficient and (b) gain of the on-silicon conventional patch antenna using 25 μm tall films. Figure 10: shows radiation patterns of the on-silicon conventional antenna using 25 μm tall films at 60 GHz. (a) E-plane; (b) H-plane where the cross-polarization levels are less than -30 dB and therefore are not shown in the graphs.

[0065] As the dielectric film is truncated to fit (or be slightly smaller than) the top conductor, significant improvements are resulted. In the example shown in Fig. 11, the top conductor 1102 of structure 1100 is extended 150 μm beyond the dielectric thin film 1104. Figs. 12 and 13 show that broadside radiation patterns are achieved, and the antenna gain is now increased to -1 dBi. This is 1.5 dB larger than that of the conventional patch antenna (previous case). Therefore, with just a simple change in the configuration, considerable increase in the antenna gain is achieved. Figure 12 graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall narrow and truncated films. Figure 13 shows radiation patterns of the on-silicon antenna using 25 μm tall narrow and truncated films where (a) is the

E-plane; (b) is the H-plane where cross-polarization levels are less than -30 dB and therefore are not shown in the graphs;

[0066] Fig. 14 shows another configuration in which narrow line posts are used in the structure 1400 where posts 1404 are space along the width of the top conductor 1402 and posts 1406 are spaced along transmission line 1408. The results in Figs. 15 and 16 show that improved characteristics are achieved and the antenna gain is about 2 dBi at 60 GHz. Figure 15 shows graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall narrow line posts. Figure 16 shows radiation patterns of the on-silicon antenna using 25 μm tall narrow line posts where (a) is the E-plane; (b) is the H-plane where the cross-polarization levels are less than -30 dB and therefore are not shown in the graphs

[0067] Figs. 17, 18, and 19 show the structure 1700 and the results for the on-silicon microstrip patch antenna 1702 using square posts 1704. The antenna gain is 4.5 dBi which is 7 dB larger than that of the conventional patch antenna (first antenna example). Similar procedure can be followed to design other types of passive microwave components with improved performance. Figure 18 graphs of (a) reflection coefficient and (b) gain of the on-silicon antenna using 25 μm tall square posts. Figure 19 shows radiation patterns of the on-silicon antenna using 25 μm tall square posts where (a) is the E-plane; (b) is the H-plane where the cross-polarization levels are less than -20 dB and are shown in dot-dash lines;

[0068] In all of the above designs, the top conductor can be deposited in multi thin layers instead of one thick layer, as shown in Fig. 20. The dielectric post 2002, has a first metallic layer 2004, a first intermediary dielectric layer 2006, a second metallic layer 2008, a second intermediary dielectric layer 2010 and a third metallic layer 2012. This technique will further increase the efficiency of the components. For example for the antenna in Fig. 17, a three layer design increases the antenna gain to over 5 dBi. About 2% change in the frequency of peak gain is however detected which can be corrected by slightly changing the antenna dimensions. Figure 21 shows a graph 2100 of gain of the on-silicon microstrip patch antenna using a multi-layer design for the top conductor.

[0069] Different procedures can be used to fabricate the proposed structures. A simplified microfabrication method is provided here and shown in Fig. 22 and referring to method 2300 of Fig. 23. The process is started by first sputtering 2 μm-thick metal with good conductivity can be acceptable such as aluminium or copper 2204 on a low resistivity silicon wafer (as the ground plane) 2202 (2302). Then photoresist (e.g., SU-8) 2206 is spin coated on top of the Aluminum (2304). The photolithography 2250 is then applied to construct the narrow film substrates or dielectric posts 2208 (2306). At the end, 2 μm thick Aluminum is sputtered 2210 through a mask on the film to construct the signal line and development process is followed to come up with the final structure (2308). In this case that we use a negative photoresist (i.e., SU-8), the unexposed photoresist is removed by a development process using a chemical solution (for example Propylene glycol monomethyl ether acetate (PGMEA) (2310) leaving behind support dielectric structures and spaces 2207 between posts 2208. In case of the multi-layer design, the sputtering in the last step must be repeated several times but much thinner layers must be deposited. Figure 22(f) shows a front view of the structure and 22(g) shows a side view air gaps 2207 created by the removal of the photoresist in the development process.

[0070] Although the structures are proposed for on-silicon applications, the method is efficient for other types of substrates. There are several advantages when these structures are compared with the conventional thin film structures. The dielectric loss and effective dielectric constant are further reduced since a larger portion of the electromagnetic wave travels through the air not the substrate, increasing efficiency and propagation velocity which is necessary for high-speed circuits. More importantly, making via holes for interconnects in RFICs is facilitated or is not considered necessary to connect through the substrate.

CLAIMS:

1. A method of passive microwave component construction, the method comprising:

   sputtering metal conductor on a silicon wafer to form a ground plane ;

   applying a photoresist dielectric film on top of the metal conductor;

   performing photolithography to construct a substrate structure using the photoresist;

   sputter a metal conductor through mask onto the substrate structure to form a top conductor; and

   performing a development process to remove unexposed photoresist leaving exposed photoresist between the top conduct and ground plane.

2. The method of claim 1 wherein the metal conducts is a conductive metal such as copper or aluminum.

3. The method of claim 1 or 2 wherein the photoresist creates a support structure.

4. The method of any one of claims 1 to 3 wherein the development process utilizes a propylene glycol monomethyl ether acetate.

5. The method of any one of claims 1 to 4 wherein the photoresist is selected from the group consisting of: SU-8 (εr = 3.2), Polyimide (εr = 3.5), benzocyclobutene or BCB (εr = 2.7), and Silicon dioxide (εr = 3.9).

6. The method of any one of claims 1 to 5 wherein the photoresist is applied at approximately 25 μm thick film of a low permittivity polymer.

7. The method of claim 6 wherein the photoresist has a dielectric constant of 3.2.

8. The method of any one of claims 1 to 7 wherein a transmission line width is created by the top conductor.

9. The method of claim 8 wherein the a characteristic impedance of a narrow film transmission line geometry is 50 Ω with w = 70 μm.

10. The method of any one of claims 1 to 9 where in the substrate width forms a narrow film transmission line is truncated to fit the 50 Ω microstrip line width.

11. The method of any one of claims 1 to 10 wherein dielectric posts are created by the substrate.

12. The method of claim 11 wherein the dielectric posts are periodically patterned along a transmission line.

13. The method of claim 12 wherein the posts are approximately 25 μm thick dielectric posts with dimensions of 100 μm × 70 μm.

14. The method of claim 13 wherein the posts are 200 μm far from each other.

15. The method of any one of claims 1 to 14 wherein the posts are varied along a line width by approximately 0.3 mm.

16. The method of any one of claims 1 to 15 wherein the method is for manufacturing a stepped impedance filter.

17. The method of claim 16 wherein the size of the posts are varied in size.

18. The method of any one of claims 1 to 15 wherein the method is for manufacturing a microstrip patch antenna.

19. The method of claim 18 wherein the antenna is implemented on a 25 μm-thick dielectric film with dielectric constant of 3 and loss tangent of 0.03.

20. The method of claim 19 wherein the dielectric film is truncated to fit or be slightly smaller than the top conductor.

21. The method of any one of claims 1 to 20 wherein narrow line posts are used in the structure where posts are space along the width of the top conductor and posts are spaced along transmission line.

22. The method of any one of claims 1 to 20 wherein the structure is a silicon antenna using 25 μm tall narrow line posts.

23. The method of any one of claims 1 to 20 wherein the structure is a microstrip patch antenna using square posts.

24. The method of any one of claims 1 to 20 further comprising repeatedly applying multiple layers and top conductive layers.

25. The method of any one of claims 1 to 24 wherein removing the photoresist creates one or more air gaps between the top conduct and the ground plane.

26. A passive microwave component comprising:

a metal conductor on a silicon wafer providing a ground plane;

a substrate deposited on the metal conductor formed during photolithography using a photoresist; and

a top metal conduct on the narrow film substrate.

27. The passive microwave component of claim 26 wherein the metal conducts is a conductive metal such as copper or aluminum.

28. The passive microwave component of claim 26 or 27 wherein the photoresist creates a support structure.

29. The passive microwave component of any one of claims 26 to 28 wherein the development process utilizes a propylene glycol monomethyl ether acetate.

30. The passive microwave component of any one of claims 26 to 29 wherein the photoresist is selected from the group consisting of: SU-8 ($\varepsilon r = 3.2$), Polyimide ($\varepsilon r = 3.5$), benzocyclobutene or BCB ($\varepsilon r = 2.7$), and Silicon dioxide ($\varepsilon r = 3.9$).

31. The passive microwave component of any one of claims 26 to 30 wherein the photoresist is applied at approximately 25 μm thick film of a low permittivity polymer.

32. The passive microwave component of claim 31 wherein the photoresist has a dielectric constant of 3.2.

33. The passive microwave component of any one of claims 26 to 32 wherein a transmission line width is created by the top conductor.

34. The passive microwave component of claim 33 wherein the a characteristic impedance of a narrow film transmission line geometry is 50 Ω with w = 70 μm.

35. The passive microwave component of any one of claims 26 to 34 where in the substrate width forms a narrow film transmission line is truncated to fit the 50 Ω microstrip line width.

36. The passive microwave component of any one of claims 26 to 35 wherein dielectric posts are created by the substrate.

37. The passive microwave component of claim 36 wherein the dielectric posts are periodically patterned along a transmission line.

38. The passive microwave component of claim 37 wherein the posts are approximately 25 μm thick dielectric posts with dimensions of 100 μm × 70 μm.

39. The passive microwave component of claim 38 wherein the posts are 200 μm far from each other.

40. The passive microwave component of any one of claims 26 to 39 wherein the posts are varied along a line width by approximately 0.3 mm.

41. The passive microwave component of any one of claims 26 to 40 wherein the passive microwave component is a stepped impedance filter.

42. The passive microwave component of claim 41 wherein the size of the posts are varied in size.

43. The passive microwave component of any one of claims 26 to 42 wherein the passive microwave component is a microstrip patch antenna.

44. The passive microwave component of claim 43 wherein the antenna is implemented on a 25 μm-thick dielectric film with dielectric constant of 3 and loss tangent of 0.03.

45. The passive microwave component of claim 44 wherein the dielectric film is truncated to fit or be slightly smaller than the top conductor.

46. The passive microwave component of any one of claims 26 to 45 wherein narrow line posts are used in the structure where posts are space along the width of the top conductor and posts are spaced along transmission line.

47. The passive microwave component of any one of claims 26 to 46 wherein the structure is a silicon antenna using 25 μm tall narrow line posts.

48. The passive microwave component of any one of claims 26 to 46 wherein the structure is a microstrip patch antenna using square posts.

49. The passive microwave component of any one of claims 26 to 48 wherein the structure comprises multiple substrate and conductive layers.

50. The passive microwave component of any one of claims 26 to 49 wherein one or more air gaps are created between the top conduct and the ground plane.

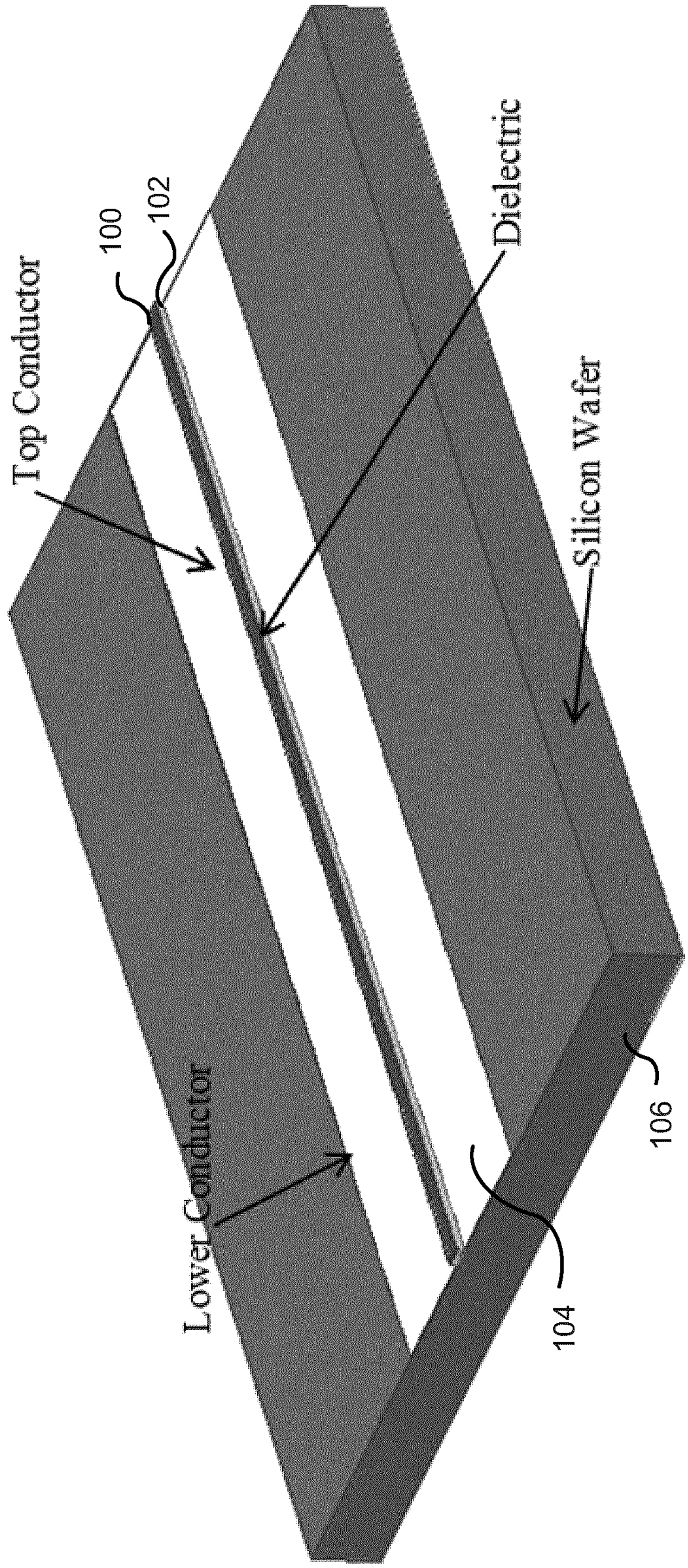

Top Conductor
Dielectric
Silicon Wafer
Lower Conductor
100
102
104
106

Figure 1

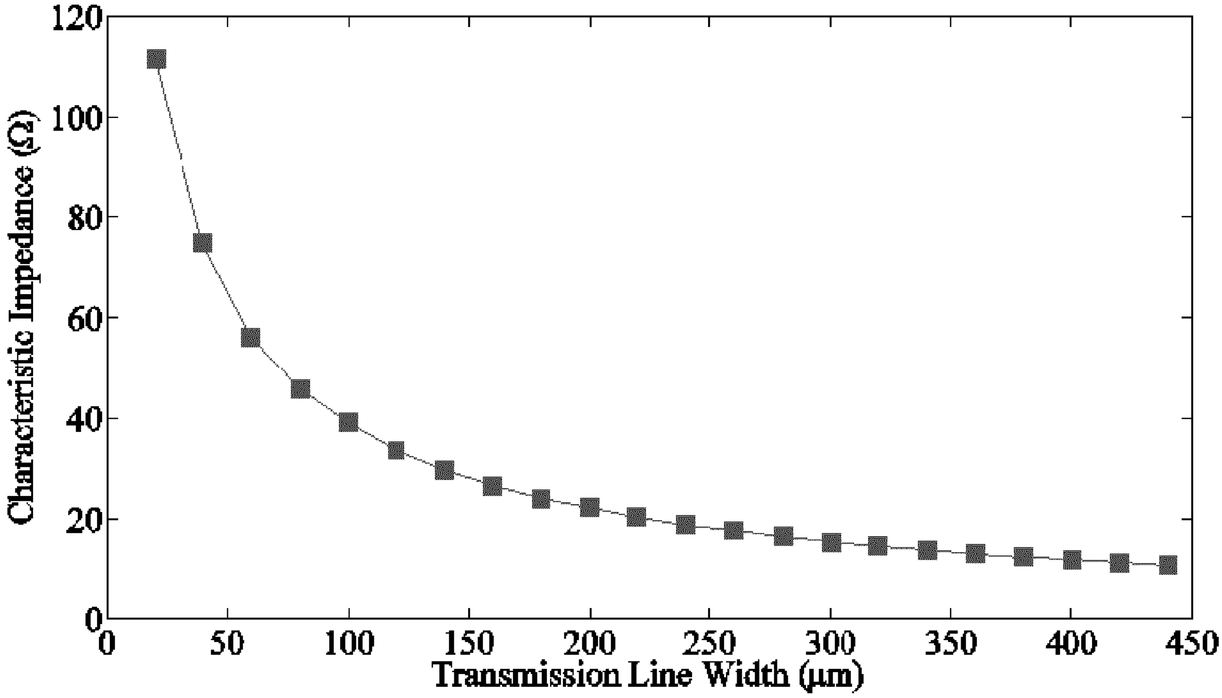

Characteristic Impedance (Ω)
0
20
40
60
80
100
120
0
50
100
150
200
250
300
350
400
450
Transmission Line Width (μm)

Figure 2

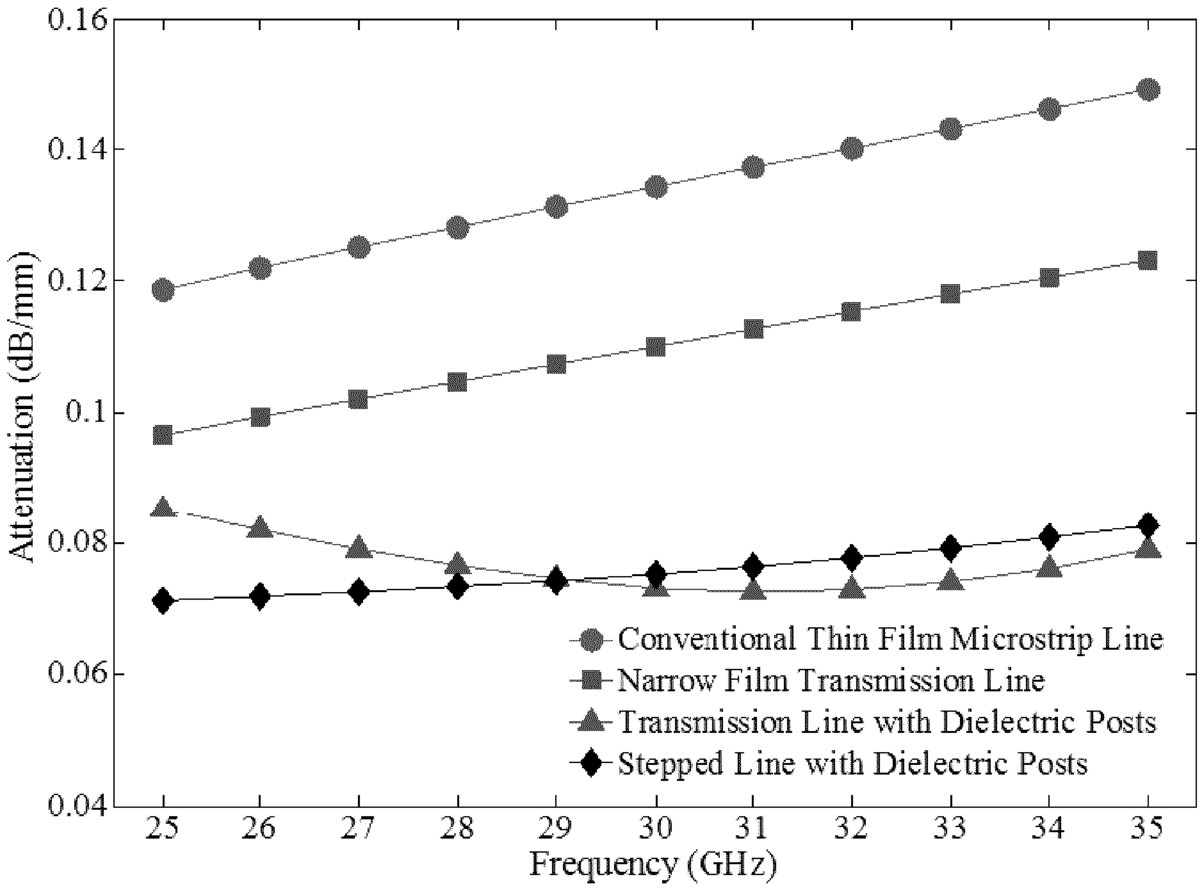

0.16
0.14
0.12
0.1
0.08
0.06
0.04
Attenuation (dB/mm)
25
26
27
28
29
30
31
32
33
34
35
Frequency (GHz)
Conventional Thin Film Microstrip Line
Narrow Film Transmission Line
Transmission Line with Dielectric Posts
Stepped Line with Dielectric Posts

Figure 3

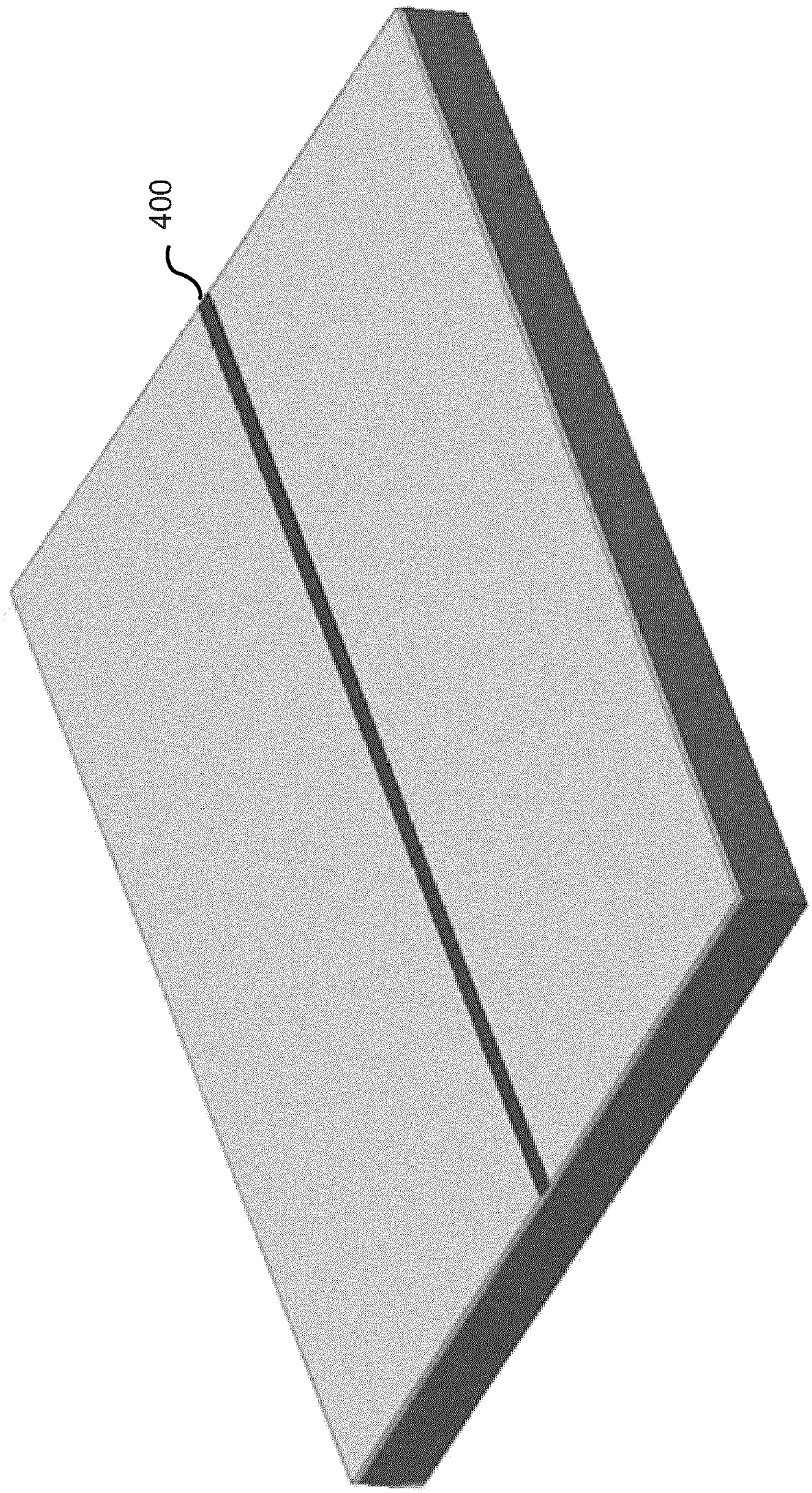


Figure 4

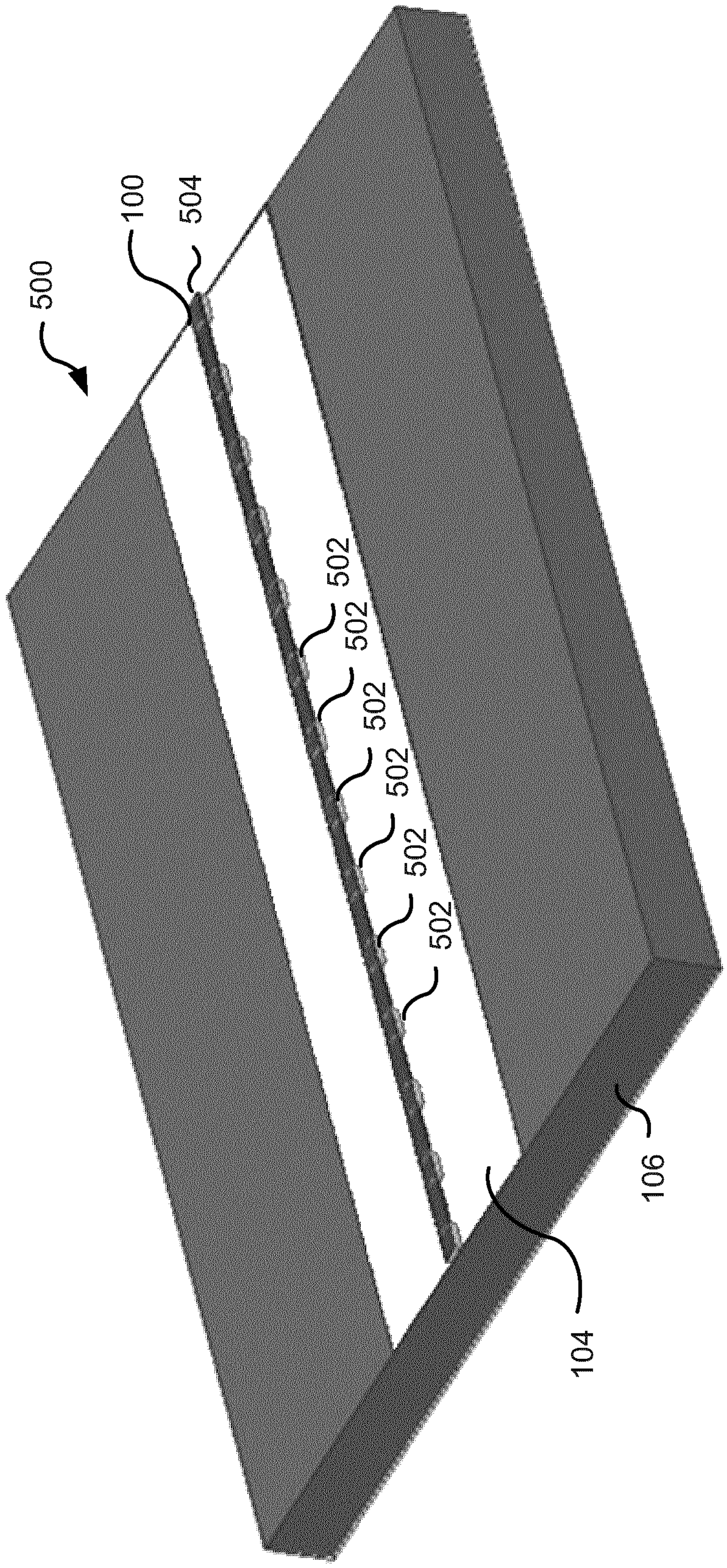


Figure 5

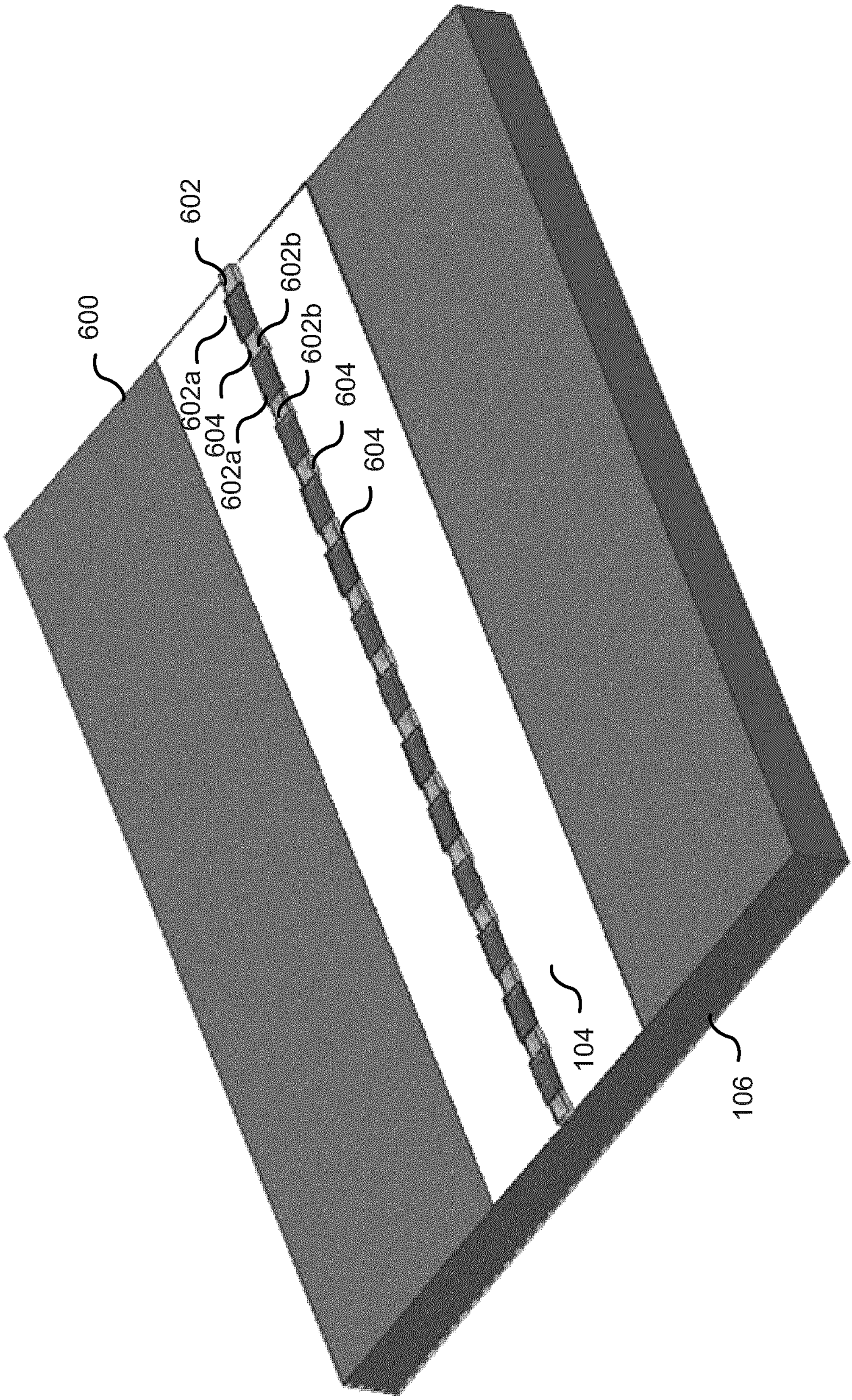


Figure 6

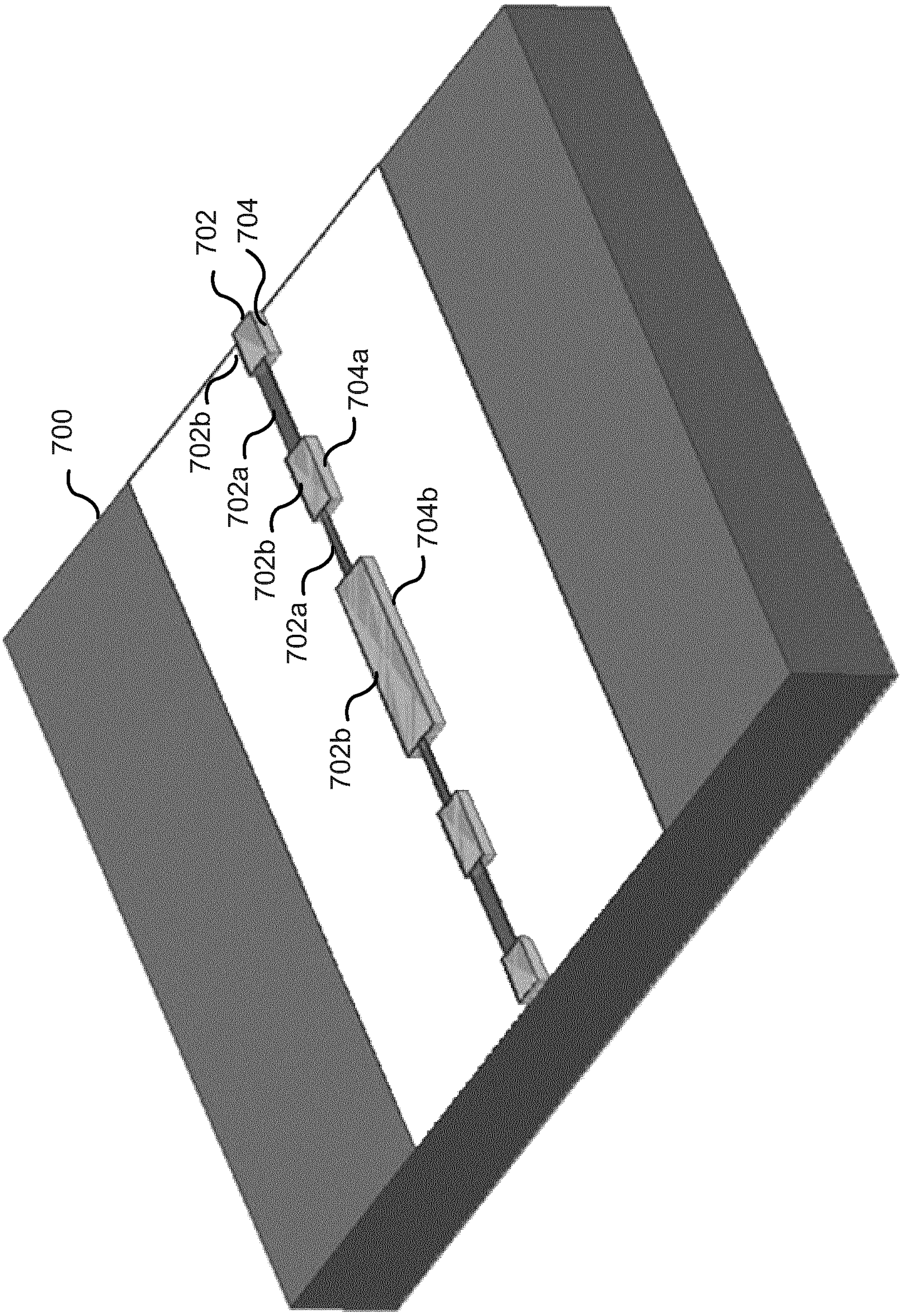


Figure 7

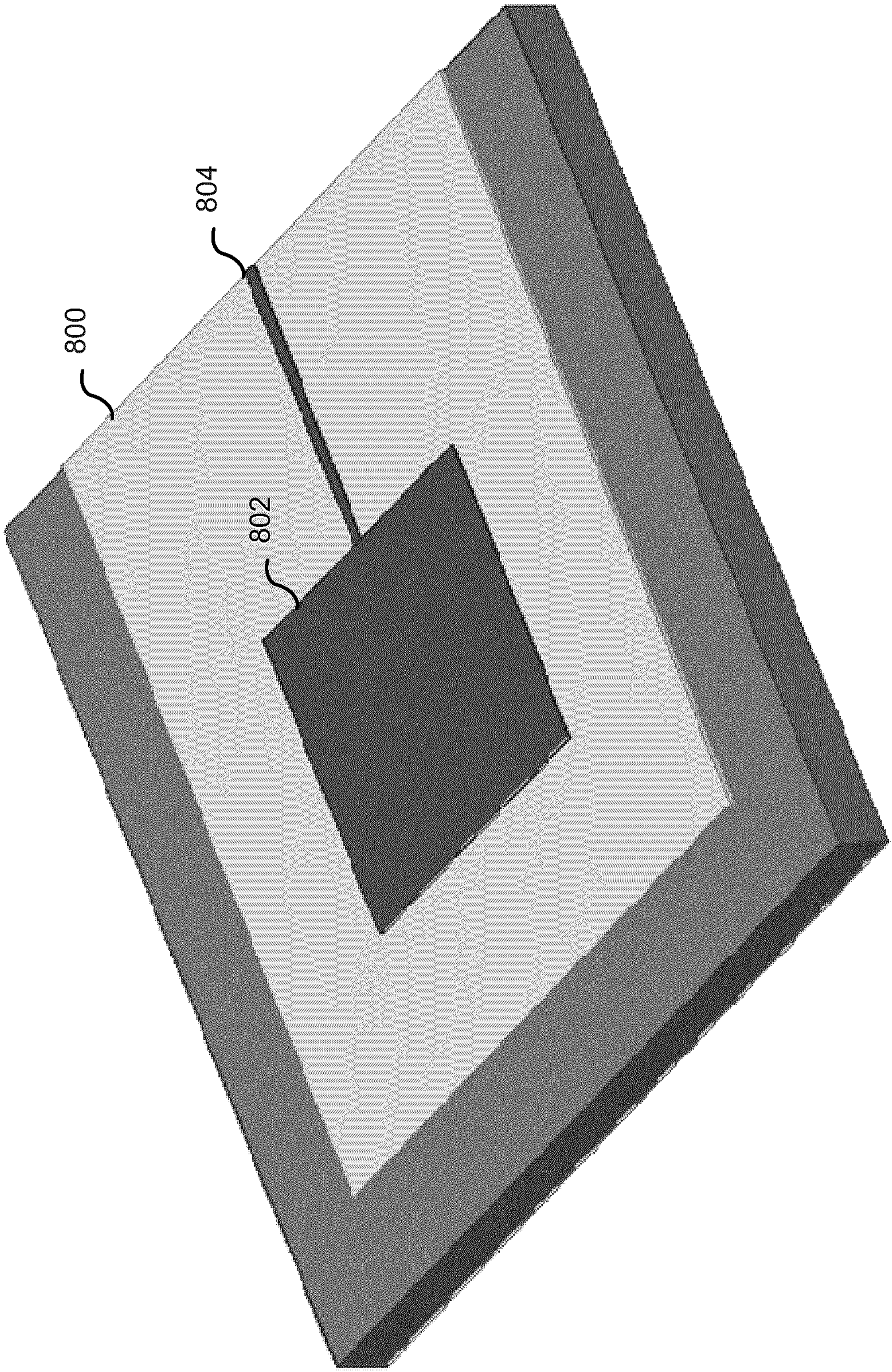
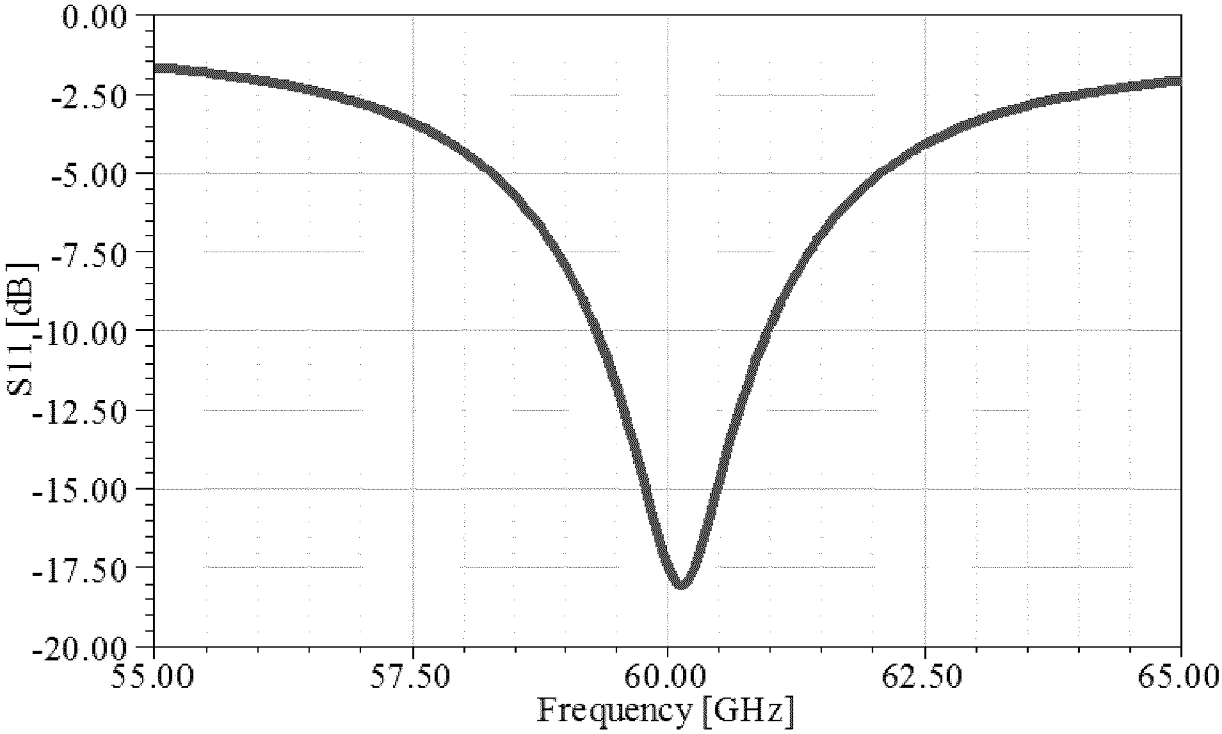
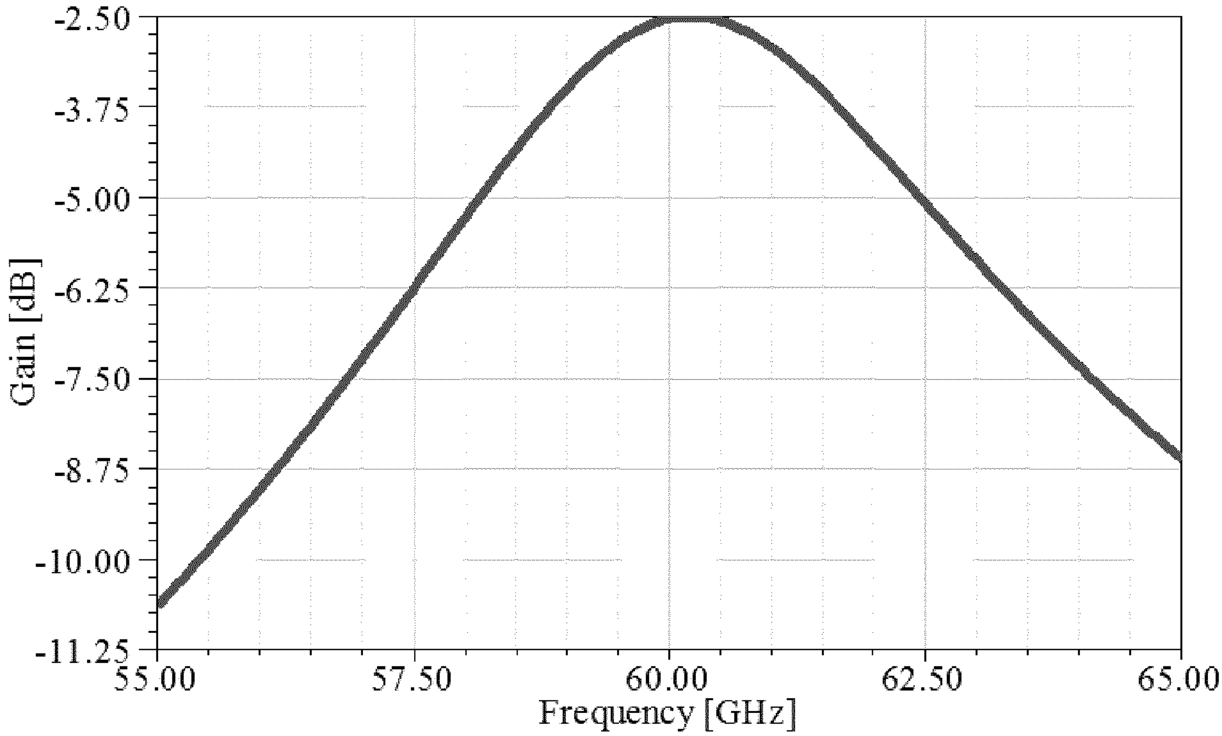


Figure 8


0.00
-2.50
-5.00
-7.50
-10.00
-12.50
-15.00
-17.50
-20.00
S11 [dB]
55.00
57.50
60.00
62.50
65.00
Frequency [GHz]

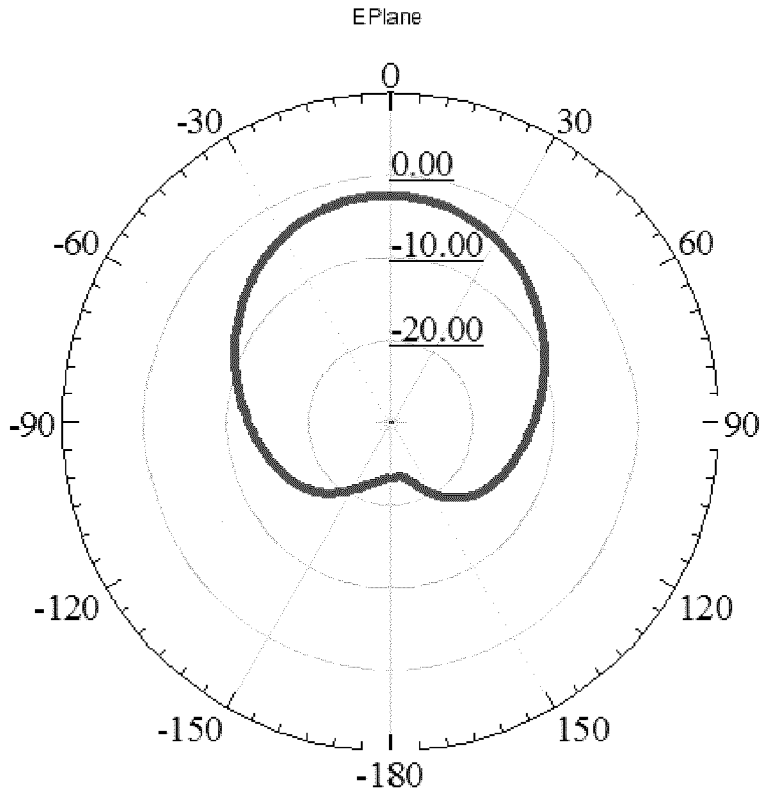
(a)


-2.50
-3.75
-5.00
-6.25
-7.50
-8.75
-10.00
-11.25
Gain [dB]
55.00
57.50
60.00
62.50
65.00
Frequency [GHz]

(b)

Figure 9

(a)


EPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

(b)

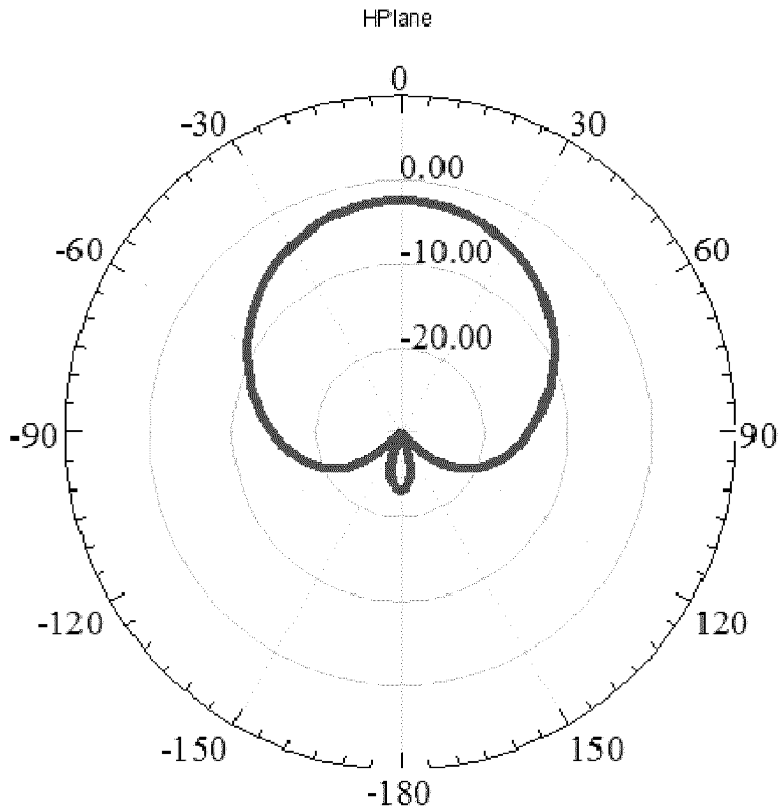

HPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

Figure 10

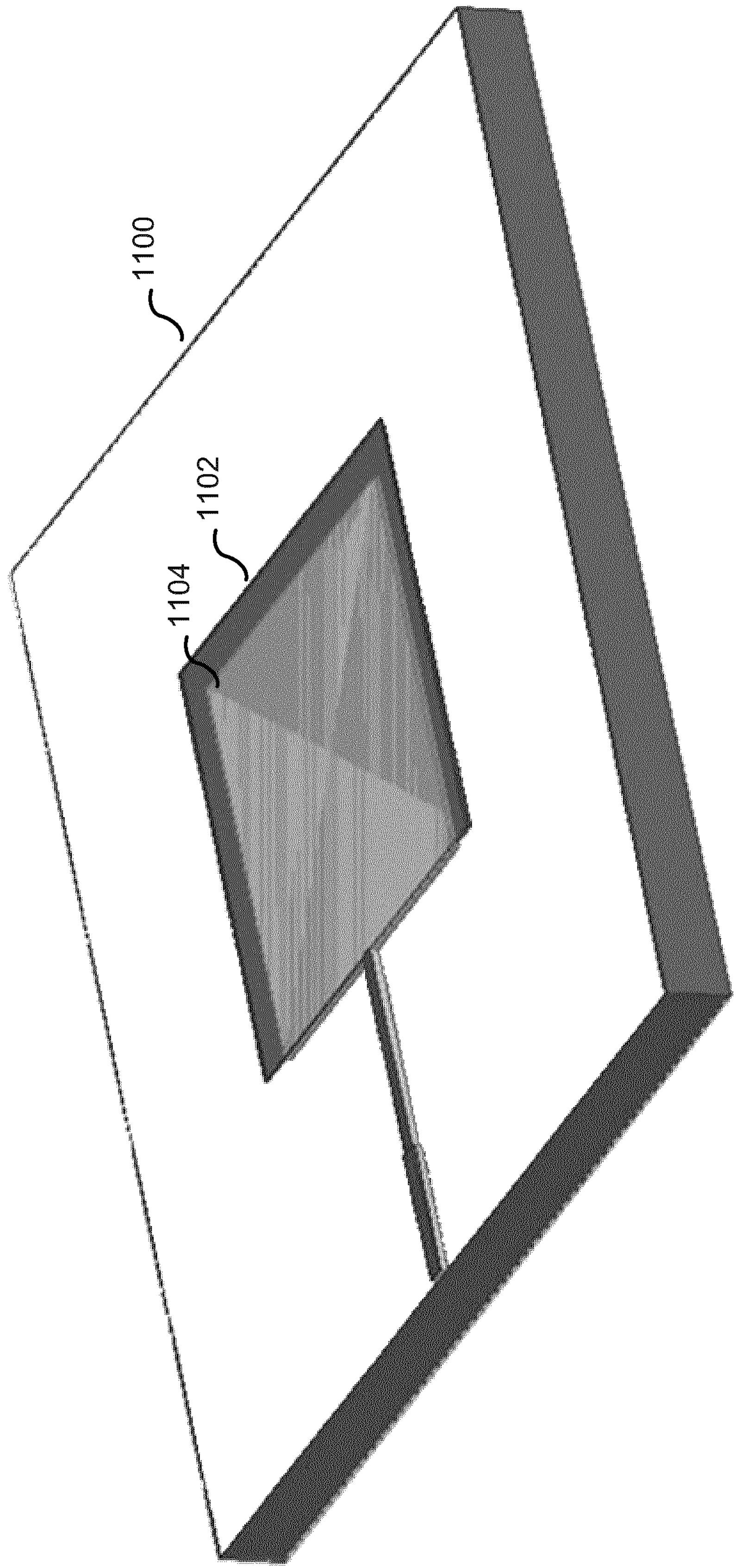
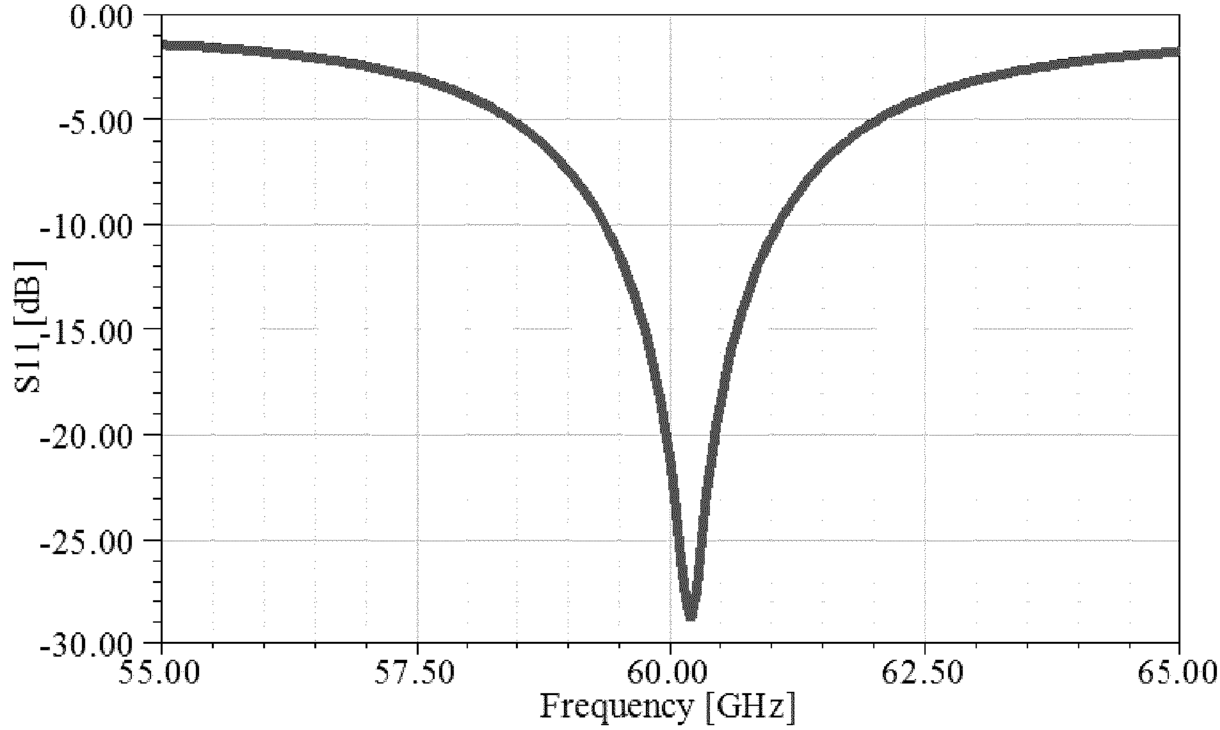
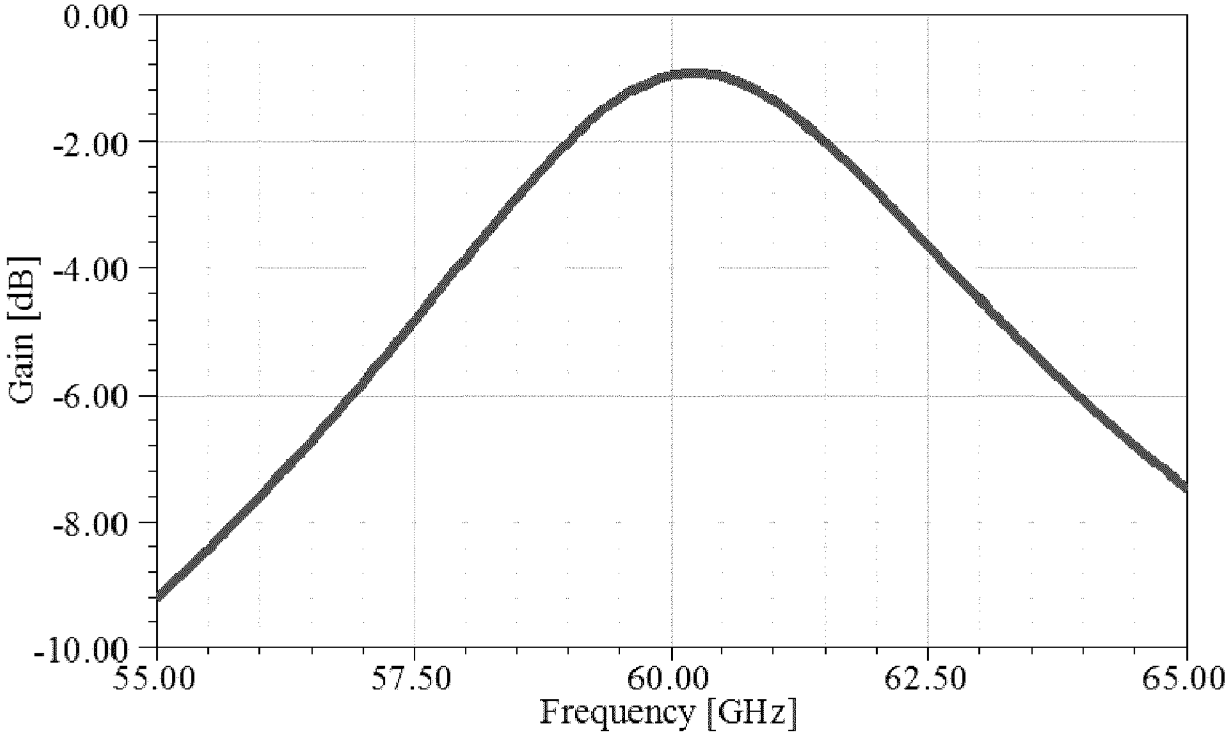


Figure 11


0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
S11 [dB]
55.00
57.50
60.00
62.50
65.00
Frequency [GHz]

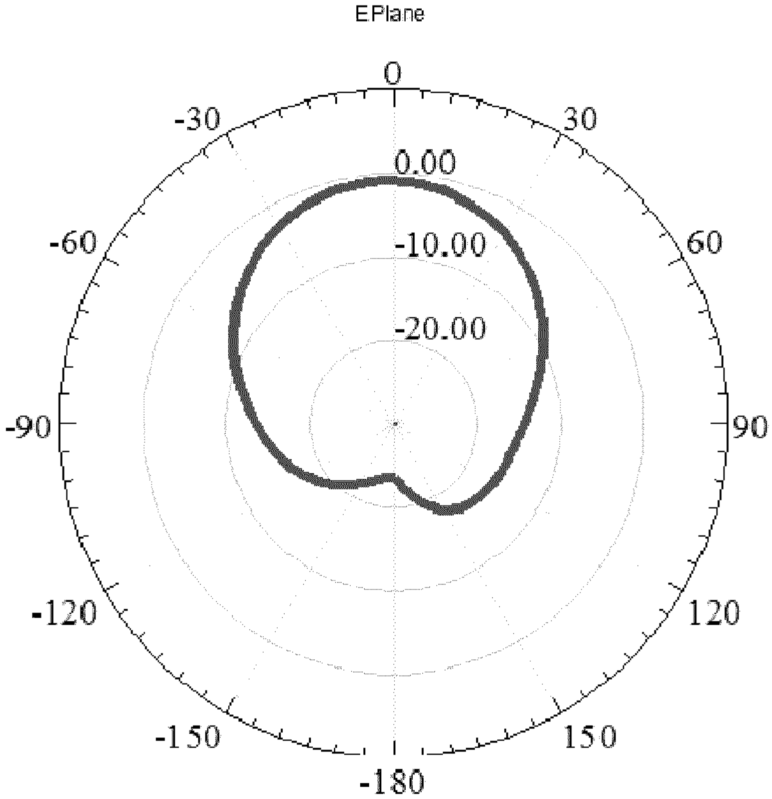
(a)


0.00
-2.00
-4.00
-6.00
-8.00
-10.00
Gain [dB]
55.00
57.50
60.00
62.50
65.00
Frequency [GHz]

(b)

Figure 12

(a)


EPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

(b)

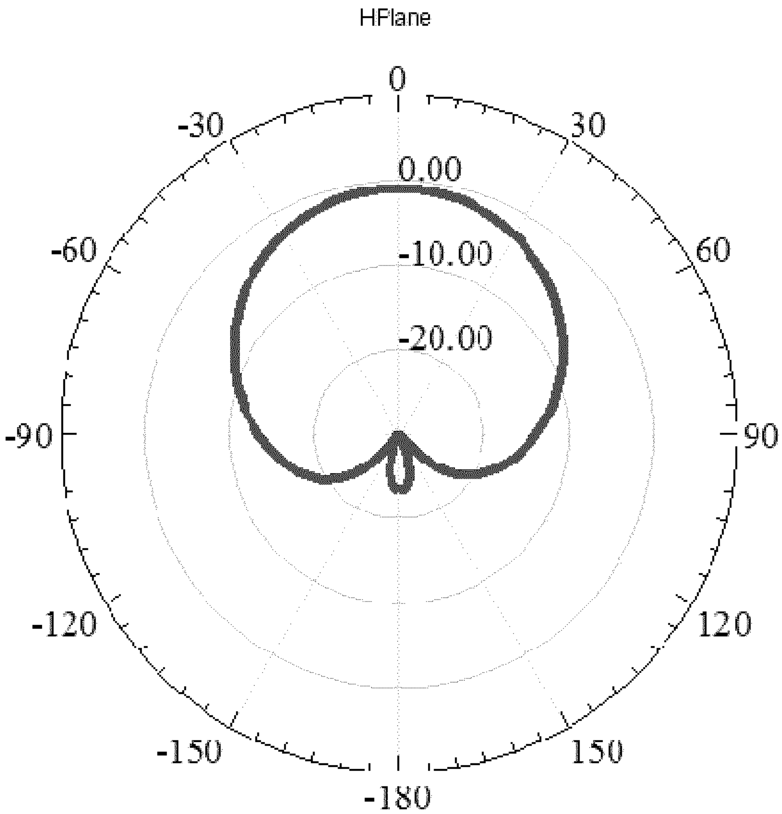

HPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

Figure 13

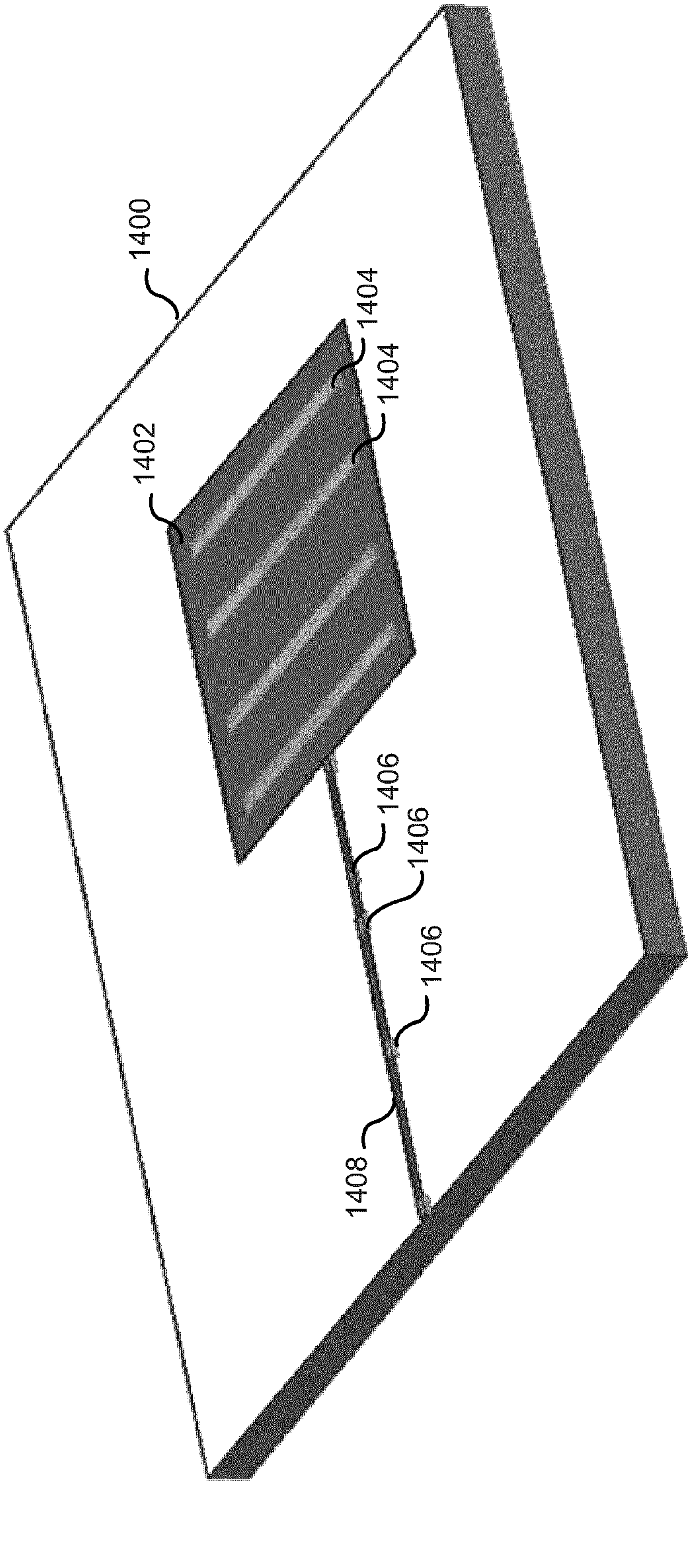
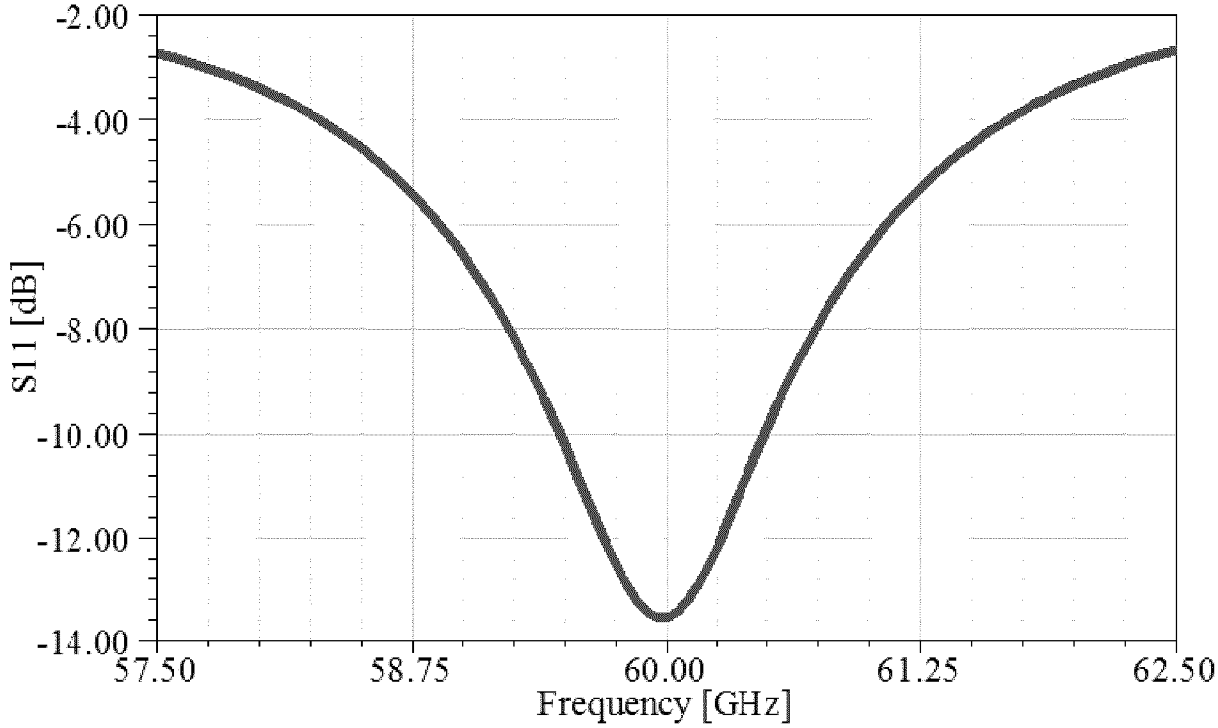
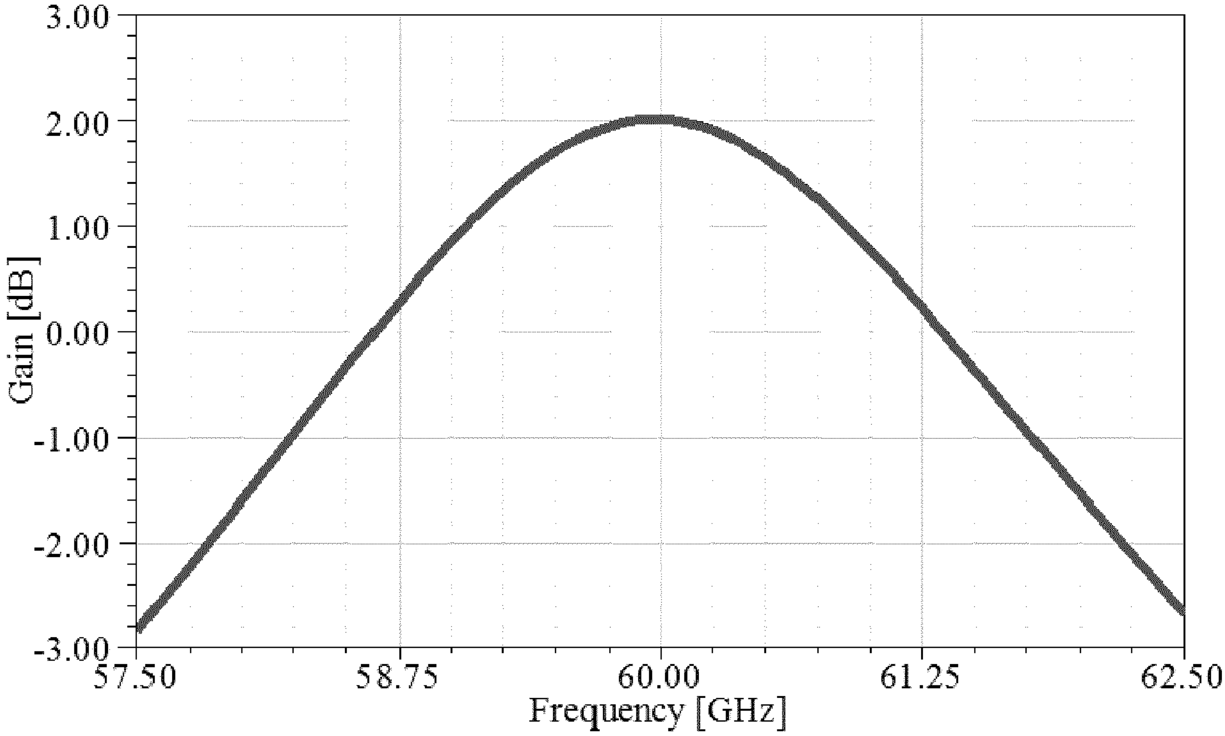


Figure 14


-2.00
-4.00
-6.00
-8.00
-10.00
-12.00
-14.00
S11 [dB]
57.50
58.75
60.00
61.25
62.50
Frequency [GHz]

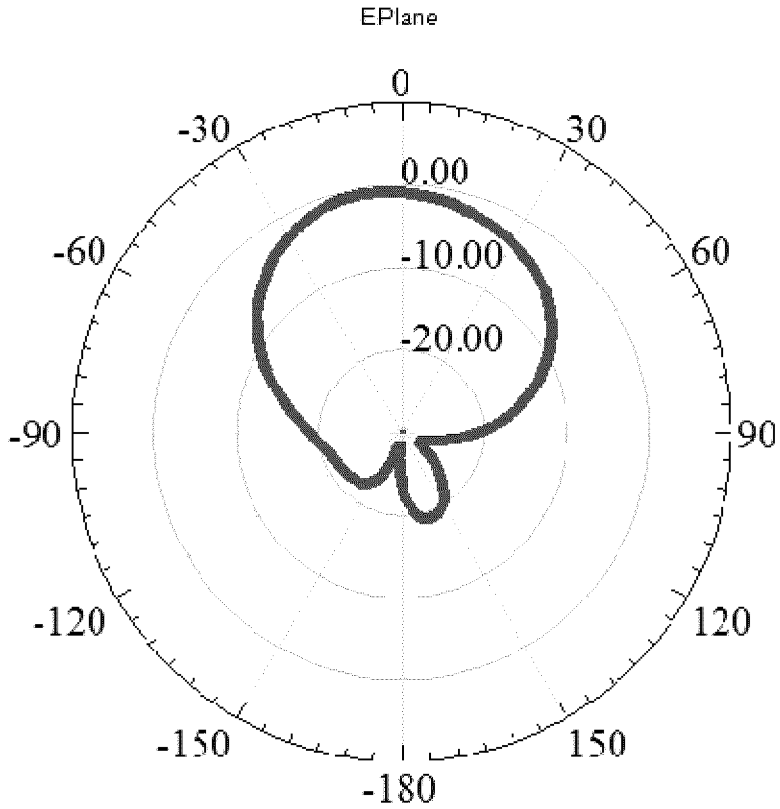
(a)


3.00
2.00
1.00
0.00
-1.00
-2.00
-3.00
Gain [dB]
57.50
58.75
60.00
61.25
62.50
Frequency [GHz]

(b)

Figure 15

(a)


EPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

(b)

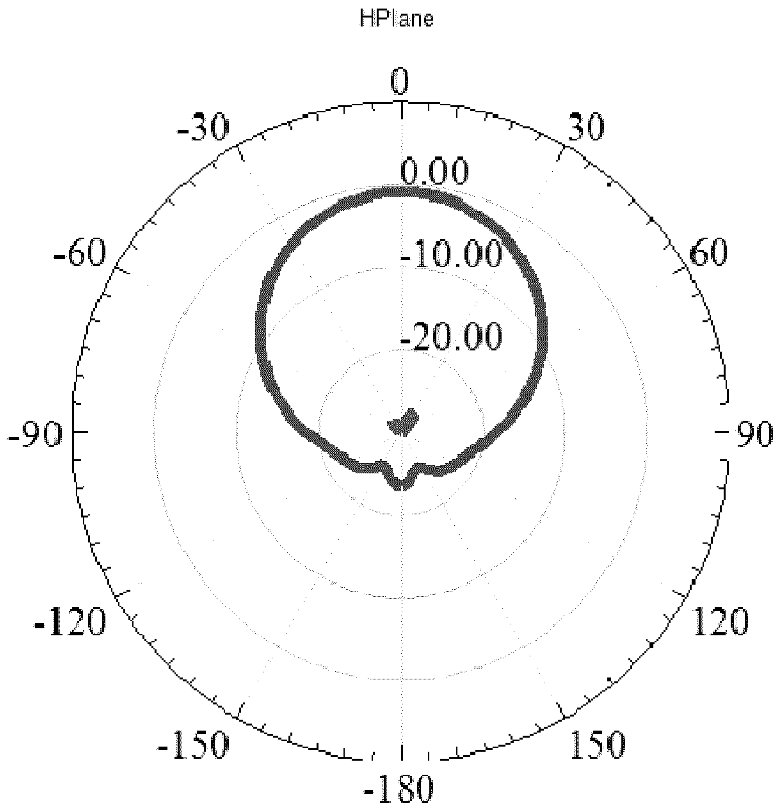

HPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

Figure 16

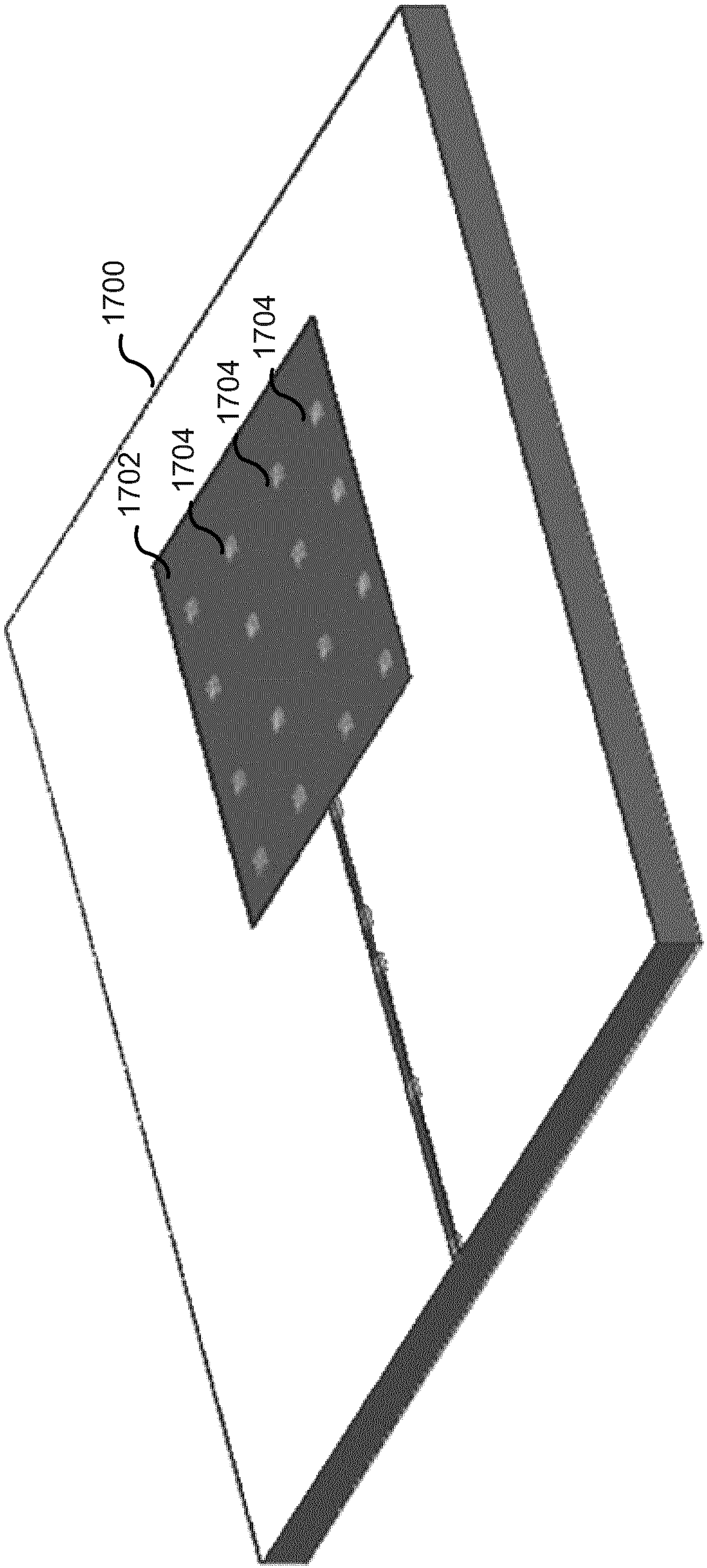
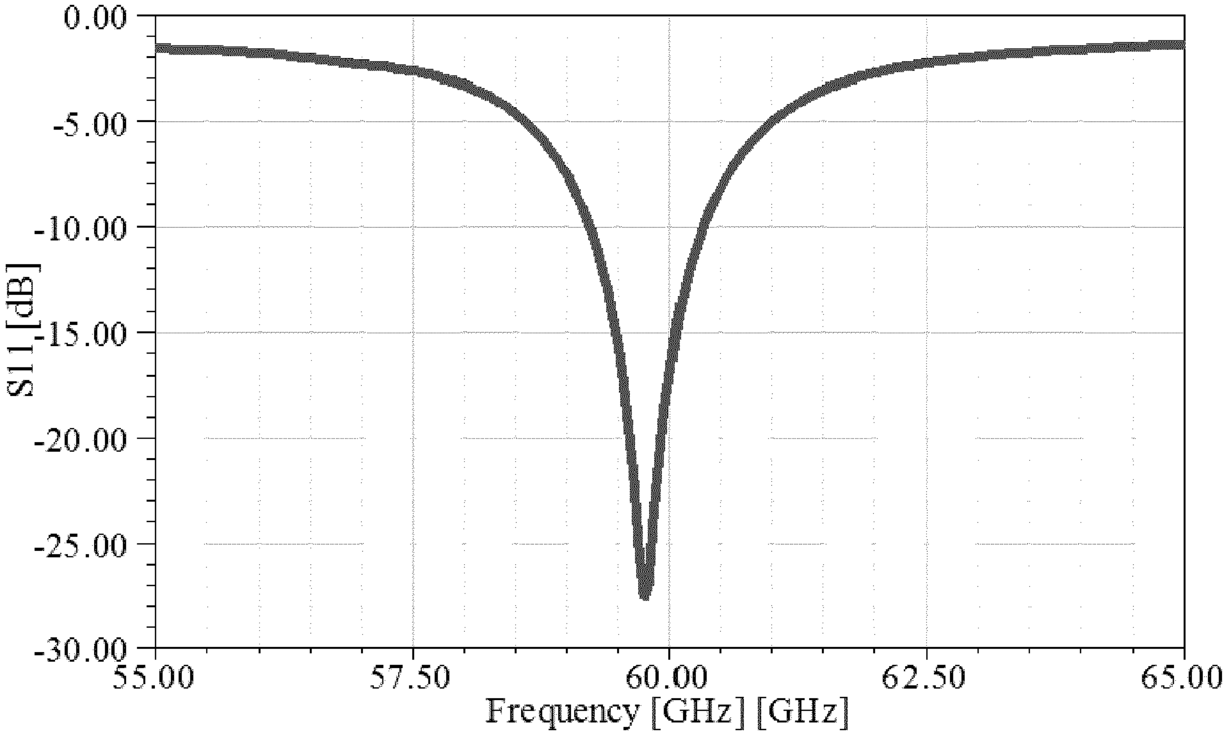
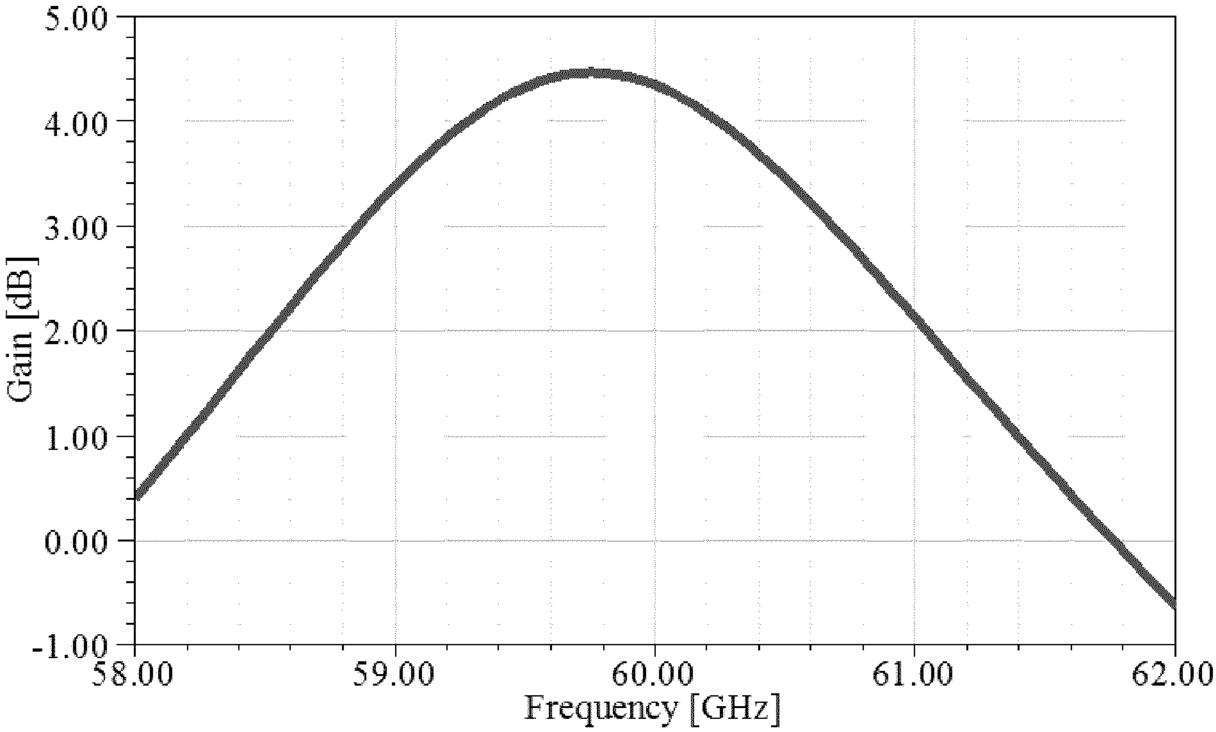


Figure 17


0.00
-5.00
-10.00
-15.00
-20.00
-25.00
-30.00
S11 [dB]
55.00
57.50
60.00
62.50
65.00
Frequency [GHz] [GHz]

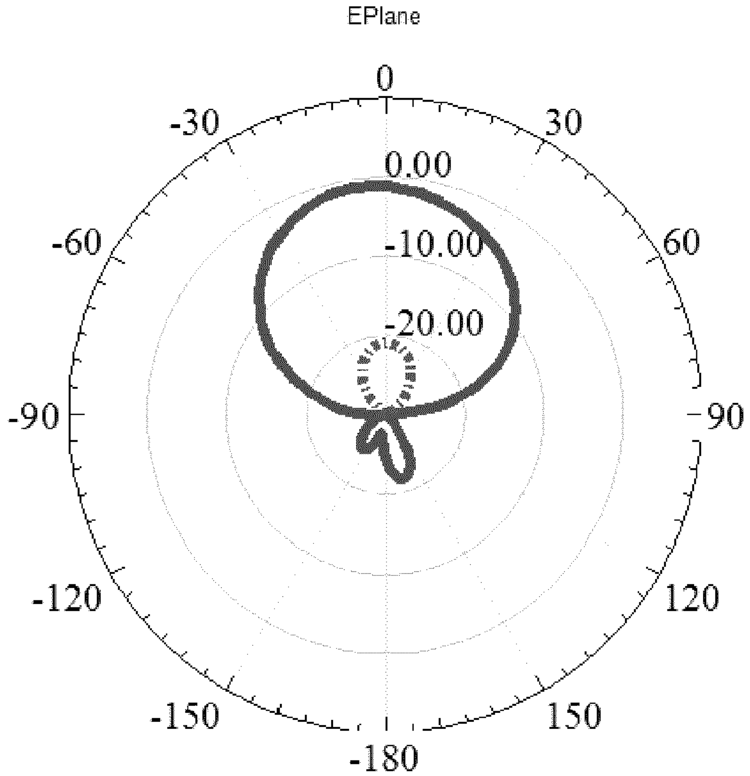
(a)


5.00
4.00
3.00
2.00
1.00
0.00
-1.00
Gain [dB]
58.00
59.00
60.00
61.00
62.00
Frequency [GHz]

(b)

Figure 18

(a)


EPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

(b)

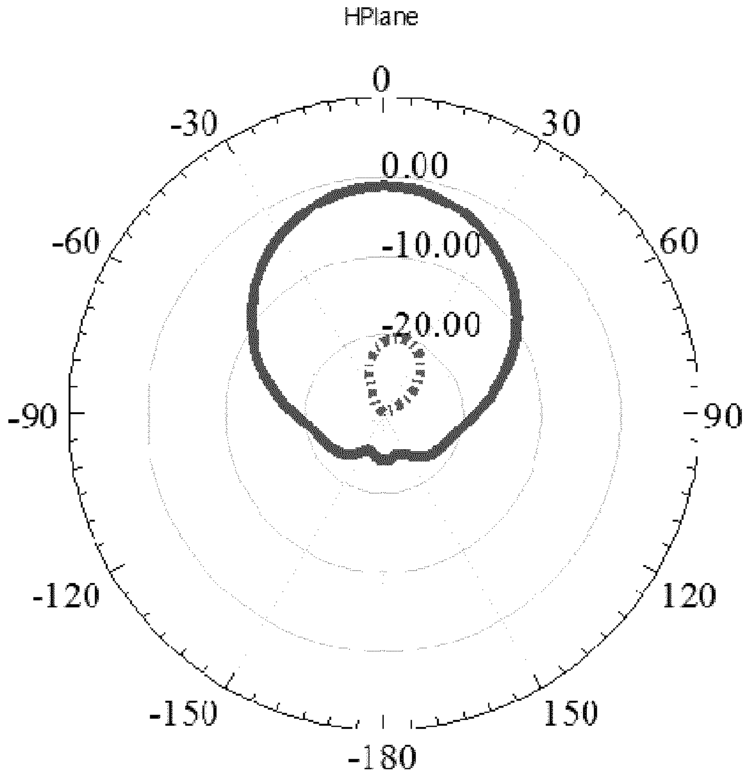

HPlane
0
30
60
90
120
150
-180
-150
-120
-90
-60
-30
0.00
-10.00
-20.00

Figure 19

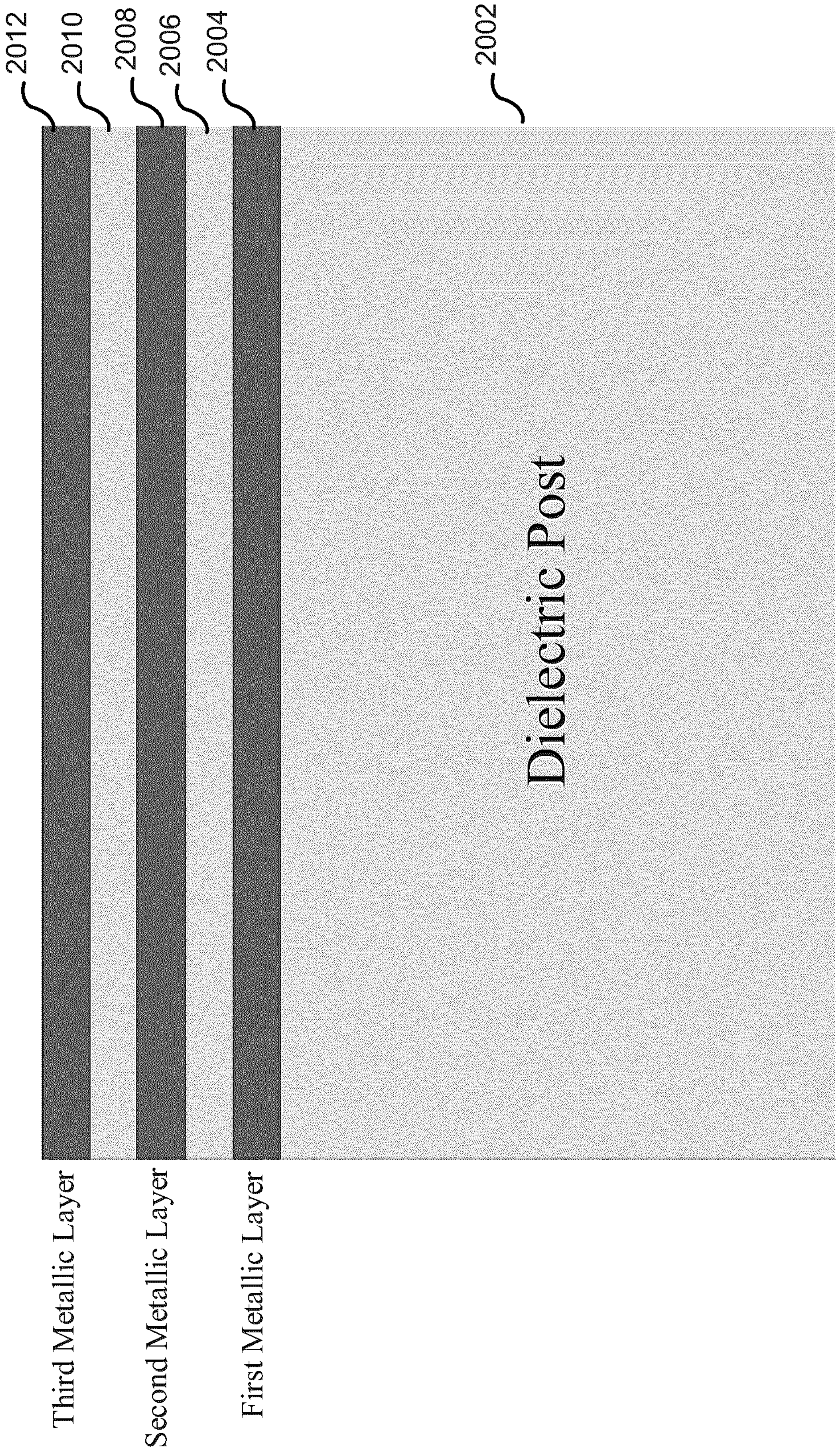

2012
2010
2008
2006
2004
2002
Dielectric Post
Third Metallic Layer
Second Metallic Layer
First Metallic Layer

Figure 20

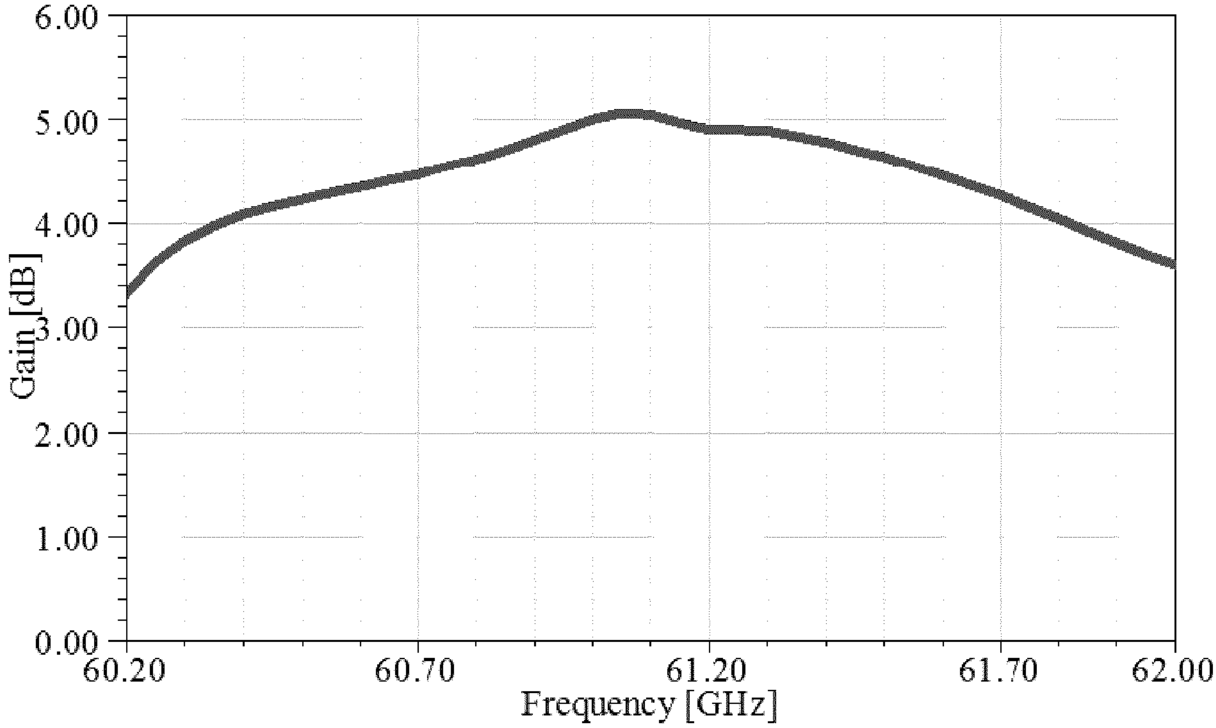

6.00
5.00
4.00
3.00
2.00
1.00
0.00
Gain [dB]
60.20
60.70
61.20
61.70
62.00
Frequency [GHz]

Figure 21

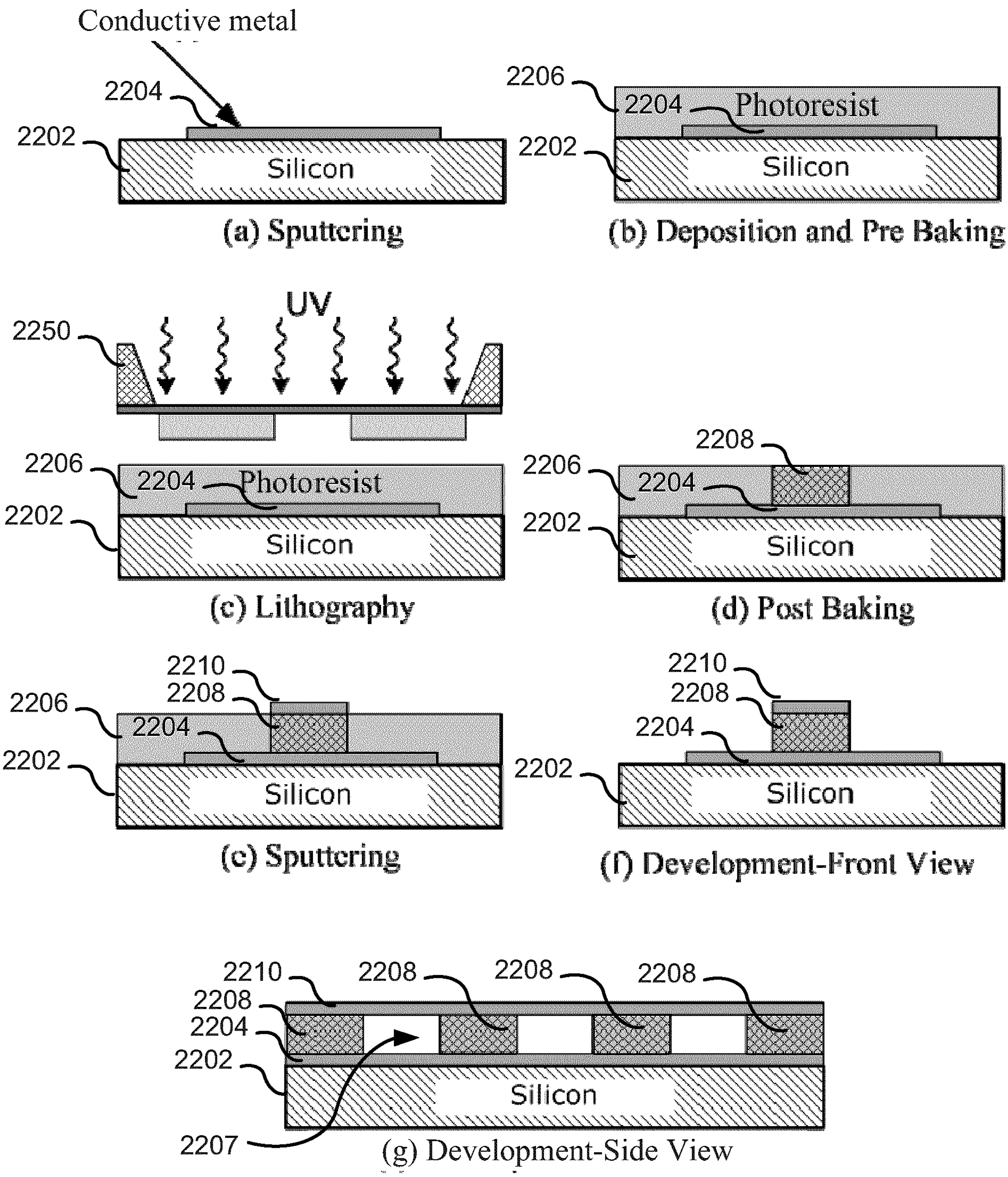

Conductive metal
2204
2202
Silicon
(a) Sputtering
2206
2204
Photoresist
2202
Silicon
(b) Deposition and Pre Baking
UV
2250
2206
2204
Photoresist
2202
Silicon
(c) Lithography
2208
2206
2204
2202
Silicon
(d) Post Baking
2210
2208
2206
2204
2202
Silicon
(e) Sputtering
2210
2208
2204
2202
Silicon
(f) Development-Front View
2210
2208
2208
2208
2208
2204
2202
Silicon
2207
(g) Development-Side View

Figure 22

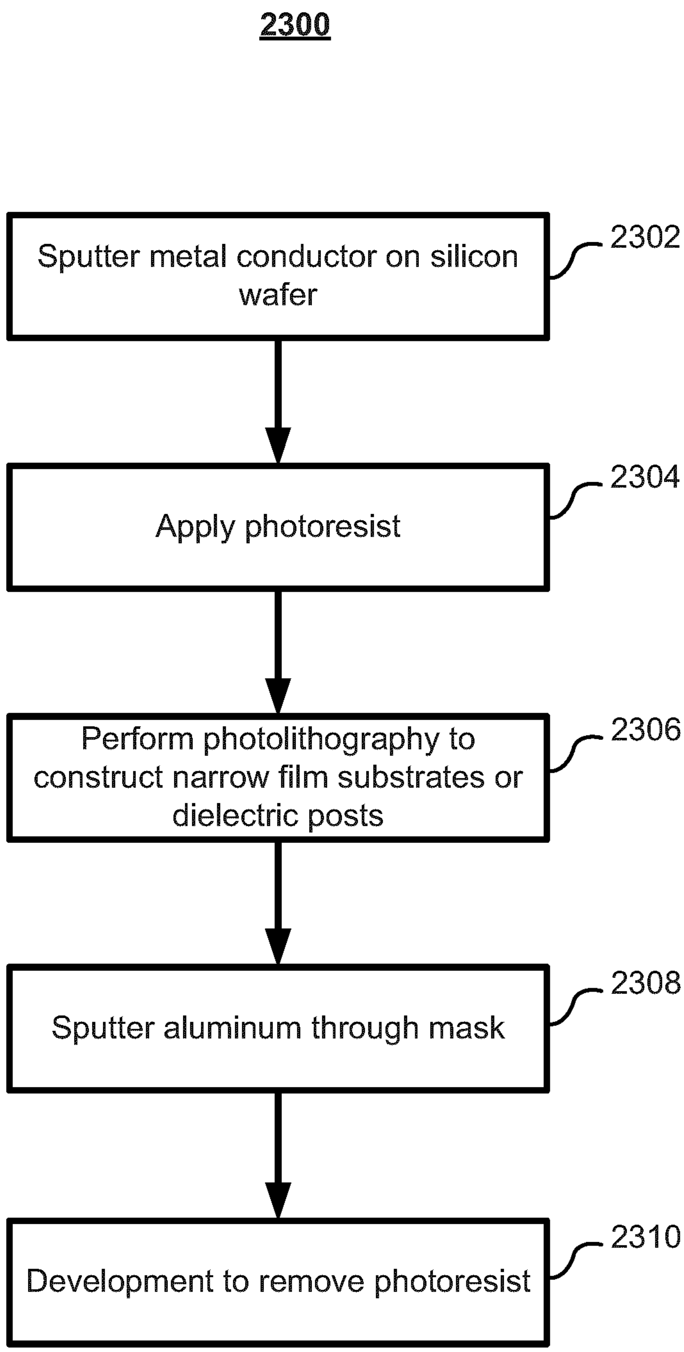

2300
Sputter metal conductor on silicon wafer
2302
Apply photoresist
2304
Perform photolithography to construct narrow film substrates or dielectric posts
2306
Sputter aluminum through mask
2308
Development to remove photoresist
2310

Figure 23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2015/050253

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***G03F 7/00*** (2006.01) , ***G03F 7/26*** (2006.01) , ***H01Q 1/38*** (2006.01) , ***H01Q 9/04*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: ***G03F 7/00*** (2006.01) , ***G03F 7/26*** (2006.01) , ***H01Q 1/38*** (2006.01) , ***H01Q 9/04*** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Canadian Patent Database, QUESTEL-ORBIT (Keywords: microwave, silicon, photoresist, photolithography, dielectric, ground, antenna)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,367,308 (WEBER) 22 November 1994 (22-11-1994) *whole document*	1-50
Y	CA 2 843 415 (RASHIDIAN et al.) 07 February 2013 (07-02-2013) *whole document*	1-50
A	US 5,858,622 (GEARHART) 12 January 1999 (12-01-1999) *whole document*	

☐ Further documents are listed in the continuation of Box C.

☑ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier application or patent but published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
08 June 2015 (08-06-2015)	23 June 2015 (23-06-2015)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Malcolm Downey (819) 934-2329

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US5367308A	22 November 1994 (22-11-1994)	None	
CA2843415A1	07 February 2013 (07-02-2013)	CA2843415A1	07 February 2013 (07-02-2013)
		CN103843198A	04 June 2014 (04-06-2014)
		EP2737575A1	04 June 2014 (04-06-2014)
		EP2737575A4	08 April 2015 (08-04-2015)
		US2014327597A1	06 November 2014 (06-11-2014)
		WO2013016815A1	07 February 2013 (07-02-2013)
US5858622A	12 January 1999 (12-01-1999)	None	