

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



WIPO | PCT

(10) International Publication Number

WO 2013/052411 A1

**(43) International Publication Date
11 April 2013 (11.04.2013)**

(51) International Patent Classification:
H01L 25/065 (2006.01) H01L 23/498 (2006.01)

(21) International Application Number: PCT/US2012/058273

(22) International Filing Date: 1 October 2012 (01.10.2012)

(25) Filing Language: English
(26) Publication Language: English

(30) Priority Data: 61/542,468, filed 2 Oct. 1, 2011 (22-10-2011) U.S.

61/542,168	3 October 2011 (03.10.2011)	US
61/542,553	3 October 2011 (03.10.2011)	US
61/600,271	17 February 2012 (17.02.2012)	US
13/440,313	5 April 2012 (05.04.2012)	US

(71) **Applicant: INVENSAS CORPORATION [US/US];**
2702 Orchard Parkway, San Jose, CA 95134 (US).

(72) **Inventors:** **CRISP, Richard, Dewitt**; C/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **ZOHNI, Wael**; C/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **HABA, Bel-gacem**; C/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US). **LAMBRECHT, Frank**; C/o Invensas Corporation, 2702 Orchard Parkway, San Jose, CA 95134 (US).

(74) **Agents:** **KARLIN, Joseph, H.** et al.; Lerner, David, Littenberg, Krumholz & Mentlik, LLP, 600 South Avenue West, Westfield, NJ 07090 (US).

(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: STUB MINIMIZATION FOR WIREBOND ASSEMBLIES WITHOUT WINDOWS

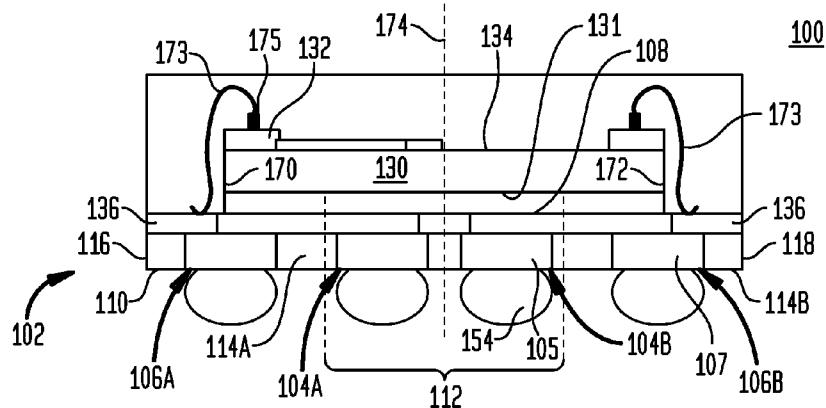


FIG. 6A

(57) Abstract: A microelectronic package (100) can include a microelectronic element (130) mounted face up on a first surface (108) of a substrate (102), with one or more columns (138, 139) of contacts (132) in a first direction (142) along the microelectronic element front face. Columns (104A, 104B, 106A, 106B) of terminals (105, 107) exposed at a second surface (110) of the substrate extend in the first direction along surface (110). First terminals (105) exposed at surface (110) in a central region (112) thereof having width (152) not more than three and one-half times a minimum pitch (150) of the columns of terminals can be configured to carry address information usable to determine an addressable memory location. An axial plane of the microelectronic element can intersect the central region.

STUB MINIMIZATION FOR WIREBOND ASSEMBLIES WITHOUT WINDOWS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of United States Application No. 13/440,313, filed April 5, 2012, which application claims the benefit of the filing date of United States Provisional Application Nos. 61/600,271 filed February 17, 2012, 61/542,488 filed October 3, 2011, and 61/542,553 filed October 3, 2011, the disclosure of all said Applications being incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The subject matter of the present application relates to microelectronic packages and assemblies incorporating microelectronic packages.

[0003] Semiconductor chips are commonly provided as individual, prepackaged units. A standard chip has a flat, rectangular body with a large front face having contacts connected to the internal circuitry of the chip. Each individual chip typically is contained in a package having external terminals connected to the contacts of the chip. In turn, the terminals, *i.e.*, the external connection points of the package, are configured to electrically connect to a circuit panel, such as a printed circuit board. In many conventional designs, the chip package occupies an area of the circuit panel considerably larger than the area of the chip itself. As used in this disclosure with reference to a flat chip having a front face, the "area of the chip" should be understood as referring to the area of the front face.

[0004] Size is a significant consideration in any physical arrangement of chips. The demand for more compact physical arrangements of chips has become even more intense with the rapid progress of portable electronic devices. Merely by way of example, devices commonly referred to as "smart phones" integrate the functions of a cellular telephone with powerful data processors, memory and ancillary devices such as global positioning system receivers, electronic cameras, and local area network connections along with high-resolution displays

and associated image processing chips. Such devices can provide capabilities such as full internet connectivity, entertainment including full-resolution video, navigation, electronic banking and more, all in a pocket-size device. Complex portable devices require packing numerous chips into a small space. Moreover, some of the chips have many input and output connections, commonly referred to as "I/Os." These I/Os must be interconnected with the I/Os of other chips. The components which form the interconnections should not greatly increase the size of the assembly. Similar needs arise in other applications as, for example, in data servers such as those used in internet search engines where increased performance and size reduction are needed.

[0005] Semiconductor chips containing memory storage arrays, particularly dynamic random access memory chips (DRAMs) and flash memory chips are commonly packaged in single- or multiple-chip packages and assemblies. Each package has many electrical connections for carrying signals, power and ground between terminals and the chips therein. The electrical connections can include different kinds of conductors such as horizontal conductors, e.g., traces, beam leads, etc., which extend in a horizontal direction relative to a contact-bearing surface of a chip, vertical conductors such as vias, which extend in a vertical direction relative to the surface of the chip, and wire bonds which extend in both horizontal and vertical directions relative to the surface of the chip.

[0006] Conventional microelectronic packages can incorporate a microelectronic element which is configured to predominantly provide memory storage array function, *i.e.*, a microelectronic element that embodies a greater number of active devices to provide memory storage array function than any other function. The microelectronic element may be or include a DRAM chip, or a stacked electrically interconnected assembly of such semiconductor chips. Typically, all of the terminals of such package are placed in sets of columns

adjacent to one or more peripheral edges of a package substrate to which the microelectronic element is mounted.

[0007] For example, in one conventional microelectronic package 12 seen in FIG. 1, three columns 14 of terminals can be disposed adjacent a first peripheral edge 16 of the package substrate 20 and three other columns 18 of terminals can be disposed adjacent a second peripheral edge 22 of the package substrate 20. A central region 24 of the package substrate 20 in the conventional package does not have any columns of terminals. FIG. 1 further shows a semiconductor chip 11 within the package having element contacts 26 on a face 28 thereof which are electrically interconnected with the columns 14, 18 of terminals of the package 12 through wire bonds 30 extending through an aperture, e.g., bond window, in the central region 24 of package substrate 20. In some cases, an adhesive layer 32 may be disposed between the face 28 of the microelectronic element 11 and the substrate 20 to reinforce the mechanical connection between the microelectronic element and the substrate, with the wire bonds extending through an opening in the adhesive layer 32.

[0008] In light of the foregoing, certain improvements in the positioning of terminals on microelectronic packages can be made in order to improve electrical performance, particularly in assemblies which include such packages and a circuit panel to which such packages can be mounted and electrically interconnected with one another.

SUMMARY OF THE INVENTION

[0009] In accordance with an aspect of the invention, a microelectronic package can include a substrate having a first surface, a second surface opposite the first surface, and a plurality of substrate contacts exposed at the second surface. The second surface can extend in the first direction and in a second direction transverse thereto. The microelectronic package includes a microelectronic element having memory storage array function, the microelectronic element having a rear face facing the first surface, a front face opposite the

first surface, and first and second opposed edges each extending between the front and rear faces and extending in the first direction parallel to the front face.

[0010] The microelectronic element can have one or more columns of element contacts exposed at the front face, each column extending in the first direction along the front face. An axial plane normal to the front face can intersect the front face along a line extending in the first direction and centered relative to the one or more columns of element contacts. Conductive structure may extend above the front face. The conductive structure can electrically connect the element contacts with the substrate contacts.

[0011] The microelectronic package may include a plurality of columns of terminals extending in the first direction which are exposed at the second surface of the substrate and electrically connected with the substrate contacts. The terminals can include first terminals exposed at the second surface in a central region of the second surface of the substrate. The first terminals can be configured to carry address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the microelectronic element. The central region can have a width in the second direction which is not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals. The axial plane can intersect the central region.

[0012] In one example, the microelectronic element may embody a greater number of active devices to provide memory storage array function than any other function.

[0013] In one embodiment, the first terminals can be configured to carry all of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array. In a particular example, the first terminals can be configured to carry information that controls an operating mode of the

microelectronic element. In one example, the first terminals can be configured to carry all of the command signals transferred to the microelectronic package, the command signals being write enable, row address strobe, and column address strobe signals. In an exemplary embodiment, the first terminals can be configured to carry clock signals transferred to the microelectronic package which are clocks usable for sampling signals carrying the address information. In a particular embodiment, the first terminals can be configured to carry all of the bank address signals transferred to the microelectronic package.

[0014] In a particular example, the terminals can be configured to connect the microelectronic package to at least one component external to the microelectronic package. In one example, the element contacts can include redistribution contacts exposed at the front face of the microelectronic element. Each redistribution contact can be electrically connected with a contact pad of the microelectronic element through at least one of a trace or a via. In one embodiment, the conductive structure can include wire bonds extending from the element contacts and electrically connected with the substrate contacts. In an exemplary embodiment, the first terminals may be arranged in no more than two of the columns of terminals. In a particular embodiment, the first terminals can be arranged in a single one of the columns of terminals. In one example, the first terminals may be arranged in no more than four of the columns of terminals.

[0015] In an exemplary embodiment, the substrate can have first and second opposed edges between the first and second opposed surfaces. The first and second edges can extend in the first direction. The second surface can have first and second peripheral regions adjacent to the first and second edges, respectively. The central region can separate the first and second peripheral regions. The terminals can include a plurality of second terminals exposed at the second surface in at least one of the peripheral regions. At least

some of the second terminals can be configured to carry information other than the address information. In one embodiment, at least some of the second terminals can be configured to carry data signals. In a particular example, the substrate can include a dielectric element having a coefficient of thermal expansion ("CTE") in the plane of the dielectric element of less than 30 parts per million per degree Celsius ("ppm/°C"). In an exemplary embodiment, the substrate can include an element having a CTE of less than 12 ppm/°C.

[0016] In accordance with another aspect of the invention, a microelectronic package can include a substrate having a first surface, a second surface opposite the first surface, a plurality of substrate contacts exposed at the first surface, and a microelectronic element having a rear face facing the first surface of the substrate, the microelectronic element having memory storage array function. In one example, the microelectronic element may have a greater number of active devices configured for providing memory storage array function than any other function. Conductive structure, which may extend above the front face, electrically connects the contacts with the substrate contacts. A plurality of parallel columns of terminals can be exposed at the second surface of the substrate and extending in a first direction along the second surface, the terminals electrically connected with the substrate contacts. The microelectronic element can have a front face opposite the front face and facing away from the first surface, and first and second opposed edges each extending between the front and rear faces and extending in a first direction parallel to the front face. The microelectronic element can have at least one column of element contacts extending in the first direction along the front face. The first and second edges can define an axial plane extending in the first direction and also in a third direction normal to the rear face of the microelectronic

element. The axial plane can be centered relative to the first and second edges.

[0017] The terminals can include first terminals exposed at the second surface of the substrate in a central region of the second surface. The first terminals can be configured to carry a majority of the address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the microelectronic element. The central region can have a width in the second direction. The width of the central region may be not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals. The axial plane can intersect the central region. In one embodiment, the first terminals can be configured to carry at least three-quarters of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

[0018] In accordance with yet another aspect of the invention, a microelectronic package can include a substrate having a first surface, a second surface opposite the first surface, a plurality of first substrate contacts exposed at the first surface and a plurality of second substrate contacts exposed at the first surface. The microelectronic package can include first and second microelectronic elements each having memory storage array function. In one example, the microelectronic package can embody a greater number of active devices to provide memory storage array function than any other function.

[0019] The first and second microelectronic elements can be spaced apart from one another on the first surface, and can have parallel first edges each extending in the first direction. An axial plane normal to the first surface of the substrate can extend in the first direction and can be centered among the first edges. The first and second

microelectronic elements can have rear faces facing the first surface, front faces opposite the rear faces, and a plurality of contacts exposed at the front faces. Conductive structure, which may extend above the front faces, can electrically connect the contacts of the first and second microelectronic elements with the first and second substrate contacts, respectively.

[0020] A plurality of parallel columns of terminals can be exposed at the second surface of the substrate and electrically connected with the first and second substrate contacts. The terminals can include first terminals exposed in a central region of the second surface of the substrate. The columns of terminals may extend in the first direction. The first terminals can be configured to carry address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within the first and second microelectronic elements. The central region can have a width in the second direction. The width of the central region may be not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals. The axial plane can intersect the central region.

[0021] In one embodiment, the first terminals can be configured to carry all of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array. In a particular example, the first terminals can be configured to carry information that controls an operating mode of a microelectronic element of the first and second microelectronic elements. In one example, the first terminals can be configured to carry clock signals and all of the command signals, address signals, and bank address signals transferred to the microelectronic package, the command signals being write enable, row address strobe, and column

address strobe, and the clock signals being clocks used for sampling signals carrying the address information.

[0022] In an exemplary embodiment, the front faces of the first and second microelectronic elements can extend in a single plane parallel to the first surface of the substrate. In a particular example, the conductive structure can include wire bonds extending from the contacts of the first and second microelectronic elements and electrically connected with the respective first and second substrate contacts. In one example, the first terminals may be arranged in no more than four of the columns of terminals. In one example, the contacts of each of the microelectronic elements can include redistribution contacts exposed at the front face of the respective microelectronic element. Each redistribution contact can be electrically connected with a contact pad of the respective microelectronic element through at least one of a trace or a via. At least some of the redistribution contacts can be displaced from the contacts of the respective microelectronic element in at least one direction along the front face of the microelectronic element.

[0023] In a particular example, the substrate can have first and second opposed edges between the first and second opposed surfaces. The first and second edges can extend in the first direction. The second surface can have first and second peripheral regions adjacent to the first and second edges, respectively. The central region can separate the first and second peripheral regions. The terminals can include a plurality of second terminals exposed at the second surface in at least one of the peripheral regions. At least some of the second terminals can be configured to carry information other than the address information. In one embodiment, at least some of the second terminals can be configured to carry data signals.

[0024] In accordance with still another aspect of the invention, a microelectronic package can include a substrate having a first surface, a plurality of first substrate

contacts exposed at the first surface, and a plurality of second substrate contacts exposed at the first surface, the package including first and second microelectronic elements having memory storage array function. In one example, each microelectronic element may embody a greater number of active devices to provide memory storage array function than any other function. The microelectronic package includes conductive structure electrically connecting the contacts of the microelectronic elements with the substrate contacts. In some cases, the conductive structure can extend above the front face of each microelectronic element, and a plurality of parallel columns of terminals can be exposed at a second surface of the substrate and electrically connected with the first and second substrate contacts. The second surface of the substrate can be opposite the first surface. The second surface can extend in a first direction and in a second direction transverse thereto.

[0025] The first and second microelectronic elements can be spaced apart from one another on the first surface, and can have first parallel edges each extending in the first direction. An axial plane normal to the first surface of the substrate can extend in the first direction and can be centered among the first edges. The first and second microelectronic elements can have rear faces facing the first surface, front faces opposite the rear faces, and a plurality of contacts exposed at the front faces. The conductive structure can electrically connect the contacts of the first and second microelectronic elements with the first and second substrate contacts, respectively.

[0026] The terminals can include first terminals exposed at the second surface in a central region of the second surface of the substrate. The first terminals can be configured to carry a majority of the address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the first and

second microelectronic elements. The central region can have a width in the second direction. The width of the central region may be not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals. The axial plane can intersect the central region. In a particular example, the terminals can be configured to carry at least three-quarters of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] FIG. 1 is a sectional view illustrating a conventional microelectronic package containing a DRAM chip.

[0028] FIG. 2 is a diagrammatic schematic diagram illustrating a microelectronic assembly, e.g., a DIMM module, incorporating a circuit panel and a plurality of microelectronic packages mounted opposite one another to first and second opposite surfaces thereof.

[0029] FIG. 3 is a sectional view further illustrating an electrical interconnection between first and second microelectronic packages and a circuit panel in an assembly such as shown in FIG. 2.

[0030] FIG. 4 is a diagrammatic plan view further illustrating the electrical interconnection between first and second microelectronic packages in an assembly such as shown in FIG. 2.

[0031] FIG. 5 is a diagrammatic plan view illustrating an arrangement and signal assignment of terminals in a microelectronic package according to an embodiment of the invention.

[0032] FIG. 6A is a sectional view through line 6A-6A of FIG. 5 further illustrating the microelectronic package shown in FIG. 5.

[0033] FIG. 6B is a plan view of the microelectronic element of FIG. 6A illustrating an arrangement of contacts in accordance with the embodiment shown in FIGS. 5 and 6A.

[0034] FIG. 6C is a plan view illustrating an alternative arrangement of contacts on a microelectronic element according to a variation of the embodiment shown in FIG. 6B.

[0035] FIG. 6D is a plan view illustrating another alternative arrangement of contacts on a microelectronic element according to a variation of the embodiment shown in FIG. 6B.

[0036] FIG. 6E is a sectional view illustrating a microelectronic package according to a variation of the embodiment shown in FIGS. 5 and 6A.

[0037] FIG. 7A is a plan view further illustrating an arrangement of terminals in accordance with the embodiment shown in FIGS. 5 and 6A.

[0038] FIG. 7B is a sectional view illustrating a microelectronic assembly and first and second microelectronic packages electrically interconnected therewith in accordance with an embodiment of the invention.

[0039] FIG. 7C is a schematic diagram illustrating a microelectronic assembly including a circuit panel and microelectronic packages electrically connected thereto, e.g., a memory module, among others, according to an embodiment of the invention.

[0040] FIG. 8 is a plan view illustrating an alternative arrangement of terminals on a microelectronic package according to a variation of the embodiment shown in FIGS. 5 and 6A.

[0041] FIG. 9A is a plan view illustrating an alternative arrangement of terminals on a microelectronic package according to another variation of the embodiment shown in FIGS. 5 and 6A.

[0042] FIG. 9B is a sectional view illustrating a microelectronic assembly and first and second microelectronic packages as shown in FIG. 9A electrically interconnected therewith in accordance with an embodiment of the invention.

[0043] FIG. 10A is a sectional view illustrating a microelectronic package including a stacked electrically

connected assembly of semiconductor chips therein in accordance with an embodiment of the invention.

[0044] FIG. 10B is a sectional view illustrating a microelectronic package according to a variation of the embodiment shown in FIG. 10A.

[0045] FIGS. 11A and 11B are a sectional view and a corresponding top view illustrating a microelectronic package including a stacked electrically connected assembly of semiconductor chips therein in accordance with an embodiment of the invention.

[0046] FIG. 12 is a sectional view illustrating a microelectronic package including a stacked electrically connected assembly of semiconductor chips therein in accordance with an embodiment of the invention.

[0047] FIG. 13A is a sectional view illustrating a microelectronic package according to a variation of the embodiment shown in FIG. 12.

[0048] FIG. 13B is a sectional view illustrating a microelectronic package according to another variation of the embodiment shown in FIG. 12.

[0049] FIG. 13C is a sectional view illustrating a microelectronic package according to a variation of the embodiment shown in FIG. 13B.

[0050] FIG. 14A is a diagrammatic plan view illustrating an arrangement and signal assignment of terminals in a microelectronic package according to another embodiment of the invention.

[0051] FIG. 14B is a plan view further illustrating an arrangement of terminals in accordance with the embodiment shown in FIG. 14A.

[0052] FIG. 15 is a sectional view through line 15-15 of FIG. 14A further illustrating the microelectronic package shown in FIG. 14A.

[0053] FIG. 16A is a diagrammatic plan view illustrating an arrangement of terminals in a microelectronic package according to yet another embodiment of the invention.

[0054] FIG. 16B is a plan view further illustrating an arrangement and signal assignment of terminals in accordance with the embodiment shown in FIG. 16A.

[0055] FIG. 17A is a diagrammatic plan view illustrating an arrangement of terminals in a microelectronic package according to a variation of the embodiment shown in FIGS. 16A and 16B.

[0056] FIG. 17B is a plan view further illustrating an arrangement and signal assignment of terminals in accordance with the embodiment shown in FIG. 17A.

[0057] FIG. 18 is a schematic sectional view illustrating a system according to an embodiment of the invention.

[0058] FIG. 19 is a schematic sectional view illustrating a system according to an embodiment of the invention.

DETAILED DESCRIPTION

[0059] In view of the illustrative conventional microelectronic package 12 described relative to FIG. 1, the inventors have recognized improvements which can be made that may help improve the electrical performance of a microelectronic package incorporating a memory storage array chip, and a microelectronic assembly that incorporates such microelectronic package.

[0060] Improvements can be made particularly for use of a microelectronic package when provided in an assembly such as shown in FIGS. 2-4, in which a package 12A is mounted to a surface of a circuit panel with another like package 12B mounted opposite thereto on an opposite surface of the circuit panel. The packages 12A, 12B typically are functionally and mechanically equivalent to one another. Other pairs 12C and 12D; and 12E and 12F, of functionally and mechanically equivalent packages typically are also mounted to the same circuit panel 34. The circuit panel and the packages assembled thereto may form a portion of an assembly commonly referred to as a dual in-line memory module ("DIMM"). The packages in each oppositely mounted pair of packages, e.g., packages 12A, 12B, connect to contacts on opposite surfaces of

the circuit panel so that the packages in each pair overlie one another typically by more than 90% of their respective areas. Local wiring within the circuit panel 34 connects terminals, e.g., the terminals labeled "1" and "5" on each package to global wiring on the circuit panel. The global wiring includes the signal conductors of a bus 36 used to conduct some signals to connection sites on the circuit panel 34 such as sites I, II and III. For example, the packages 12A, 12B are electrically connected to the bus 36 by local wiring coupled to a connection site I, packages 12C, 12D are electrically connected to the bus by local wiring coupled to connection site II, and packages 12E, 12F are electrically connected to the bus by local wiring coupled to connection site III.

[0061] The circuit panel 34 electrically interconnects the terminals of the respective packages 12A, 12B using local interconnect wiring that appears similar to a crisscross or "shoelace" pattern in which a terminal labeled "1" near one edge 16 of package 12A connects through the circuit panel 34 to a terminal labeled "1" of package 12B near the same edge 16 of package 12B. However, the edge 16 of package 12B as assembled to circuit panel 34 is far from the edge 16 of package 12A. FIGS. 2-4 further shows that a terminal labeled "5" near an edge 22 of package 12A is connected through the circuit panel 34 to a terminal labeled "5" of package 12B near the same edge 22 of package 12B. In assembly 38 the edge 22 of package 12A is far from the edge 22 of package 12B.

[0062] Connections through the circuit panel between terminals on each package, e.g., package 12A, to the corresponding terminals on the package mounted opposite thereto, i.e., package 12B, are fairly long. As further seen in FIG. 3, in such assembly of like microelectronic packages 12A, 12B, the circuit panel 34 may electrically interconnect a signal conductor of the bus 36 with the terminal of package 12A marked "1" and the corresponding terminal of package 12B marked "1", when the same signal from the bus is to be

transmitted to each package. Similarly, the circuit panel 34 may electrically interconnect another signal conductor of the bus 36 with the terminal of package 12A marked "2" and the corresponding terminal of package 12B marked "2". The same connection arrangement may also apply to other signal conductors of the bus and corresponding terminals of each package.

[0063] Local wiring between the bus 36 on the circuit panel 34 and each package of the respective pair of packages, e.g., packages 12A, 12B (FIG. 2) at a connection site I of the board can be in form of unterminated stubs. Such local wiring when relatively long may in some cases impact the performance of the assembly 38 as discussed below. Moreover, the circuit panel 34 also requires local wiring to electrically interconnect certain terminals of other packages: the pair of packages 12C and 12D, and the pair of packages 12E and 12F to the global wiring of the bus 36, and such wiring can also impact the performance of the assembly in the same way.

[0064] FIG. 4 further illustrates the interconnection between microelectronic packages 12A, 12B of respective pairs of terminals assigned to carry signals "1", "2", "3", "4", "5", "6", "7", and "8". As seen in FIG. 4, because the columns 14, 18 of terminals are near the edges 16, 22, respectively, of each package 12A, 12B, the wiring needed to traverse the circuit panel 34 in a direction 40 transverse to the direction 42 in which the columns 14, 18 of terminals extend can be quite long. In recognition that the length of a DRAM chip can be in the range of ten millimeters on each side, the length of the local wiring in a circuit panel 34 in an assembly 38 seen in FIGS. 2-4 that is required to route the same signal to the corresponding terminals of two oppositely mounted packages 12A, 12B can range between five and ten millimeters and may typically be about seven millimeters.

[0065] In some cases, relatively long unterminated wiring on a circuit panel which connects the terminals of a package may not severely impact the electrical performance of the

assembly 38. However, when a signal is transferred from a bus 36 of the circuit panel to each of multiple pairs of packages connected to the circuit panel as shown in FIG. 2, the inventors recognize that the electrical lengths of the stubs, *i.e.*, the local wiring, that extend from the bus 36 to the terminal connected thereto on each package potentially impacts the performance of the assembly 38. Signal reflections on the unterminated stubs can travel in the reverse direction from the connected terminals of each package back onto the bus 36, and thus degrade the signals being transferred from the bus 36 to the packages. The impacts may be tolerable for some packages containing microelectronic elements of current manufacture. However, in present or future assemblies which operate with increased signal switching frequencies, low voltage swing signals or both, the inventors recognize that the impacts can become severe. For these assemblies, settling time, ringing, jitter, or intersymbol interference of a transmitted signal may increase to an unacceptable degree.

[0066] The inventors further recognize that the electrical lengths of the unterminated stubs are usually longer than the local wiring that connects the bus 36 on the circuit panel with the terminals of the packages mounted thereto. Unterminated wiring within each package from the package terminals to the semiconductor chip therein adds to the lengths of the stubs.

[0067] In a specific example, the bus 36 is a command-address bus of an assembly having a predominant memory storage array function such as a DIMM. The command-address bus 36 can be configured to carry address information transferred to the microelectronic packages that is usable by circuitry within the packages, *e.g.*, row address and column address decoders, and bank selection circuitry, if present, to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within a microelectronic element in the packages. The command-address bus 36 can be configured to carry the above-noted

address information to connection sites, e.g., sites I, II, and III shown in FIG. 2. These above-noted address information can then be distributed by local wiring to respective sets of panel contacts on opposite surfaces of the circuit panel, to which packages 12A, 12B, 12C, 12D, 12E and 12F are connected.

[0068] In a particular example, when the microelectronic element is or includes a DRAM chip, command-address bus 36 can be configured to carry all of a group of signals of a command-address bus of the microelectronic element, i.e., command signals, address signals, bank address signals and clock signals that are transferred to the microelectronic packages, wherein the command signals include write enable, row address strobe, and column address strobe signals, and the clock signals are clocks used for sampling the address signals. While the clock signals can be of various types, in one embodiment, the clock signals carried by these terminals can be one or more pairs of differential clock signals received as differential or true and complement clock signals.

[0069] Accordingly, certain embodiments of the invention described herein provide a microelectronic package configured so as to permit the lengths of stubs to be reduced when first and second such packages are mounted opposite one another on opposite surfaces of a circuit panel, e.g., a circuit board, module board or card, or flexible circuit panel. Assemblies which incorporate first and second microelectronic packages mounted opposite one another on a circuit panel can have significantly reduced stub lengths between the respective packages. Reducing the stub lengths within such assemblies can improve electrical performance, such as by reducing one or more of settling time, ringing, jitter, or intersymbol interference, among others. Moreover, it may be possible to obtain other benefits as well, such as simplifying the structure of the circuit panel or reducing the complexity and cost of designing or manufacturing the circuit panel, or for both designing and manufacturing the circuit panel.

[0070] Thus, a microelectronic package 100 according to an embodiment of the invention is illustrated in FIGS. 5 through 6B. As seen therein, the package can include a substrate 102 on which a plurality of columns 104A, 104B are disposed, each column 104A and 104B having at least some first terminals 105 disposed within the column. Optionally, a plurality of columns 106A, 106B are also disposed on the substrate 102, each column 106A and 106B having second terminals 107 disposed within the column.

[0071] As used herein, a statement that an electrically conductive element such as a terminal, or a contact, is "on" or "disposed on" a supporting element such as a substrate of a package or a circuit panel does not require that the electrically conductive element overlie a surface of the supporting element, so long as the electrically conductive element is available at the surface of the supporting element for contact with a theoretical point moving in a direction perpendicular to the surface of the supporting element. Thus, the terminal or contact may project above the surface, be recessed relative to the surface, or be flush with the surface.

[0072] The substrate may include a dielectric element, which in some cases can consist essentially of polymeric material, e.g., a resin or polyimide, among others, and which may be sheet-like. Alternatively, the substrate 102 can include a dielectric element having a composite construction such as glass-reinforced epoxy, e.g., of BT resin or FR-4 construction. In another example, the substrate can include a supporting element of material having a coefficient of thermal expansion ("CTE") of less than 12 parts per million per degree Celsius ("ppm/°C"), on which the terminals and other conductive structure are disposed. For example, such low CTE element can consist essentially of glass, ceramic or semiconductor material or liquid crystal polymer material, or a combination of such materials.

[0073] The terminals 105 and 107 can be disposed at positions within a plurality of columns 104A, 104B, 106A and 106B exposed at a surface 110 of the substrate. As used herein, a statement that an electrically conductive element is "exposed at" a surface of a structure indicates that the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to the surface toward the surface from outside the structure. Thus, a terminal or other conductive element which is exposed at a surface of a structure can project from such surface; can be flush with such surface; or can be recessed relative to such surface and exposed through a hole or depression in the structure. In the example shown in FIG. 5, columns 104A and 104B each extend in a first direction along the surface 110 and includes a plurality of first terminals 105. Columns 106A, 106B may each include a plurality of second terminals 107 and may in some cases be parallel with the columns 104A, 104B and extend in the first direction as well. In a particular example, some second terminals can also be disposed within columns 104A, 104B. The central region 112 is not wider than three and one-half times a minimum pitch between adjacent ones of the parallel columns of the terminals, as seen and further described relative to FIG. 7A below.

[0074] In one example, the first terminals can be configured to carry address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within the microelectronic element. Thus, in one embodiment, the first terminals are configured to carry address information transferred to the microelectronic package which is usable by circuitry within the package, e.g., row address and column address decoders, and bank selection circuitry, if present, to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within a microelectronic element in the package. Typically, the address information

carried by the first terminals is sufficient to determine the addressable memory location. In a particular embodiment, the first terminals can be configured to carry all the address information used by such circuitry within the package to determine an addressable memory location within such memory storage array.

[0075] In a variation of such embodiment, the first terminals can be configured to carry a majority of the address information that is used by such circuitry within the package to determine an addressable memory location within such memory storage array, and then other terminals such as the above-referenced second terminals on the package would then be configured to carry the remaining part of the address information. In such variation, in a particular embodiment, the first terminals are configured to carry three quarters or more of the address information that is used by such circuitry within the package to determine an addressable memory location within such memory storage array.

[0076] In a particular embodiment, the first terminals may not be configured to carry chip select information, e.g., information usable to select a particular chip within the package for access to a memory storage location within the chip. In another embodiment, the first terminals may indeed carry chip select information.

[0077] A variety of microelectronic elements, e.g., semiconductor chips, are configured to provide memory storage array function. In one example, a microelectronic element may contain a greater number of active devices to provide memory storage array function than any other function. In one type of such microelectronic element, each one of some contacts of a plurality of external contacts at an exterior of the microelectronic element is dedicated to receiving a respective address signal of a plurality of address signals supplied to the microelectronic element. In this case, each of such contacts is able to receive one address signal of the plurality of address signals supplied to the microelectronic

element from an external component, e.g., from a circuit panel via connections through a microelectronic package in which the microelectronic element is incorporated.

[0078] In one particular example of this type of microelectronic element, each of the plurality of address signals present at the external contacts can be sampled relative to an edge of a clock used by the microelectronic element, i.e., upon on a transition of the clock between first and second different voltage states. That is, each address signal can be sampled upon a rising transition between a lower voltage state and a higher voltage state of the clock, or upon a falling transition between a higher voltage state and a lower voltage state of the clock. Thus, the plurality of address signals may all be sampled upon the rising transition of the clock, or may all be sampled upon the falling transition of the clock, or in another example, the address signal at one of the external contacts can be sampled upon the rising transition of the clock and the address signal at one other external contact can be sampled upon the falling transition of the clock.

[0079] In another type of microelectronic element configured to predominantly provide memory storage array function, one or more of the address contacts thereon can be used in a multiplexed manner. In this example, a particular external contact of the microelectronic element can be configured to receive two or more different signals supplied to the microelectronic element from the outside. Thus, a first address signal can be sampled at the particular contact upon a first transition of the clock between the first and second different voltage states (e.g., a rising transition), and a signal other than the first address signal can be sampled at the particular contact upon a second transition of the clock (e.g., a falling transition) between the first and second voltage states that is opposite the first transition.

[0080] In such a multiplexed manner, two different signals can be received within the same cycle of the clock on the same

external contact of the microelectronic element. In a particular case, multiplexing in this manner can allow a first address signal and a different signal to be received in the same clock cycle on the same external contact of the microelectronic element. In yet another example, multiplexing in this manner can allow a first address signal and a second different address signal to be received in the same clock cycle on the same external contact of the microelectronic element.

[0081] In a particular example, the first terminals can be configured to carry all of a group of command signals, address signals, bank address signals and clock signals which are transferred to the microelectronic package. As mentioned above, the "command signals" are a write enable signal, row address strobe signal, and column address strobe signal utilized by a microelectronic element within the microelectronic package, when such microelectronic element is a dynamic random access memory storage device. "Clock signals" are signals used as clocks for sampling the address signals. For example, as seen in FIG. 5, the first terminals can include clock signals CK and CKB, row address strobe RAS, column address strobe CAS and write enable signals WE, as well as address signals A0 through A15 inclusive, and bank address signals BA0, BA1 and BA2.

[0082] Although not specifically shown in FIG. 5, other terminals, e.g., second terminals, can also be disposed in the central region and be configured to carry other signals, e.g., data signals to and or from the microelectronic element of the package. Although some first terminals in FIG. 5 are assigned for carrying a power supply voltage (VDD), the power supply connections as well as connections to ground can be among any of the first or second terminals. For ease and clarity of description, the terminals used for connecting to a power supply or to ground are omitted from the drawings and need not be mentioned further in the description which follows.

[0083] Typically, when the microelectronic package has second terminals, the second terminals are arranged in one or more columns each having a plurality of second terminals. The second terminals 106A, 106B may be arranged in one or more of first and second peripheral regions 114A, 114B of the substrate surface 110, the peripheral regions 114A, 114B being adjacent to first and second opposed edges 116, 118 of the surface 110. The central region 112 can be disposed between the first and second peripheral regions 114A, 114B.

[0084] As seen in the sectional view of FIG. 6A, a microelectronic element 130 within microelectronic package 100 has a rear face 131 facing the first surface 110 of the substrate 102, and a front face 134 opposite the rear face 131, and first and second opposed edges 170, 172 extending between the front and rear faces. The microelectronic element, *e.g.*, a semiconductor chip, or stacked arrangement of semiconductor chips, can be configured to provide memory storage array function, and in one example, may be configured to predominantly provide memory storage array function. In such microelectronic element, the number of active devices, *e.g.*, transistors, therein which are configured, *i.e.*, constructed and interconnected with other devices, to provide memory storage array function may be greater than the number of active devices which are configured to provide any other function.

[0085] Thus, in one example, a microelectronic element such as a DRAM chip may have memory storage array function as its primary or sole function. Alternatively, in another example, such microelectronic element may have mixed use and may incorporate active devices configured to provide memory storage array function, and also incorporate other active devices configured to provide another function such as processor function, or signal processor or graphics processor function, among others. In this case, the microelectronic element may in some cases still have a greater number of active devices configured to provide the memory storage array

function than any other function of the microelectronic element.

[0086] An axial plane 174 normal to the face 134 of the microelectronic element 130 intersects the second surface 110 of the substrate 102 along a line which extends in the first direction and is parallel to and centered with respect to the first and second edges 170, 172 of the microelectronic element 130. As further seen in FIG. 6A and in a corresponding plan view of FIG. 6B, an edge 170 of microelectronic element 130 extends in the first direction 142 and a column 138 of contacts 132 exposed at the front face 134 of the microelectronic element and adjacent to edge 170 can extend in the same first direction 142 along the front face 134. Another edge 172 of microelectronic element 130, parallel to edge 170, extends in the first direction 142 and a second column 139 of contacts 132 exposed at the front face 134 of the microelectronic element may extend in the same first direction 142 along the front face 134 adjacent to edge 172. As further shown in FIG. 6B, a column of contacts on the microelectronic element can be fully populated as in the case of column 138, or a column of contacts may have only have contacts at some of the positions within the column, as in the case of column 139. Conductive structure such as wire bonds 173 (FIG. 6A) may electrically connect the contacts 132 with corresponding contacts 136 on a first surface 108 of the substrate.

[0087] Referring to FIG. 6A, the axial plane 174 of microelectronic element 130, extending in the first direction parallel to edges 170, 172, intersects the central region 112 of the second surface 110 of the substrate, the central region 112 of the substrate surface being where at least a first column 104A and a second column 104B of terminals, each having at least some first terminals 105 are disposed within the column of the microelectronic package. Second terminals, if present, may be disposed in one or more of the peripheral regions 114A, 114B of the substrate surface 110.

Alternatively or in addition thereto, one or more second terminals may be disposed in the central region, such as can be disposed within columns 104A, 104B. As further seen in FIG. 6A, joining elements 154 attached to terminals can include a bond metal, e.g., solder, tin, indium or eutectic, or other electrically conductive bond material attached to the terminals that can be used to join the terminals of the package 100 to a component external to the package, such as to corresponding contacts of a circuit panel.

[0088] FIG. 6C illustrates a variation of the embodiment shown in FIG. 6B in which the contacts 132 of a microelectronic element 180 exposed at the front face thereof are disposed in columns or rows adjacent to and aligned with respective peripheral edges 170, 172, 176, 178 of the microelectronic element 180. Edges 170, 172 are parallel and extend in a first direction 142. FIG. 6C illustrates the location of an axial plane 174 of the microelectronic element 180. In such variation, the axial plane 174 is shown to extend in the first direction and is centered among the parallel edges 170, 172.

[0089] FIG. 6D illustrates another variation of the embodiment shown in FIG. 6B in which the contacts of a microelectronic element 190 are disposed in columns 188 and 189 adjacent to edges 170, 172 of the microelectronic element. However, in this case, the microelectronic element 190 includes a semiconductor chip having a conductive redistribution layer thereon, and the contacts 132 can include redistribution contacts which are connected to the contacts 192, 194 of the semiconductor chip by conductive traces, or metalized vias formed in contact with the contacts 192, 194 of the semiconductor chip (or which can be connected to the contacts 192, 194 of the chip by both metalized vias and traces). In this example, the axial plane 174 intersects the face 196 of the microelectronic element along a line centered among the columns of 188, 189 of redistribution contacts.

[0090] In the package 100 as shown in FIG. 6A, the wire bonds 173 electrically connecting the microelectronic element 130 with the substrate 102 may be formed starting from the microelectronic element 130, in which case the wire bond forms a ball 175 on the contact 132 of the microelectronic element and is wedge-bonded to the corresponding substrate contact 136. FIG. 6E shows a package 101 according to a variation thereof in which the wire bond 183 forms a ball 185 on the contact 136 of the substrate and is wedge-bonded to the corresponding contact 132 of the microelectronic element 130. The variation of FIG. 6E may be employed if desired to reduce a height 103 of the microelectronic package 101, as the wire bonds 183 formed in this way can generally have lower height excursion above the contacts 132 than the wire bonds 173 shown in FIG. 6A.

[0091] FIG. 7A is a plan view of the package 100 looking toward a terminal-bearing surface 110 of the substrate therein. Columns 104A, 104B in which first terminals are disposed can lie within a central region 112 of the surface 110, and columns 106A, 106B in which second terminals are disposed can lie within one or more peripheral regions 114A, 114B of the surface 110. The smallest distance between any two adjacent columns of terminals on the substrate is the minimum pitch 150 as shown in FIG. 7A. The minimum pitch is in a direction 164 perpendicular to the direction 162 in which the terminals in a particular column, *e.g.*, column 104A are arranged. In the example shown in FIG. 7A, the minimum pitch 150 occurs between columns 104A, 104B which are closest to one another. With continued reference to FIG. 7A, the central region 112 has a width 152 along the substrate surface 110 in the direction 164 of the pitch. In a particular example, the width 152 may be not greater than three and one-half times the minimum pitch 150 between any two adjacent columns of the terminals, *i.e.*, not more than three and one-half times the minimum pitch 150 between the closest adjacent columns 104A, 104B.

[0092] FIG. 7B illustrates a microelectronic assembly 300 of a circuit panel 354 and first and second microelectronic packages 100A, 100B, each being a microelectronic package 100 having a structure according to one or more of the embodiments described above relative to FIGS. 5-6E. Referring to FIG. 7A, each package 100A, 100B may have the same signals assigned to the respective locations of terminals on the package, and the columns 104A, 104B, 106A, 106B of terminals on each package can be arranged at the same locations in x and y orthogonal directions 164, 162 relative to an edge 116 of the substrate. The packages 100A, 100B are electrically connected to contacts 360, 362, respectively, exposed at first and second opposite surfaces 350, 352 of the circuit panel 354, respectively.

[0093] The circuit panel can be of various types, such as a printed circuit board used in a dual inline memory module ("DIMM") module, a circuit board or panel to be connected with other components in a system, or a motherboard, among others. In a particular embodiment, the circuit panel may include an element having a coefficient of thermal expansion ("CTE") of less than 12 parts per million per degree Celsius ("ppm/°C"), wherein the panel contacts at the first and second surfaces are connected by vias extending through the element. For example, the element may consist essentially of semiconductor, glass, ceramic or liquid crystal polymer material.

[0094] In the example shown in FIG. 7B, the first terminals 105 in the columns 104A, 104B can be disposed at positions within a grid 104 on the first package 100A, and the first terminals 105 in the columns 104A, 104B on the second package 100B can be disposed at positions of within a similar grid 104. Each grid of terminals may be fully populated, *i.e.*, having a terminal at each position of each grid. Alternatively, there may not be a terminal disposed at one or more positions of the grid on a package. As apparent from FIG. 7B, the grids 104 which include first terminals on each package 100A, 100B can be aligned within a distance of one ball pitch of one another in x and y orthogonal directions

parallel to the surface 350 of the circuit panel, the ball pitch being no greater than a minimum pitch between any two adjacent parallel columns of the terminals on either package. In a particular example, the grids 104 may be coincident with one another. As used herein, when grids of terminals of packages at opposite surfaces of a circuit panel are "coincident" with one another, the alignment can be within customary manufacturing tolerances or can be within a tolerance of less than one-half of one ball pitch of one another in x and y orthogonal directions parallel to the first and second circuit panel surfaces, the ball pitch being as described above.

[0095] Wiring within the circuit panel 354 electrically connects the terminals in column 104A of package 100A with terminals in column 104A of package 100B, as shown. The wiring that forms the electrical connections is shown schematically by the dashed line 320 in FIG. 7B, since the wiring can be hidden from view in the example shown in FIG. 7B. Similarly, wiring within the circuit panel 354 electrically connects the terminals in column 104B of package 100A with terminals in column 104B of package 100B, and the electrical interconnections between such terminals is shown schematically by the dashed line 322 in FIG. 7B.

[0096] Further, in a particular example as shown in FIG. 7B, since there are two columns 104A, 104B of first terminals in each grid, and the grids are aligned within at least one ball pitch of one another, then the wiring on the circuit panel 354 required to connect one of the first terminals labeled "A" of package 100A with a corresponding one of the first terminals labeled "A" of package 100B can be relatively short. Specifically, when each grid 104 on each package has two columns 104A, 104B, and the grids 104 are aligned in the above-described manner, then a terminal of the first column 104A of the first package 100A is aligned within one ball pitch of a terminal of the second column 104B of the second package 100B in x and y orthogonal directions parallel to the

first surface 350 of the circuit panel, the first surface 350 being a major surface of the circuit panel. In addition, a terminal of the second column 104B of the first package 100A is aligned within one ball pitch of a terminal of the first column 104A of the second package in x and y orthogonal directions parallel to the first surface 350 of the circuit panel.

[0097] Therefore, the electrical lengths of stubs on the circuit panel 354 that electrically connect a first terminal of the first column of package 100A with the corresponding first terminal of the first column of the second package 100B can be less than seven times a minimum pitch of the first terminals on each package: for example, less than seven times the pitch 150 between columns 104A, 104B of first terminals in FIG. 7A. Stated another way, the total combined length of the conductive elements connecting a pair of electrically coupled first and second panel contacts 360, 362 exposed at the first and second surfaces of the circuit panel to the corresponding conductor of the bus 36 on the circuit panel can be less than seven times a smallest pitch of the panel contacts.

[0098] In another example, the total combined length of the conductive elements connecting a pair of electrically coupled first and second panel contacts 360, 362 may be approximately the same as a thickness 356 of the circuit panel 354 between first and second surfaces 350, 352. In yet another example, the electrical length of the connection between a first terminal in column 104A of the first package 100A with the corresponding first terminal in column 104A on the second package 100B may be approximately the same as the thickness 356 of the circuit panel 354.

[0099] The reductions in the lengths of these electrical connections can reduce stub lengths from bus 36 (FIG. 2) on the circuit panel to the connection sites of the packages thereon. The reduced stub lengths can improve electrical performance, such as by reducing one or more of settling time,

ringing, jitter, or intersymbol interference, among others, for the above-noted signals of the bus 36.

[0100] Moreover, it may be possible to obtain other benefits as well, such as simplifying the structure of the circuit panel 354 or reducing the complexity and cost of designing or manufacturing the circuit panel. That is, connections on the circuit panel may require fewer layers of wiring to interconnect first terminals of each package to routing layers within the circuit panel which constitute a set of conductors which carry the address information or carry the address information and other information as described above.

[0101] In addition, the number of global routing layers of wiring on the circuit panel needed to implement a bus 36 such as used to transmit the above-noted address information or command and address information as described above can also be reduced when the microelectronic packages attached thereto are constructed according to the principles herein. Specifically, the number of required routing layers may in some cases be reduced to two or fewer routing layers. In a particular example, there may be no more than one routing layer for routing of the above-noted address information, or for routing of all above-noted command signals, address signals, bank address signals, and clock signals of a command-address bus 36. However, on the circuit panel, there may be a greater number of routing layers which carry information other than the above-noted address information or carry signals other than the command-address bus signals.

[0102] In a particular example in which the first terminals of each microelectronic package are disposed at positions within a single column of the grid 104 of the respective microelectronic package, the circuit panel 354 may include no more than one routing layer for global routing of all of the address information between a connection site on the circuit panel at which the terminals of the first and second microelectronic packages 100A, 100B are electrically connected and a different connection site at which the terminals of at

least a third microelectronic package are electrically connected.

[0103] In one embodiment in which the first terminals of each microelectronic package are disposed at positions within no more than two parallel columns of the grid 104 of the respective microelectronic package, the circuit panel 354 may include no more than two routing layers for global routing of all of the address information between a connection site on the circuit panel at which the terminals of the first and second microelectronic packages 100A, 100B are electrically connected and a different connection site at which the terminals of at least a third microelectronic package are electrically connected. In a particular example, in such an embodiment, there may be no more than one routing layer for the above-noted global routing.

[0104] FIG. 7C illustrates a microelectronic assembly such as, for example, a DIMM, among others, incorporating a circuit panel and a plurality of microelectronic packages mounted opposite one another to first and second opposite surfaces thereof. As seen in FIG. 7C, the above-noted address signals or command-address bus signals can be routed on a bus 36, e.g., an address bus or command-address bus on the circuit panel or circuit board 354 in at least one direction 143 between connection sites I, II or III at which respective pairs of microelectronic packages 100A, 110B are connected to opposite sides of the circuit panel. Signals of such bus 36 reach each pair of packages at the respective connection sites I, II or III at slightly different times.

[0105] The at least one direction 143 can be transverse or orthogonal to a direction 142 in which at least one column 138 of a plurality of contacts on at least one microelectronic element within each package 100A or 100B extends. In such way, the signal conductors of the bus 36 on (i.e., on or within) the circuit panel 354 can in some cases be spaced apart from one another in a direction 142 which is parallel to the at least one column 138 of contacts on a microelectronic

element within a package 100A, or 100B connected to the circuit panel.

[0106] Such configuration, particularly when the first terminals 105 of each microelectronic package are arranged in one or more columns 104A, 104B extending in such direction 142, may help simplify the routing of signal conductors of one or more global routing layers on the circuit panel used to route the signals of the bus 36. For example, it may be possible to simplify routing of the command-address bus signals on a circuit panel when relatively few first terminals are disposed at the same vertical layout position on each package. Thus, in the example shown in FIG. 5, only two first terminals are disposed at the same vertical layout position on each package, such as the first terminals configured to receive address signals A3 and A1.

[0107] In an exemplary embodiment, the microelectronic assembly 354 can have a microelectronic element 358 that can include a semiconductor chip configured to perform buffering of at least some signals transferred to the microelectronic packages 100A, 100B of the assembly 354. The microelectronic element 358 can be configured predominantly to perform a logic function, such as a solid state drive controller, and one or more of the microelectronic elements 358 in the microelectronic packages 100A and 100B can each include memory storage elements such as nonvolatile flash memory.

[0108] The microelectronic element 358 can include a special purpose processor that is configured to relieve a central processing unit of a system such as the system 1500 (FIG. 18) from supervision of transfers of data to and from the memory storage elements included in the microelectronic elements 358. Such a microelectronic element 358 including a solid state drive controller can provide direct memory access to and from a data bus on a motherboard (e.g., the circuit panel 1502 shown in FIG. 18) of a system such as the system 1300. In a particular embodiment, the microelectronic element 358 can have a buffering function. Such a microelectronic

element 358 can be configured to help provide impedance isolation for each of the microelectronic elements 358 with respect to components external to the microelectronic assembly 354.

[0109] In a particular embodiment, the first terminals 104 of the microelectronic package can be configured to carry information that controls an operating mode of the microelectronic element 101. More specifically, the first terminals can be configured to carry all of a particular set of command signals and/or clock signals transferred to the microelectronic package 100. In one embodiment, the first terminals 104 can be configured to carry all of the command signals, address signals, bank address signals, and clock signals transferred to the microelectronic package 100 from an external component, wherein the command signals include row address strobe, column address strobe and write enable. In such embodiment, the first chip can be configured to regenerate the information that controls the operating mode. Alternatively, or in addition thereto, the first chip can be configured to partially or fully decode the information that controls the operating mode of the microelectronic element. In such embodiment, each second chip may or may not be configured to fully decode one or more of address information, command information, or information that controls an operating mode of the microelectronic element.

[0110] Microelectronic packages having other arrangements of terminals thereon can be provided. For example, in the microelectronic package 400 illustrated in FIG. 8, four columns 404A, 404B, 404C, and 404D of terminals are disposed in a central region 112 of the substrate surface, these columns containing the first terminals that are configured to carry the above-noted address information, or in a particular embodiment, are configured to carry all of the above-noted command signals, address signals, bank address signals and clock signals used to sample the address signals. In a particular example thereof, second terminals can also be

disposed within the columns 404A, 404B, 404C, 404D, which are configured to carry information other than the above-noted information or signals carried by the first terminals. In another example (not shown), it is also possible for the first terminals of a microelectronic package to be disposed at positions within three columns of terminals.

[0111] In the microelectronic package 500 illustrated in FIGS. 9A and 9B, the first terminals are arranged at positions within a single column 504 disposed in the central region 512 of the substrate surface, the single column extending in a direction parallel to the edges 516, 518 of the microelectronic package. Hereinafter, unless otherwise noted, for ease and clarity of description, the second terminals may be omitted from the figures illustrating various aspects of the invention, although the second terminals may nevertheless be present in such embodiments.

[0112] In the particular example seen in FIG. 9A, the minimum pitch between any two columns of terminals on the substrate is the pitch 552 between the adjacent columns 506B and 506C of second terminals disposed in peripheral region 514B of the substrate surface. The width 554 of the central region is not greater than three and one-half times the minimum pitch 552 between the columns 506B and 506C of terminals.

[0113] FIG. 10A illustrates a microelectronic package 600 according to a particular example in which the microelectronic element includes a vertical stack 630 of an electrically interconnected first semiconductor chip 632 and a plurality of second semiconductor chips 634, each having a contact-bearing face 631 that faces away from the substrate 602. Wire bonds 635 electrically interconnect the contacts 626 on the semiconductor chips 632, 634 with corresponding contacts 636 on the substrate. Spacers 638 can be disposed between adjacent faces of the semiconductor chips 634, and a spacer 638 can be disposed between the contact-bearing face 631 of the semiconductor chip 632 and a rear face of semiconductor

chip 634. In some cases, adhesive layers (not shown) can be provided between each spacer and the faces of the semiconductor chips adjacent to such spacer. As shown in FIG. 10A, the one or more second semiconductor chips 634 are electrically interconnected with the first semiconductor chip 632. For example, as seen in FIG. 10A, there are three vertically stacked second semiconductor chips 634 in which the faces 631 thereof are parallel to one another.

[0114] In the microelectronic package 600 seen in FIG. 10A, each of the first and second semiconductor chips 632, 634 can be configured such that each such semiconductor chip embodies a greater number of active devices to provide memory storage array function than any other function. For example, each of the first and second semiconductor chips may include a memory storage array and all circuitry required for inputting data to and outputting data from the memory storage array. For example, when the memory storage array in each semiconductor chip is writeable, each of the semiconductor chips may include circuitry configured to receive external data input from terminals of the package, as well as circuitry configured to transfer data output from such semiconductor chip to terminals of the package. Thus, each first and each second semiconductor chip 632, 634 can be a dynamic random access memory ("DRAM") chip or other memory chip which is capable of inputting and outputting data from the memory storage array within such semiconductor chip and receiving and transmitting such data to a component external to the microelectronic package. Stated another way, in such case, signals to and from the memory storage array within each DRAM chip or other memory chip does not require buffering by an additional semiconductor chip within the microelectronic package.

[0115] Alternatively, in another example, the one or more second semiconductor chips 634 may embody a greater number of active devices to provide memory storage array function than any other function, but the first semiconductor chip 632 may be a different type of chip. In this case, the first

semiconductor chip 632 can be configured, e.g., designed, constructed, or set up, to buffer signals, i.e., regenerate signals received at the terminals for transfer to the one or more second semiconductor chips 634, or to regenerate signals received from one or more of the second semiconductor chips 634 for transfer to the terminals, or to regenerate signals being transferred in both directions from the terminals to the one or more second semiconductor chips 634; and from the one or more semiconductor chips to the terminals of the microelectronic package. Alternatively or in addition to regenerating signals as described above, in a particular example, the first semiconductor chip can be configured to partially or fully decode at least one of address information or command information received at the terminals, such as at the first terminals. The first chip can then output the result of such partial or full decoding for transfer to the one or more second semiconductor chips 634.

[0116] In a particular example, the first semiconductor chip can be configured to buffer the command signals, address signals and clock signals which are transferred to the one or more second semiconductor chips. For example, the first semiconductor chip 632 can be a buffer chip which embodies a greater number of active devices to provide a buffering function in transferring signals to other devices, e.g., to the one or more second semiconductor chips 634, than for any other function. Then, the one or more second semiconductor chips may be reduced function chips which have memory storage arrays but which can omit circuitry common to DRAM chips, such as buffer circuitry, decoders or predecoders or wordline drivers, among others. In that case, the first chip 632 may function as a "master" chip in the stack and to control operations in each of the second semiconductor chips 634.

[0117] In a particular example, the second semiconductor chips may be configured such that they are not capable of performing the buffering function, and so the stacked arrangement of the first and second semiconductor chips is

configured such that the buffering function required in the microelectronic package can be performed by the first semiconductor chip, and cannot be performed by any of the second semiconductor chips in the stacked arrangement.

[0118] In any of the embodiments described herein, the one or more second semiconductor chips can be implemented in one or more of the following technologies: DRAM, NAND flash memory, RRAM ("resistive RAM" or "resistive random access memory"), phase-change memory ("PCM"), magnetoresistive random access memory, e.g. such as may embodiment tunnel junction devices, static random access memory ("SRAM"), spin-torque RAM, or content-addressable memory, among others.

[0119] FIG. 10B illustrates a variation of the above-described embodiment in which the first semiconductor chip 633 within microelectronic package 601 is configured to buffer at least some signals received at terminals of the package, e.g., the first terminals, for transmission to other semiconductor chips 634 within the package. In this variation, the first semiconductor chip 633 can be mounted to the substrate 602 in flip-chip orientation, i.e., having contacts 643 on a face thereof facing corresponding contacts on the substrate 602 and being joined thereto such as by solder, other bond metal or other conductive material.

[0120] FIG. 11A is a sectional view and FIG. 11B is a corresponding plan view illustrating a microelectronic package 660 according to a further variation in which the second semiconductor chips 634 are mounted in stair-step manner relative to one another such that the contacts of the first semiconductor chip 632 are exposed beyond an edge 618 of the second semiconductor chip 634A immediately above the first semiconductor chip 632, and the contacts of that semiconductor chip 634A are exposed beyond an edge 618 of the second semiconductor chip 634B immediately above that second semiconductor chip. Electrical connections between the first and second chips and the substrate and among the chips can be provided by wire bonds 635 which electrically connect adjacent

chips within the stack of semiconductor chips, or wire bonds 637 which electrically connect the chips directly to the package substrate 662.

[0121] FIG. 12 illustrates a microelectronic package 670 according to a further variation of the embodiment described above relative to FIG. 10, in which connections between contacts of the one or more second semiconductor chips 634 can include traces or leads 640 which extend along one or more edges of a unit of stacked semiconductor chips 630, i.e., along edges of the semiconductor chips 634 within such unit 630. Unit 630 is mounted and electrically interconnected with contacts 627 of the first semiconductor chip 632, such as with a bond metal, e.g., solder, tin, gold, indium, a eutectic, or electrically conductive bumps, or both, which may in some cases include conductive posts, e.g., micropillars. Traces 654 may extend along a face 631 of the first semiconductor chip from the contacts 627 to second contacts 626, which in turn can be electrically connected with the substrate, such as through wire bonds 645.

[0122] The electrical connections between the second semiconductor chips 634 may further include traces 644 which extend along front faces of the second semiconductor chips 634. As further shown in FIG. 12, the front faces 642 of the second semiconductor chips may face upwardly away from the substrate 602 or downwardly towards the substrate 602.

[0123] FIG. 13A further illustrates a microelectronic package 680 in which a second semiconductor chip 634 has contacts 647 facing contacts 627 of the first chip and joined thereto in flip-chip manner, such as through a bond metal, e.g., solder, tin, gold, indium, a eutectic, or electrically conductive bumps, or both. Traces 654 may electrically connect the contacts 627 with other contacts 626 on the first chip that are electrically connected to the substrate, such as through wire bonds.

[0124] FIG. 13B further illustrates a microelectronic package 690 according to a particular example in which the one

or more second semiconductor chips 634 are electrically connected with one another by through-silicon vias ("TSVs") 650 that extend in a direction of the thicknesses 652 of at least some of the second semiconductor chips 634, *i.e.*, in a direction normal to the faces 642 of the chips 634. As seen in FIG. 13B, in one example, the TSVs 650 can be electrically connected with contacts 627 of the first semiconductor chip 632, such as through a bond metal, *e.g.*, solder, tin, gold, indium, a eutectic, or electrically conductive bumps, or both, which may in some cases include conductive posts, *e.g.*, micropillars. Traces 654 may extend along a face 631 of the first semiconductor chip from the contacts 627 to second contacts 626, which in turn can be wire-bonded to the substrate.

[0125] In one example, information or signals received at terminals of the package 690, such as at the first terminals, the second terminals, or both, can be received by the first semiconductor chip 632 through wire bonds 645 that are joined to substrate contacts 636, which in turn are joined to such terminals of the microelectronic package. The first semiconductor chip 632, operating as a buffer element, can then regenerate the received information or signals and then transfer the regenerated information or signals to the one or more second semiconductor chips, *e.g.*, through the connections between the first and second chips 632, 634 and through the TSVs 650 within the stack of second chips 634.

[0126] FIG. 13C illustrates a variation of the microelectronic package shown in FIG. 13B. Unlike the package shown in FIG. 13B, semiconductor chip 664, which is configured to regenerate or at least partially decode address information or other information, *e.g.*, regenerate signals for transfer to other semiconductor chips in the package, is not located adjacent to the first surface 108 of the substrate 602. Rather, in this case, the semiconductor chip 664 can be disposed at a position within the package that overlies one or more other semiconductor chips. For example, as shown in FIG.

13C, the chip 664 at least partially overlies the semiconductor chip 662 that is disposed adjacent to the first surface 108 of the substrate 602 and at least partially overlies semiconductor chips 663A, 663B and 663C which are disposed atop semiconductor chip 662.

[0127] In one example, the semiconductor chips 662 and 663A, 663B and 663C may include memory storage arrays. As in the examples described above, such chips 662, and 663A, 663B and 663C may each incorporate circuits configured to buffer, e.g., temporarily store, data that is to be written to such chip, or data that is being read from such chip, or both. Alternatively, the chips 662, and 663A, 663B and 663C may be more limited in function and may need to be used together with at least one other chip that is configured to temporarily store data that is to be written to such chip or data that is being read from such chip, or both.

[0128] The semiconductor chip 664 can be electrically connected to terminals of the microelectronic package, e.g., to grids in which the first terminals 604 and the second terminals 606 are disposed, through electrically conductive structure, e.g., wire bonds 665, that partially overlies a front face 631 of the semiconductor chip 663A and that connects to contacts 636 exposed at the first surface 108 of the substrate 602. The electrically conductive structure, e.g., the wire bonds 665, can electrically connect to the semiconductor chip 664 through contacts 638 on a chip 663A and through conductors (not shown) that extend along the face 631 of the chip 663A, or along a confronting face 641 of the chip 664, or along the faces 631, 641 of both of the chips 663A, 664. As indicated above, the semiconductor chip 664 may be configured to regenerate or at least partially decode signals or information that it receives through the conductive structure, e.g., the wire bonds 665, and it may be configured to transfer the regenerated or at least partially decoded signals or information to other chips within the package such as to the chips 662, and 663A, 663B and 663C.

[0129] As further seen in FIG. 13C, the semiconductor chips 662, 663A, 663B and 663C can be electrically connected to the semiconductor chip 664 and to one another by a plurality of through-silicon vias ("TSVs") 672, 674, and 676 that can extend through one, two, or three or more of such chips. Each such TSV may electrically connect with wiring within the package, e.g., conductive pads or traces of two or more of the semiconductor chips 662, 663A, 663B and 663C and 664. In a particular example (not shown), through silicon vias may extend through the thicknesses of all semiconductor chips 662, 663A, 663B and 663C, even though each through silicon via may not electrically connect with each such semiconductor chip through which it extends.

[0130] As further seen in FIG. 13C, a heat sink or heat spreader 668, which may include a plurality of fins 671, can be thermally coupled to a face of the semiconductor chip 664, e.g., a rear face 633 thereof, such as through a thermally conductive material such as thermal adhesive, thermally conductive grease, or solder, among others.

[0131] The microelectronic assembly 695 shown in FIG. 13C may be configured to operate as a memory module capable of transferring a designated number of data bits per cycle onto or off of the microelectronic package through the first and second terminals provided therefor on the substrate. For example, the microelectronic assembly may be configured to transfer a number of data bits such as thirty-two data bits, sixty-four data bits, or ninety-six data bits, among other possible configurations, to or from an external component such as a circuit panel that can be electrically connected with the terminals 604, 606. In another example, when the bits transferred to and from the package include error correction code bits, the number of bits transferred per cycle to or from the package may be thirty-six bits, seventy-two bits, or one-hundred-eight bits. Other data widths are possible other than those that are specifically described here.

[0132] FIGS. 14A, 14B, and 15 illustrate a microelectronic package 1100 according to a further variation of one or more of the above-described embodiments. As seen in FIGS. 14A, 14B, and 15, the package 1100 includes first and second microelectronic elements 1130, 1131 that are spaced apart from one another on a first surface 1108 of the substrate 1102. Each microelectronic element 1130, 1131 has first parallel edges 1170 extending away from a face 1142 of the respective microelectronic element which faces away from the substrate 1102, and second parallel edges 1172 that extend in a direction transverse or orthogonal to a direction in which the first edges extend.

[0133] The contacts 1138 of the microelectronic elements are electrically connected with corresponding substrate contacts 1148 on the first surface 1108 of the substrate 1102. In turn, some of the substrate contacts 1148 are electrically connected with first terminals 1104 disposed in a central region 1112 on the second surface 1110, such as through electrically conductive traces 1144, or through electrically conductive vias 1146, or through both traces and vias. In some embodiments, some of the substrate contacts 1148 may instead be electrically connected with second terminals 1162 in one or more peripheral regions 1164 of the second surface. FIG. 14A illustrates possible signal assignments of the terminals 1104, 1162 on the package.

[0134] As in the above-described embodiments, the central region 1112 of the substrate surface 1110 has a width 1154 that is not greater than three and one-half times a minimum pitch 1152 between any two adjacent columns of terminals on the package, where each of the two adjacent columns has a plurality of terminals therein. An axial plane 1150 normal to the surface 1110 of the substrate 1102 intersects the surface 1110 along a line which is parallel to and centered among the first edges 1170 of the first and second microelectronic elements 1130, 1131. In one example, an axis 1151 along which a column of first terminals 1104 extends can be disposed

between adjacent edges 1134, 1135 of the first and second microelectronic elements as shown therein. This can be true for the axes of more than one columns of the terminals.

[0135] Alternatively, although not shown in FIGS. 14A-B and 15, the axis along which a column of the first terminals 1104 extends can overlie one or more of the faces 1140 of the first and second microelectronic elements 1130, 1131, and this may be true for the axes of more than one column. There may be four columns of terminals or fewer in the central region 1112 of the surface 1110. As in the above-described embodiments, there need not be more than a single column of first terminals 1104 in the central region. As further shown in FIG. 15, the faces 1142 of the first and second microelectronic elements can extend within a single plane 1124 parallel to the first surface 1108 of the substrate 1102.

[0136] FIGS. 16A-16B illustrate a microelectronic package 1200 according to a variation of the embodiment seen in FIGS. 14A-B and 15 which, in addition to first and second microelectronic elements 1230, 1231 having the same arrangement and electrical interconnections within the package 1200 as discussed above regarding microelectronic package 1100 (FIGS. 14A-B, 15), further includes third and fourth microelectronic elements 1233 and 1235. Like the first and second microelectronic elements, each of the third and fourth microelectronic elements may embody a greater number of active devices to provide memory storage array function than any other function. Like the first and second microelectronic elements, the third and fourth microelectronic elements 1233 and 1235 are mounted face-up on the substrate 1202 and are electrically interconnected with the first terminals 1204 of the package, such as through electrical connections extending above the respective contact-bearing faces (not shown) of the microelectronic elements. The electrical connections can be wire bonds, as discussed above.

[0137] The terminals 1204 of the microelectronic package can be arranged within a central region 1212 having width 1252

no greater than three and one-half times the minimum pitch between columns of terminals, as described above. As further shown in FIG. 16A, the intersection of the axial plane 1250 with the substrate 1202 can be centered among all of the parallel first edges 1270 of the first, second, third and fourth microelectronic elements within the package 1200.

[0138] In like manner to that described above relative to FIGS. 14A-B and 15, the contact-bearing faces (not shown) of the microelectronic elements 1230, 1231, 1233 and 1235 can be arranged within the package 1200 such that all of such faces are co-planar, *i.e.*, extend within a single plane, *i.e.*, such as a single plane 1124 as illustrated in FIG. 15.

[0139] FIG. 16B illustrates a possible signal assignment of terminals on the package 1200 in which first terminals 1204 are arranged in one or more columns in the central region and second terminals 1206 are arranged in multiple areas near peripheral edges 1260, 1261, 1262 and 1263 of the package. In this case, some of the second terminals 1206 can be disposed at positions within a grid such as grid 1270, and some second terminals can be disposed at positions within a grid such as grid 1272. In addition, some second terminals can be disposed at positions within a grid such as grid 1274, and some second terminals can be disposed at positions within a grid 1276.

[0140] As shown in FIG. 16B, the signal class assignments of the second terminals 1206 in the grid 1276 can be symmetric about a vertical axis 1251 that can extend within the axial plane 1250, and the signal class assignments of the second terminals in the grid 1274 can be symmetric about the vertical axis 1251. As used herein, two signal class assignments can be symmetric with respect to one another if the signal assignments are in the same class of assignments, even if the numerical index within the class differs. Exemplary signal class assignments can include data signals, data strobe signals, data strobe complement signals, and data mask signals. In a particular example, in the grid 1276, the second terminals 1206 having signal assignments DQSH# and

DQSL# are symmetric about the vertical axis 1251 with respect to their signal class assignment, which is data strobe complement, even though those second terminals have different signal assignments.

[0141] As further shown in FIG. 16B, the assignments of the data signals to the spatial positions of the second terminals on the microelectronic package, such as for data signals DQ0, DQ1, ..., for example, can have modulo-X symmetry about the vertical axis 1251. The modulo-X symmetry can help preserve signal integrity in an assembly 300 such as seen in FIG. 7B, in which one or more pairs of first and second packages are mounted opposite one another to a circuit panel, and the circuit panel electrically connects corresponding pairs of second terminals of those first and second packages in each oppositely-mounted package pair. As used herein, when the signal assignments of terminals have "modulo-X symmetry" about an axis, terminals that carry signals that have the same number "modulo-X" are disposed at positions that are symmetric about the axis. Thus, in such assembly 300 such as in FIG. 7B, modulo-X symmetry can permit electrical connections to be made through the circuit panel so that a terminal DQ0 of a first package can be electrically connected through the circuit panel to a terminal DQ8 of the second package that has the same index number modulo X (X being 8 in this case), so that the connection can be made in a direction essentially straight through, *i.e.*, normal to, the thickness of the circuit panel.

[0142] In one example, "X" can be a number 2^n (2 to the power of n), wherein n is greater than or equal to 2, or X can be $8 \times N$, N being two or more. Thus, in one example, X may be equal to the number of bits in a half-byte (4 bits), byte (8 bits), multiple bytes ($8 \times N$, N being two or more), a word (32 bits) or multiple words. In such way, in one example, when there is modulo-8 symmetry as shown in FIG. 16B, the signal assignment of a package terminal DQ0 in grid 1274 configured to carry data signal DQ0 is symmetric about the vertical axis

1251 with the signal assignment of another package terminal configured to carry data signal DQ8. Moreover, the same is true for the signal assignments of package terminals DQ0 and DQ8 in grid 1276. As further seen in FIG. 16B, the signal assignments of package terminals DQ2 and DQ10 in grid 1274 have modulo-8 symmetry about the vertical axis, and the same is also true for grid 1276. Modulo-8 symmetry such as described herein can be seen in grids 1274, 1276 with respect to each of the signal assignments of package terminals DQ0 through DQ15.

[0143] It is important to note that, although not shown, the modulo number "X" can be a number other than 2^n (2 to the power of n) and can be any number greater than two. Thus, the modulo number X upon which the symmetry is based can depend upon how many bits are present in a data size for which the package is constructed or configured. For example, when the data size is 10 bits instead of 8, then the signal assignments may have modulo-10 symmetry. It may even be the case that when the data size has an odd number of bits, the modulo number X can have such number.

[0144] FIGS. 17A and 17B illustrate a microelectronic package 1300 according to a variation of the embodiment 1200 described above relative to FIGS. 16A and 16B, the package 1300 having a substrate surface 1310 having a central region 1312 in which first terminals 1304 are disposed. As seen therein, microelectronic elements 1330, 1331 are arranged on substrate 1302 in a manner similar to the arrangement of microelectronic elements 1130, 1131 of microelectronic package 1100 (FIGS. 14A-B, 15), in that edges 1360 of adjacent microelectronic elements 1130, 1131 are parallel to each other and extend in the same first direction 1342. Edges 1362 of microelectronic elements extend in a direction 1344 transverse to, and typically orthogonal to the direction 1342.

[0145] In some cases, the first edges 1360 of a respective microelectronic element can have greater length than the second edges 1362 of such microelectronic element. However,

in other cases, the second edges 1362 can have greater length than the first edges 1360. In the particular package seen in FIG. 17A, a plane 1370 that contains either first edge 1360 of any of the microelectronic elements 1330, 1331, 1332, or 1333 and which is normal to the face of such microelectronic element intersects the edge 1360 of another microelectronic element within the package 1300. For example, as shown in FIG. 17A, the plane 1370 that contains the edge 1360 of microelectronic element 1333 extends in direction 1344 and intersects the edge 1360 of microelectronic element 1330 within the package. In a particular embodiment, planes 1370A and 1370B that contain the first edges of microelectronic element 1333 intersect the first edge of no more than one other microelectronic element within the package. Thus, plane 1370A intersects edges 1360 of only microelectronic element 1330.

[0146] In addition, as further seen in FIG. 17A, the central region 1312 can be further limited. Specifically, FIG. 17A shows that there is a rectangular subsection area 1372 on the surface 1302 of the substrate 1302, beyond which none of the faces of the first, second, third and fourth microelectronic elements 1330, 1331, 1332 and 1333 extend. In the microelectronic package 1300 depicted in FIGS. 17A-17B, the central region 1312 does not extend beyond the boundaries of such rectangular subsection area 1372.

[0147] FIG. 17B further illustrates a possible arrangement of terminals within microelectronic package 1300 in which first terminals 1304 are disposed within the central region 1312 which spans a width 1354 in a direction orthogonal to opposed edges 1316, 1318 of the package that is no greater than three and one-half times the minimum pitch between the closest two adjacent columns of terminals on the package. Peripheral regions take up the remaining area of the surface 1310 of the substrate 1302, spanning widths 1356, 1357 between edges of the central region and the opposed edges 1316, 1318 of the package, respectively.

[0148] The microelectronic packages and microelectronic assemblies described above with reference to FIGS. 5 through 17B can be utilized in construction of diverse electronic systems, such as the system 1500 shown in FIG. 18. For example, the system 1500 in accordance with a further embodiment of the invention includes a plurality of modules or components 1506 such as the microelectronic packages and/or microelectronic assemblies as described above in conjunction with other electronic components 1508 and 1510.

[0149] In the exemplary system 1500 shown, the system can include a circuit panel, motherboard, or riser panel 1502 such as a flexible printed circuit board, and the circuit panel can include numerous conductors 1504, of which only one is depicted in FIG. 18, interconnecting the modules or components 1506 with one another. Such a circuit panel 1502 can transport signals to and from each of the microelectronic packages and/or microelectronic assemblies included in the system 1500. However, this is merely exemplary; any suitable structure for making electrical connections between the modules or components 1506 can be used.

[0150] In a particular embodiment, the system 1500 can also include a processor such as the semiconductor chip 1508, such that each module or component 1506 can be configured to transfer a number N of data bits in parallel in a clock cycle, and the processor can be configured to transfer a number M of data bits in parallel in a clock cycle, M being greater than or equal to N .

[0151] In one example, the system 1500 can include a processor chip 1508 that is configured to transfer thirty-two data bits in parallel in a clock cycle, and the system can also include four modules 1506 such as the microelectronic package 100 described with reference to FIG. 5, each module 1506 configured to transfer eight data bits in parallel in a clock cycle (*i.e.*, each module 1506 can include first and second microelectronic elements, each of the two

microelectronic elements being configured to transfer four data bits in parallel in a clock cycle).

[0152] In another example, the system 1500 can include a processor chip 1508 that is configured to transfer sixty-four data bits in parallel in a clock cycle, and the system can also include four modules 1506 such as the microelectronic package 1200 described with reference to FIGS. 16A-B, each module 1506 configured to transfer sixteen data bits in parallel in a clock cycle (*i.e.*, each module 1506 can include four microelectronic elements, each of the four microelectronic elements being configured to transfer four data bits in parallel in a clock cycle).

[0153] In the example depicted in FIG. 18, the component 1508 is a semiconductor chip and component 1510 is a display screen, but any other components can be used in the system 1500. Of course, although only two additional components 1508 and 1510 are depicted in FIG. 18 for clarity of illustration, the system 1500 can include any number of such components.

[0154] Modules or components 1506 and components 1508 and 1510 can be mounted in a common housing 1501, schematically depicted in broken lines, and can be electrically interconnected with one another as necessary to form the desired circuit. The housing 1501 is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen 1510 can be exposed at the surface of the housing. In embodiments where a structure 1506 includes a light-sensitive element such as an imaging chip, a lens 1511 or other optical device also can be provided for routing light to the structure. Again, the simplified system shown in FIG. 18 is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like can be made using the structures discussed above.

[0155] The microelectronic packages and microelectronic assemblies described above with reference to FIGS. 5-17B can also be utilized in construction of an electronic system such

as the system 1600 shown in FIG. 19. For example, the system 1600 in accordance with a further embodiment of the invention is the same as the system 1500 shown in FIG. 18, except the component 1506 has been replaced by a plurality of components 1606.

[0156] Each of the components 1606 can be or can include one or more of the microelectronic packages or microelectronic assemblies described above with reference to FIGS. 5-17B. In a particular example, one or more of the components 1606 can be a variation of the microelectronic assembly 300 shown in FIG. 7B, in which the circuit panel 354 includes exposed edge contacts, and the circuit panel 354 of each microelectronic assembly 300 can be suitable for insertion into a socket 1605.

[0157] Each socket 1605 can include a plurality of contacts 1607 at one or both sides of the socket, such that each socket 1605 can be suitable for mating with corresponding exposed edge contacts of a corresponding component 1606 such as the above-described variation of the microelectronic assembly 300. In the exemplary system 1600 shown, the system can include a second circuit panel 1602 or motherboard such as a flexible printed circuit board, and the second circuit panel can include numerous conductors 1604, of which only one is depicted in FIG. 19, interconnecting the components 1606 with one another.

[0158] In a particular example, a module such as the system 1600 can include a plurality of components 1606, each component 1606 being the above-described variation of the microelectronic assembly 300. Each component 1606 can be mounted to, and electrically connected with the second circuit panel 1602 for transport of signals to and from each component 1606. The specific example of the system 1600 is merely exemplary; any suitable structure for making electrical connections between the components 1606 can be used.

[0159] Various features of the above-described embodiments of the invention can be combined in ways other than as specifically described above without departing from the scope

or spirit of the invention. It is intended for the present disclosure to cover all such combinations and variations of embodiments of the invention described above.

[0160] It will be appreciated that the various dependent claims and the features set forth therein can be combined in different ways than presented in the initial claims. It will also be appreciated that the features described in connection with individual embodiments may be shared with others of the described embodiments.

CLAIMS:

1. A microelectronic package, comprising:
 - a substrate having a first surface, a second surface opposite the first surface, and a plurality of substrate contacts exposed at the first surface, the second surface extending in a first direction and in a second direction transverse thereto;
 - a microelectronic element having memory storage array function, the microelectronic element having a rear face facing the first surface, a front face opposite the first surface, and first and second opposed edges each extending between the front and rear faces and extending in the first direction parallel to the front face, the microelectronic element having one or more columns of element contacts exposed at the front face, each column extending in a first direction along the front face, such that an axial plane normal to the front face intersects the front face along a line extending in the first direction and is centered relative to the one or more columns of element contacts;
 - conductive structure electrically connecting the element contacts with the substrate contacts; and
 - a plurality of parallel columns of terminals extending in the first direction exposed at the second surface and electrically connected with the substrate contacts, the terminals including first terminals exposed in a central region of the second surface of the substrate, the first terminals configured to carry address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the microelectronic element, and
- wherein the central region has a width in the second direction, the width of the central region not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals, and the axial plane intersects the central region.

2. The microelectronic package as claimed in claim 1, wherein each of the first and second microelectronic elements embodies a greater number of active devices to provide memory storage array function than any other function.

3. The microelectronic package as claimed in claim 1, wherein the first terminals are configured to carry all of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

4. The microelectronic package as claimed in claim 1, wherein the first terminals are configured to carry information that controls an operating mode of the microelectronic element.

5. The microelectronic package as claimed in claim 4, wherein the first terminals are configured to carry all of the command signals transferred to the microelectronic package, the command signals being write enable, row address strobe, and column address strobe signals.

6. The microelectronic package as claimed in claim 1, wherein the first terminals are configured to carry clock signals transferred to the microelectronic package which are clocks used for sampling signals carrying the address information.

7. The microelectronic package as claimed in claim 1, wherein the first terminals are configured to carry all of the bank address signals transferred to the microelectronic package.

8. The microelectronic package as claimed in claim 1, wherein the terminals are configured to connect the microelectronic package to at least one component external to the microelectronic package.

9. The microelectronic package as claimed in claim 1, wherein the element contacts include redistribution contacts exposed at the front face of the microelectronic element, each

redistribution contact being electrically connected with a contact pad of the microelectronic element through at least one of a trace or a via.

10. The microelectronic package as claimed in claim 1, wherein the conductive structure includes wire bonds extending from the element contacts and electrically connected with the substrate contacts.

11. The microelectronic package as claimed in claim 1, wherein the first terminals are arranged in no more than two of the columns of terminals.

12. The microelectronic package as claimed in claim 1, wherein the first terminals are arranged in a single one of the columns of terminals.

13. The microelectronic package as claimed in claim 1, wherein the first terminals are arranged in no more than four of the columns of terminals.

14. The microelectronic package as claimed in claim 1, wherein the substrate has first and second opposed edges between the first and second opposed surfaces, the first and second edges extending in the first direction, the second surface having first and second peripheral regions adjacent to the first and second edges, respectively, wherein the central region separates the first and second peripheral regions,

the terminals including a plurality of second terminals exposed at the second surface in at least one of the peripheral regions, at least some of the second terminals configured to carry information other the address information.

15. The microelectronic package as claimed in claim 14, wherein at least some of the second terminals are configured to carry data signals.

16. The microelectronic package as claimed in claim 1, wherein the substrate includes a dielectric element having a coefficient of thermal expansion ("CTE") in the plane of the

dielectric element of less than 30 parts per million per degree Celsius ("ppm/°C").

17. The microelectronic package as claimed in claim 1, wherein the substrate includes an element having a CTE of less than 12 ppm/°C.

18. A microelectronic package, comprising:

a substrate having a first surface, a second surface opposite the first surface, and a plurality of substrate contacts exposed at the first surface, the second surface extending in a first direction and in a second direction transverse thereto;

a microelectronic element having memory storage array function, the microelectronic element having a rear face facing the first surface, a front face opposite the first surface, and first and second opposed edges each extending between the front and rear faces and extending in the first direction parallel to the front face, the microelectronic element having one or more columns of element contacts exposed at the front face, each column extending in a first direction along the front face, such that an axial plane normal to the front face intersects the front face along a line extending in the first direction and is centered relative to the one or more columns of element contacts;

conductive structure electrically connecting the element contacts with the substrate contacts; and

a plurality of parallel columns of terminals extending in the first direction along the second surface and electrically connected with the substrate contacts, the terminals including first terminals exposed at the second surface in a central region of the second surface of the substrate, the first terminals configured to carry a majority of the address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the microelectronic element, and

wherein the central region has a width in the second direction, the width of the central region not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals, and the axial plane intersects the central region.

19. The microelectronic package as claimed in claim 18, wherein the terminals are configured to carry at least three-quarters of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

20. A microelectronic package, comprising:
a substrate having first and second opposed surfaces, a plurality of first substrate contacts exposed at the first surface and a plurality of second substrate contacts exposed at the first surface, the first and second surfaces extending in a first direction and in a second direction transverse thereto; and

first and second microelectronic elements each having memory storage array function, the first and second microelectronic elements being spaced apart from one another on the first surface, and having parallel first edges each extending in the first direction, wherein an axial plane normal to the first surface of the substrate extends in the first direction and is centered among the first edges, the first and second microelectronic elements having rear faces facing the first surface, front faces opposite the rear faces, and a plurality of contacts exposed at the front faces;

conductive structure electrically connecting the contacts of the first and second microelectronic elements with the first and second substrate contacts, respectively; and

a plurality of parallel columns of terminals exposed at the second surface and electrically connected with the first and second substrate contacts, the terminals including first terminals exposed in a central region of the second surface of the substrate, the first terminals configured to carry address

information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the first and second microelectronic elements, and

wherein the central region has a width in the second direction, the width of the central region not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals, and the axial plane intersects the central region.

21. The microelectronic package as claimed in claim 20, wherein each of the first and second microelectronic elements embodies a greater number of active devices to provide memory storage array function than any other function.

22. The microelectronic package as claimed in claim 20, wherein the first terminals are configured to carry all of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

23. The microelectronic package as claimed in claim 20, wherein the first terminals are configured to carry information that controls an operating mode of a microelectronic element of the first and second microelectronic elements.

24. The microelectronic package as claimed in claim 20, wherein the first terminals are configured to carry clock signals and all of the command signals, address signals, and bank address signals transferred to the microelectronic package, the command signals being write enable, row address strobe, and column address strobe, and the clock signals being clocks used for sampling signals carrying the address information.

25. The microelectronic package as claimed in claim 20, wherein the front faces of the first and second

microelectronic elements extend in a single plane parallel to the first surface of the substrate.

26. The microelectronic package as claimed in claim 20, wherein the conductive structure includes wire bonds extending from the contacts of the first and second microelectronic elements and electrically connected with the respective first and second substrate contacts.

27. The microelectronic package as claimed in claim 20, wherein the first terminals are arranged in no more than four of the columns of terminals.

28. The microelectronic package as claimed in claim 20, wherein the contacts of each of the microelectronic elements include redistribution contacts exposed at the front face of the respective microelectronic element, each redistribution contact being electrically connected with a contact pad of the respective microelectronic element through at least one of a trace or a via, at least some of the redistribution contacts being displaced from the contacts of the respective microelectronic element in at least one direction along the front face of the microelectronic element.

29. The microelectronic package as claimed in claim 20, wherein the substrate has first and second opposed edges between the first and second opposed surfaces, the first and second edges extending in the first direction, the second surface having first and second peripheral regions adjacent to the first and second edges, respectively, wherein the central region separates the first and second peripheral regions,

the terminals including a plurality of second terminals exposed at the second surface in at least one of the peripheral regions, at least some of the second terminals configured to carry information other than the address information.

30. The microelectronic package as claimed in claim 29, wherein at least some of the second terminals are configured to carry data signals.

31. A microelectronic package, comprising:

a substrate having first and second opposed surfaces, a plurality of first substrate contacts exposed at the first surface and a plurality of second substrate contacts exposed at the first surface, the first and second surfaces extending in a first direction and in a second direction transverse thereto; and

first and second microelectronic elements each embodying a greater number of active devices to provide memory storage array function than any other function, the first and second microelectronic elements being spaced apart from one another on the first surface, and having parallel first edges each extending in the first direction, wherein an axial plane normal to the first surface of the substrate extends in the first direction and is centered among the first edges, the first and second microelectronic elements having rear faces facing the first surface, front faces opposite the rear faces, and a plurality of contacts exposed at the front faces;

conductive structure extending above the front faces electrically connecting the contacts of the first and second microelectronic elements with the first and second substrate contacts, respectively; and

a plurality of parallel columns of terminals exposed at the second surface and electrically connected with the first and second substrate contacts, the terminals including first terminals exposed in a central region of the second surface of the substrate, the first terminals configured to carry a majority of the address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array of the first and second microelectronic elements, and

wherein the central region has a width in the second direction, the width of the central region not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals, and the axial plane intersects the central region.

32. The microelectronic package as claimed in claim 31, wherein the terminals are configured to carry at least three-quarters of the address information usable by the circuitry within the package to determine the addressable memory location in the memory storage array.

FIG. 1
(PRIOR ART)

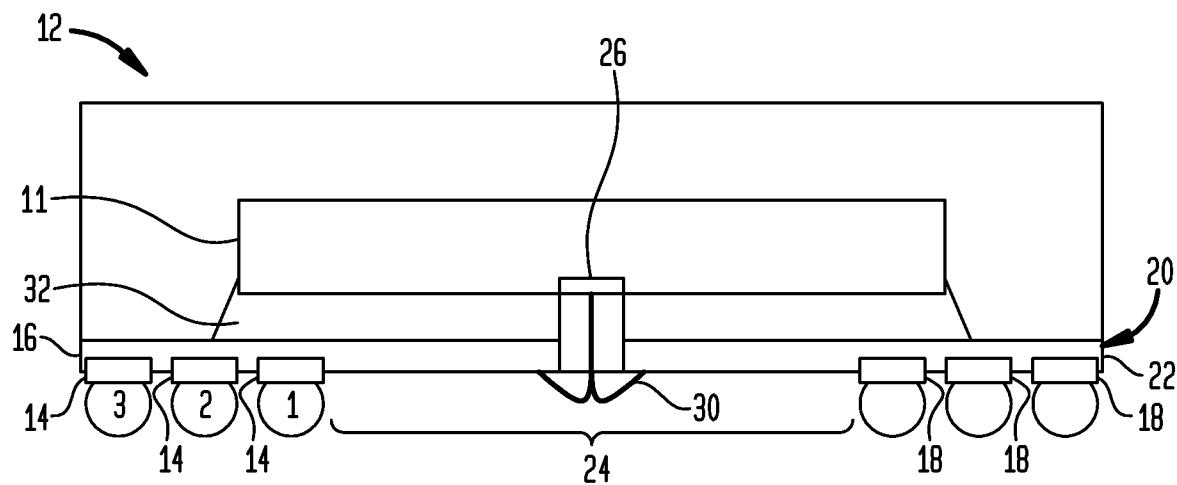


FIG. 2

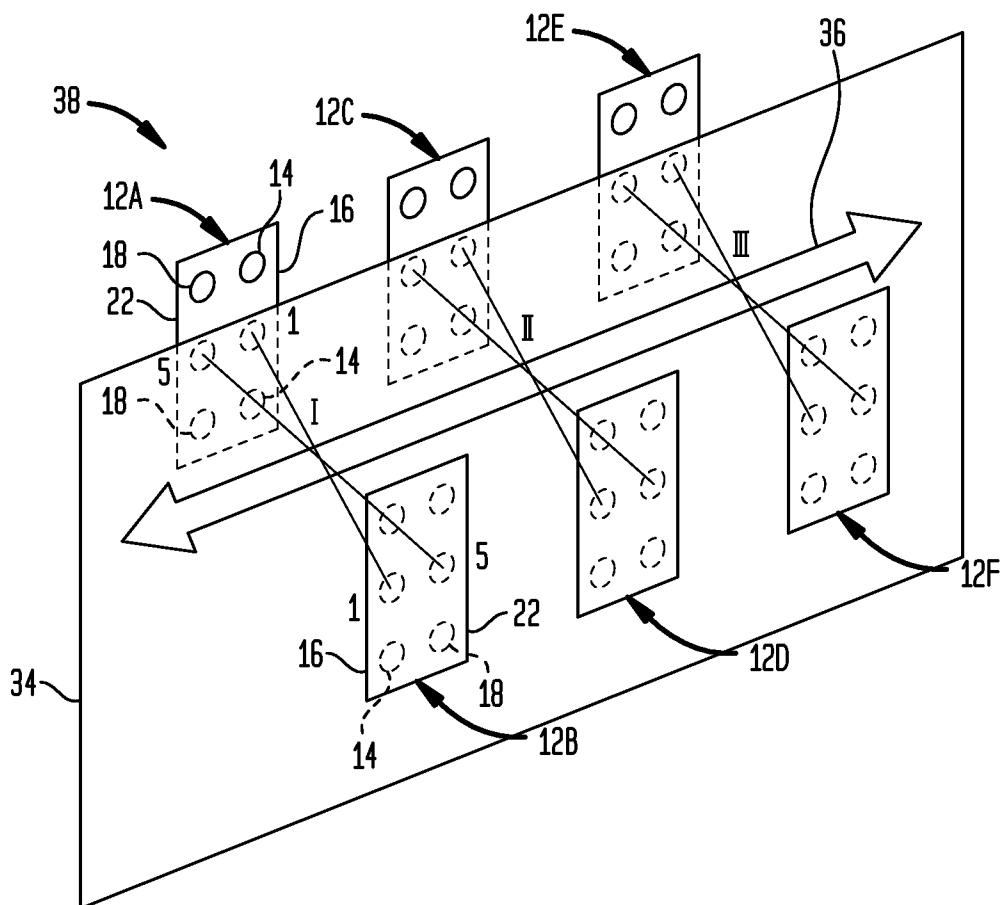
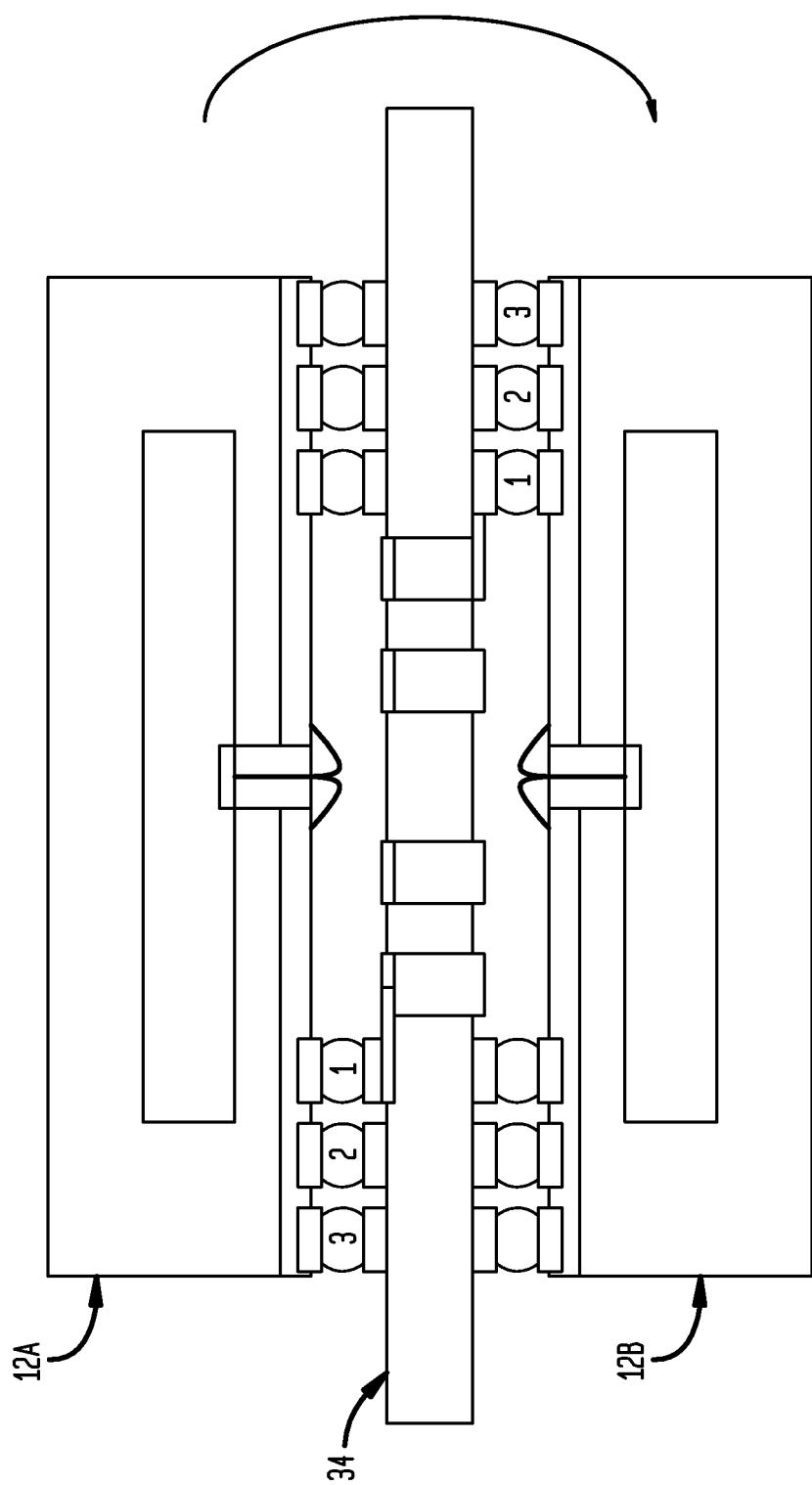
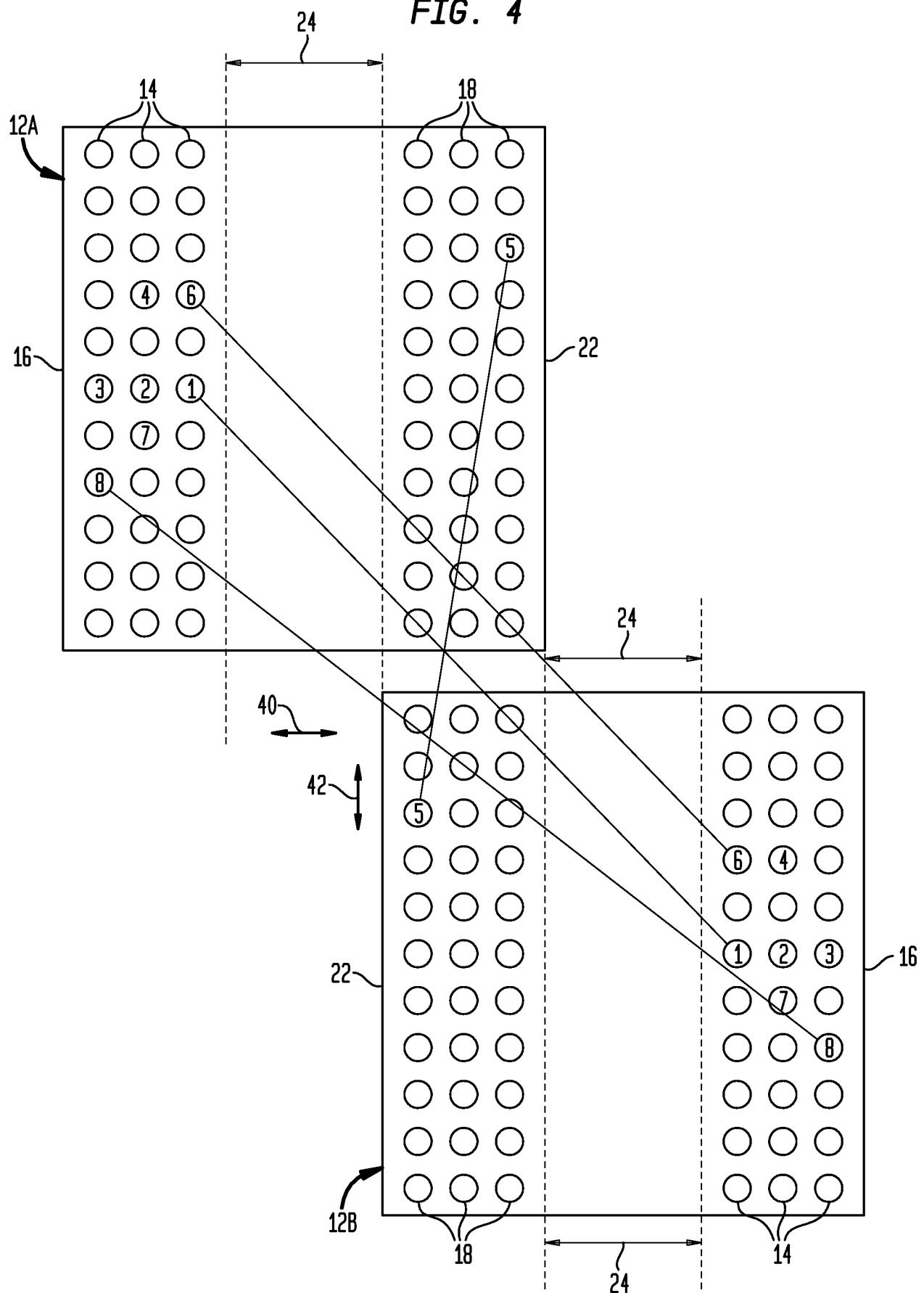


FIG. 3



3/22
FIG. 4

4/22

FIG. 5

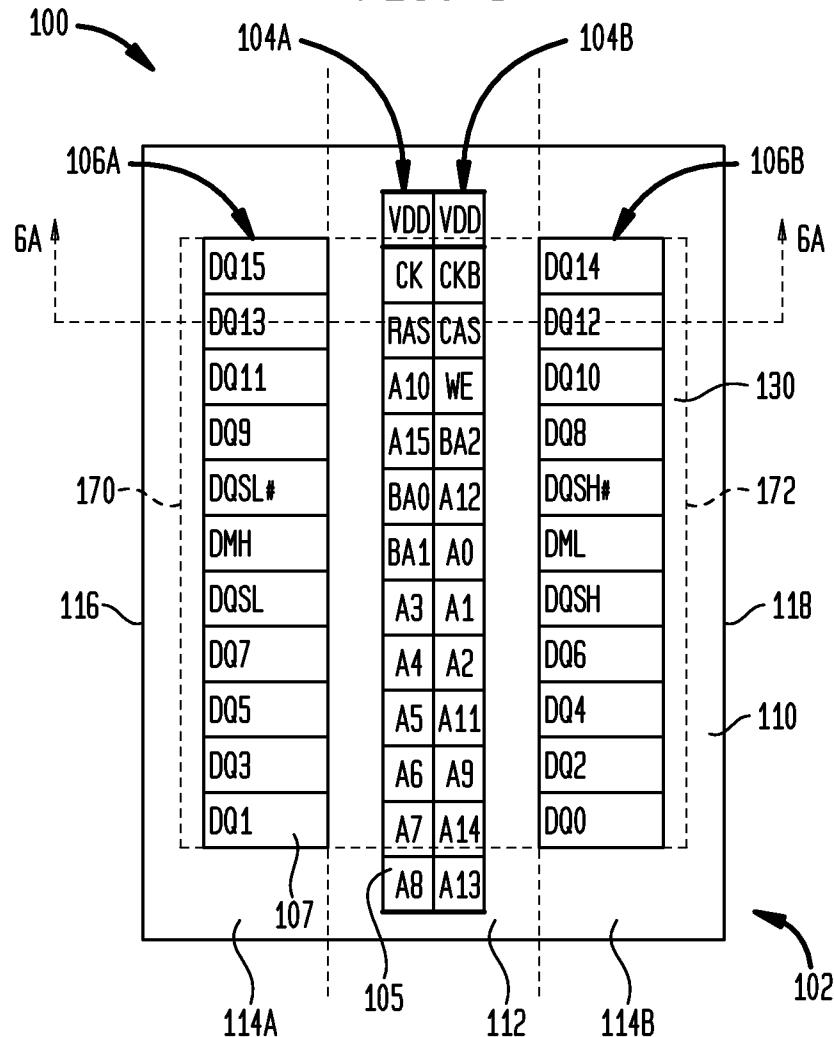
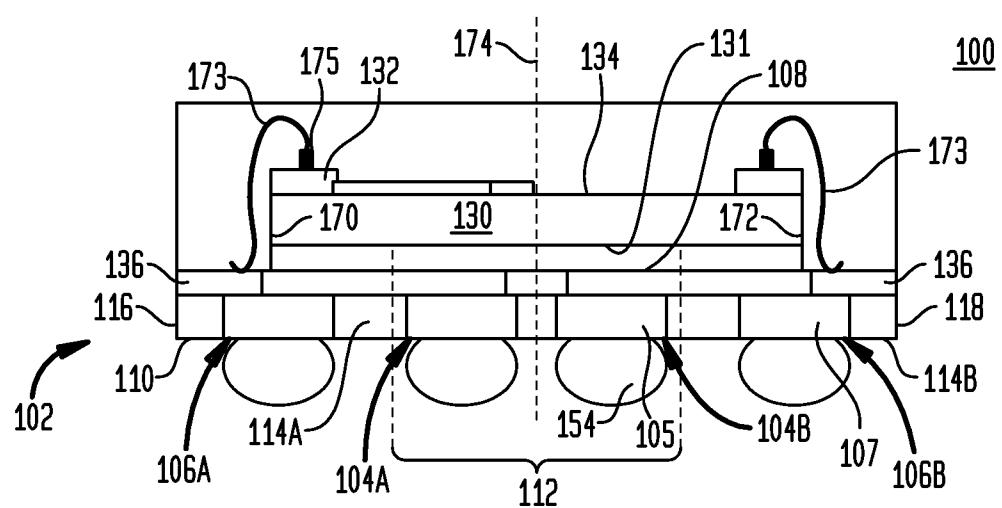


FIG. 6A



5/22

FIG. 6B

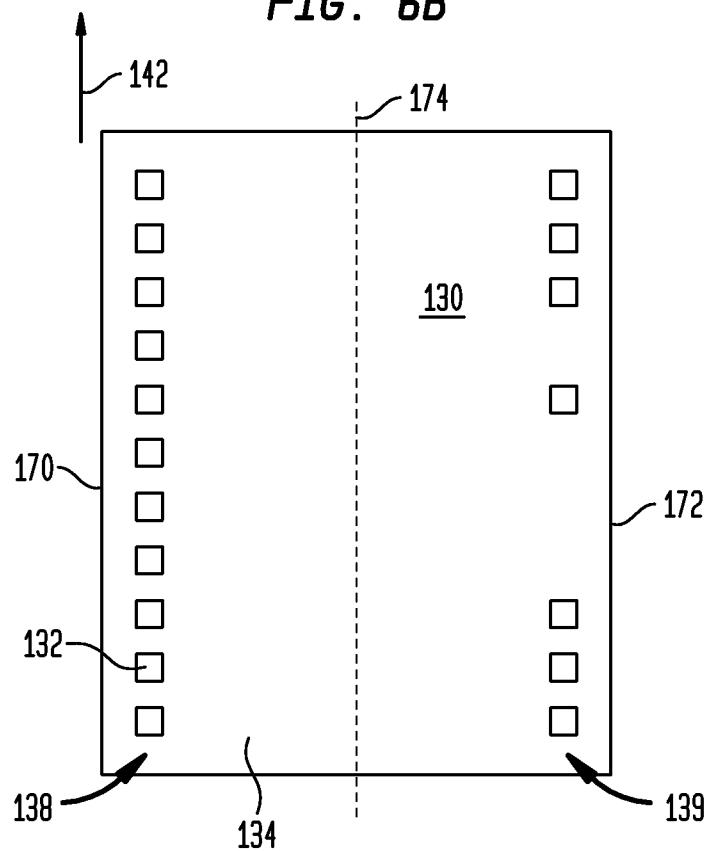


FIG. 6C

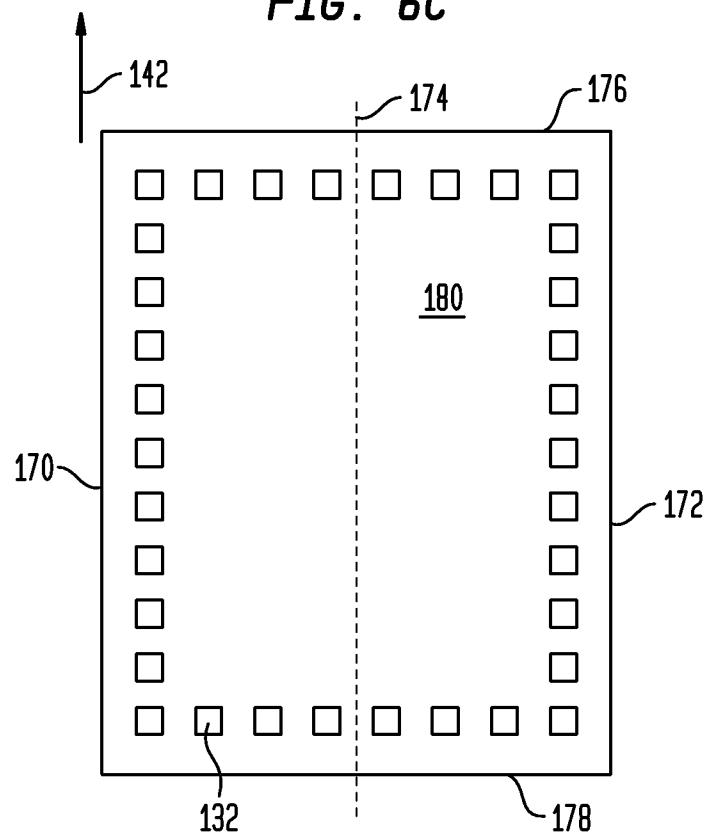


FIG. 6D

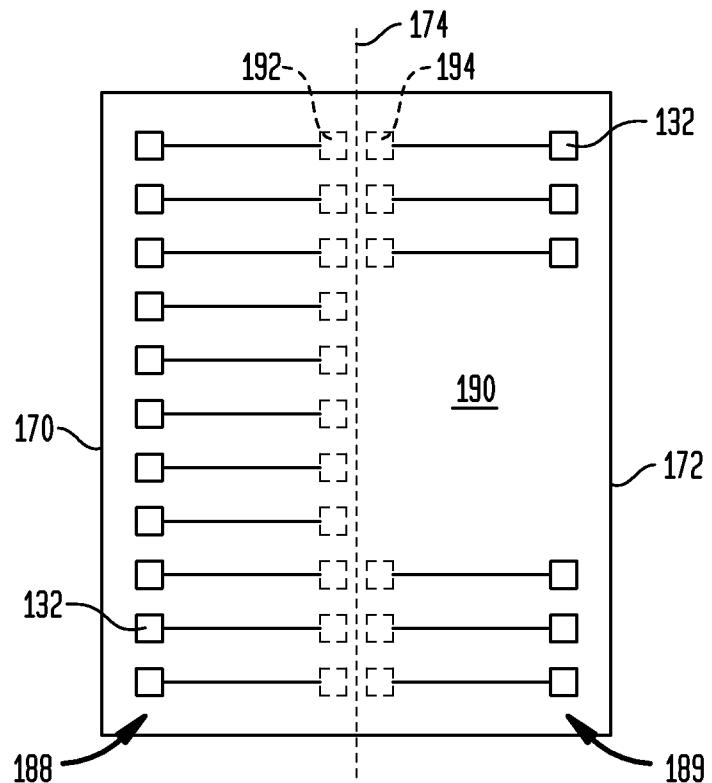


FIG. 6E

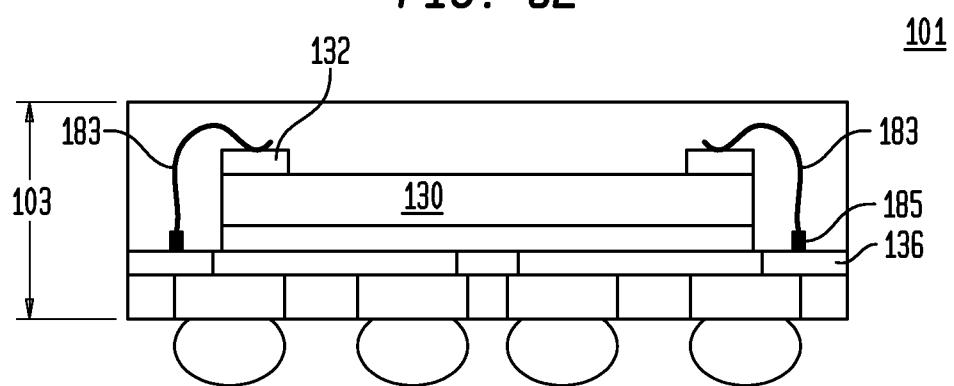


FIG. 7A

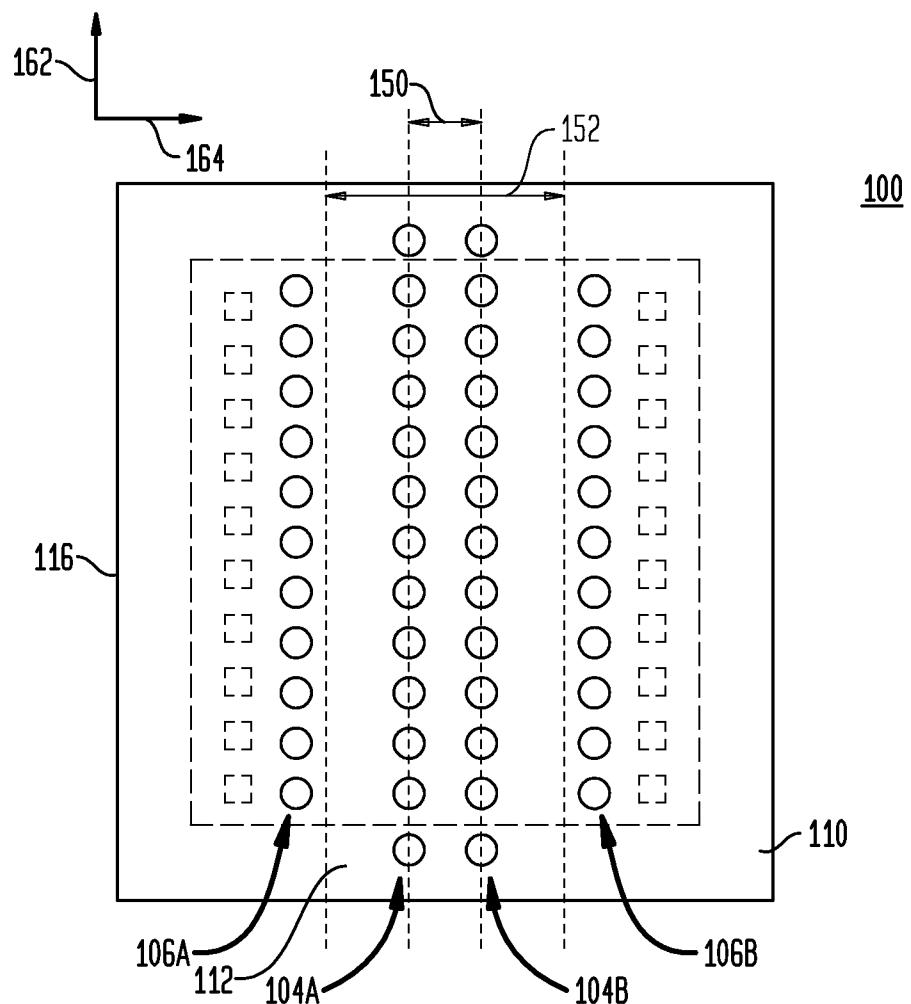


FIG. 7B

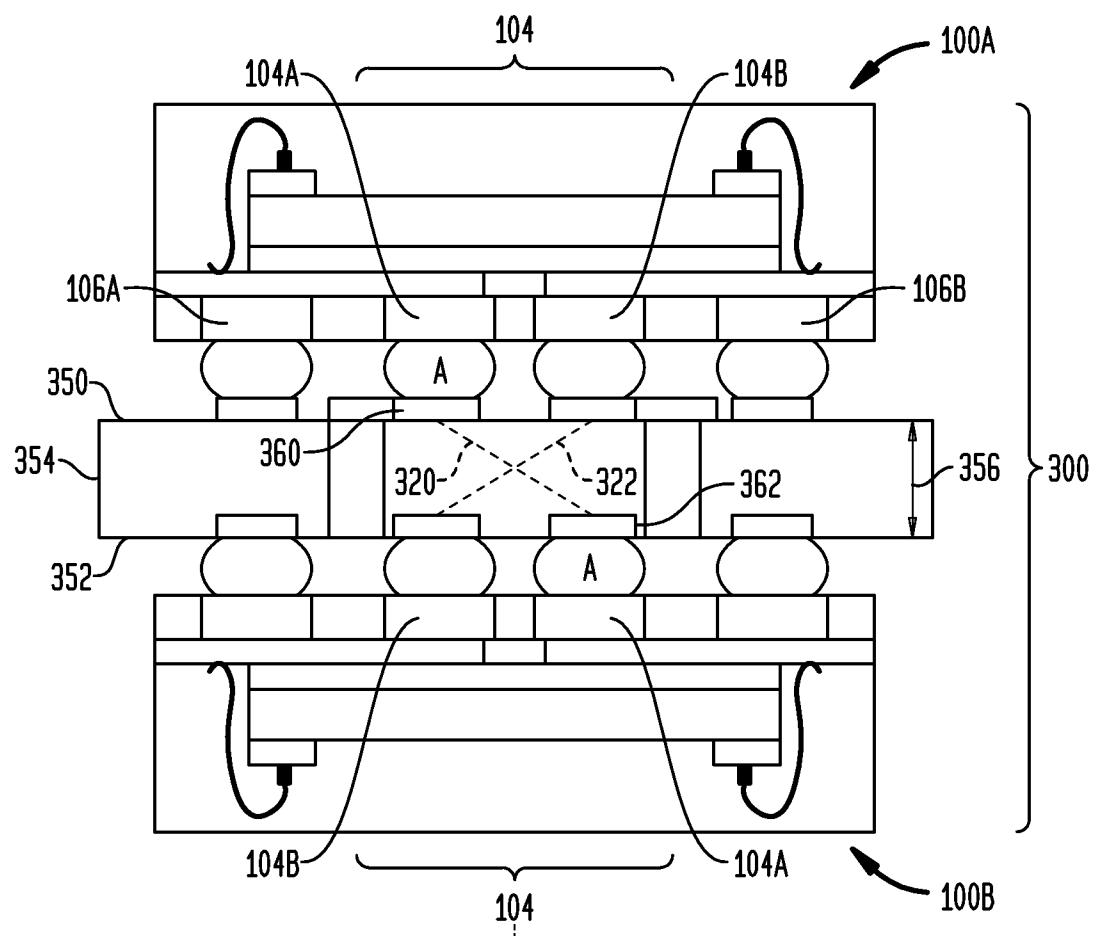


FIG. 7C

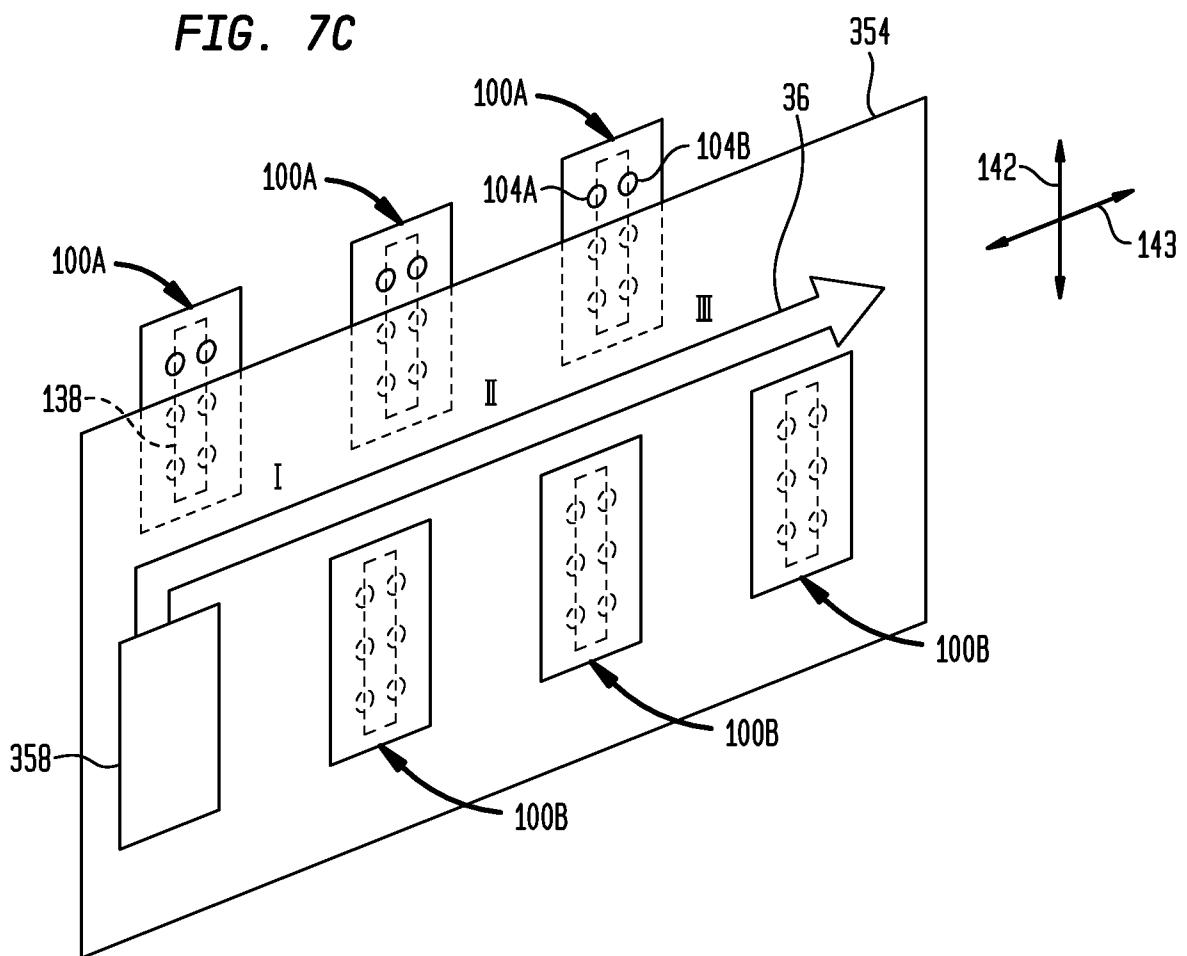


FIG. 8

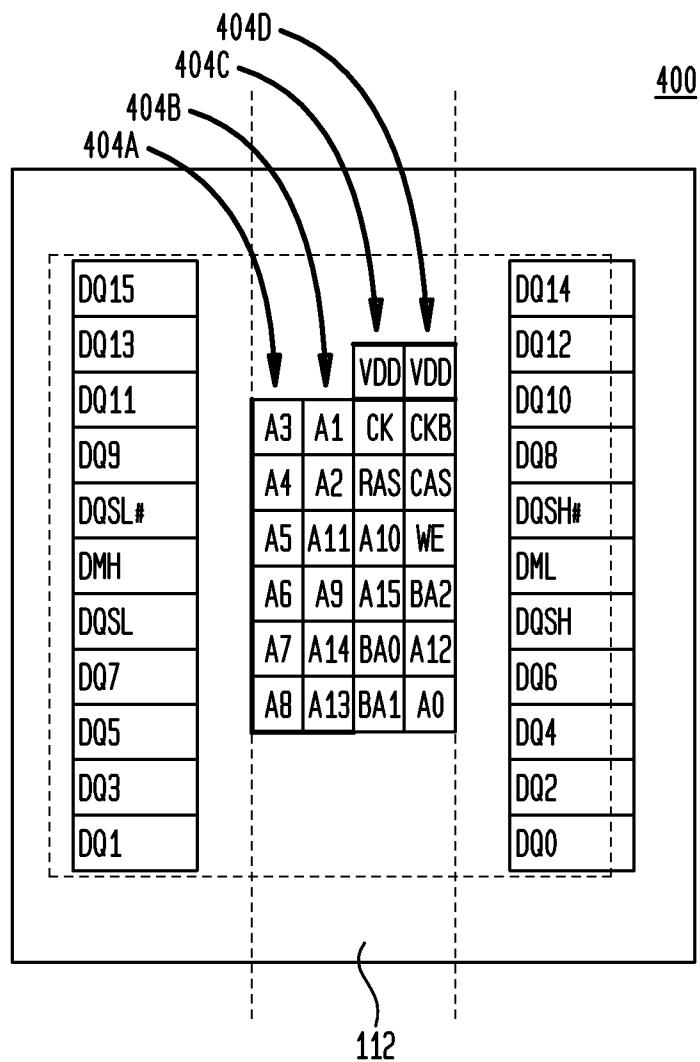


FIG. 9A

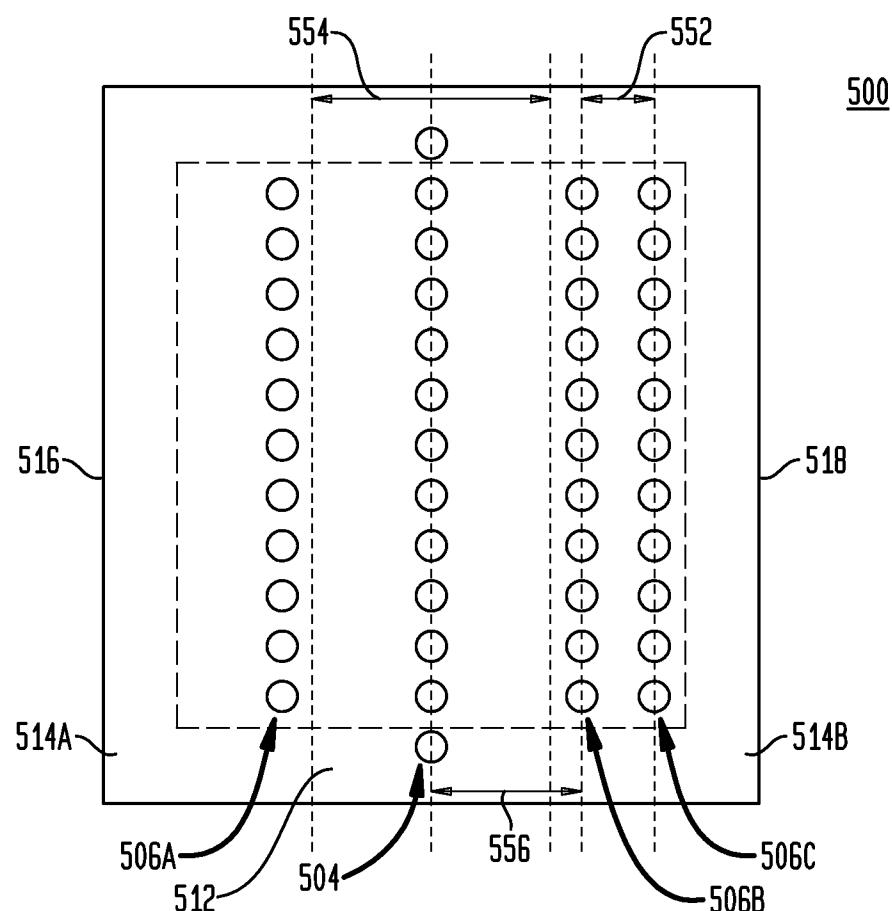


FIG. 9B

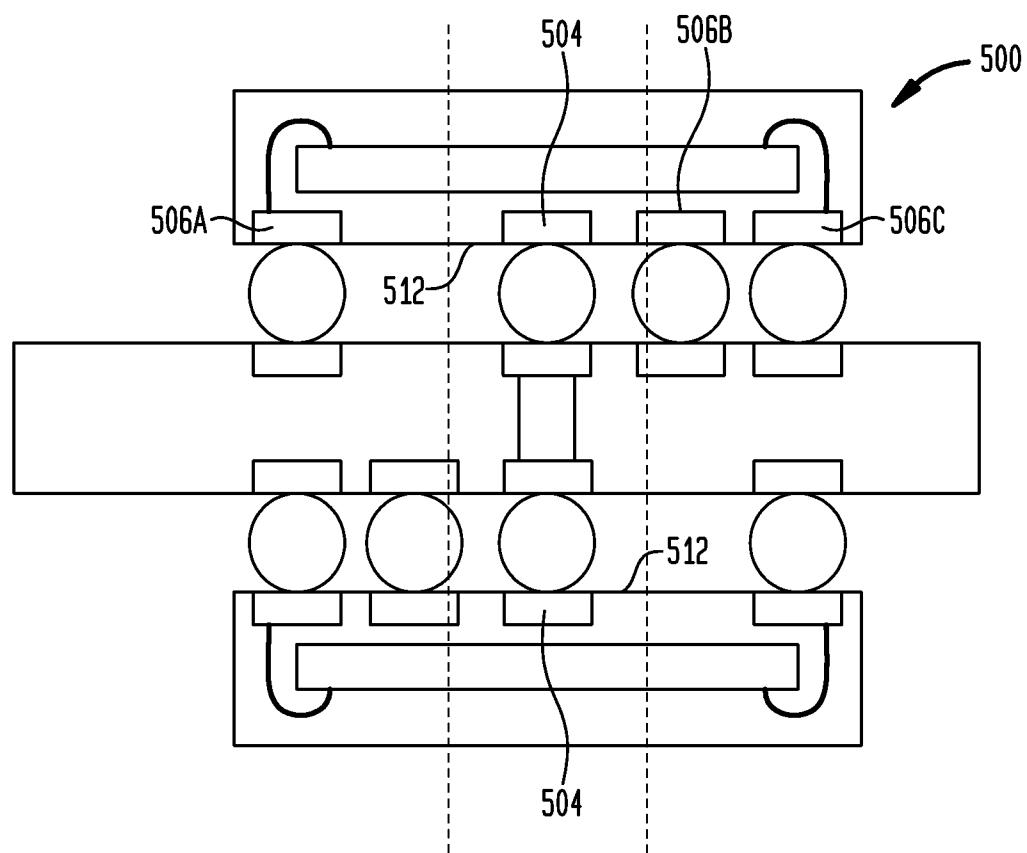


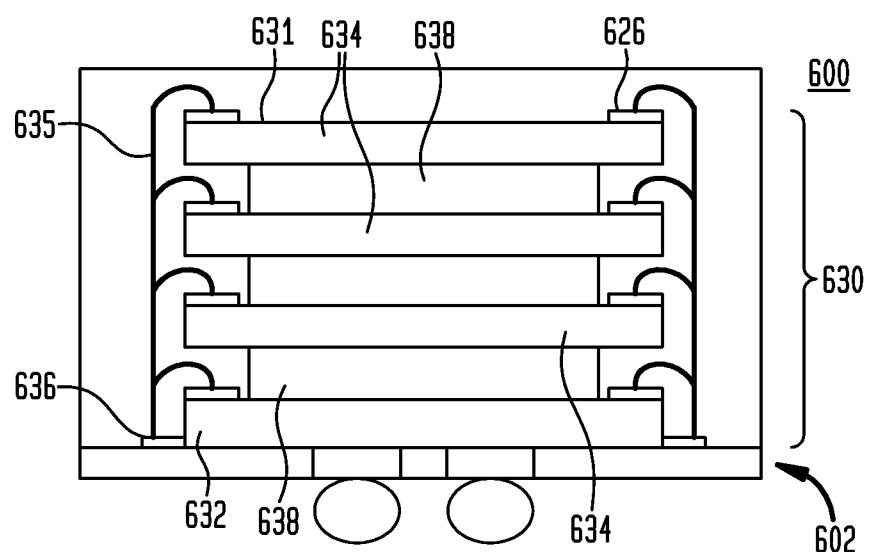
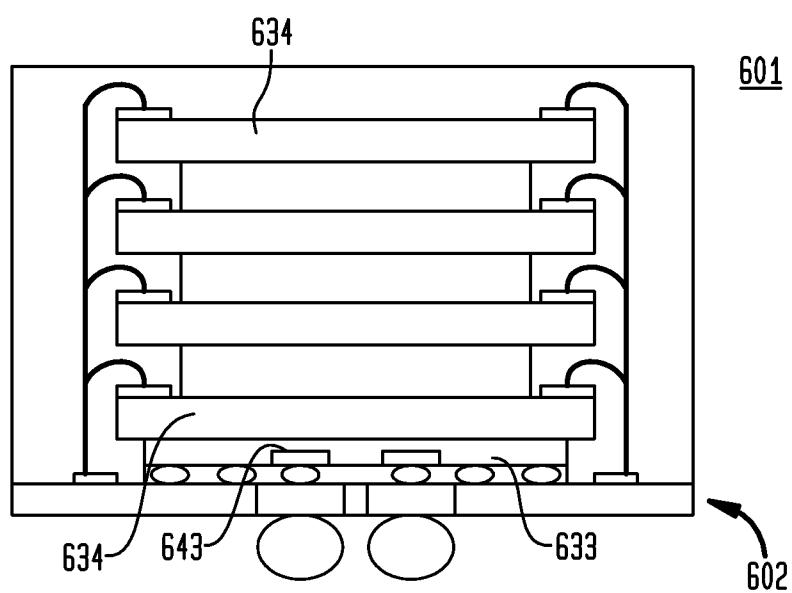
FIG. 10A*FIG. 10B*

FIG. 11A

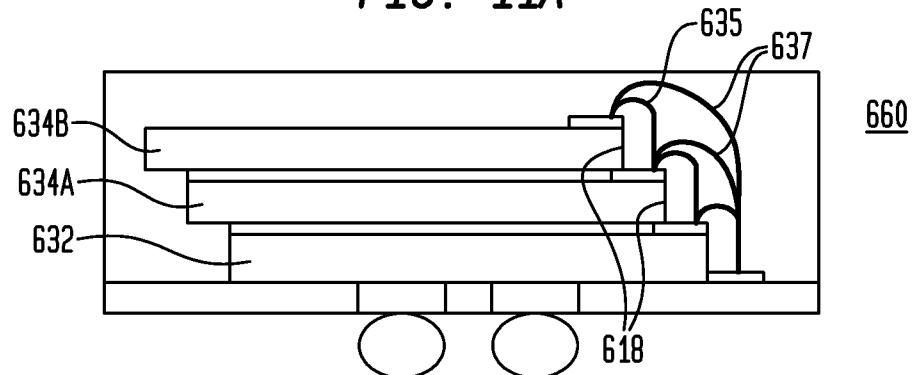
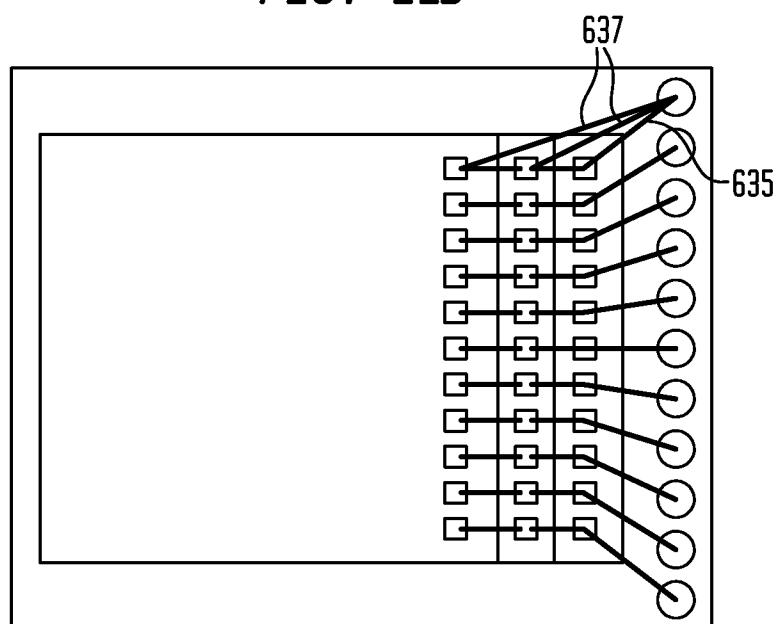


FIG. 11B



15/22
FIG. 12

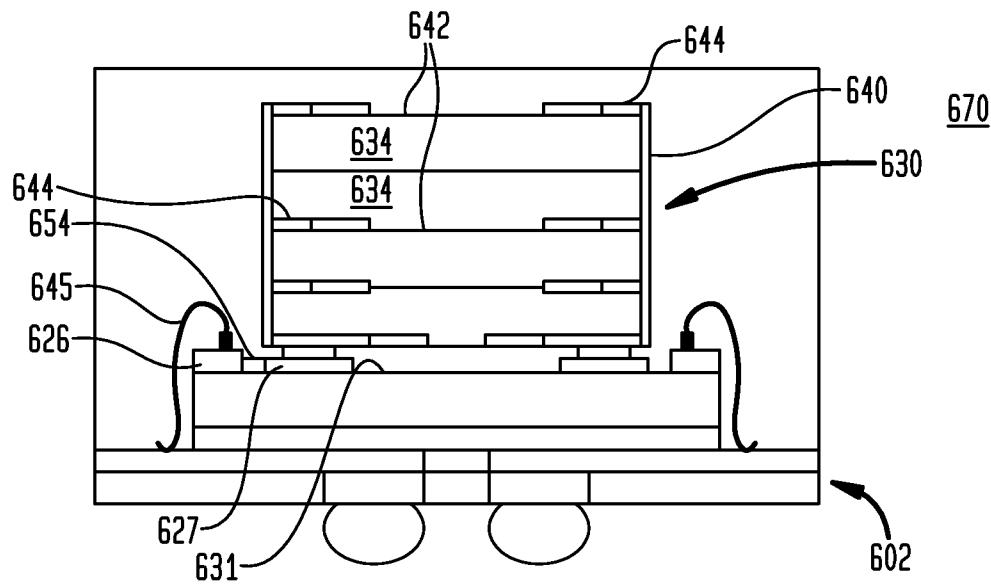


FIG. 13A

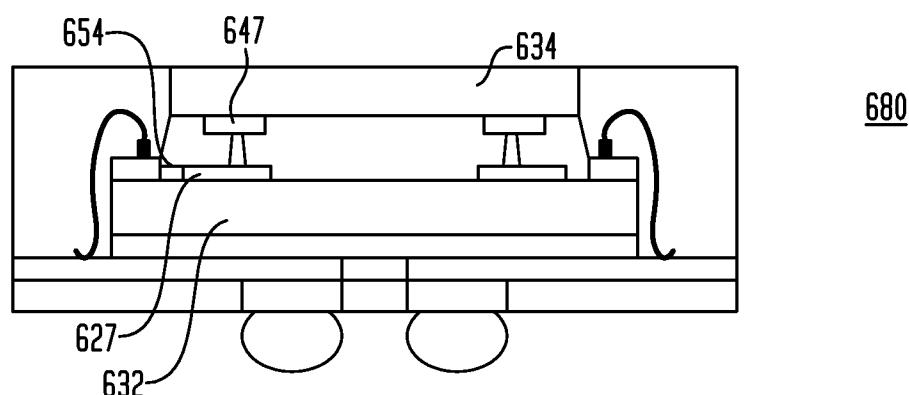
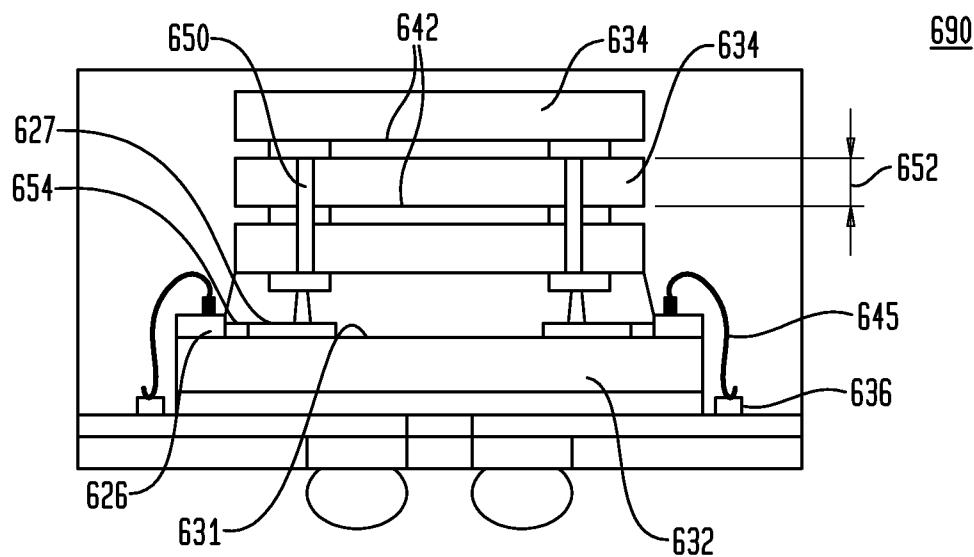


FIG. 13B



16/22

FIG. 13C

695

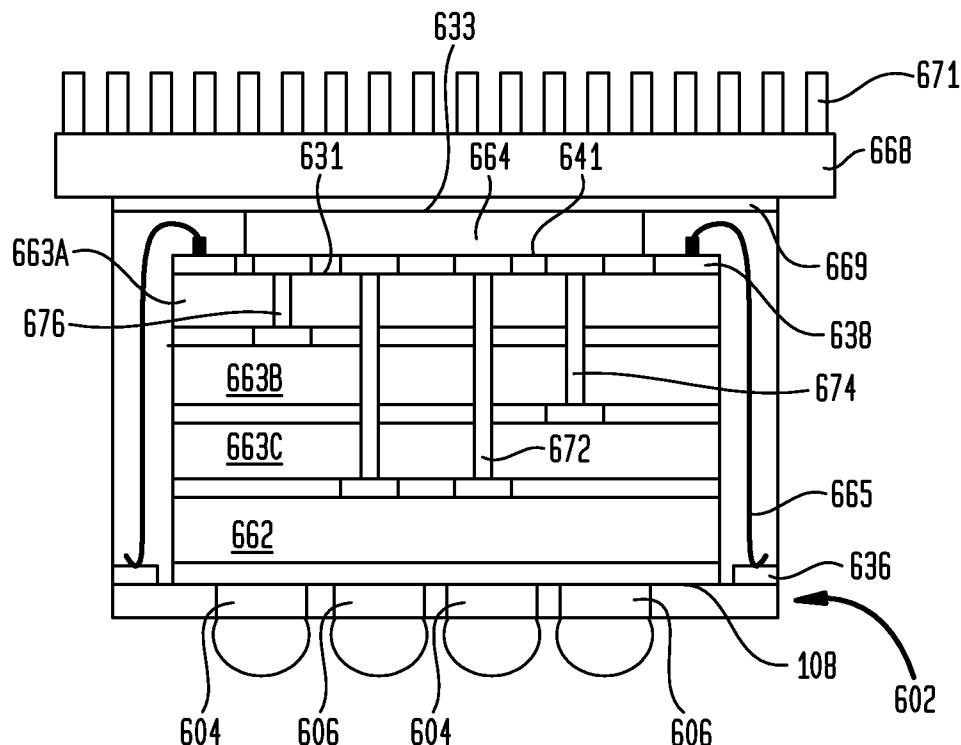


FIG. 14A

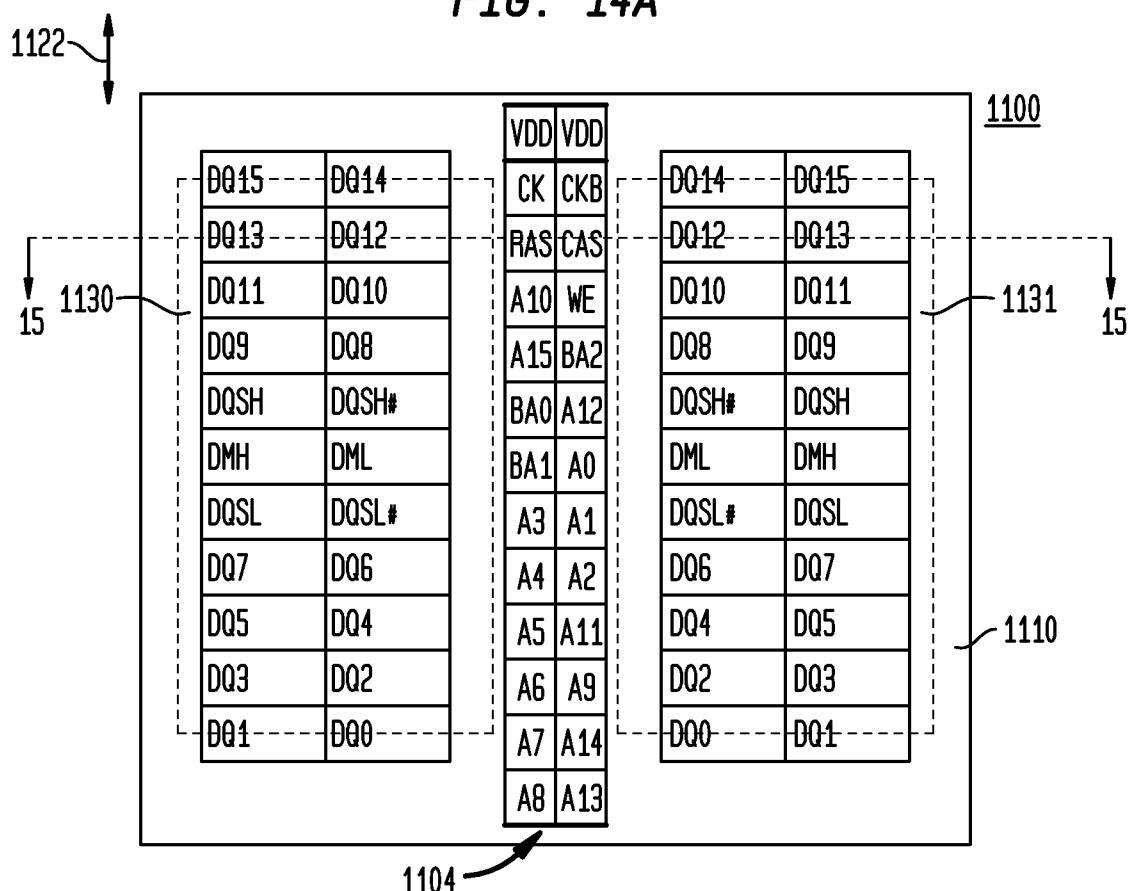
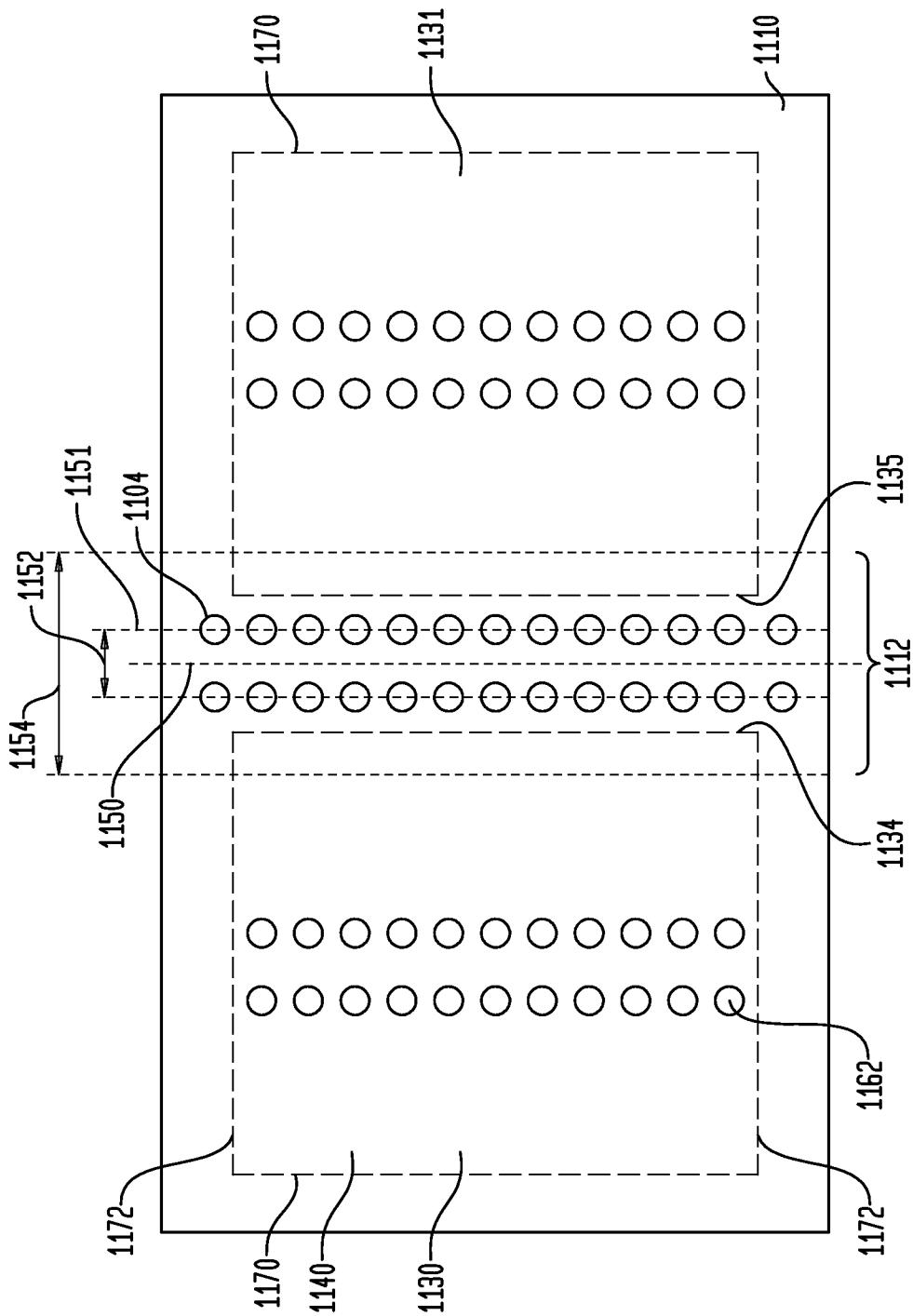


FIG. 14B



18/22

FIG. 15

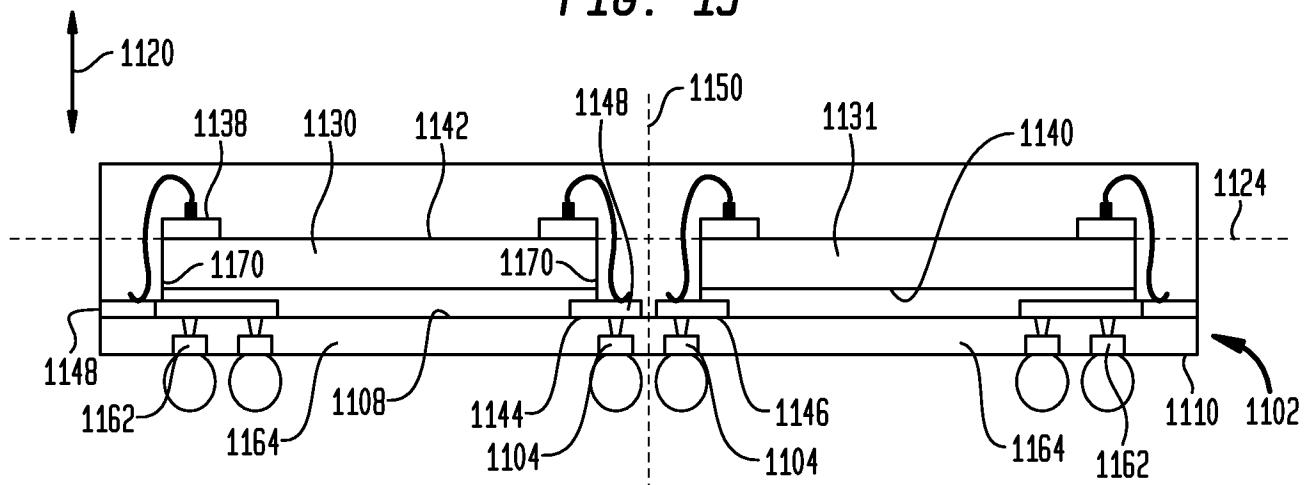


FIG. 16A

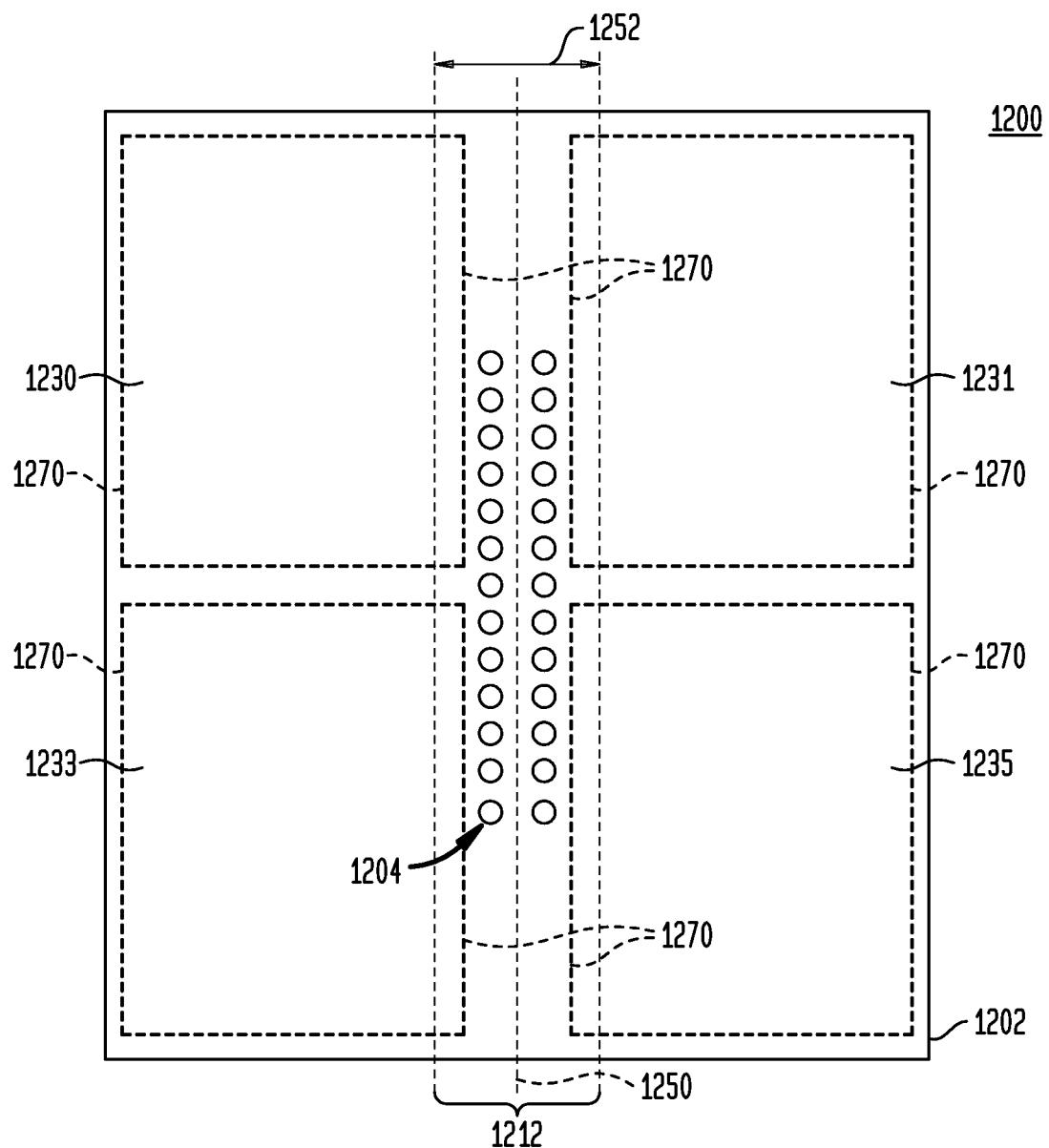


FIG. 16B

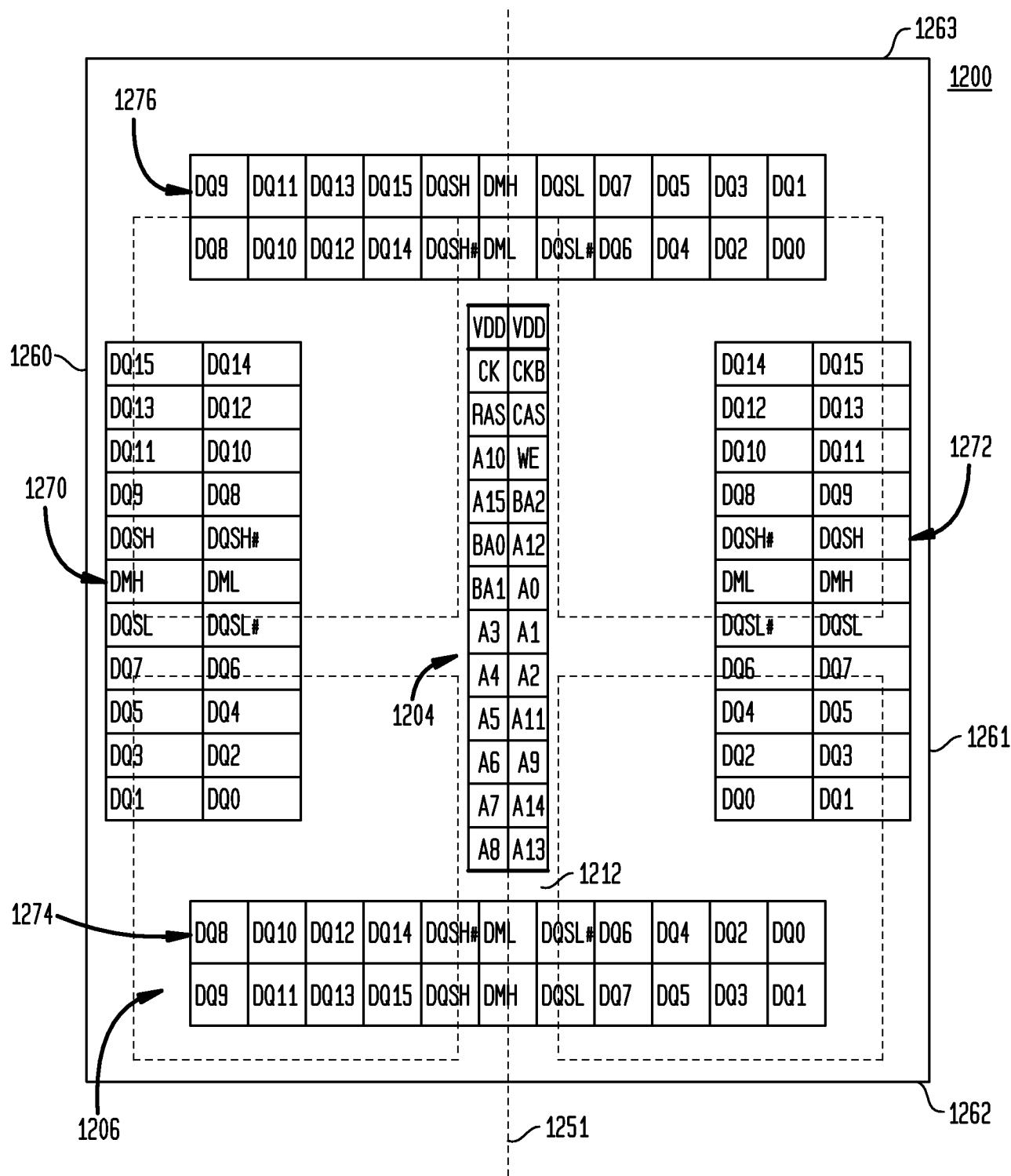


FIG. 17A

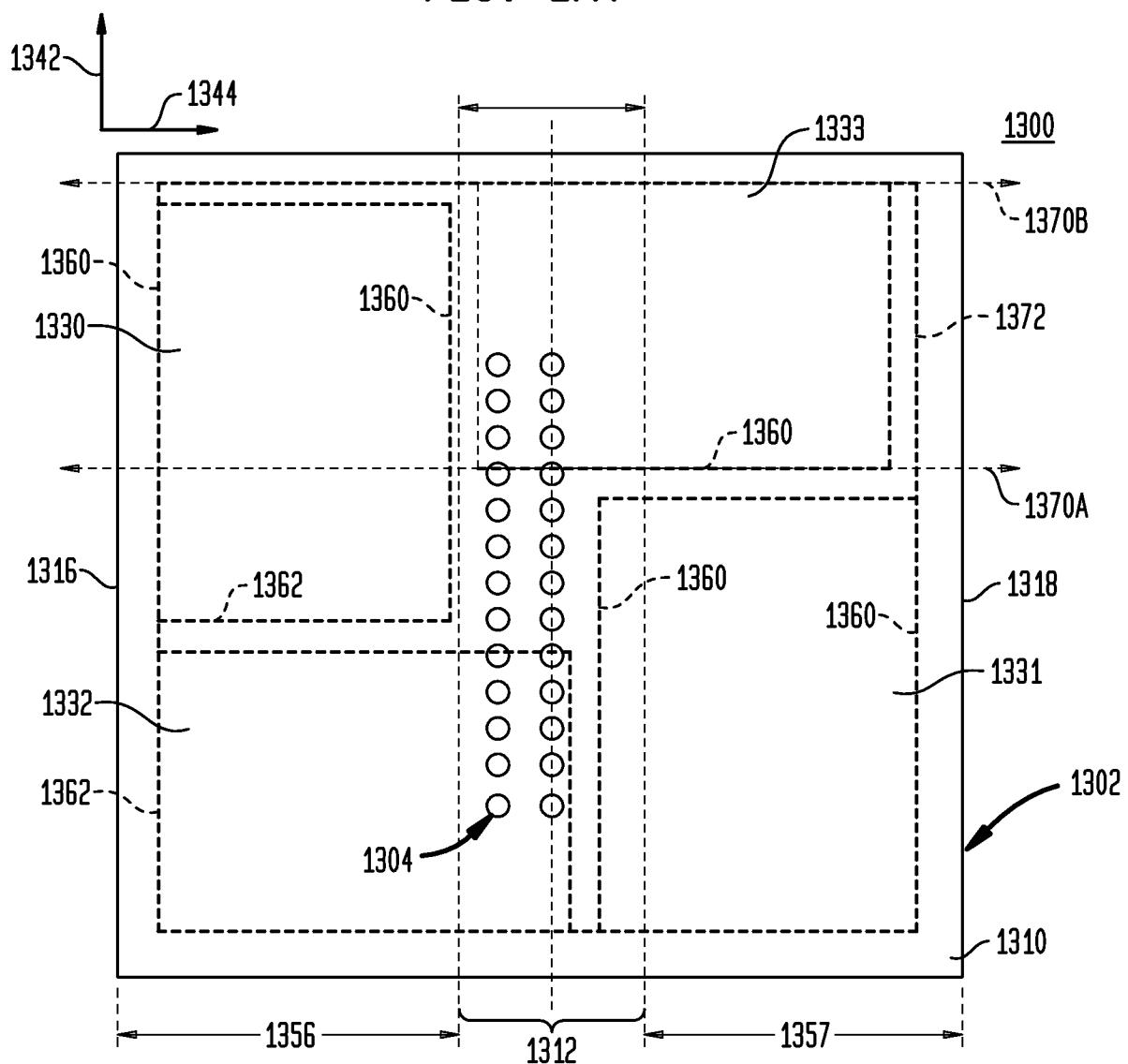
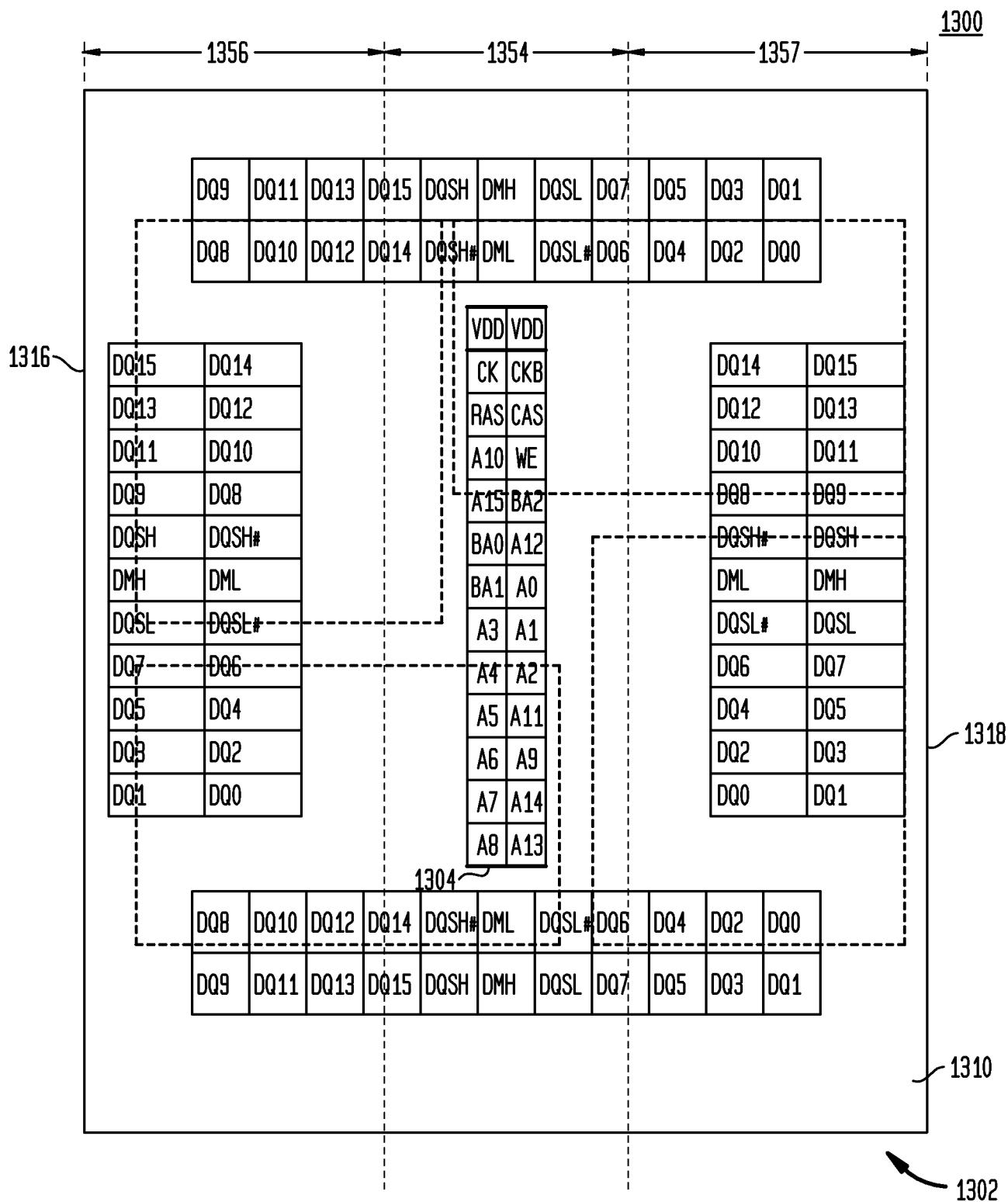


FIG. 17B



22/22

FIG. 18

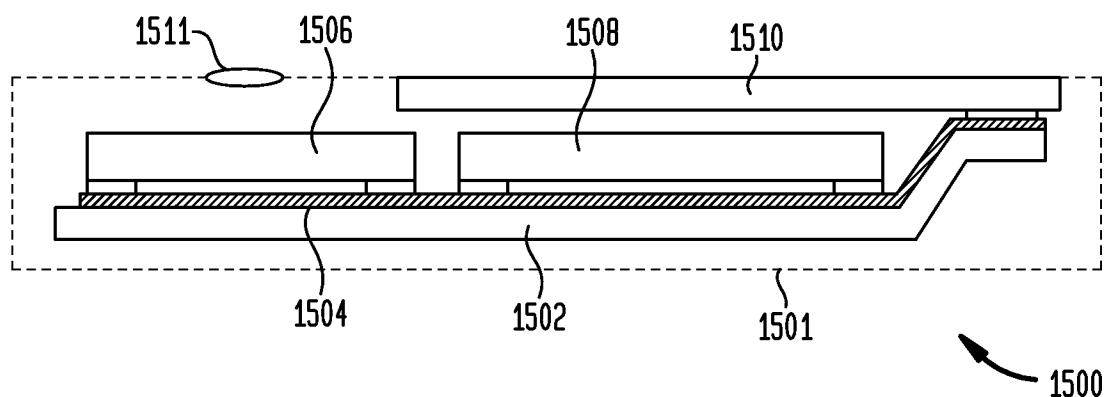
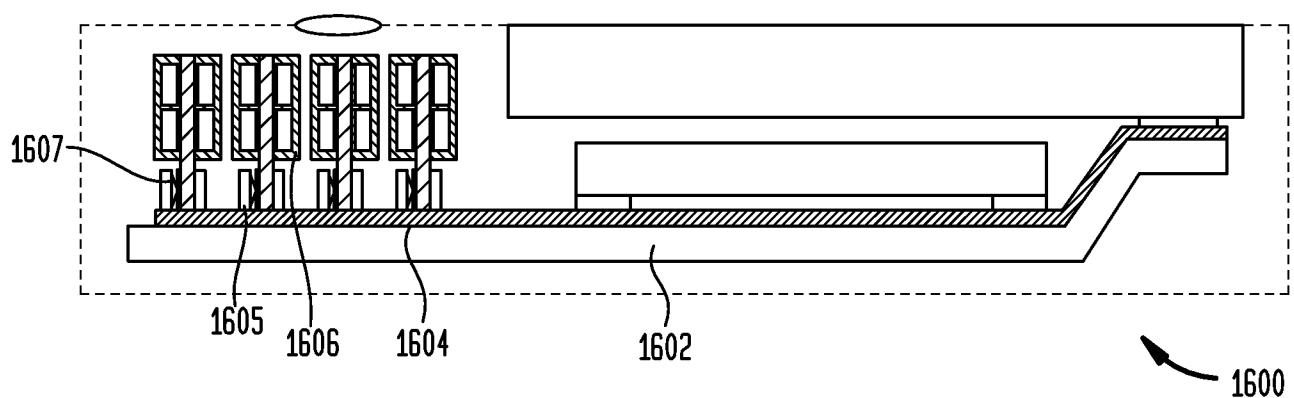


FIG. 19



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/058273

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/065 H01L23/498
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/027019 A1 (HASHIMOTO NOBUAKI [JP]) 7 March 2002 (2002-03-07) paragraphs [0126], [0096], [0170], [0116], [0169]; figures 2,10,11 -----	1,2,8, 14,18



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

17 January 2013

06/03/2013

Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Manook, Rhoda

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/058273

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1, 2, 8, 14, 18

Remark on Protest

The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2012/058273

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002027019	A1 07-03-2002	JP 3874062 B2	31-01-2007
		JP 2002083897 A	22-03-2002
		US 2002027019 A1	07-03-2002
		US 2003116349 A1	26-06-2003
		US 2006090931 A1	04-05-2006

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2, 8, 14, 18

The discernible subject-matter of identical independent product claims 1 and 18 is already known in view of document US2002/027019 (D1) and cannot therefore serve as a common concept (Rule 13(1) PCT) for claims 2-14, 16-17, 19, 20 which are directly dependent upon this common concept.

Document D1 discloses: A microelectronic package (fig. 11), comprising:

a substrate (20) having a first surface, a second surface opposite the first surface, and a plurality of substrate contacts (330) exposed at the first surface, the second surface extending in a first direction and in a second direction transverse thereto; a microelectronic element (10) having memory storage array function (10; par. 126; memory chip), the microelectronic element having a rear face facing the first surface, a front face opposite the first surface, and first and second opposed edges each extending between the front and rear faces and extending in the first direction parallel to the front face, the microelectronic element having one or more columns of element contacts (12) exposed at the front face, each column extending in a first direction along the front face, such that an axial plane normal to the front face intersects the front face along a line extending in the first direction and is centered relative to the one or more columns of element contacts (par. 96); conductive structure (14) electrically connecting the element contacts (12) with the substrate contacts (330); and a plurality of parallel columns of terminals extending in the first direction exposed at the second surface and electrically connected with the substrate contacts, the terminals including first terminals (350) exposed in a central region of the second surface of the substrate (figs. 2 and 11), and wherein the central region has a width in the second direction, the width of the central region not more than three and one-half times a minimum pitch between any two adjacent columns of the parallel columns of the terminals, and the axial plane intersects the central region (figs. 2 and 11 and par. 116).
(cf. claim 2)

With regards to claim 2, the special technical feature with respect to the known claim 1 is the microelectronic element embodies a greater number of active devices to provide memory storage array function than any other function.

The problem to be solved by claim 2 is defining features of the microelectronic element so that it can perform additional tasks.

1.1. claims: 8(completely); 14(partially)

Although the special technical features of the dependent claims 8 and 14 are not the same, they could be searched

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

without any effort and are thus included in the first searched group of claims.

2. claim: 9

(re. claim 9)

With regards to claim 9, the special technical feature with respect to the known claim 1 is that the element contacts include redistribution contacts exposed at the front face of the microelectronic element, each redistribution contact being electrically connected with a contact pad of the microelectronic element through at least one of a trace or a via.

The problem to be solved by claim 9 is to ensure that all parts of the microelectronic element itself can be effectively contacted to the outside via its contact pads, such as for example the face of the microelectronic element opposite to the contact pads.

3. claim: 10

(re. claim 10)

With regards to claim 10, the special technical feature with respect to the known claim 1 is that the conductive structure includes wire bonds extending from the element contacts and electrically connected with the substrate contacts.

The problem to be solved by claim 10 is to find the appropriate conductive structure to maintain a minimal electrical resistance between the microelectronic element and the substrate.

4. claims: 11-13

(re. claims 11,12,13)

With regards to claim 11, the special technical feature with respect to the known claim 1 is the first terminals are arranged in no more than two of the columns of terminals.

With regards to claim 12, the special technical feature with respect to the known claim 1 is the first terminals are arranged in a single one of the columns of terminals.

With regards to claim 13, the special technical feature with respect to the known claim 1 is the first terminals are arranged in no more than four of the columns of terminals.

The problem to be solved by claims 11,12 or 13 is ensuring the electrical connection between the microelectronic element and the outside world is kept particularly short.

5. claims: 16, 17

(re. claims 16,17)

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

With regards to claim 16, the special technical feature with respect to the known claim 1 is that the substrate includes a dielectric element having a coefficient of thermal expansion ("CTE") in the plane of the dielectric element of less than 30 parts per million per degree Celsius ("ppm/°C").

With regards to claim 17, the special technical feature with respect to the known claim 1 is that the substrate includes an element having a CTE of less than 12 ppm/°C.

The problem to be solved by claims 16 or 17 is to ensure the assembly package is resistant to warping.

6. claims: 20, 21, 25-29, 31

(re. claim 20)

With regards to claim 20, the special technical feature with respect to the known claim 1 is that a second microelectronic element exists also having memory storage array function and the first and second microelectronic elements being spaced apart from one another on the first surface, and having parallel first edges each extending in the first direction, wherein an axial plane normal to the first surface of the substrate extends in the first direction and is centered among the first edges, the first and second microelectronic elements having rear faces facing the first surface, front faces opposite the rear faces, and a plurality of contacts exposed at the front faces; the conductive structure also contacts the contacts of the second microelectronic element with second substrate contacts; and the plurality of parallel columns of terminals exposed at the second surface are electrically connected with the second substrate contacts.

The problem to be solved by claim 20 is how to increase the assembly density whilst maintaining the same assembly thickness.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 3-7, 15, 19, 22-24, 32(completely); 1, 14, 18, 20, 29, 31(partially)

1 The subject matter of claims 1, 3-7, 14, 15, 18-20, 22-24, 29, 30, 31 and 32 as currently defined have been directed to product claims only and the features of applying signals can only be physically apparent in the form of the physical electrical connection such as eg. a wirebond. For example, the feature of the first terminals 'being configured to carry address information usable by circuitry within the package to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within the microelectronic element' within independent product claims 1, 18, 20, 31 is rendered superfluous to the product claim, since it refers solely to the method of use of the physical product, namely the first terminal, by reference to a particular 'signal', and does not in any way further define a physical technical feature (Art. 6 PCT). 1.1 Product claims such as currently are defined in the application as originally filed cannot be defined by the use to which they are to be put (see also PCT guidelines Section IV 5.21 and the annex A5.21). Thus for the purposes of assessing the novelty and inventiveness of product claims this is not limiting and the use of the physical features for a particular type of use in these independent and dependent product claims 1, 3-7, 14, 15, 18-20, 22-24, 29, 30, 31 and 32 is therefore also not taken into consideration(Art. 17 (2)(a)(i) and PCT Guidelines 9.19, 17.29). 2 Although claims 1 and 18 have been drafted as separate independent claims, they appear to relate effectively to the same subject-matter and to differ from each other only with regard to the definition of the subject-matter for which protection is sought and/or in respect of the terminology used for the features of that subject-matter. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of Article 6 PCT. Since the signalling use within the first terminals are effectively ignored in the product claims 1 and 18 (see section 1.1), the subject matter of independent product claims 1 and 18 is the same and therefore independent claim 18 is rendered superfluous for the purposes of this communication. 3 The subject matter of independent claim 20 contains all the subject matter of independent claim 1 and thus is understood to be a claim dependent upon independent claim 1. 3.1 The subject matter of independent claim 31 also contains all the subject matter of claim 20 and thus is understood to be a claim dependent upon claim 20.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.2),

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

should the problems which led to the Article 17(2) declaration be overcome.