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(54) **OPERATIONAL AMPLIFIER HAVING IMPROVED SLEW RATE**

OPERATIONSVERSTÄRKER MIT VERBESSERTER ANSTIEGSRATE

AMPLIFICATEUR OPÉRATIONNEL À VITESSE DE BALAYAGE AMÉLIORÉE

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Description

[0001] This application claims priority to Indian Patent Application Serial No. 542/MUM/2010 filed March 2, 2010. The present application also claims priority to a corresponding U.S. patent application having application serial number 12/764,294 filed on April 21, 2010.

BACKGROUND

[0002] A common two-stage operational amplifier includes an input stage and a second stage. The input stage is usually a differential amplifier with a transconductance characteristic, producing an output current from the differential voltage inputs. Transconductance is typically very high, and thus a fairly small input voltage may be sufficient to cause the input stage to saturate, and accordingly produce a constant current output.

[0003] The current output from the input stage is received by the second stage, where frequency compensation is accomplished. The low pass characteristic of this stage approximates an integrator, and a current input which can therefore produce a linearly increasing output if current input is constant. The input current to the second stage along with the compensation capacitance and gain-bandwidth of the amplifier all affect the slew rate of the two-stage operational amplifier.

[0004] The slew rate of an amplifier represents the maximum rate of change of a signal at any point in the circuit. In other words, limitations in slew rates may result in non-linear effects that may significantly distort amplifier output if the input signal is at a frequency exceeding the slew rate limitations of the amplifier. As such, the frequency of the input signal is often limited by the capabilities of an amplifier during circuit design.

[0005] Documents US2007252647 and KR20040084000 disclose examples of amplifier circuits that comprise means for improving the slew rate of said amplifier circuits.

SUMMARY

[0006] In an example, an operational amplifier circuit having improved slew rate is provided. The operational amplifier circuit includes an operational amplifier receiving a first voltage input and a second voltage input. The operational amplifier circuit further includes a current booster circuit comprising a first current source, a second current source, a third current source, and a fourth current source. The operational amplifier circuit also includes a first comparator having a non-inverting input, an inverting input and an output, the non-inverting input coupled to the first voltage input and the inverting input coupled to the second voltage input; and a second comparator having a non-inverting input, an inverting input and an output, the non-inverting input coupled to the second voltage input and the inverting input coupled to the first voltage input. The outputs of the first and second comparators control the first, second, third and fourth current sources to supply additional current improving the slew rate of the operational amplifier circuit.

[0007] In another example, the first comparator and the second comparator of the circuit are implemented with transistors having different dimensions. The different dimensions may be different channel lengths. In addition, the first comparator detects the onset of a positive slewing operation, and the second comparator detects the onset of a negative slewing operation, such that the first and third current sources are activated when the onset of a positive slewing operation is detected by the first comparator, and the second and fourth current sources are activated when the onset of a negative slewing operation is detected by the second comparator. Further, the onset of a positive slewing operation is detected when the difference between the first voltage input and the second voltage input is a positive value greater than a threshold voltage, and the onset of a negative slewing operation is detected when the difference between the first voltage input and the second voltage input is a negative value having an absolute value greater than a threshold voltage. The comparators of the operational amplifier may further be implemented using FinFET devices.

[0008] In an example, a method for improving a slew rate of an operational amplifier is also provided. The method includes detecting the onset of a slewing operation, activating additional current sources during the slewing operation to improve the slew rate, deactivating the additional current sources when no slewing operation is detected, thereby minimizing additional power dissipation from additional current flow. In addition, detecting the onset of a slewing operation may further comprise comparing the difference between a first voltage and a second voltage at the input of the operational amplifier against the switching threshold voltages of one or more comparators. In one example, the additional current sources of the operational amplifier are activated depend on whether the detected slewing operation is positive or negative. The slewing operation may be positive if the difference between the input voltages is positive and greater than the switching threshold voltages of the one or more comparators, and the slewing operation may be negative if the difference between the input voltages is negative and the absolute value of the difference is greater than the switching threshold voltages of the one or more comparators.

[0009] In another example, the two input transistors of the one or more comparators for improving slew rate have different dimensions. The different dimensions may include different channel lengths. In addition, the first comparator

and the second comparator may be implemented using FinFET devices.

[0010] In another example, a slew rate improvement circuit for an operational amplifier is provided. The slew rate improvement circuit includes a current booster circuit comprising a first current source, a second current source, a third current source, and a fourth current source, and a comparator circuit comprising a first comparator and a second comparator, wherein the first comparator has a non-inverting input, an inverting input and an output, the non-inverting input coupled to a first voltage input and the inverting input coupled to a second voltage input, wherein the second comparator has a non-inverting input, an inverting input and an output, the non-inverting input coupled to the second voltage input and the inverting input coupled to the first voltage input; wherein the outputs of the first and second comparators control the first, second, third and fourth current sources to supply additional current improving the slew rate of the operational amplifier circuit. The first voltage input and the second voltage input may further be voltage inputs to the operational amplifier.

[0011] The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE FIGURES

[0012] The embodiments will be further elucidated by means of the following description and the appended drawings.

Figure 1 is an illustrative circuit diagram of an operational amplifier circuit having improved slew rate.

Figure 2a is an illustrative circuit schematic for a FinFET implementation of a two-stage operational amplifier.

Figure 2b is an illustrative circuit schematic for a FinFET implementation of a first comparator with first and third current sources.

Figure 2c is an illustrative circuit schematic for a FinFET implementation of a second comparator with second and fourth current sources.

Figure 3 is a graph comparing the slew rates of a two-stage operational amplifier and an operational amplifier circuit having improved slew rate embodiment of the present application.

Figure 4 is a graph comparing the transient responses of a first two-stage operational amplifier, a second two-stage operational amplifier and an operational amplifier circuit having improved slew rate embodiment of the present application.

DETAILED DESCRIPTION

[0013] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented herein. It will be readily understood that the aspects of the present disclosure, as generally described herein, and illustrated in the figures, can be arranged, substituted, combined, separated, and designed in a wide variety of different configurations, all of which are explicitly contemplated herein.

[0014] The present application provides an operational amplifier circuit having a high slew rate while maintaining a low power overhead and basic performance measures. In an embodiment, the principle behind the operation of the circuit relies on detecting the onset of a slewing operation of the circuit and accordingly activating additional current sources. Because the additional current sources are only activated during the slewing operation of the circuit, power dissipation and other performance measures of the operational amplifier circuit remain unchanged.

[0015] Figure 1 is an illustrative circuit diagram of an embodiment of an operational amplifier circuit 100 having improved slew rate. The operational amplifier circuit 100 comprises a two-stage operational amplifier circuit 102, additional current sources 104 and a comparator circuit 106. The two-stage operational amplifier circuit 102 comprises a first amplifier 108 and a second amplifier 110 connected in series, wherein the first amplifier 108 receives voltage inputs V_{in1} and V_{in2}, and the second amplifier 110 outputs a voltage V_{out}. A resistor 112 in series with a compensator capacitor 114 are coupled in parallel to the second amplifier. The output end of the two-stage operational amplifier circuit 102 is coupled to a load capacitor 128.

[0016] The comparator circuit 106 comprises a first comparator 124 and a second comparator 126, both receiving the voltage inputs V_{in1} and V_{in2} and having a first comparator output C_1 and a second comparator output C_2, respectively. The additional current sources 104 comprises a first current source 116, a second current source 118, a third current source 120 and a fourth current source 122. The first current source 116 and third current source 120 are controlled according to the first comparator output C_1, while the second current source 118 and the fourth current source 122 are controlled according to the second comparator output C_2. The first current source 116 and the second current source

118 are coupled to the output of the two-stage operational amplifier circuit 102, while the third current source 120 and the fourth current source 122 are coupled to the power source of the first amplifier 108 of operational amplifier 102.

[0017] As shown in Figure 1, the additional current sources 104 and the comparator circuit 106 are circuit additions that are be used to improve the slew rate of the two-stage operational amplifier circuit 102. The additional current sources 104 is effectively a current boosting module for the two-stage operational amplifier circuit 102, and the comparator circuit 106 is effectively a detection circuit for detecting the onset of slewing.

[0018] As shown in Figure 1, the first comparator 124 and the second comparator 126 are asymmetrical. Asymmetrical comparators have asymmetrical input differential stages, which results in an artificial input offset voltage that is the differential switching threshold voltage of the comparator. Such asymmetrical input differential stages can be implemented by using either differently sized comparator input transistors, or differently sized comparator input stage load transistors. In an embodiment of the present application, the first comparator 124 and second comparator 126 are implemented with input transistors of different channel lengths. The comparators 124 and 126 may further be designed to keep the output of the control logic circuit at a proper logic level (i.e. logic "High" or logic "Low" depending on the polarity of the four additional current sources 116, 118, 120, 122) when the absolute value of the difference between voltage inputs V_{in1} and V_{in2} is less than a threshold value V_{sw}. In the case of the present embodiment, when no slewing onset is detected, the outputs of the first comparator 124 and the second comparator 126 are either at V_{DD} when controlling P-FinFET current sources or at ground when controlling N-FinFET current sources.

[0019] As described above, the first current source 116 and the third current source 120 are controlled by the first comparator 124, and the second current source 11 8 and the fourth current source 122 are controlled by the second comparator 126. The first current source 116 and the third current source 120 may be approximately equal in current value, while the second current source 118 and the fourth current source 122 may also be approximately equal in value.

[0020] Functionally, the first comparator 124 operates in a positive slewing mode when V_{in1} is greater than V_{in2} by some marginal value, while the second comparator 126 operates in a negative slewing mode when V_{in1} is less than V_{in2} by some marginal value. In the event that the difference between voltage inputs V_{in1} and V_{in2} exceeds a threshold voltage, such as V_{sw}, the inverted output of the first comparator, $\overline{C_1}$ becomes low, and the first current source 116 and the third current source 120 become activated. The activation of the first current source 116 provides additional current through the compensation capacitor 114, while the activation of the third current source 120 provides a path to discharge the opposite terminal of the compensation capacitor 114. As a result, the third current source 120 assists the first current source 116 in improving the positive slew rate of the circuit.

[0021] Analogously, when the onset of a negative slewing operation is detected (absolute value of difference between voltage inputs V_{in1} and V_{in2} exceeds the threshold voltage V_{sw}), the output of the second comparator C_2 becomes high. In this case, the second current source 118 and the fourth current source 122 are activated, and the negative slew rate is improved. In both cases, the threshold voltage V_{sw} determines the switching point of the detector circuit and can be designed to adapt to different operational amplifier applications.

[0022] In one embodiment of the present application, the operational amplifier having improved slew rate is implemented using FinFET devices at 45 nm technology. The FinFET technology parameters used in this embodiment have a minimum channel length (L) of 20 nm, effective oxide thickness (EOT) of 0.9 nm, fin width (WFIN) of 6 nm, and fin height (HFIN) of 30 nm. The channel doping is 1×10^{15} cm^{-3} and the source/drain doping is 1×10^{20} cm^{-3} with an overlap distance (LOV) of 2 nm and a 1 nm/decade Gaussian doping gradient into the channel.

[0023] Figure 2a is an illustrative circuit schematic 202 for a FinFET implementation of a two-stage operational amplifier; Figure 2b is an illustrative circuit schematic 204 for a FinFET implementation of a first comparator with first and third current sources; Figure 2c is an illustrative circuit schematic 206 for a FinFET implementation of a second comparator with second and fourth current sources. In the example embodiment shown in Figures 2a-2c, the numbers in the bracket indicate the number of fins for the respective FinFET device. Example values for capacitors and resistors are also provided.

[0024] As shown in Figure 2a, the two-stage operational amplifier parameters are designed and optimized for the maximum slew rate under a given power constraint, and accordingly used for simulations to demonstrate slew rate improvement as a result of implementing the comparator and current booster circuits shown in Figures 2b and 2c.

[0025] In the embodiment of Figure 2, the operational amplifier circuit 202 is designed using FinFET devices of channel length 50 nm. In order to obtain the required threshold (switching voltage) V_{sw}, however, it is desirable to use asymmetric comparators by implementing asymmetric input devices. As discussed above, asymmetry in the comparator circuits 204 and 206 may be implemented in different ways, such as by introducing mismatches between lengths or number of fingers of the two corresponding input transistors. In the example embodiment shown in Figure 2, FinFET devices with different channel lengths are used in the input stage to achieve the required asymmetry.

[0026] In the first comparator circuit 204 of Figure 2b, the input transistors M10 and M11 of the comparator in Figure 2b have different channel lengths. The channel lengths of M10 and the other FinFET devices in the first comparator circuit 204 are 50nm, while the input transistor M11 has a channel length of 100nm. Similarly, the M23 and M24 transistors of the second comparator circuit 206 of Figure 2c are of different channel lengths. The channel lengths of M23 and the

other FinFET devices in the second comparator circuit 206 are 50nm, while the input transistor M24 has a channel length of 100nm.

[0027] As discussed above, demonstration of the slew rate improvement for an operational amplifier circuit begins with optimizing the parameters of the operational amplifier circuit 202 of Figure 2a under given power constraints. The optimized parameters, as well as slew rate values are shown in Table 1. The slew rate values are measured for an input signal with rise and fall times of 100*p*s. In the discussions below, this circuit is referred to as the "Two-Stage Op-Amp 1."

TABLE 1

	Desired Values	**Best Obtained Values (Two-Stage Op-Amp 1)**
Gain	≥ 80 dB	79.65 dB
Phase Margin	≥ 65°	61°
Unity Gain Frequency	≥ 500 MHz	695 MHz
Power Dissipation	≤ 50 μW	46 μW
Offset Voltage	≤ 50 μV	83 μV
Slew Rate Rise	≥ 500 V/μS	273 V/μS
Slew Rate Fall	≥ 500 V/μS	271 V/μS

[0028] After the parameters for the two-stage operational amplifier 202 have been optimized, the first and second comparator circuits 204 and 206 are designed. In this embodiment, the switching voltage V_{SW} is set at 55 mV. Consistent with the discussions above, the input transistors of the comparator circuits 204 and 206 are asymmetrical. The number of fins for FinFET devices in the current source circuits of the comparator circuits 204 and 206 can also be tuned to provide the best settling time during slewing operations.

[0029] Once the parameters for the first and second comparator circuits 204 and 206 have been optimized, simulations were performed to compare the slew rate of the optimized two-stage operational amplifier circuit 202 individually, with the slew rate of the optimized two-stage operational amplifier circuit 202 in combination with the slew rate improving circuit comprising comparator circuits 204 and 206, current sources 116, 118, 120, 122 and control logic. In the discussions below, the combination of the Two-Stage Op-Amp 1 and the slew-rate improvement circuit is referred as the "SR-Improved Op-Amp." The results of the simulations are shown in Table 2.

TABLE 2

	Two-Stage Op-Amp 1	**SR-Improved Op-Amp**
Gain	79.65 dB	79.65 dB
Phase Margin	61°	61°
Unity Gain Frequency	695 MHz	695 MHz
Power Dissipation	46 μW	78 μW
Offset Voltage	83 μV	83 μV
Slew Rate Rise	273 V/μS	6171 V/μS
Slew Rate Fall	271 V/μS	5590 V/μS

[0030] As shown in Table 2, the slew rate of the SR-Improved Op-Amp improved to 5590 V/μS from the slew rate of Two-Stage Op-Amp 1 of 271 V/μS, while the power dissipation increased from 46 μW to 78 μW, and other parameters remain the same. The increase in power dissipation is marginal in comparison to improvement observed in slew rates. It should also be noted that some of the increased power dissipation is from the comparator circuits 204 and 206.

[0031] Figure 3 is a graph 300 comparing the slew rates of the Two-Stage Op-Amp 1 and the SR-Improved Op-Amp. The slew rates of the Two-Stage Op-Amp 1 and the SR-Improved Op-Amp are measured for an input signal having rise and fall times varying in the range of 25 *p*s to 2 *n*s. As shown, the slew rate of Two-Stage Op-Amp 1 is generally independent of input rise time. On the other hand, slew rate of the SR-Improved Op-Amp circuit increases significantly as the input signal rise time decreases, down to the range of 100 *p*s. As such, an operational amplifier circuit in combination with the slew rate improvement circuitry provided in an embodiment of the present application is capable of tracking input signals with rise/fall times as short as 100ps.

[0032] To further demonstrate the slew rate improvements achieved through the comparator circuits 204 and 206, a second two-stage operational amplifier circuit was optimized for maximum slew rate, without any power constraints. The slew rate of this circuit, referred to as "Two-Stage Op-Amp 2" came in at 650 V/μS with a power dissipation of 113 μW. In this case, the power dissipation for Two-Stage Op-Amp 2 is greater than both the originally optimized, power dissipation constrained Two-Stage Op-Amp 1 as well as the SR-Improved Op-Amp. Further, the slew rate for Two-Stage Op-Amp 2 is around one tenth of that of the SR-Improved Op-Amp embodiment in the present application.

[0033] Figure 4 is a graph 400 comparing the transient responses of Two-Stage Op-Amp 1, Two-Stage Op-Amp 2 and the SR-Improved Op-Amp given an input signal with a rise time of 100 *p*s. As compared to the two two-stage operational amplifiers, the SR-Improved Op-Amp shows a noticeably high slew rate.

[0034] In addition to the slew rate, the settling time of the circuits are also compared. Settling time is measured as the time required for the output to reach and remain with 2% of its final value. Table 3 shows a comparison of the rising edge and falling edge settling times for the Two-Stage Op-Amp 1, the Two-Stage Op-Amp 2, and the SR-Improved Op-Amp, each with a load capacitance of 20 *f*F. In Table 3, settling time is provided in units of picoseconds (*ps*).

TABLE 3

	SR-Improved Op-amp	**Two-stage Op-amp 1**	**Two-stage Op-amp 2**
$t_{s,r}$*(ps)*	310	1490	620
$t_{s,f}$*(ps)*	600	1610	660

[0035] As shown in Table 3, the rising edge settling time of SR-Improved Op-Amp is significantly smaller than those of the two two-stage operational amplifiers. On the other hand, the falling edge settling time of the slew SR-Improved Op-Amp is significantly smaller than the falling edge settling time of two-stage operational amplifier 1, but comparable to the falling edge settling time of two-stage operational amplifier 2. It should be noted that Two-Stage Op-Amp 2 was designed with no power constraints and consumes additional power in the interest of a better slew rate (113 μW vs 78 μW for the SR-Improved Op-Amp circuit).

[0036] To further improve the power efficiency, alternative embodiments of the slew rate improved operational amplifier may include multiple two-stage operational amplifiers sharing the same comparator circuits, thus reducing the increased power dissipation per additional operational amplifier in a circuit.

[0037] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the scope being indicated by the following claims.

Claims

1. An operational amplifier circuit (100), comprising:

a two-stage operational amplifier (102) adapted to receive a first voltage input (V_{in1}) and a second voltage input (V_{in2}) comprising a first amplifier (108) and a second amplifier (110) electrically coupled in series, and a resistor (112) in series with a capacitor (114) electrically coupled in parallel between an input and an output of the second amplifier;

a current booster circuit (104) comprising a first current source (116), a second current source (118), a third current source (120), and a fourth current source (122);

a first comparator (124) having a non-inverting input, an inverting input, a first switching threshold voltage and an output, the non-inverting input electrically coupled to the first voltage input and the inverting input electrically coupled to the second voltage input; and

a second comparator (126) having a non-inverting input, an inverting input, a second switching threshold voltage and an output, the non-inverting input being electrically coupled to the second voltage input and the inverting input being electrically coupled to the first voltage input;

wherein the output of the first comparator is adapted to control the first and third current source and the output of the second comparator is adapted to control the second, and fourth current source to supply additional current and to improve a slew rate of the operational amplifier circuit, wherein the first current source (116) and the second current source (118) are electrically coupled to the output of the two-stage operational amplifier (102), while the third current source (120) and the fourth current source (122) are electrically coupled to a power source of the first amplifier (108) of the two-stage operational amplifier (102).

2. The operational amplifier circuit of claim 1, wherein the first comparator and the second comparator comprise transistors having different dimensions, and/or wherein the different dimensions comprise different channel lengths.

3. The operational amplifier circuit of claim 1 or 2, wherein the first comparator is configured to detect an onset of a positive slewing operation.

4. The operational amplifier circuit as in one of claims 1 to 3, wherein the second comparator is configured to detect an onset of a negative slewing operation.

5. The operational amplifier circuit as in claim 2, wherein the first and third current sources are configured to activate in response to detection, by the first comparator, of an onset of a positive slewing operation.

6. The operational amplifier circuit as in claim 2 or 5, wherein the first comparator is configured to detect an onset of a positive slewing operation in response to a difference between the first voltage input and the second voltage input being a positive value greater than a threshold voltage.

7. The operational amplifier circuit as in claim 4, wherein the second and fourth current sources are configured to activate in response to detection, by the second comparator, of the onset of a negative slewing operation.

8. The operational amplifier circuit as in claim 4 or 7, wherein the second comparator is configured to detect the onset of a negative slewing operation in response to a difference between the first voltage input and the second voltage input being a negative value having an absolute value greater than a threshold voltage.

9. The operational amplifier circuit as in one of claims 1 to 8, wherein the two-stage operational amplifier, first comparator and second comparator comprise FinFET devices.

10. A method to improve a slew rate of a two-stage operational amplifier (102) with first and second stages, comprising:

detecting an onset of a slewing operation, wherein detecting the onset of the slewing operation comprises comparing a difference between a first voltage. (V_{in1}) and a second (V_{in2}) at the input of the two-stage operational amplifier against a first and a second switching threshold voltage;
activating additional current sources during the slewing operation to improve the slew rate;
deactivating the additional current sources in response to no slewing operation being detected, thereby reducing additional power dissipation from additional current flow,
wherein the additional current sources comprise a first current source (116), a second current source (118), a third current source (120), and a fourth current source (122),
wherein the first current source (116) and the second current source (118) are electrically coupled to an output of the two-stage operational amplifier (102), while the third current source (120) and the fourth current source (122) are electrically coupled to a power source of the first amplifier (108) of the two-stage operational amplifier (102),
wherein a resistor (112) in series with a capacitor (114) is electrically coupled in parallel between an input and an output of the second stage of the two-stage amplifier,
and wherein activating additional current sources during the slewing operation comprises activating the first and third current sources if the difference between the first and second voltages is positive and greater than the first switching threshold voltage and activating the second and fourth current sources if the difference between the first and second voltages is negative and an absolute value of the difference is greater than the second switching threshold voltage.

11. The method of claim 10,
wherein the first switching threshold voltage is of a first comparator, and/or
wherein the second switching threshold voltage is of a second comparator.

12. The method as in claim 10 or 11, wherein two input transistors of one or more of the comparators have different dimensions, and/or
wherein the different dimensions comprise different channel lengths.

13. The method as in claim 11, wherein the operational amplifier, the first comparator and the second comparator are implemented with FinFET devices.

Patentansprüche

1. Operationsverstärkerschaltkreis (100), umfassend:

einen zweistufigen Operationsverstärker (102), der dazu eingerichtet ist, einen ersten Spannungseingang (V_{in1}) und einen zweiten Spannungseingang (V_{in2}) zu empfangen, umfassend einen ersten Verstärker (108) und einen zweiten Verstärker (110), die elektrisch in Reihe geschaltet sind, und einen Widerstand (112) in Reihe mit einem Kondensator (114), der zwischen einen Eingang und einen Ausgang des zweiten Verstärkers elektrisch parallelgeschaltet ist;
einen Stromanhebungsschaltkreis (104), umfassend eine erste Stromquelle (116), eine zweite Stromquelle (118), eine dritte Stromquelle (120) und eine vierte Stromquelle (122);
einen ersten Komparator (124), der einen nicht-invertierenden Eingang, einen invertierenden Eingang, eine erste Umschaltschwellenspannung und einen Ausgang hat, wobei der nicht invertierende Eingang mit dem ersten Spannungseingang elektrisch verbunden ist und der invertierende Eingang mit dem zweiten Spannungseingang elektrisch verbunden ist; und
einen zweiten Komparator (126), der einen nicht-invertierenden Eingang, einen invertierenden Eingang, eine zweite Umschaltschwellenspannung und einen Ausgang hat, wobei der nicht-invertierende Eingang mit dem zweiten Spannungseingang elektrisch verbunden ist und der invertierende Eingang mit dem ersten Spannungseingang elektrisch verbunden ist;
wobei der Ausgang des ersten Komparators dazu eingerichtet ist, die erste und die dritte Stromquelle zu steuern, und der Ausgang des zweiten Komparators dazu eingerichtet ist, die zweite und vierte Stromquelle zu steuern, um zusätzlichen Strom zuzuführen und eine Anstiegsrate des Operationsverstärkerschaltkreises zu verbessern, wobei die erste Stromquelle (116) und die zweite Stromquelle (118) mit dem Ausgang des zweistufigen Operationsverstärkers (102) elektrisch verbunden sind, während die dritte Stromquelle (120) und die vierte Stromquelle (122) mit einer Stromquelle des ersten Verstärkers (108) des zweistufigen Operationsverstärkers (102) elektrisch verbunden sind.

2. Operationsverstärkerschaltkreis nach Anspruch 1, bei dem der erste Komparator und der zweite Komparator Transistoren umfassen, die unterschiedliche Dimensionen haben, und/oder die unterschiedlichen Dimensionen unterschiedliche Kanallängen umfassen.

3. Operationsverstärkerschaltkreis nach Anspruch 1 oder 2, bei dem der erste Komparator dazu eingerichtet ist, einen Beginn eines positiven Anstiegsvorgangs zu erfassen.

4. Operationsverstärkerschaltkreis nach einem der Ansprüche 1 bis 3, bei dem der zweite Komparator dazu eingerichtet ist, einen Beginn eines negativen Anstiegsvorgangs zu erfassen.

5. Operationsverstärkerschaltkreis nach Anspruch 2, bei dem die erste und die dritte Stromquelle dazu eingerichtet sind, sich in Erwiderung auf die Erfassung des Beginns eines positiven Anstiegsvorgangs durch den ersten Komparator zu aktivieren.

6. Operationsverstärkerschaltkreis nach Anspruch 2 oder 5, bei dem der erste Komparator dazu eingerichtet ist, den Beginn eines positiven Anstiegsvorgangs in Erwiderung darauf zu erfassen, dass eine Differenz zwischen dem ersten Spannungseingang und dem zweiten Spannungseingang ein positiver Wert größer als eine Schwellenspannung ist.

7. Operationsverstärkerschaltkreis nach Anspruch 4, bei dem die zweite und die vierte Stromquelle dazu eingerichtet sind, sich in Erwiderung auf die Erfassung des Beginns eines negativen Anstiegsvorgangs durch den zweiten Komparator zu aktivieren.

8. Operationsverstärkerschaltkreis nach Anspruch 4 oder 7, bei dem der zweite Komparator dazu eingerichtet ist, den Beginn eines negativen Anstiegsvorgangs in Erwiderung darauf zu erfassen, dass eine Differenz zwischen dem ersten Spannungseingang und dem zweiten Spannungseingang ein negativer Wert ist, der einen absoluten Wert hat, der größer als eine Schwellenspannung ist.

9. Operationsverstärkerschaltkreis nach einem der Ansprüche 1 bis 8, bei dem der zweistufige Operationsverstärker, der erste Komparator und der zweite Komparator FinFET-Vorrichtungen umfassen.

10. Verfahren für die Verbesserung einer Anstiegsrate eines zweistufigen Operationsverstärkers (102) mit ersten und zweiten Stufen, umfassend:

Erfassen eines Beginns eines Anstiegsvorgangs, wobei das Erfassen des Beginns des Anstiegsvorgangs, das Vergleichen einer Differenz zwischen einer ersten Spannung (V_{in1}) und einer zweiten Spannung (V_{in2}) an dem Eingang des zweistufigen Operationsverstärkers mit einer ersten sowie einer zweiten Umschaltschwellenspannung umfasst;
Aktivieren zusätzlicher Stromquellen während des Anstiegsvorgangs, um die Anstiegsrate zu verbessern;
Deaktivieren der zusätzlichen Stromquellen in Erwiderung darauf, dass kein Anstiegsvorgang erfasst wird, wodurch ein zusätzlicher Leistungsverlust aus einem zusätzlichen Stromfluss verringert wird,
wobei die zusätzlichen Stromquellen eine erste Stromquelle (116), eine zweite Stromquelle (118), eine dritte Stromquelle (120) und eine vierte Stromquelle (122) umfassen,
die erste Stromquelle (116) und die zweite Stromquelle (118) mit einem Ausgang des zweitstufigen Operationsverstärkers (102) elektrisch verbunden sind, während die dritte Stromquelle (120) und die vierte Stromquelle (122) mit einer Stromquelle des ersten Verstärkers (108) des zweistufigen Operationsverstärkers (102) elektrisch verbunden sind,
ein Widerstand (112) in Reihe mit einem Kondensator (114) elektrisch parallel zwischen einen Eingang und einen Ausgang der zweiten Stufe des zweistufigen Verstärkers geschaltet ist und
das Aktivieren zusätzlicher Stromquellen während des Anstiegsvorgangs das Aktivieren der ersten und der dritten Stromquelle, wenn die Differenz zwischen der ersten und der zweiten Spannung positiv und größer als die erste Umschaltschwellenspannung ist, und das Aktivieren der zweiten und der vierten Stromquelle umfasst, wenn die Differenz zwischen der ersten und der zweiten Spannung negativ ist und ein absoluter Wert der Differenz größer als die zweite Umschaltschwellenspannung ist.

11. Verfahren nach Anspruch 10, bei dem die erste Umschaltschwellenspannung aus einem ersten Komparator stammt und/oder die zweite Umschaltschwellenspannung aus einem zweiten Komparator stammt.

12. Verfahren nach Anspruch 10 oder 11, bei dem zwei Eingangstransistoren eines oder mehrerer der Komparatoren unterschiedliche Dimensionen haben und/oder die unterschiedlichen Dimensionen unterschiedliche Kanallängen umfassen.

13. Verfahren nach Anspruch 11, bei dem der Operationsverstärker, der erste Komparator und der zweite Komparator mit FinFET ausgeführt sind.

Revendications

1. Circuit d'amplificateur opérationnel (100), comprenant :

un amplificateur opérationnel à deux étages (102) adapté pour recevoir une première entrée de tension (V_{in1}) et une deuxième entrée de tension (V_{in2}), comprenant un premier amplificateur (108) et un deuxième amplificateur (110) connectés électriquement en série, et une résistance (112) en série avec un condensateur (114) connectés électriquement en parallèle entre une entrée et une sortie du deuxième amplificateur ;
un circuit d'augmentation de courant (104) comprenant une première source de courant (116), une deuxième source de courant (118), une troisième source de courant (120) et une quatrième source de courant (122) ;
un premier comparateur (124) comprenant une entrée non inverseuse, une entrée inverseuse, une première tension seuil de commutation et une sortie, l'entrée non inverseuse étant connectée électriquement à la première entrée de tension et l'entrée inverseuse étant connectée électriquement à la deuxième entrée de tension ; et
un deuxième comparateur (126) comprenant une entrée non inverseuse, une entrée inverseuse, une deuxième tension seuil de commutation et une sortie, l'entrée non inverseuse étant connectée électriquement à la deuxième entrée de tension et l'entrée inverseuse étant connectée électriquement à la première entrée de tension ;
dans lequel la sortie du premier comparateur est adaptée pour contrôler la première source de courant et la troisième source de courant, et la sortie du deuxième comparateur est adaptée pour contrôler la deuxième source de courant et la quatrième source de courant, pour fournir un courant additionnel et améliorer la vitesse de balayage du circuit d'amplificateur opérationnel,
dans lequel la première source de courant (116) et la deuxième source de courant (118) sont connectées électriquement à la sortie de l'amplificateur opérationnel à deux étages (102), alors que la troisième source de courant (120) et la quatrième source de courant (122) sont connectées électriquement à une source d'alimen-

tation du premier amplificateur (108) de l'amplificateur opérationnel à deux étages (102).

2. Circuit d'amplificateur opérationnel selon la revendication 1, dans lequel le premier comparateur et le deuxième comparateur comprennent des transistors ayant des dimensions différentes, et/ou dans lequel les dimensions différentes comprennent des longueurs de canal différentes.

3. Circuit d'amplificateur opérationnel selon la revendication 1 ou 2, dans lequel le premier comparateur est configuré pour détecter le début d'une opération de balayage positif.

4. Circuit d'amplificateur opérationnel selon l'une des revendications 1 à 3, dans lequel le deuxième comparateur est configuré pour détecter le début d'une opération de balayage négatif.

5. Circuit d'amplificateur opérationnel selon la revendication 2, dans lequel les première et troisième sources de courant sont configurées pour s'activer en réponse à la détection par le premier comparateur d'un début d'opération de balayage positif.

6. Circuit d'amplificateur opérationnel selon la revendication 2 ou 5, dans lequel le premier comparateur est configuré pour détecter le début d'une opération de balayage positif en réponse au fait qu'une différence entre la première entrée de tension et la deuxième entrée de tension est une valeur positive supérieure à une tension seuil.

7. Circuit d'amplificateur opérationnel selon la revendication 4, dans lequel les deuxième et quatrième sources de courant sont configurées pour s'activer en réponse à la détection par le deuxième comparateur du début d'une opération de balayage négatif.

8. Circuit d'amplificateur opérationnel selon la revendication 4 ou 7, dans lequel le deuxième comparateur est configuré pour détecter le début d'une opération de balayage négatif en réponse au fait qu'une différence entre la première entrée de tension et la deuxième entrée de tension est une valeur négative dont la valeur absolue est supérieure à une tension seuil.

9. Circuit d'amplificateur opérationnel selon l'une des revendications 1 à 8, dans lequel l'amplificateur opérationnel à deux étages, le premier comparateur et le deuxième comparateur comprennent des dispositifs FinFET.

10. Procédé d'amélioration de la vitesse de balayage d'un amplificateur opérationnel à deux étages (102) ayant un premier étage et un deuxième étage, comprenant :

la détection d'un début d'opération de balayage, dans lequel la détection du début de l'opération de balayage comprend la comparaison d'une différence entre une première tension (V_{in1}) et une deuxième tension (V_{in2}), à l'entrée de l'amplificateur opérationnel à deux étages, à une première tension seuil de commutation et à une deuxième tension seuil de commutation ;
l'activation de sources de courant additionnel durant l'opération de balayage pour améliorer la vitesse de balayage ;
la désactivation des sources de courant additionnel en réponse à l'absence de détection d'une opération de balayage, ce qui réduit la dissipation de puissance additionnelle du courant additionnel,
dans lequel les sources de courant additionnel comprennent une première source de courant (116), une deuxième source de courant (118), une troisième source de courant (120) et une quatrième source de courant (122),
dans lequel la première source de courant (116) et la deuxième source de courant (118) sont connectées électriquement à une sortie de l'amplificateur opérationnel à deux étages (102), alors que la troisième source de courant (120) et la quatrième source de courant (122) sont connectées électriquement à une source d'alimentation du premier amplificateur (108) de l'amplificateur opérationnel à deux étages (102),
dans lequel une résistance (112) en série avec un condensateur (114) sont connectés électriquement en parallèle entre une entrée et une sortie du deuxième étage de l'amplificateur à deux étages,
et dans lequel l'activation de sources de courant additionnel durant l'opération de balayage comprend l'activation des première et troisième sources de courant si la différence entre les première et deuxième tensions est positive et supérieure à la première tension seuil de commutation, et l'activation des deuxième et quatrième sources de courant si la différence entre les première et deuxième tensions est négative et une valeur absolue de la différence est supérieure à la deuxième tension seuil de commutation.

11. Procédé selon la revendication 10,

dans lequel la première tension seuil de commutation correspond à un premier comparateur, et/ou
dans lequel la deuxième tension seuil de commutation correspond à un deuxième comparateur.

12. Procédé selon la revendication 10 ou 11, dans lequel deux transistors d'entrée d'un ou plusieurs desdits comparateurs ont des dimensions différentes, et/ou
dans lequel les dimensions différentes comprennent des longueurs de canal différentes.

13. Procédé selon la revendication 11, dans lequel l'amplificateur opérationnel, le premier comparateur et le deuxième comparateur sont réalisés avec des dispositifs FinFET.

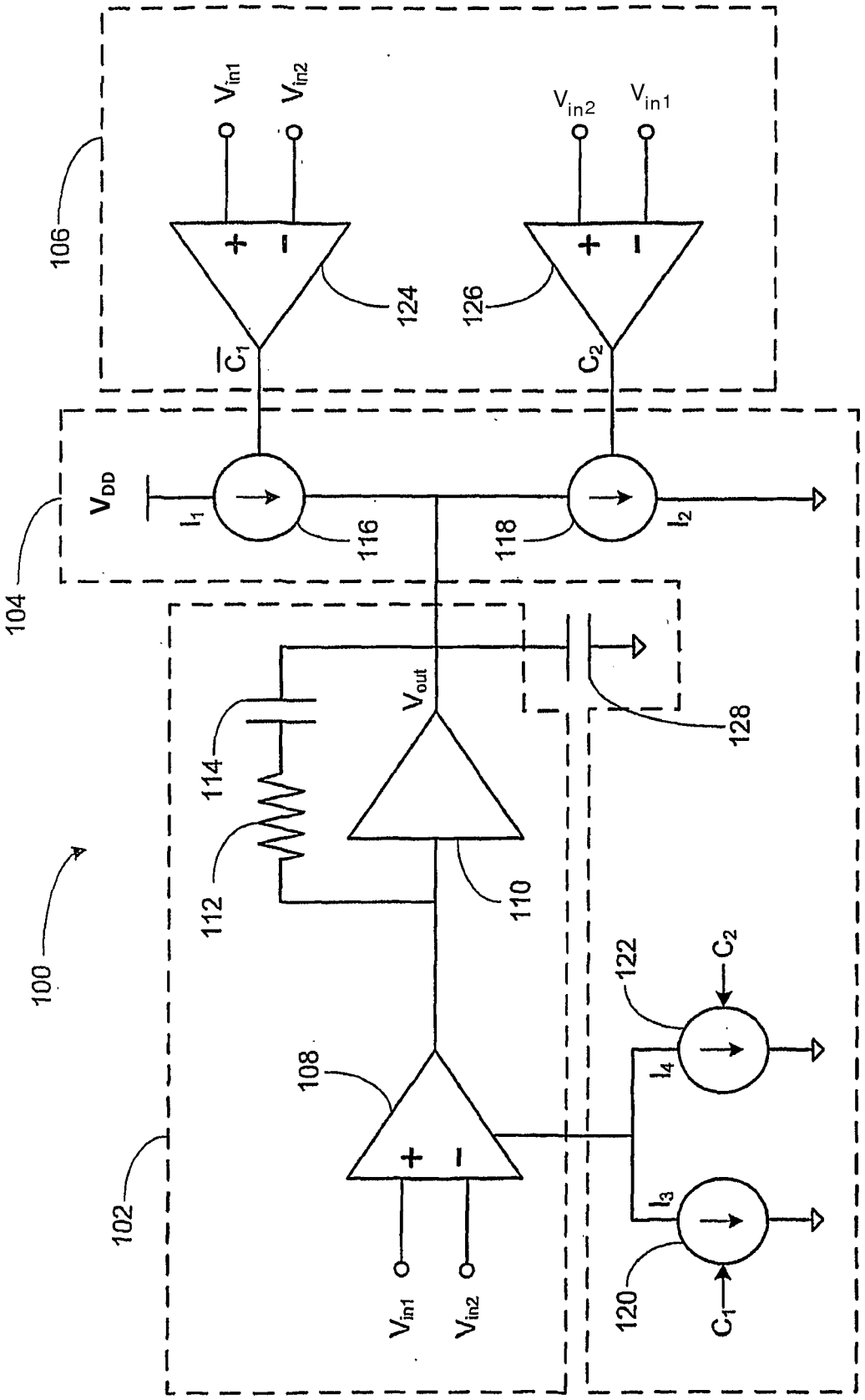
100
102
104
106
108
110
112
114
116
118
120
122
124
126
128
V_{in1}
V_{in2}
V_{in2}
V_{in1}
V_{DD}
I_1
I_2
I_3
I_4
V_{out}
$\overline{C_1}$
C_2
C_2
C_1
+
-

FIGURE 1

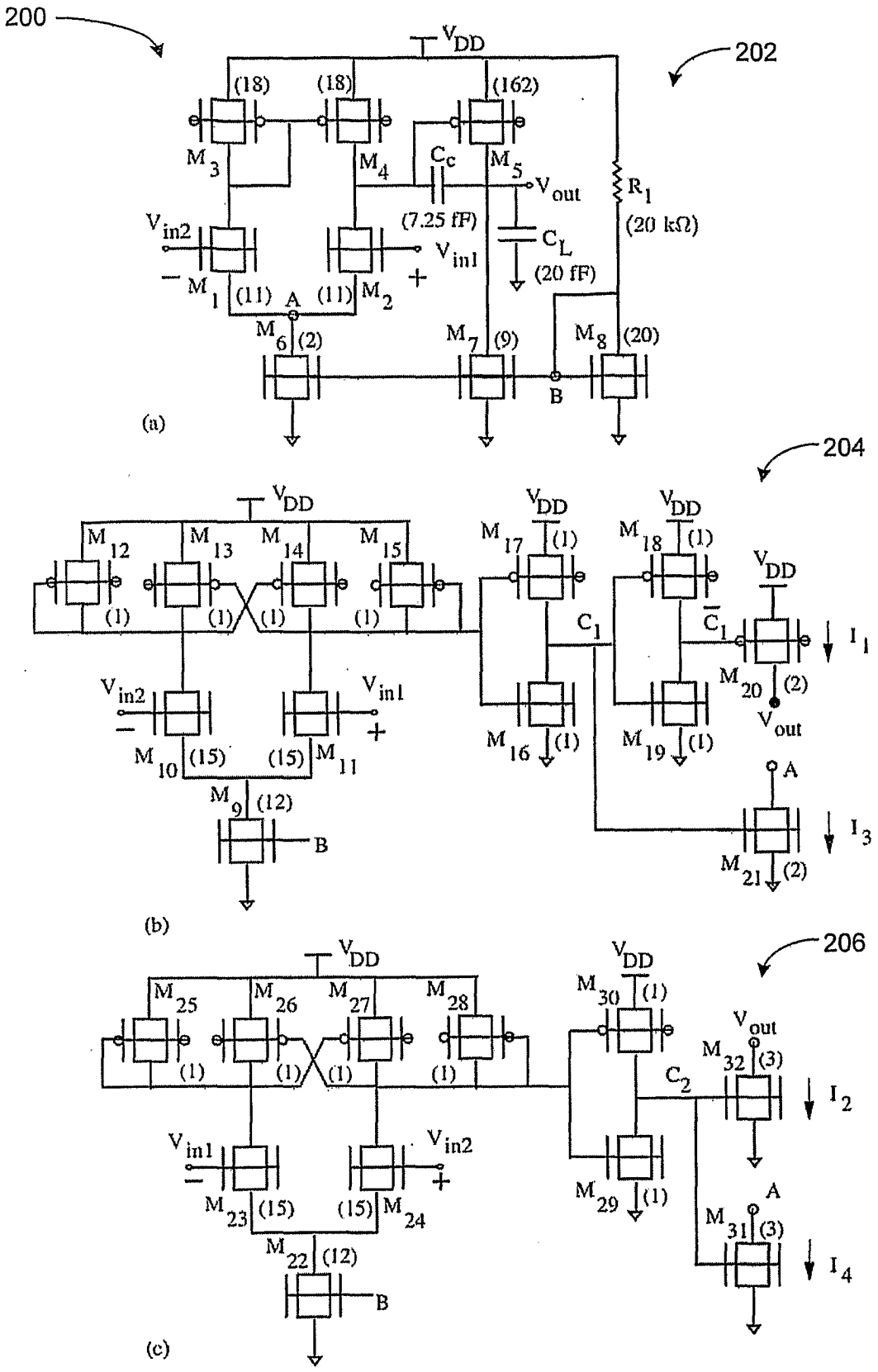
200
202
204
206
V_{DD}
(18)
(18)
(162)
M_3
M_4
C_c
M_5
V_{out}
R_1
(20 kΩ)
(7.25 fF)
C_L
(20 fF)
V_{in2}
V_{in1}
M_1 (11) A (11) M_2
M_6 (2)
M_7 (9)
M_8 (20)
B
(a)
M_{12} M_{13} M_{14} M_{15}
(1) (1) (1) (1)
M_{17} (1)
M_{18} (1)
C_1
$\overline{C}_1$
I_1
M_{20} (2)
V_{out}
M_{16} (1)
M_{19} (1)
A
I_3
M_{21} (2)
M_{10} (15) (15) M_{11}
M_9 (12)
B
(b)
M_{25} M_{26} M_{27} M_{28}
(1) (1) (1) (1)
M_{30} (1)
V_{out}
M_{32} (3)
C_2
I_2
M_{29} (1)
A
M_{31} (3)
I_4
M_{23} (15) (15) M_{24}
M_{22} (12)
B
(c)

FIGURE 2

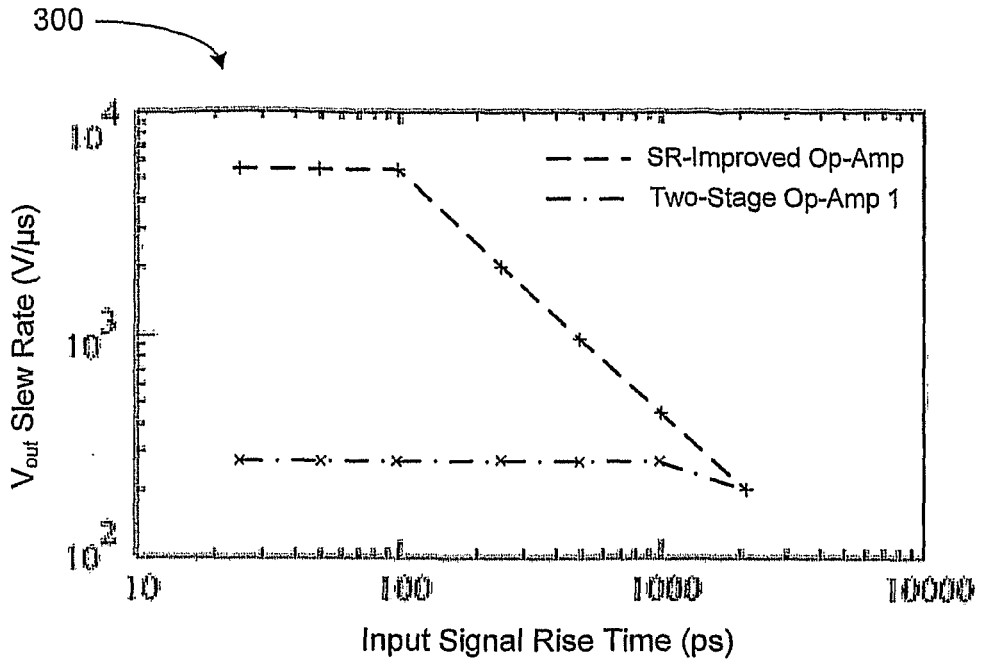

FIGURE 3

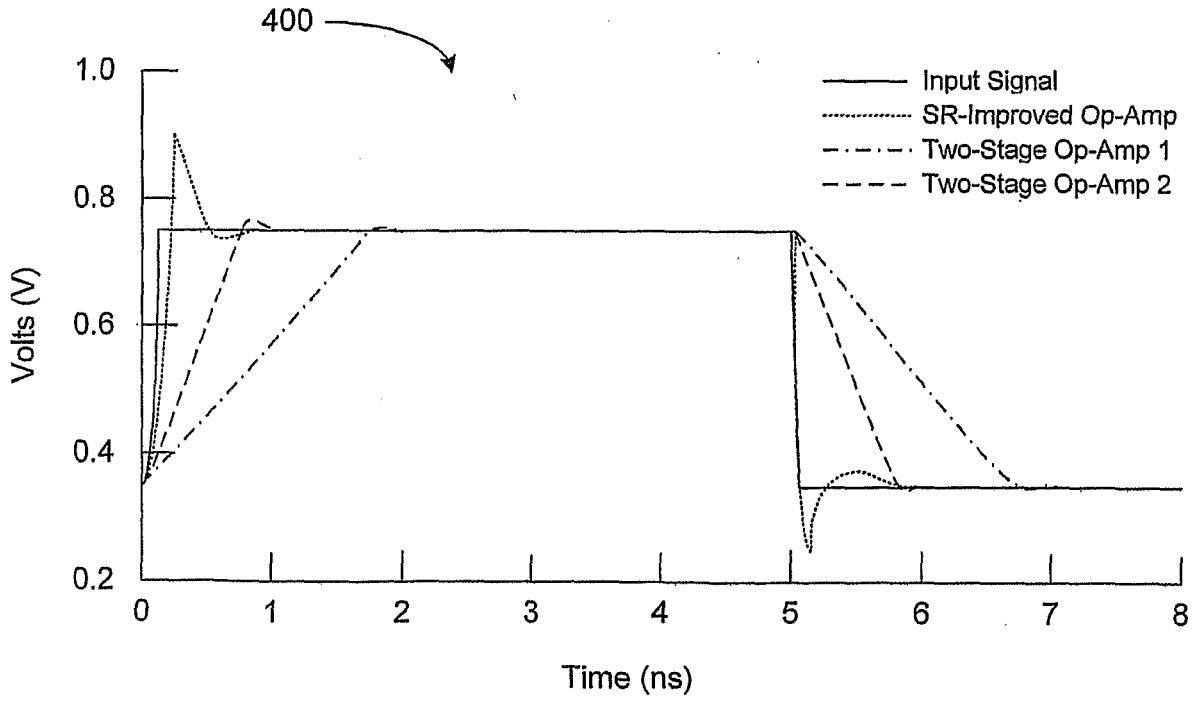

FIGURE 4

REFERENCES CITED IN THE DESCRIPTION

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