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(54) Title: RENAMING FOR REGISTER WITH MULTIPLE BIT FIELDS

(57) Abstract: An apparatus and method are provided for renaming a logical register for which bit accesses of varying lengths are permitted, such as a predicate register. Rename logic supports renaming for both partial-bit accesses and bulk-bit accesses to bits of the register. Rename logic utilizes a rename map table associated with the logical register to be renamed and also includes a plurality of physical rename registers. They physical rename registers include a set of skinny physical rename registers to be used for renaming for partial-bit writes. The physical rename registers also include a set of fat physical rename registers to be used for renaming for bulk-bit writes. Additional sizes of physical rename registers may also be employed. The entries of the single physical rename map table may point to either fat or skinny physical rename registers.



INTERNATIONAL SEARCH REPORT

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A. CLASSI	FICATION OF SUBJECT MATTER G06F9/38							
According to International Patent Classification (IPC) or to both national classification and IPC								
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Minimum do	cumentation searched (classification system followed by classification G06F	on symbols)						
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Documentat	ion searched other than minimum documentation to the extent that s	uch documents are included, in the fields so	earched					
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Electronic d	ata base consulted during the international search (name of data bas	se and, where practical, search terms used)					
EPO-In	ternal							
C. DOCUM	ENTS CONSIDERED TO BE RELEVANT							
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'P' docume	ent published prior to the international filing date but	in the art. *&' document member of the same patent	•					
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