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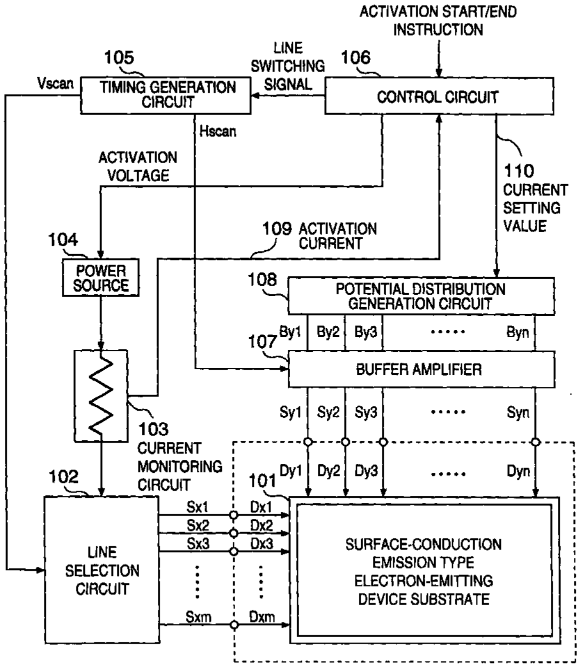
(54) Method and apparatus for manufacturing electron source, and method of manufacturing image forming apparatus

(57) This invention discloses an electron source manufacturing method including the step of applying a voltage to a plurality of conductive members by applying a potential to first portions of the plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and applying a potential to second portions of the plurality of conductive members, wherein the potential applied to the second portions of the plurality of conductive members is set to relax the difference in voltage applied to the plurality of conductive members owing to the difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to an electron source and an image forming apparatus as an application of the electron source.

DESCRIPTION OF THE RELATED ART

[0002] Conventionally, two types of devices, namely hot and cold cathode devices, are known as electron-emitting devices. Known examples of the cold cathode devices are field emission type electron-emitting devices (to be referred to as FE type electron-emitting devices hereinafter), metal/insulator/metal type electron-emitting devices (to be referred to as MIM type electron-emitting devices hereinafter), and surface-conduction emission (SCE) type electron-emitting devices.

[0003] Known examples of the FE type electron-emitting devices are described in W.P. Dyke and W.W. Dolan, "Field emission", Advance in Electron Physics, 8, 89 (1956) and C.A. Spindt, "Physical properties of thin-film field emission cathodes with molybdenium cones", J. Appl. Phys., 47,5248 (1976).

[0004] A known example of the MIM type electron-emitting devices is described in C.A. Mead, "Operation of Tunnel-Emission Devices", J. Appl. Phys., 32,646 (1961).

[0005] A known example of the surface-conduction emission type electron-emitting devices is described in, e.g., M.I. Elinson, "Radio Eng. Electron Phys., 10, 1290 (1965) and other examples will be described later.

[0006] The surface-conduction emission type electron-emitting device utilizes the phenomenon that electrons are emitted from a small-area thin film formed on a substrate by flowing a current parallel through the film surface. The surface-conduction emission type electron-emitting device includes electron-emitting devices using an Au thin film [G. Dittmer, "Thin Solid Films", 9,317 (1972)], an In_2O_3/SnO_2 thin film [M. Hartwell and C.G. Fonstad, "IEEE Trans. ED Conf.", 519 (1975)], a carbon thin film [Hisashi Araki et al., "Vacuum", Vol. 26, No. 1, p. 22 (1983)], and the like, in addition to an SnO_2 thin film according to Elinson mentioned above.

[0007] Fig. 36 is a plan view showing the device by M. Hartwell et al. described above as a typical example of the device structures of these surface-conduction emission type electron-emitting devices. Referring to Fig. 36, reference numeral 3001 denotes a substrate; and 3004, a conductive thin film made of a metal oxide formed by sputtering. This conductive thin film 3004 has an H-shaped pattern, as shown in Fig. 36. An electron-emitting portion 3005 is formed by performing electrification processing (referred to as forming processing to be described later) with respect to the conductive thin film 3004. An interval L in Fig. 36 is set to 0.5 to 1 mm, and a width W is set to 0.1 mm. The electron-emitting portion 3005 is shown in a rectangular shape at the center of the conductive thin film 3004 for the sake of illustrative convenience. However, this does not exactly show the actual position and shape of the electron-emitting portion.

[0008] In the above surface-conduction emission type electron-emitting devices by M. Hartwell et al. and the like, typically the electron-emitting portion 3005 is formed by performing electrification processing called forming processing for the conductive thin film 3004 before electron emission. In the forming processing, for example, a constant DC voltage or a DC voltage which increases at a very low rate of, e.g., 1 V/min is applied across the two ends of the conductive thin film 3004 to partially destroy or deform the conductive thin film 3004, thereby forming the electron-emitting portion 3005 with an electrically high resistance. Note that the destroyed or deformed part of the conductive thin film 3004 has a fissure. Upon application of an appropriate voltage to the conductive thin film 3004 after the forming processing, electrons are emitted near the fissure.

[0009] The above surface-conduction emission type electron-emitting devices are advantageous because they have a simple structure and can be easily manufactured. For this reason, many devices can be formed on a wide area. As disclosed in Japanese Patent Laid-Open No. 64-31332 filed by the present applicant, a method of arranging and driving a lot of devices has been studied.

[0010] Regarding applications of surface-conduction emission type electron-emitting devices to, e.g., image forming apparatuses such as an image display apparatus and an image recording apparatus, electron-beam sources, and the like have been studied.

[0011] As an application to image display apparatuses, in particular, as disclosed in the U.S. Patent No. 5,066,883 and Japanese Patent Laid-Open No. 2-257551 filed by the present applicant, an image display apparatus using the combination of an surface-conduction emission type electron-emitting device and a fluorescent substance which emits light upon reception of an electron beam has been studied. This type of image display apparatus using the combination of the surface-conduction emission type electron-emitting device and the fluorescent substance is expected to have more excellent characteristics than other conventional image display apparatuses. For example, in comparison with recent popular liquid crystal display apparatuses, the above display apparatus is superior in that it does not require a backlight because it is of a self-emission type and that it has a wide view angle.

[0012] Other prior arts are disclosed in Japanese Patent Laid-Open Nos. 7-176265 and 8-248920.

SUMMARY OF THE INVENTION

[0013] It is an object of the present invention to realize a more preferable electron source manufacturing method, image forming apparatus manufacturing method, or electron source manufacturing apparatus.

[0014] According to the present invention, an electron source manufacturing method is characterized by comprising the step of applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and applying a potential to second portions of the plurality of conductive members, thereby applying a voltage to the plurality of conductive members, wherein the potential applied to the second portions of the plurality of conductive members is set to relax a difference in voltage applied to the plurality of conductive members owing to a difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

[0015] Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Fig. 1 is a block diagram showing an activation apparatus according to the first embodiment of the present invention;

Fig. 2 is a circuit diagram showing a line selection circuit used in the first embodiment;

Fig. 3 is a circuit diagram showing a potential distribution generation circuit used in the first embodiment;

Fig. 4 is a circuit diagram showing a driving example of activating devices on a given line in the first embodiment;

Figs. 5A and 5B are graphs each showing the driving voltage distribution of respective devices when the devices on a given line are activated in the first embodiment;

Fig. 6 is a block diagram showing an activation apparatus according to the second embodiment of the present invention;

Figs. 7A and 7B are graphs each showing the driving voltage distribution of respective devices when the devices on a given line are activated in the second embodiment;

Fig. 8 is a block diagram showing an activation apparatus according to the third embodiment of the present invention;

Fig. 9 is a circuit diagram showing a driving example of activating devices on a given line in the third embodiment;

Figs. 10A and 10B are graphs each showing the driving voltage distribution of respective devices when devices on a given line are activated in the third embodiment;

Fig. 11 is a block diagram showing an activation apparatus according to the fourth embodiment of the present invention;

Fig. 12 is a circuit diagram showing a driving example of activating devices on a given line in the fourth embodiment;

Fig. 13 is a block diagram showing an activation apparatus according to the fifth embodiment of the present invention;

Fig. 14 is a circuit diagram showing a driving example of activating devices on a given line in the fifth embodiment;

Fig. 15 is a flow chart showing a control procedure when activation is performed by a procedure of completing activation in units of lines and switching lines;

Fig. 16 is a block diagram showing an activation apparatus according to the sixth embodiment of the present invention;

Fig. 17 is a circuit diagram showing a driving example of activating devices on a given line in the sixth embodiment;

Fig. 18 is a block diagram showing an activation apparatus for a surface-conduction emission type electron-emitting device according to the seventh embodiment;

Fig. 19 is a circuit diagram showing a line selection circuit used in the activation apparatus of the seventh embodiment;

Figs. 20A and 20B are waveform charts each showing a driving voltage waveform applied to each terminal of a surface-conduction emission type electron-emitting device substrate in the seventh embodiment;

Fig. 21 is a flow chart showing a control procedure when activation is performed by a procedure of completing activation in units of lines and switching lines;

Fig. 22 is a partially cutaway perspective view showing the display panel of an image display apparatus according to the embodiment of the present invention;

Figs. 23A and 23B are plan views showing examples of the alignment of fluorescent substances on the face plate of the display panel;

Figs. 24A and 24B are a plan view and a sectional view, respectively, showing a flat surface-conduction emission type electron-emitting device used in the embodiment;

Figs. 25A, 25B, 25C, 25D, and 25E are sectional views showing the steps in manufacturing the flat surface-conduction emission type electron-emitting device;

Fig. 26 is a graph showing an application voltage waveform in forming processing;

Figs. 27A and 27B are graphs respectively showing the an application voltage waveform and a change in emission current Ie in the activation processing;

Fig. 28 is a sectional view showing a step surface-conduction emission type electron-emitting device used in the embodiment;

Figs. 29A, 29B, 29C, 29D, 29E, and 29F are sectional views showing the steps in manufacturing the step surface-conduction emission type electron-emitting device;

Fig. 30 is a graph showing the typical characteristics of the surface-conduction emission type electron-emitting device used in the embodiment;

Fig. 31 is a plan view showing the substrate of a multi electron-beam source used in the embodiment;

Fig. 32 is a sectional view showing part of the substrate of the multi electron-beam source used in the embodiment;

Fig. 33 is a block diagram showing an activation apparatus used in the eighth embodiment;

Fig. 34 is a table showing the contents of a memory used in the eighth embodiment;

Fig. 35 is a graph for explaining the progress of activation in the eighth embodiment;

Fig. 36 is a plan view showing the prior art;

Figs. 37, 38, 39, 40A, and 40B are circuit diagrams for explaining problems;

Figs. 41 and 42 are graphs for explaining problems; and

Figs. 43A and 43B are a circuit diagram and a graph, respectively, for explaining problems.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Detailed problems will be described below.

[0018] The present inventors have examined surface-conduction emission type electron-emitting devices of various materials, various manufacturing methods, and various structures, in addition to the above-mentioned conventional surface-conduction emission type electron-emitting device. Further, the present inventors have made extensive studies on a multi electron-beam source having a large number of surface-conduction emission type electron-emitting devices, and an image display apparatus using this multi electron-beam source.

[0019] The present inventors have examined a multi electron-beam source having an electrical wiring method shown in, e.g., Fig. 37. That is, a large number of surface-conduction emission type electron-emitting devices are two-dimensionally arranged in a matrix to obtain a multi electron-beam source, as shown in Fig. 37.

[0020] Referring to Fig. 37, numeral 4001 denotes a surface-conduction emission type electron-emitting device; 4002, a row-direction wiring; and 4003, a column-direction wiring. The row- and column-direction wirings 4002 and 4003 actually have finite electrical resistances, which are represented as wiring resistances 4004 and 4005 in Fig. 37. This wiring method is called a simple matrix wiring method.

[0021] For the illustrative convenience, the multi electron-beam source is illustrated in a 6 x 6 matrix, but the size of the matrix is not limited to this. For example, in a multi electron-beam source for an image display apparatus, a number of devices enough to perform a desired image display are arranged and wired.

[0022] In a multi electron-beam source in which surface-conduction emission type electron-emitting devices are arranged in a simple matrix, appropriate electrical signals are applied to the row- and column-direction wirings 4002 and 4003 to output a desired electron beam. For example, to drive the surface-conduction emission type electron-emitting devices on an arbitrary row in the matrix, a selection potential Vs is applied to the column-direction wiring 4002 on the row to be selected, and at the same time, a non-selection potential Vns is applied to the row-direction wirings 4002 on unselected rows. In synchronism with this, a driving potential Ve for outputting an electron beam is applied to the column-direction wirings 4003. According to this method, when potential drops across the wiring resistances 4004 and 4005 are neglected, a voltage (Ve - Vs) is applied to the surface-conduction emission type electron-emitting device on the selected row, and a voltage (Ve - Vns) is applied to the surface-conduction emission type electron-emitting devices on the unselected rows. When the potentials Ve, Vs, and Vns are set to appropriate levels, an electron beam having a desired intensity must be output from only the surface-conduction emission type electron-emitting device on the selected row. When different driving potentials Ve are applied to the respective column-direction wirings, electron beams having different intensities must be output from respective devices on the selected row. Since the surface-conduction emission type electron-emitting device has a high response speed, a time for outputting an electron beam can be changed by changing a time for applying the driving potential Ve.

[0023] A multi electron-beam source obtained by arranging surface-conduction emission type electron-emitting devices in a simple matrix has a variety of applications. For example, when a voltage signal corresponding to image information is appropriately applied, the multi electron-beam source can be applied as an electron source for an image display apparatus.

[0024] The present inventors have made extensive studies for improving the characteristics of the surface-conduction emission type electron-emitting device to find that activation processing is effectively performed during the manufacture.

[0025] As described above, the electron-emitting portion of the surface-conduction emission type electron-emitting device is formed by processing (forming processing) of flowing a current through a conductive thin film to partially destroy or deform this thin film, thereby forming a fissure. If activation processing is performed subsequently, electron-emitting characteristics can be greatly improved.

[0026] In activation processing, the electron-emitting portion formed by the forming processing is electrified under appropriate conditions to deposit a deposit such as carbon or carbon compound around the electron-emitting portion. For example, graphite monocrystalline, graphite polycrystalline, amorphous carbon, or mixture thereof is deposited to a thickness of 500 angstroms or less around the electron-emitting portion by periodically applying a voltage pulse in a vacuum atmosphere in which an organic substance exists at an appropriate partial pressure and the total pressure is 10^{-4} to 10^{-5} Torr. These conditions are merely an example and properly changed in accordance with the material and shape of the surface-conduction emission type electron-emitting device.

[0027] This processing can increase the emission current at the same application voltage typically 100 times or greater the emission current immediately after forming processing. (Note that the partial pressure of the organic substance in the vacuum atmosphere is desirably reduced after activation processing.)

[0028] For this reason, activation processing is desirably performed for each device in manufacturing a multi electron-beam source formed by arranging a large number of surface-conduction emission type electron-emitting devices in a simple matrix.

[0029] When the surface-conduction emission type electron-emitting device which undergoes high-resistance processing and activation processing by forming processing during the manufacture is applied to an image forming apparatus, the following problem arises. The problem of activation processing during the manufacture will be explained.

[0030] Various image forming panels to which the surface-conduction emission type electron-emitting device is applied are demanded for high-quality, high-resolution images, as a matter of course. This is realized using a large number of surface-conduction emission type electron-emitting devices arranged in, e.g., a simple matrix. Accordingly, many device lines having several hundred to several thousand rows and columns are required, whereas the surface-conduction emission type electron-emitting devices are desired to have uniform device characteristics. To actually manufacture various high-quality, high-resolution image forming panels, a large number of surface-conduction emission type electron-emitting devices must be formed uniform.

[0031] For example, as a method of forming a large number of surface-conduction emission type electron-emitting devices by activation processing, the present applicant adopted a method of dividing surface-conduction emission type electron-emitting devices arranged in a matrix into a plurality of groups and sequentially applying an activation voltage in units of groups. That is, an activation voltage was sequentially applied to M x N surface-conduction emission type electron-emitting devices as shown in Fig. 38 in units of rows. In Fig. 38, reference symbols EY1 to EYn and EX1 to EXn denote wirings.

[0032] Fig. 39 shows the case in which an activation voltage is applied to surface-conduction emission type electron-emitting devices (black devices in Fig. 39) on the second row. As shown in Fig. 39, the wiring EX2 is connected to an activation potential source, and the remaining electrodes are set to the ground level, i.e., 0 V. According to this method, only the surface-conduction emission type electron-emitting devices on the second row receive the activation voltage in principle, and the remaining surface-conduction emission type electron-emitting devices do not receive any voltage or current. Activation was actually performed by this method to find that the surface-conduction emission type electron-emitting devices exhibited more uniform electron-emitting characteristics.

[0033] However, it is difficult to completely eliminate variations in electron-emitting characteristics, and particularly devices having different electron-emitting characteristics are distributed along one side of the matrix. More specifically, surface-conduction emission type electron-emitting devices on a side farther from the feeding terminal in activation, i.e., on the right side in Fig. 39 exhibited poor electron-emitting characteristics. If such devices are used for the electron source of an image forming apparatus, the brightness or density on one side of an image becomes short.

[0034] The present inventors have extensively studied and cleared up the cause of this problem as follows.

[0035] According to the above-mentioned method shown in Fig. 39, an activation voltage can be applied to only surface-conduction emission type electron-emitting devices on one row in principle. However, since the electrical resistances of the wirings EY1 to EYn and EX1 to EXn are not 0 in practice, a current flows to cause a potential drop. To prevent this, attention is paid to a group of surface-conduction emission type electron-emitting devices on the second row which receive an activation voltage in Fig. 39. A model including their wiring resistances is shown in Fig. 40A.

[0036] In Fig. 40A, reference symbols F1 to FN denote surface-conduction emission type electron-emitting devices; r1 to rN, wiring resistances between devices on the row wiring EX2; and ry, a wiring resistance from the feeding terminal of each of the wirings EY1 to EYN to a corresponding surface-conduction emission type electron-emitting device. Since the row wiring EX2 is generally designed to be formed from a material having a constant line width and thickness, r1 to rN can be considered to be equal except for variations in the manufacture. Since the wirings EY1 to EYN are generally designed to be uniform, the resistances ry of the respective wirings can be considered to be equal.

[0037] A current flowing through the model shown in Fig. 40A will be explained with reference to Fig. 40B. In Fig. 40B, letting I be a current supplied from the activation potential source, and i1 to iN be currents flowing through the surface-conduction emission type electron-emitting devices F1 to FN, the current I is given by the sum of device currents ik flowing through devices Fk, i.e.,

$$I = \Sigma\{k = 1 \text{ to } N\}ik$$

[0038] In addition, letting ir1 to irN be currents flowing through the wiring resistances r1 to rN of respective devices in the row direction,

$$irp = I - \Sigma\ \{k = 0 \text{ to } p-1\}ik$$

(where i0 = 0, and p = integer of 1 to N)

[0039] In other words, the current ir1 flowing through r1 is equal to the sum of currents flowing through all surface-conduction emission type electron-emitting devices, and the current ir2 flowing through r2 is equal to the difference obtained by subtracting the current i1 flowing through the surface-conduction emission type electron-emitting device F1 from the sum of currents flowing through all surface-conduction emission type electron-emitting devices. The current irN flowing through rN is equal to the current iN flowing through the surface-conduction emission type electron-emitting device FN. Therefore, a row-direction wiring nearer the power source flows a larger current.

[0040] In activation processing, changes in device current and emission current are observed with the elapse of time after the start of activation. This will be explained with reference to Fig. 41. Fig. 41 is a graph showing activation characteristics when one of surface-conduction emission type electron-emitting devices arranged in a matrix is activated. As shown in Fig. 41, when activation processing starts, the device current (If in Fig. 41) and emission current (Ie in Fig. 41) flowing through the surface-conduction emission type electron-emitting device increase along with electrification and saturate at last. That is, the current flowing through the surface-conduction emission type electron-emitting device increases along with the progress of activation processing, and the largest current flows through the surface-conduction emission type electron-emitting device at the end of activation processing.

[0041] When an activation voltage is sequentially applied in units of rows in Figs. 40A, 40B, and 41, potential drops occur via the wiring resistances r1 to rN in accordance with the device currents If flowing through respective devices along with the progress of activation, and the potential drops are maximized at the end of activation. At this time, surface-conduction emission type electron-emitting devices aligned on the same row exhibit a voltage distribution shown in Fig. 42. In Fig. 42, the abscissa represents the number of each surface-conduction emission type electron-emitting device, and the ordinate represents a voltage applied to the surface-conduction emission type electron-emitting device. Note that Eac on the ordinate represents the output potential of the activation potential source. If activation processing is performed in units of rows in this manner, voltages applied to respective devices at the end of activation are greatly distributed. As a result, devices having different electron-emitting characteristics are distributed along one side of the matrix. In particular, a device farther from the feeding terminal upon activation cannot receive a sufficient activation voltage, and ideal activation shown in Fig. 41 fails, resulting in poor electron-emitting characteristics of the surface-conduction emission type electron-emitting device. Hence, when devices arranged in a matrix are used for the electron source of an image forming apparatus, the brightness or density on one side of an image becomes short.

[0042] The above description concerns activation processing performed from one side of the substrate for surface-conduction emission type electron-emitting devices arranged in a simple matrix. The same problem also arises when electrodes are extracted from two sides. Fig. 43A is a circuit diagram showing an electrification circuit when electrodes are extracted from two sides, and Fig. 43B shows a device application voltage distribution in this case. As is apparent from Figs. 43A and 43B, in electrification processing from electrodes on two sides, the characteristics of a surface-conduction emission type electron-emitting device at the center degrade due to the same reason as described in electrification processing from one side.

[0043] To solve this problem, a manufacturing method and apparatus which allow an electron source formed by arranging surface-conduction emission type electron-emitting devices in a simple matrix to obtain uniform electron-emitting characteristics, and an electron source manufactured by this method will be explained in the following embodiments.

[0044] The aspects of the present invention will be described.

[0045] According to one aspect of the present invention, an electron source manufacturing method is characterized by comprising the step of applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and applying a potential to second portions of the plurality of conductive members, thereby applying a voltage to the plurality of conductive members, wherein the potential applied to the second portions of the plurality of conductive members is set to relax the difference in voltage applied to the plurality of conductive members owing to the difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

[0046] A voltage corresponding to the potential difference between the potentials of the first and second portions of the conductive member is applied to the conductive member. For example, when the potentials differ between respective portions on the wiring, if the potentials of the second portions of the conductive members are set equal, voltages applied between the first and second portions of the conductive members become different from each other. According to the present invention, voltages applied to the first and second portions of the conductive members can be made close to each other by setting the potential of the second portion to relax the difference between voltages.

[0047] To substantially apply a voltage between the first and second portions, different potentials are applied to the first and second portions. Either one potential may be the ground potential.

[0048] As the conductive member which receives the voltage and serves as at least part of the electron-emitting device, one having undergone, e.g., the forming step of the surface-conduction emission type electron-emitting device can be suitably used.

[0049] As the conductive member, a conductive film can be used. As the form of a conductive member which receives the voltage, a form having a high-resistance portion between the first and second portions, e.g., a gap formed between the first and second portions can be adopted. The voltage application step can be particularly applied to the step of depositing a deposit in or near the gap. This voltage application step is suitable when a current flowing through the conductive member increases or a current flowing through the conductive member increases or a current flowing through a wiring connected to the conductive member increases, as will be described in the following embodiments.

[0050] When the electron source has pluralities of row and column wirings constituting a matrix, the voltage application step is performed for a plurality of conductive members having first portions connected to one row wiring by a potential applied to the row wiring and a potential applied to column wirings each connected to the second portion of each conductive member.

[0051] The potential applied to the second portion may be changed in accordance with a change in potential applied to the first portion. Especially when the resistance value between the first and second portions of the conductive member changes along with voltage application, the degree of potential drop on the wiring also changes, the potential of the first portion changes, and thus the potential applied to the second portion is desirably controlled in accordance with the change in potential of the first portion.

[0052] The potential applied to the first portion need not necessarily be measured. For example, this potential can be estimated by measuring a current flowing through the conductive member. A circuit for automatically setting the second potential in accordance with the measured current may be employed.

[0053] In addition, one or both of the potential applied to the first portion and the potential applied to the second portion are preferably applied as pulses.

[0054] In particular, preferably, a potential applied to the wiring commonly connected to the plurality of conductive members and the potential applied to the second portion are applied as pulses, and the pulse-like potential applied to the wiring commonly connected to the plurality of conductive members is applied after the pulse-like potential applied to the second portion.

[0055] The conductive member is preferably connected to one of a plurality of row wirings and one of a plurality of column wirings that constitute a matrix, and the voltage application step preferably comprises the step of applying a voltage to conductive members connected to a row wiring selected from the plurality of row wirings by a potential applied to the first portions in accordance with a potential applied to the selected row wiring and a potential applied to the second portions in accordance with a potential applied to the plurality of column wirings.

[0056] In the voltage application step, an unselected row wiring out of the plurality of row wirings preferably receives a potential for suppressing a current flowing through the unselected row wiring owing to the potential difference from the potential applied to the column wiring.

[0057] Further, one or both of the potential applied to the unselected row wiring and the potential applied to the column wiring are preferably set to set the potential of the unselected row wiring to a potential between the maximum and minimum values of the potential applied to the plurality of column wirings, e.g., to an intermediate value between the maximum and minimum values.

[0058] One or both of the potential applied to the unselected row wiring and the potential applied to the column wiring are preferably set to set the ground potential between the maximum and minimum values of the potential applied to the plurality of column wirings.

[0059] The electron source manufacturing method preferably comprises the step of applying the voltage while sequentially switching row wirings to be selected, and more preferably comprises the step of selecting a given row wiring and applying the voltage to conductive members connected to the selected row wiring at a time interval, thereby applying the voltage and the step of selecting another row wiring during the time interval and applying the voltage to conductive members connected to this another row wiring.

[0060] As another aspect of the present invention, a method of manufacturing an image forming apparatus having an electron source and an image forming member for forming an image upon irradiation of electrons emitted by the electron source is characterized by comprising the steps of manufacturing the electron source by the electron source manufacturing method described above, and assembling the electron source and the image forming member.

[0061] As still another aspect of the present invention, an electron source manufacturing apparatus is characterized by comprising a first circuit for applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and a second circuit for applying a potential to second portions of the plurality of conductive members, wherein the second circuit sets the potential applied to the second-portions of the plurality of conductive members so as to relax a difference in voltage applied to the plurality of conductive members owing to a difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

[0062] For example, the apparatus preferably comprises a current monitoring circuit for monitoring a current flowing through the conductive member.

[0063] The second circuit preferably sets the potential on the basis of a current flowing through the conductive member.

[0064] The second circuit preferably controls the potential applied to the second portion in accordance with the application time of the potential to the second portion.

[0065] The second circuit may comprise memory means which is referred to in order to set the potential applied to the second portion.

[0066] The second circuit may include a circuit which generates potential differences which are equal to potential differences at the portions respectively connected to the first portions of the plurality of conductive members commonly connected in the wiring The configuration can be realized by, for example, sinking an electric current from each of the plurality of conductive member or supplying an electric current to each of the plurality of conductive member at predetermined points of an equivalent wiring resistance array having a resistance substantially equal to the resistance of the wiring. The value of the current flowing the plurality of conductive members can be acquired by monitoring the current flowing the wiring and dividing the monitored values by the number of conductive members connected with the wiring. Alternatively, the current value flowing the plurality of conductive members can be acquired by measuring a current flowing the each wiring connected with the second portion. Further, the current can be acquired according to data previously measured. The potentials to be applied to the respective second portions are obtained by superposing the potential distribution and an offset potential.

[0067] If the first circuit applies a potential from the two sides of the wiring, the degree of potential drop can be suppressed.

[0068] A voltage applying circuit applying a voltage to a plurality of conductive members connected with a plurality of row wirings and a plurality of column wirings which form a matrix, comprising:

> first circuit supplying a predetermined potential to a row wiring selected among the plurality of row wirings; and
> second circuit supplying a predetermined potential to each of the plurality of column wirings,
> wherein said second circuit includes a potential distribution generating circuit having an equivalent wiring resistance array and a source of a control current, wherein the equivalent wiring resistance array has a resistance substantially equal to the resistance of the row wiring, and the source of the control current serves to sink or supply a current flowing said plurality of conductive members.

[0069] The second circuit preferably has a circuit for superposing the potential distribution generated by said potential distribution generating circuit and an offset potential. For instance, a buffer amplifier may serve as such circuit.

[0070] The aforementioned conductive member may have various configurations. For instance, the conductive member may have a pair of electrodes which pass an electric current when different potentials are applied.

[0071] Detailed embodiments will be described below.

[First Embodiment]

[0072] An activation apparatus for a surface-conduction emission type electron-emitting device according to an embodiment of the present invention will be described with reference to Fig. 1. First, the arrangement and manufacturing method of a display panel to which the present invention is applied will be exemplified.

(Arrangement and Manufacturing Method of Display Panel)

[0073] Fig. 22 is a partially cutaway perspective view of a display panel 101 used in the embodiment in Fig. 1, showing the internal structure of the panel.

[0074] In Fig. 22, reference numeral 1005 denotes a rear plate; 1006, a side wall; and 1007, a face plate. These parts 1005 to 1007 constitute an airtight container for maintaining the inside of the display panel vacuum. To construct the airtight container, it is necessary to seal-connect the respective parts to obtain sufficient strength and maintain airtight condition. For example, frit glass is applied to junction portions, and sintered at 400 to 500°C in air or nitrogen atmosphere, thus the parts are seal-connected. A method for exhausting air from the inside of the container will be described later.

[0075] The rear plate 1005 has a substrate 1001 fixed thereon, on which N x M cold cathode devices 1002 are formed (M, N = positive integer equal to 2 or more, properly set in accordance with a desired number of display pixels. For example, in a display apparatus for high-resolution television display, preferably N = 3,000 or more, M = 1,000 or more. In the first embodiment, N = 3,072 or more, M = 1,024.) The N x M cold cathode devices are arranged in a simple matrix with M row-direction wirings 1003 and N column-direction wirings 1004. The portion constituted by the components denoted by references 1001 to 1004 will be referred to as a multi electron-beam source. The manufacturing method and structure of the multi electron-beam source will be described in detail later.

[0076] In this embodiment, the substrate 1001 of the multi electron-beam source is fixed to the rear plate 1005 of the airtight container. If, however, the substrate 1001 of the multi electron-beam source has sufficient strength, the substrate 1001 of the multi electron-beam source may also serve as the rear plate of the airtight container.

[0077] A fluorescent film 1008 is formed on the lower surface of the face plate 1007. As this embodiment is a color display apparatus, the fluorescent film 1008 is coated with red, green, and blue fluorescent substances, i.e., three primary color fluorescent substances used in the CRT field. As shown in Fig. 23A, the respective color fluorescent substances are formed into a striped structure, and black conductive members 1010 are provided between the stripes of the fluorescent substances. The purpose of providing the black conductive members 1010 is to prevent display color misregistration even if the electron-beam irradiation position is shifted to some extent, to prevent degradation of display contrast by shutting off reflection of external light, to prevent the charge-up of the fluorescent film by the electron beam, and the like. As a material for the black conductive members 1010, graphite is used as a main component, but other materials may be used so long as the above purpose is attained.

[0078] Further, three-primary colors of the fluorescent film is not limited to the stripes as shown in Fig. 23A. For example, delta arrangement as shown in Fig. 23B or any other arrangement may be employed.

[0079] Note that when a monochrome display panel is formed, a single-color fluorescent substance may be applied to the fluorescent film 1008, and the black conductive member may be omitted.

[0080] Furthermore, a metal back 1009, which is well-known in the CRT field, is provided on the fluorescent film 1008 on the rear plate side. The purpose of providing the metal back 1009 is to improve the light-utilization ratio by mirror-reflecting part of the light emitted by the fluorescent film 1008, to protect the fluorescent film 1008 from collision with negative ions, to be used as an electrode for applying an electron-beam accelerating voltage, to be used as a conductive path for electrons which excited the fluorescent film 1008, and the like. The metal back 1009 is formed by forming the fluorescent film 1008 on the face plate substrate 1007, smoothing the front surface of the fluorescent film, and depositing Al thereon by vacuum deposition. Note that when fluorescent substances for a low voltage is used for the fluorescent film 1008, the metal back 1009 is not used.

[0081] Furthermore, for application of an accelerating voltage or improvement of the conductivity of the fluorescent film, transparent electrodes made of, e.g., ITO may be provided between the face plate substrate 1007 and the fluorescent film 1008, although such electrodes are not used in this embodiment.

[0082] Dx1 to Dxm, Dy1 to Dyn, and Hv are electric connection terminals for an airtight structure provided to electrically connect the display panel to an electric circuit (not shown). Dx1 to Dxm are electrically connected to the row-direction wirings 1003 of the multi electron-beam source; Dy1 to Dyn, to the column-direction wirings 1004 of the multi electron-beam source; and Hv, to the metal back 1009 of the face plate.

[0083] To evacuate the airtight container, after forming the airtight container, an exhaust pipe and a vacuum pump (neither is shown) are connected, and the airtight container is evacuated to a vacuum of about 10^{-7} Torr. Thereafter, the exhaust pipe is sealed. To maintain the vacuum in the airtight container, a getter film (not shown) is formed at a predetermined position in the airtight container immediately before/after the sealing. The getter film is a film formed by heating and evaporating a getter material mainly consisting of, e.g., Ba, by heating or RF heating. The suction effect of the getter film maintains a vacuum of 1×10^{-5} or 1×10^{-7} Torr in the container.

[0084] The basic arrangement and manufacturing method of the display panel according to the first embodiment of the present invention have been briefly described above.

[0085] A method of manufacturing the multi electron-beam source used in the display panel of this embodiment will be described below. In manufacturing the multi electron-beam source used in the image display apparatus of the present invention, any material, shape, and manufacturing method for cold cathode device devices may be employed as long as an electron source can be obtained by arranging cold cathode devices in a simple matrix. Therefore, cold cathode devices such as surface-conduction emission type electron-emitting devices, FE type devices, or MIM type devices can be used.

[0086] Under circumstances where inexpensive display apparatuses having large display areas are required, a surface-conduction emission type electron-emitting device, of these cold cathode devices, is especially preferable. More specifically, the electron-emitting characteristic of an FE type device is greatly influenced by the relative positions and shapes of the emitter cone and the gate electrode, and hence a high-precision manufacturing technique is required to manufacture this device. This poses a disadvantageous factor in attaining a large display area and a low manufacturing cost. According to an MIM type device, the thicknesses of the insulating layer and the upper electrode must be decreased and made uniform. This also poses a disadvantageous factor in attaining a large display area and a low manufacturing cost. In contrast to this, a surface-conduction emission type electron-emitting device can be manufactured by a relatively simple manufacturing method, and hence an increase in display area and a decrease in manufacturing cost can be attained. The present inventors have also found that among the surface-conduction emission type electron-emitting devices, an electron beam source having an electron-emitting portion or its peripheral portion consisting of a fine particle film is excellent in electron-emitting characteristic and can be easily manufactured. Such a device can therefore be most suitably used for the multi electron-beam source of a high-brightness, large-screen image display apparatus. For this reason, in the display panel of this embodiment, surface-conduction emission type electron-emitting devices each having an electron-emitting portion or its peripheral portion made of a fine particle film are used. The basic structure, manufacturing method, and characteristics of the preferred surface-conduction emission type electron-emitting device will be described first. The structure of the multi electron-beam source having many devices arranged in a simple matrix will be described later.

(Preferred Structure of Surface-Conduction Emission Type Electron-Emitting Device and Preferred Manufacturing Method)

[0087] Typical examples of surface-conduction emission type electron-emitting devices each having an electron-emitting portion or its peripheral portion made of a fine particle film include two types of devices, namely flat and step type devices.

(Flat Surface-Conduction Emission Type Electron-Emitting Device)

[0088] First, the structure and manufacturing method of a flat surface-conduction emission type electron-emitting device will be described. Figs. 24A and 24B are a plan view and a sectional view, respectively, for explaining the structure of the flat surface-conduction emission type electron-emitting device. Referring to Figs. 24A and 24B, reference numeral 1101 denotes a substrate; 1102 and 1103, device electrodes; 1104, a conductive thin film; 1105, an electron-emitting portion formed by the forming processing; and 1113, a thin film formed by the activation processing.

[0089] As the substrate 1101, various glass substrates of, e.g., quartz glass and soda-lime glass, various ceramic substrates of, e.g., alumina, or any of those substrates with an insulating layer formed thereon can be employed.

[0090] The device electrodes 1102 and 1103, provided in parallel to the substrate 1101 and opposing to each other, comprise conductive material. For example, any material of metals such as Ni, Cr, Au, Mo, W, Pt, Ti, Cu, Pd and Ag, or alloys of these metals, otherwise metal oxides such as In_2O_3-SnO_2, or semiconductive material such as polysilicon, can be employed. These electrodes 1102 and 1103 can be easily formed by the combination of a film-forming technique such as vacuum-evaporation and a patterning technique such as photolithography or etching, however, any other method (e.g., printing technique) may be employed.

[0091] The shape of the electrodes 1102 and 1103 is appropriately designed in accordance with an application object of the electron-emitting device. Generally, an interval L between electrodes is designed by selecting an appropriate value in a range from hundreds angstroms to hundreds micrometers. Most preferable range for a display apparatus is from several micrometers to ten micrometers. As for electrode thickness d, an appropriate value is selected in a range from hundreds angstroms to several micrometers.

[0092] The conductive thin film 1104 comprises a fine particle film. The "fine particle film" is a film which contains a lot of fine particles (including masses of particles) as film-constituting members. In microscopic view, normally individual particles exist in the film at predetermined intervals, or in adjacent to each other, or overlapped with each other.

[0093] One particle has a diameter within a range from several angstroms to thousand angstroms. Preferably, the diameter is within a range from 10 angstroms to 200 angstroms. The thickness of the fine particle film is appropriately set in consideration of conditions as follows. That is, condition necessary for electrical connection to the device electrode 1102 or 1103, condition for the forming processing to be described later, condition for setting electrical resistance of the fine particle film itself to an appropriate value to be described later etc.

[0094] Specifically, the thickness of the film is set in a range from several angstroms to thousand angstroms, more preferably, 10 angstroms to 500 angstroms.

[0095] Materials used for forming the fine particle film are, e.g., metals such as Pd, Pt, Ru, Ag, Au, Ti, In, Cu, Cr, Fe, Zn, Sn, Ta, W and Pb, oxides such as PdO, SnO_2, In_2O_3, PbO and Sb_2O_3, borides such as HfB_2, ZrB_2, LaB_6, CeB_6, YB_4 and GdB_4, carbides such as TiC, ZrC, HfC, TaC, SiC, and WC, nitrides such as TiN, ZrN and HfN, semiconductors such as Si and Ge, and carbons. Any of appropriate material(s) is appropriately selected.

[0096] As described above, the conductive thin film 1104 is formed with a fine particle film, and sheet resistance of the film is set to reside within a range from 10^3 to 10^7 (Ω/sq).

[0097] As it is preferable that the conductive thin film 1104 is electrically connected to the device electrodes 1102 and 1103, they are arranged so as to overlap with each other at one portion. In Figs. 24A and 24B, the respective parts are overlapped in order of, the substrate, the device electrodes, and the conductive thin film, from the bottom. This overlapping order may be, the substrate, the conductive thin film, and the device electrodes, from the bottom.

[0098] The electron-emitting portion 1105 is a fissured portion formed at a part of the conductive thin film 1104. The electron-emitting portion 1105 has a resistance characteristic higher than peripheral conductive thin film. The fissure is formed by the forming processing to be described later on the conductive thin film 1104. In some cases, particles, having a diameter of several angstroms to hundreds angstroms, are arranged within the fissured portion. As it is difficult to exactly illustrate actual position and shape of the electron-emitting portion, therefore, Figs. 24A and 24B show the fissured portion schematically.

[0099] The thin film 1113, which comprises carbon or carbon compound material, covers the electron-emitting portion 1115 and its peripheral portion. The thin film 1113 is formed by the activation processing to be described later after the forming processing.

[0100] The thin film 1113 is preferably graphite monocrystalline, graphite polycrystalline, amorphous carbon, or mixture thereof, and its thickness is 500 angstroms or less, more preferably, 300 angstroms or less.

[0101] As it is difficult to exactly illustrate actual position or shape of the thin film 1113, Figs. 24A and 24B show the film schematically. Fig. 24A shows the device where a part of the thin film 1113 is removed.

[0102] The preferred basic structure of the surface-conduction emission type electron-emitting device is as described above. In the embodiment, the device has the following constituents.

[0103] That is, the substrate 1101 comprises a soda-lime glass, and the device electrodes 1102 and 1103, an Ni thin film. The electrode thickness d is 1,000 angstroms and the electrode interval L is 2 μm.

[0104] The main material of the fine particle film is Pd or PdO. The thickness of the fine particle film is about 100 angstroms, and its width W is 100 μm.

[0105] Next, a method of manufacturing a preferred flat surface-conduction emission type electron-emitting device will be described with reference to Figs. 25A to 25D which are sectional views showing the manufacturing processes of the surface-conduction emission type electron-emitting device. Note that reference numerals are the same as those in Fig. 24B.

1) First, as shown in Fig. 25A, the device electrodes 1102 and 1103 are formed on the substrate 1101.

In formation, first, the substrate 1101 is fully washed with a detergent, pure water and an organic solvent, then, material of the device electrodes is deposited there. (As a depositing method, a vacuum film-forming technique such as evaporation and sputtering may be used.) Thereafter, patterning using a photolithography etching technique is performed on the deposited electrode material. Thus, the pair of device electrodes (1102 and 1103) shown in Fig. 24A are formed.

2) Next, as shown in Fig. 25B, the conductive thin film 1104 is formed.

In formation, first, an organic metal solvent is applied to the substrate in Fig. 25A, then the applied solvent is dried and sintered, thus forming a fine particle film. Thereafter, the fine particle film is patterned into a predetermined shape by the photolithography etching method. The organic metal solvent means a solvent of organic metal compound containing material of minute particles, used for forming the conductive thin film, as main component. (More specifically, Pd is used in this embodiment. In the embodiment, application of organic metal solvent is made by dipping, however, any other method such as a spinner method and spraying method may be employed.)

As a film-forming method of the conductive thin film made with the minute particles, the application of organic metal solvent used in the embodiment can be replaced with any other method such as a vacuum evaporation method, a sputtering method or a chemical vapor-phase accumulation method.

3) Then, as shown in Fig. 25C, appropriate voltage is applied between the device electrodes 1102 and 1103, from a power source 1110 for the forming processing, then the forming processing is performed, thus forming the electron-emitting portion 1105.

The forming processing here is electric energization of a conductive thin film 1104 to appropriately destroy, deform, or deteriorate a part of the conductive thin film, thus changing the film to have a structure suitable for electron emission. In this embodiment, a fine particle film is used as the conductive thin film 1104. In the conductive thin film made of the fine particle film, the portion changed for electron emission (i.e., electron-emitting portion 1105) has an appropriate fissure in the thin film. Comparing the thin film 1104 having the electron-emitting portion 1105 with the thin film before the forming processing, the electrical resistance measured between the device electrodes 1102 and 1103 has greatly increased.

The electrification method will be explained in more detail with reference to Fig. 26 showing an example of waveform of appropriate voltage applied from the forming power source 1110. Preferably, in case of forming a conductive thin-film of a fine particle film, a pulse-like voltage is employed. In this embodiment, as shown in Fig. 26, a triangular-wave pulse having a pulse width T1 is continuously applied at pulse interval of T2. Upon application, a wave peak value Vpf of the triangular-wave pulse is sequentially increased. Further, a monitor pulse Pm to monitor status of forming the electron-emitting portion 1105 is inserted between the triangular-wave pulses at appropriate intervals, and current that flows at the insertion is measured by a galvanometer 1111.

In this embodiment, in 10^{-5} Torr vacuum atmosphere, the pulse width T1 is set to 1 msec; and the pulse interval T2, to 10 msec. The wave peak value Vpf is increased by 0.1 V, at each pulse. Each time the triangular-wave has been applied for five pulses, the monitor pulse Pm is inserted. To avoid ill-effecting the forming processing, a voltage Vpm of the monitor pulse is set to 0.1 V. When the electrical resistance between the device electrodes 1102 and 1103 becomes $1 \times 10^6\ \Omega$, i.e., the current measured by the galvanometer 1111 upon application of monitor pulse becomes 1×10^{-7} A or less, the electrification of the forming processing is terminated.

Note that the above processing method is preferable to the surface-conduction emission type electron-emitting device of this embodiment. In case of changing the design of the surface-conduction emission type electron-emitting device concerning, e.g., the material or thickness of the fine particle film, or the device electrode interval L, the conditions for electrification are preferably changed in accordance with the change of device design.

(4) Next, as shown in Fig. 25D, appropriate voltage is applied, from an activation power source 1112, between the device electrodes 1102 and 1103, and the activation processing is performed to improve electron-emitting characteristic.

The activation processing here is electrification of the electron-emitting portion, particularly, the electron-emitting portion 1105 formed by the forming processing, on appropriate condition(s), for depositing carbon or carbon compound around the electron-emitting portion 1105. In Fig. 25D, the deposited material of carbon or carbon compound is shown as material 1113. Comparing the electron-emitting portion 1105 with that before the activation processing, the emission current at the same application voltage has become, typically 100 times or greater.

The activation is made by periodically applying a voltage pulse in 10^{-4} or 10^{-5} Torr vacuum atmosphere, to accumulate carbon or carbon compound mainly derived from organic compound (s) existing in the vacuum atmosphere. The accumulated material 1113 is any of graphite monocrystalline, graphite polycrystalline, amorphous carbon or mixture thereof. The thickness of the accumulated material 1113 is 500 angstroms or less, more preferably, 300 angstroms or less.

The electrification method will be described in more detail with reference to Fig. 27A showing an example of waveform of appropriate voltage applied from the activation power source 1112. In this embodiment, the activation processing is performed by periodically applying a rectangular wave at a predetermined voltage. A rectangular-wave voltage Vac is set to 14 V; a pulse width T3, to 1 msec; and a pulse interval T4, to 10 msec. Note that the above electrification conditions are preferable for the surface-conduction emission type electron-emitting device of the embodiment. In the case in which the design of the surface-conduction emission type electron-emitting device is changed, the electrification conditions are preferably changed in accordance with the change of device design.

[0106] In Fig. 25D, reference numeral 1114 denotes an anode electrode, connected to a direct-current (DC) high-voltage power source 1115 and a galvanometer 1116, for capturing emission current Ie emitted from the surface-conduction emission type electron-emitting device. (In the case in which the substrate 1101 is incorporated into the display panel before the activation processing, the Al layer on the fluorescent surface of the display panel is used as the anode electrode 1114.) While applying voltage from the activation power source 1112, the galvanometer 1116 measures the emission current Ie, thus monitors the progress of activation processing, to control the operation of the activation power source 1112. Fig. 27B shows an example of the emission current Ie measured by the galvanometer 1116. As application of pulse voltage from the activation power source 1112 is started in this manner, the emission current Ie increases with elapse of time, gradually comes into saturation, and almost never increases then. At the substantial saturation point, the voltage application from the activation power source 1112 is stopped, then the activation processing is terminated.

[0107] Note that the above electrification conditions are preferable to the surface-conduction emission type electron-emitting device of the embodiment. In case of changing the design of the surface-conduction emission type electron-emitting device, the conditions are preferably changed in accordance with the change of device design.

[0108] As described above, the surface-conduction emission type electron-emitting device as shown in Fig. 25E is manufactured.

(Step Surface-Conduction Emission Type Electron-Emitting Device)

[0109] Next, another typical structure of the surface-conduction emission type electron-emitting device where an electron-emitting portion or its peripheral portion is formed of a fine particle film, i.e., a stepped surface-conduction emission type electron-emitting device will be described.

[0110] Fig. 28 is a sectional view schematically showing the basic construction of the step surface-conduction emission type electron-emitting device. Referring to Fig. 28, reference numeral 1201 denotes a substrate; 1202 and 1203, device electrodes; 1206, a step-forming member for making height difference between the electrodes 1202 and 1203; 1204, a conductive thin film using a fine particle film; 1205, an electron-emitting portion formed by the forming processing; and 1213, a thin film formed by the activation processing.

[0111] Difference between the step device from the above-described flat device is that one of the device electrodes (1202 in this example) is provided on the step-forming member 1206 and the conductive thin film 1204 covers the side surface of the step-forming member 1206. The device interval L in Fig. 24A is set in this structure as a height difference Ls corresponding to the height of the step-forming member 1206. Note that the substrate 1201, the device electrodes 1202 and 1203, the conductive thin film 1204 using the fine particle film can comprise the materials given in the explanation of the flat surface-conduction emission type electron-emitting device. Further, the step-forming member 1206 comprises electrically insulating material such as SiO_2.

[0112] Next, a method of manufacturing the stepped surface-conduction emission type electron-emitting device will be described with reference Figs. 29A to 29F which are sectional views showing the manufacturing processes. In these figures, reference numerals of the respective parts are the same as those in Fig. 28.

(1) First, as shown in Fig. 29A, the device electrode 1203 is formed on the substrate 1201.
(2) Next, as shown in Fig. 29B, an insulating layer for forming the step-forming member is deposited. The insulating layer may be formed by accumulating, e.g., SiO_2 by a sputtering method, however, the insulating layer may be formed by a film-forming method such as a vacuum evaporation method or a printing method.
(3) Next, as shown in Fig. 29C, the device electrode 1202 is formed on the insulating layer.
(4) Next, as shown in Fig. 29D, a part of the insulating layer is removed by using, e.g., an etching method, to expose the device electrode 1203.
(5) Next, as shown in Fig. 29E, the conductive thin film 1204 using the fine particle film is formed. Upon formation, similar to the above-described flat device structure, a film-forming technique such as an applying method is used.
(6) Next, similar to the flat device structure, the forming processing is performed to form an electron-emitting portion. (The forming processing similar to that explained using Fig. 25C may be performed.)
(7) Next, similar to the flat device structure, the activation processing is performed to deposit carbon or carbon compound around the electron-emitting portion. (Activation processing similar to that explained using Fig. 25D may be performed).

[0113] As described above, the stepped surface-conduction emission type electron-emitting device shown in Fig. 29F is manufactured.

(Characteristic of Surface-Conduction Emission Type Electron-Emitting Device Used in Display Apparatus)

[0114] The structure and manufacturing method of the flat surface-conduction emission type electron-emitting device and those of the stepped surface-conduction emission type electron-emitting device are as described above. Next, the characteristic of the electron-emitting device used in the display apparatus will be described below.

[0115] Fig. 30 shows a typical example of (emission current Ie) to (device voltage (i.e., voltage to be applied to the device) Vf) characteristic and (device current If) to (device application voltage Vf) characteristic of the device used in the display apparatus. Note that compared with the device current If, the emission current Ie is very small, therefore it is difficult to illustrate the emission current Ie by the same measure of that for the device current If. In addition, these characteristics change due to change of designing parameters such as the size or shape of the device. For these reasons, two lines in the graph of Fig. 30 are respectively given in arbitrary units.

[0116] Regarding the emission current Ie, the device used in the display apparatus has three characteristics as follows:

[0117] First, when voltage of a predetermined level (referred to as "threshold voltage Vth") or greater is applied to the device, the emission current Ie drastically increases, however, with voltage lower than the threshold voltage Vth, almost no emission current Ie is detected.

[0118] That is, regarding the emission current Ie, the device has a nonlinear characteristic based on the clear threshold voltage Vth.

[0119] Second, the emission current Ie changes in dependence upon the device application voltage Vf. Accordingly, the emission current Ie can be controlled by changing the device voltage Vf.

[0120] Third, the emission current Ie is output quickly in response to application of the device voltage Vf to the device. Accordingly, an electrical charge amount of electrons to be emitted from the device can be controlled by changing period of application of the device voltage Vf.

[0121] The surface-conduction emission type electron-emitting device with the above three characteristics is preferably applied to the display apparatus. For example, in a display apparatus having a large number of devices provided corresponding to the number of pixels of a display screen, if the first characteristic is utilized, display by sequential scanning of display screen is possible. This means that the threshold voltage Vth or greater is appropriately applied to a driven device in accordance with a desired emission luminance, while voltage lower than the threshold voltage Vth is applied to an unselected device. In this manner, sequentially changing the driven devices enables display by sequential scanning of display screen.

[0122] Further, emission luminance can be controlled by utilizing the second or third characteristic, which enables multi-gradation display.

(Structure of Multi Electron-Beam Source With Many Devices Arranged in Simple Matrix)

[0123] Next, the structure of the multi electron-beam source having the above-described surface-conduction emission type electron-emitting devices arranged on the substrate with the simple-matrix wiring will be described below.

[0124] Fig. 31 is a plan view of the multi electron-beam source used in the display panel in Fig. 22. There are surface-conduction emission type electron-emitting devices like the one shown in Figs. 24A and 24B on a substrate. These devices are arranged in a simple matrix with the row-direction wiring 1003 and the column-direction wiring 1004. At an intersection of the wirings 1003 and 1004, an insulating layer (not shown) is formed between the wires, to maintain electrical insulation.

[0125] Fig. 32 shows a cross-section cut out along the line A - A' in Fig. 31.

[0126] Note that a multi electron-beam source having such a structure is manufactured by forming the row- and column-direction wirings 1003 and 1004, the inter-electrode insulating layers (not shown), and the device electrodes and conductive thin films of the surface-conduction emission type electron-emitting devices on the substrate, then supplying electricity to the respective devices via the row- and column-direction wirings 1003 and 1004, thus performing the forming processing and the activation processing.

〈Arrangement of Activation Apparatus〉

[0127] The structure and manufacturing method of the display panel have been described. Next, the aforementioned activation of the surface-conduction emission type electron-emitting device will be explained below with reference to the accompanying drawings.

[0128] In Fig. 1, a plurality of surface-conduction emission type electron-emitting devices are arranged in a matrix on a surface-conduction emission type electron-emitting device substrate 101 to be activated, and have already undergone forming processing. The substrate 101 is connected to an evacuation device (not shown) and evacuated to about 10^{-4} to 10^{-5} Torr. The substrate 101 is further connected to an external electric circuit via row-direction wiring terminals Dx1 to Dxm and column-direction wiring terminals Dy1 to Dyn. A line selection circuit 102 for selecting a line to be activated selects a row-direction wiring in accordance with an instruction from a timing generation circuit 105, and applies a selection potential of a power source 104 to the selected row-direction wiring. A current monitoring circuit 103 monitors a current flowing through the selected row upon applying the selection potential to the selected row-direction wiring. The current monitoring circuit 103 is made up of a detection resistance Rmon and a measurement amplifier for measuring a potential difference generated across the resistance. With these components, the current monitoring circuit 103 detects the current If and outputs it as an activation current value 109 to a control circuit 106. Note that the resistance value of the detection resistance Rmon is set small enough to prevent influence on an application voltage to the surface-conduction emission type electron-emitting device by a potential drop caused by the flowing device current If. The power source 104 generates a potential to be applied to the row-direction wiring of the electron source in accordance with a command value from the control circuit 106.

[0129] A buffer amplifier circuit 107 drives the column-direction wiring terminals Dy1 to Dyn of the surface-conduction emission type electron-emitting device substrate 101 at a timing synchronized with a control clock signal Hscan from the timing generation circuit 105. An input value to the buffer amplifier, i.e., a potential amplitude value for driving the terminals Dy1 to Dyn is determined by a potential distribution generation circuit 108.

[0130] In the first embodiment, the progress of activation is grasped by detecting a current amount flowing upon activation, i.e., the activation current 109 as output data from the current monitoring circuit 103. The control circuit 106 starts activation in response to an activation start command, and sequentially corrects the potential distribution of devices in the column direction that changes with the progress of activation, as will be described in detail later. That is, the control circuit 106 estimates a device current flowing through each device using an output from the current monitoring circuit 103, and sets the estimated value as a current setting value 110 in the potential distribution generation circuit 108. The potential distribution generation circuit 108 calculates a potential distribution generated in devices in the column direction in accordance with the current setting value 110 and generates this distribution as a potential. The calculated potential is applied to the column-direction electrode of each device via the buffer amplifier 107. In each device, a potential distribution generated by the device current and wiring resistance is corrected to suppress the difference in voltage applied to the device. The potential distribution is corrected until the end of activation by sequentially updating data of the potential distribution generation circuit 108 in accordance with the progress of activation.

⟨Line Selection Circuit⟩

[0131] The line selection circuit 102 will be described with reference to Fig. 2.

[0132] This circuit incorporates m switching elements (SWX1 to SWXm). Each switching element selects either one of the output potential of the power source 104 and 0 V (ground level), and the m switching elements are electrically connected to the terminals Dx1 to Dxm of the surface-conduction emission type electron-emitting device substrate 101, respectively. Each switching element operates based on a control signal Vscan output from the timing generation circuit 105. In practice, the switching elements can be easily constituted by a combination of switching elements such as FETs or relays. In Fig. 2, the first line (Sx1) is selected, the output potential of the power source 104 is applied to only the row-direction wiring Dx1, and the remaining lines are grounded.

⟨Potential Distribution Generation Circuit⟩

[0133] Fig. 3 is a circuit diagram showing the arrangement of the potential distribution generation circuit 108.

[0134] The circuit 108 operates to automatically calculate a compensation potential amount to be applied in the column direction and output it to the buffer amplifier 107 in order to compensate a potential drop caused by a device current flowing through each device and a row-direction wiring resistance (r1 to rN in Fig. 40) along with the progress of activation, as described above.

[0135] To achieve this operation, the potential distribution generation circuit 108 is made up of an equivalent wiring resistance array 301 and a constant current circuit 302.

[0136] The equivalent wiring resistance array 301 is a resistance array having a value equivalent to the wiring resistance on a given row wiring of the surface-conduction emission type electron-emitting device substrate 101 having a simple matrix arrangement (see Fig. 40). Resistances rd1 to rdN are set equal to the values r1 to rN of the wiring resistances of respective portions on the row wiring. Although a method of forming an electrode on the surface-conduction emission type electron-emitting device substrate 101 will be described below, the electrode is designed to be formed from a material having a constant line width and thickness, rd1 to rdN can be considered to be equal except for variations in the manufacture. The equivalent wiring resistance array 301 can therefore be constituted by aligning simulation resistances equal to an actual resistance value on an array. Alternatively, an extra wiring for one line may be formed at the end of the surface-conduction emission type electron-emitting device substrate 101 and extracted to constitute the equivalent wiring resistance array 301.

[0137] The constant current circuit 302 includes a total of n constant current circuits each made up of a transistor and resistance R in correspondence with the column-direction wiring terminals Dy1 to Dyn of the surface-conduction emission type electron-emitting device substrate 101. Each constant current circuit operates to sink a current amount:

$$(\text{Base Input Potential} - 0.6 + V)/R$$

Note that the transistors of the constant current circuit 302 share a base, which receives a current setting value 303 as an input potential. Accordingly, all the constant current circuits operate to have the same current setting value.

⟨Activation Processing⟩

[0138] Subsequently, a procedure of activating the surface-conduction emission type electron-emitting device substrate 101 using the apparatus of the first embodiment will be described with reference to Figs. 1, 4, 5A and 5B. Activation is performed to set the device currents of all devices to a target value. This target current value is determined in advance from a necessary electron-emitting amount or the like. In the first embodiment, activation processing is performed while monitoring an output from the current monitoring circuit 103 so as to set the device currents of respective devices on the surface-conduction emission type electron-emitting device substrate 101 to 2 mA at last.

[0139] An activation flow will be explained.

[0140] In Fig. 1, when the control circuit 106 receives an activation start command, it controls the timing generation circuit 105 and power source 104 in order to perform electrification processing in units of rows.

[0141] The control circuit 106 sets the current setting value 110 so as to set the column-direction wiring terminals Dy1 to Dyn to the ground potential, and sequentially applies pulses of the activation potential Eac to the row-direction wiring terminals Dx1 to Dxm. This pulse has, for example, a pulse width of 1 msec and a pulse height of 18 V. Then, the pulse potentials are sequentially applied to the surface-conduction emission type electron-emitting device substrate 101 in units of rows to start activation in units of lines.

[0142] The first embodiment will exemplify activation when n devices on the line of the row-direction wiring terminal Dx1 are activated.

[0143] Attention is paid to a surface-conduction emission type device group on the first row to which an activation voltage is applied, a surface-conduction emission type electron-emitting device group 401 is represented by a model including the wiring resistance, and the state in which this device group is activated will be explained with reference to Fig. 4. In Fig. 4, reference symbols F1 to Fn denote surface-conduction emission type electron-emitting devices on the line of the row-direction wiring terminal Dx1; r1 to rn, wring resistances at respective portions on a row wiring Ex1; and Ry, a wiring resistance from the feeding terminal of each of the wirings Dy1 to Dyn to a corresponding surface-conduction emission type electron-emitting device. Since the row wiring is designed to be formed from a material having a constant line width and thickness in the first embodiment, r1 to rN can be considered to be equal except for variations in the manufacture. Since the wirings are designed to be uniform, the resistances Ry of the respective wirings can be considered to be equal. Although the equivalent resistance value of the surface-conduction emission type electron-emitting device changes (decreases) before and after activation, the equivalent resistance of each device is much higher than the value Ry, and Ry is substantially negligible in the first embodiment. The equivalent resistance value of the surface-conduction emission type electron-emitting device is designed higher than r1 to rN.

[0144] To activate the surface-conduction emission type electron-emitting device group 401, the control circuit 106 controls the line selection circuit 102 via the timing generation circuit 105, and connects the power source 104 for outputting the activation potential Eac and the current monitoring circuit 103 to the row-direction wiring terminal Dx1. Thus, the terminal Dx1 receives the activation potential Eac.

[0145] On the other hand, the terminals Dy1 to Dyn as other electrode terminals of devices on the line Dx1 are driven by the buffer amplifier 107. The buffer amplifier 107 operates to sink activation currents i1 to in from the devices F1 to FN, and the output potential amplitude is determined by the potential distribution generation circuit 108.

[0146] The potential distribution circuit 108 is made up of the equivalent wiring resistance array 301 and constant current circuit 302, as described above. The resistance values rd1 to rdn of the equivalent wiring resistance array 301 are set equal to the wiring resistance values r1 to rn of the row wiring Dx1. N constant current sources CI1 to CIn constituting the constant current circuit 302 correspond to the devices F1 to FN of the surface-conduction emission type electron-emitting device group 401, and equivalently replace device currents flowing through the devices along with the progress of activation.

[0147] In activation, the electrical characteristics of the device change as shown in Fig. 41. That is, the device current does not substantially flow at the start of activation, starts flowing at the same time as electrification, and saturates. At this time, the terminal potential of the device group on the row wiring Dx1 is monitored to find changes in potentials Gy1 to Gyn due to the influence of the wiring resistances r1 to rn. The potential change increases with the progress of activation and maximizes at the end of activation. For example, for an activation current of 2 mA/device, r1 to rn = 10 mΩ, and n = 1000, a potential change:

$$\Delta V = 1/2 \times 1000 \times 1001 \times 2\ \mathrm{mA} \times 10\mathrm{m}\ \Omega \fallingdotseq 10\ \mathrm{V}$$

occurs at the terminal Gyn of the device Fn farthest from the feeding terminal.

[0148] To prevent this, a potential distribution identical to this potential distribution is generated by the potential distribution generation circuit 108, and the terminals Dy1 to Dyn are driven by outputs Sy1 to Syn from the buffer amplifier 107 so as to cancel the differences in voltages applied to the respective devices.

[0149] More specifically, the potential drop distribution at the terminals Gy1 to Gyn produced by currents flowing through the devices F1 to Fn along with the progress of activation is reproduced by outputs By1 to Byn from the potential distribution generation circuit 108. If activation of the devices F1 to Fn substantially uniformly progresses, the device currents i1 to in flowing through the respective devices are almost equal, and the current value can be given using a current amount I detected by the current monitoring circuit 103:

$$iave = i1 = i2 = \ldots = in = I/n \qquad (1)$$

[0150] By setting this iave as a current setting value in the potential distribution generation circuit 108, a distribution identical to the potential drop distribution at the terminals Gy1 to Gyn produced by currents flowing through the devices F1 to Fn is generated at the outputs By1 to Byn of the potential distribution generation circuit 108. By applying these potentials to the terminals Dy1 to Dyn via the outputs Sy1 to Syn of the buffer amplifier 107, voltages applied between the terminals of the devices F1 to Fn can be made uniform regardless of the device number and the progress of activation.

[0151] Figs. 5A and 5B show the distributions of potentials applied across the devices F1 to Fn at the start and end of activation. Fig. 5A shows a potential distribution immediately after the start of activation. The abscissa represents device numbers F1 to Fn, which indicate device positions. The ordinate represents terminal potentials at the two terminals of each device. As described above, currents flowing through respective devices are small immediately after the start of activation. Therefore, the activation potential Eac = 18 V is applied from the power source 104 to the terminals Gy1 to Gyn of the respective devices. Since almost no activation current flows, the current setting value of the potential distribution generation circuit 108 is almost 0, and the outputs By1 to Byn of the potential distribution generation circuit 108 and the outputs Sy1 to Syn of the buffer 107 are also at almost 0 V. For this reason, a predetermined application voltage up to 18 V is applied to the respective devices to progress activation.

[0152] Fig. 5B shows a potential distribution at the end of activation. At the end of activation, currents flowing through respective devices are almost 2 mA. The activation potential Eac = 18 V applied from the power source 104 decreases owing to the influence of a potential drop caused by the wiring resistance upon application to the terminals Gy1 to Gyn of the respective devices. At this time, if the current setting value of the potential distribution generation circuit 108 is set to 2 mA, the outputs By1 to Byn of the potential distribution generation circuit 108 and the outputs Sy1 to Syn of the buffer 107 have the same distribution as Gy1 to Gyn. As a result, a predetermined application voltage up to 18 V is applied to the respective devices to activate them.

[0153] More specifically, when the device current increases with the progress of activation, the distribution of potentials applied to devices always changes due to the influence of the wiring resistance. In this case, the control circuit 106 obtains a device current value in accordance with equation (1) from a current value detected by the current monitoring circuit 103 along with the progress of activation, and sets a current value corresponding to the obtained value as the current setting value of the potential distribution generation circuit 108. In this way, the outputs By1 to Byn of the potential distribution generation circuit 108 are sequentially updated to activate all devices by a constant voltage from the start to end of activation. When the device current of each device reaches 2 mA, activation ends.

[0154] The outputs By1 to Byn of the potential distribution generation circuit 108 described in the first embodiment have a very high response speed in updating the current setting value, so that the distribution can be updated every time a pulse voltage is applied from the power source 104.

[0155] Fig. 15 shows an example of a control procedure by the control circuit 106 when activation is performed by a procedure of completing activation in units of lines and switching lines. Fig. 15 shows a procedure for one line. Since the substrate 101 generally has a plurality of lines, this control procedure is repeatedly executed for a plurality of lines.

[0156] In Fig. 15, the control circuit 106 calculates the average device current iave from an input value from the current monitoring circuit (step S3401). Since the device current is very small before activation, as shown in Fig. 5A, the first pulse can be set to iave ≒ 0 or to an initial value obtained experimentally. The control circuit 106 updates the current setting value 110 in accordance with the obtained device current value (step S3402). In this state, the control circuit 106 applies the activation potential to a selected line (step S3403). Upon completion of a predetermined activation procedure for the selected line, activation for this line ends (YES in step S3404). If a next line exists, the control circuit 106 outputs a line switching signal to select the next line. If activation for the selected line has not been completed yet, the control circuit 106 returns to step S3401 to read an activation current value with respect to the activation potential applied in step S3403 from the current monitoring circuit 103, update the current setting value, and apply a next pulse to the selected line. This is repeatedly executed until activation ends.

[0157] The above description is directed to activation of devices on the row wiring Dx1. This procedure can similarly apply to activation of devices on another line. In this way, activation of all surface-conduction emission type electron-emitting devices on the substrate 101 is completed.

[0158] In activation, after activation of devices on a given line is completed, the line selection circuit 102 is switched to activate another activation line. Instead, a plurality of lines may be simultaneously activated while sequentially switching activation lines. In this case, the progress of activation may vary between lines. To prevent this, the average device currents of respective lines are sequentially stored in a memory or the like, and activation is performed while updating the output of the potential distribution generation circuit 108 at a high speed using the average device current stored in the memory in switching lines. Consequently, uniform activation can be realized. In Fig. 15, activation is completed in units of lines. When a plurality of lines are activated parallel while sequentially switching lines, a line switching signal must be output between steps S3403 and S3404.

[0159] To quickly complete activation of the surface-conduction emission type electron-emitting device substrate 101, a plurality of lines may be simultaneously driven. In this case, the current monitoring circuit 103 detects the sum of device currents for the plurality of lines. Consideration must be taken in estimating the current setting value set in the potential distribution generation circuit 108.

[0160] In the first embodiment, the power source 104 has a positive output, and activation is performed to flow a current from the terminal Dx1 to the terminals Dy1 to Dyn. Alternatively, the polarity may be inverted, and activation may be performed to flow a current from the terminals Dy1 to Dyn to the terminal Dx1. In this case, since the potential distribution is also inverted, the buffer amplifier 107 is constituted as a (-1)-time inverting buffer amplifier to source the current, thereby obtaining the same effects.

[0161] As described above, the activation apparatus of the first embodiment can make the electron-emitting characteristics of all devices uniform. This electron source substrate is used to realize a high-quality image display apparatus almost free from variations in luminance or density.

[Second Embodiment]

[0162] An activation apparatus for the surface-conduction emission type electron-emitting device according to the second embodiment of the present invention will be described with reference to Fig. 6.

[0163] In Fig. 6, a surface-conduction emission type electron-emitting device substrate 601 is different from the substrate 101 in Fig. 1 in that row-direction wiring terminals Dx1 to Dxm are arranged on two sides. The terminals Dx1 to Dxm extracted from the two sides as shown in Fig. 6 are connected to corresponding terminals on the same lines, and connected to a line selection circuit 602.

[0164] The operation of the whole apparatus, the activation procedure, and the like are the same as in the first embodiment, and a description thereof will be omitted. Since the wiring terminal extraction method is different, a potential distribution applied to the device upon activation changes, and thus the driving method is slightly different from that in the first embodiment and will be described.

[0165] Fig. 43A shows an equivalent circuit when the surface-conduction emission type electron-emitting device substrate 601 according to the second embodiment is activated. Fig. 43B shows a device application potential distribution when devices on the second line are activated in Fig. 43A. In two-side extraction, the distribution has a mirror-symmetrical profile.

[0166] Hence, a potential distribution amount to be applied to column-direction wiring terminals Dy1 to Dyn in Fig. 6 also has a mirror-symmetrical profile. This potential distribution can be reproduced by constituting a potential distribution circuit 608 by 1 to (n/2) resistance arrays and constant current sources. If the output impedance of a buffer 607 is set sufficiently low, the circuit can be simplified by preparing (n/2) buffer amplifiers 607, and commonly connecting and driving terminals (e.g.; Dy1 and Dyn, Dy2 and Dyn-1, and the like) having a symmetrical potential distribution. For example, in Fig. 4, the output Sy1 of the first column extending from the buffer amplifier is connected to the terminals Dy1 and Dyn, the output Sy2 of the second column is connected to the terminals Dy2 and Dyn-1,..., and the output Syj of the jth column is connected to the terminals Dyj and Dyn-j+1 . If n is an odd number, the output of the (n+1)/2 column is connected to only the terminal Dy(n+1)/2 .

[0167] Fig. 7 shows the potential distribution of respective devices upon driving in the second embodiment. As described above, a mirror-symmetrical potential distribution profile can be obtained. The driving potentials Sy1 to Syn of the column-direction wiring terminals Dy1 to Dyn also change with the progress of activation and are compensated to always apply a predetermined activation voltage to respective devices.

[0168] As described above, the apparatus of the second embodiment allows manufacturing an electron source in which all devices have uniform electron-emitting characteristics.

[Third Embodiment]

[0169] An activation apparatus for the surface-conduction emission type electron-emitting device according to the third embodiment of the present invention will be described with reference to Fig. 8.

[0170] In Fig. 8, a surface-conduction emission type electron-emitting device substrate 801 is the same as the substrate 101 in Fig. 1. The operation of the whole apparatus, the activation procedure, and the like are the same as in the first embodiment, and a description thereof will be omitted.

[0171] The third embodiment is slightly different from the first embodiment in driving method in which an output from a potential distribution circuit 808 is not directly applied to column-direction wiring terminals Dy1 to Dyn, as will be described.

[0172] Similar to the first embodiment, attention is paid to a surface-conduction emission type device group on the first row to which an activation voltage is applied, a surface-conduction emission type electron-emitting device group 901 is represented by a model including the wiring resistance, and the state in which this device group is activated will be explained with reference to Fig. 9. In Fig. 9, reference symbols F1 to Fn denote surface-conduction emission type electron-emitting devices on the line of a row-direction wiring terminal Dx1; r1 to rn, wring resistances at respective portions on a row wiring Ex1; and Ry, a wiring resistance from the feeding terminal of each of the wirings Dy1 to Dyn to a corresponding surface-conduction emission type electron-emitting device.

[0173] To activate the surface-conduction emission type electron-emitting device group 901, a control circuit 806 controls a line selection circuit 802 via a timing generation circuit 805, and connects a power source 804 for outputting the activation potential Eac and a current monitoring circuit 803 to the row-direction wiring terminal Dx1. Thus, the terminal Dx1 is driven by the activation potential Eac.

[0174] On the other hand, the terminals Dy1 to Dyn as other column-direction terminals of devices on the line Dx1 are driven by a buffer amplifier 807. In this case, the buffer amplifier 807 operates to sink activation currents i1 to in from the devices F1 to FN, and the output potential amplitude is determined by the potential distribution generation circuit 808. This operation is the same as in the first embodiment.

[0175] Also in the third embodiment, a potential distribution produced along with the progress of activation is generated by the potential distribution generation circuit 808, and the terminals Dy1 to Dyn are driven by outputs Sy1 to Syn from the buffer amplifier 807 so as to cancel the potential distribution. At this time, output potential values By1 to Byn from the potential distribution circuit 808 are not directly applied to the terminals, but are added to an offset setting value 812 by the buffer amplifier 807 and then applied to the terminals,. This offset setting value 812 is also added to an activation potential and applied as the amplitude of the power source 804.

[0176] The offset potential is added owing to the following reason. According to the present invention, when activation is performed in units of rows, a potential drop distribution generated in the column direction on the same row is compensated by application potentials from the column-direction wiring terminals Dy1 to Dyn. The application potentials from the column-direction wiring terminals Dy1 to Dyn are applied to not only devices on an activated line but also devices on an inactivated line because surface-conduction emission type electron-emitting devices are arranged in a simple matrix. As a matter of course, the potentials of the column-direction wiring terminals Dy1 to Dyn are as low as several V in maximum, so no problem arises even if these potentials are applied to devices on an inactivated line. It is however desirable to reduce changes in substrate temperature or a temperature distribution caused by application of potentials to devices on an inactivated line. Therefore, the offset potential is added to minimize the absolute values of potentials applied from the column-direction wiring terminals Dy1 to Dyn, thereby driving the terminals Dy1 to Dyn.

[0177] The offset potential value to be added is determined as follows. The difference between maximum and minimum potentials generated at respective terminals at the output of the potential distribution circuit 808 is calculated as a potential drop amount 811. More specifically, in Fig. 9, the potential drop amount at the outputs By1 to Byn of the potential distribution circuit 808 is calculated by

$$\text{Potential Drop Amount 811} = \text{Potential By1} - \text{Potential Byn}$$

Thus, the offset setting value 812 is determined by

$$\text{Offset Potential 812} = 1/2 \times \text{Potential Drop Amount 811}$$

and added. As a result, the absolute values of potentials applied from the column-direction wiring terminals Dy1 to Dyn can be halved compared to the first embodiment.

[0178] Figs. 10A and 10B show the potential distributions of respective devices upon driving in the third embodiment. Fig. 10A shows a potential difference immediately after activation. At this time, since almost no device current flows, as described in the first embodiment, almost no potential distribution is generated, the offset potential value 821 is almost 0 V, and the potential distribution is almost the same as in Fig. 5A of the first embodiment. However, when activation progresses to generate a potential drop, the offset potential 821 is generated to obtain a potential distribution profile like the one shown in Fig. 10B. As shown in Fig. 10B, the potential distribution of respective devices is the same as in Fig. 5B of the first embodiment except that the offset potential is applied to the driving potentials Sy1 to Syn to be applied to the column-direction wiring terminals Dy1 to Dyn to decrease the absolute values of the driving potentials. Fig. 10B also shows the state in which the potential applied from the row-direction wiring terminal Dx1 also changes to 18 V + Voff along with this.

[0179] By applying the potential added with the offset potential used in the third embodiment, surface-conduction emission type electron-emitting devices having uniform characteristics can be attained similar to the first embodiment. In addition, the power applied in activating the surface-conduction emission type electron-emitting device substrate can be reduced. Note that the offset potential determination method is not limited to the above one, and the offset potential may be determined to minimize the power value applied to the entire surface-conduction emission type electron-emitting device substrate.

[Fourth Embodiment]

[0180] An activation apparatus for the surface-conduction emission type electron-emitting device according to the fourth embodiment of the present invention will be described with reference to Fig. 11.

[0181] Also in Fig. 11, a surface-conduction emission type electron-emitting device substrate 1101 is the same as the substrate 101 in Fig. 1. The operation of the whole apparatus, the activation procedure, and the like are the same as in the first embodiment, and a description thereof will be omitted.

[0182] The fourth embodiment is slightly different from the first embodiment in arrangements of a current monitoring circuit 1103 and a potential distribution circuit 1108, as will be described. That is, the current monitoring circuit 1103 is interposed between column-direction wiring terminals Dy1 to Dyn and a buffer amplifier 1107 to individually monitor device currents flowing through respective devices upon activation.

[0183] Similar to the first embodiment, attention is paid to a surface-conduction emission type device group on the first row to which an activation voltage is applied, a surface-conduction emission type electron-emitting device group 1201 is represented by a model including the wiring resistance, and the state in which this device group is activated will be explained with reference to Fig. 12.

[0184] Also in the fourth embodiment, a potential distribution produced along with the progress of activation is generated by the potential distribution generation circuit 1108, and the terminals Dy1 to Dyn are driven by outputs Sy1 to Syn from the buffer amplifier 1107 so as to cancel the potential distribution. In this case, the arrangement of a constant current circuit 302 constituting the potential distribution circuit 1108 is slightly different from that in the above embodiments. In other words, the constant current circuit 302 is changed to individually set the current setting values of n constant current sources constituting the constant current circuit 302. The circuit arrangement is changed from the circuit of Fig. 3 so as to individually set the base potentials of transistors constituting the constant current sources. With this change, current setting values 1110 corresponding to the n constant current sources can be externally supplied to individually drive the constant current sources in the potential distribution circuit 1108 shown in Fig. 12.

[0185] At the same time, the current monitoring circuit 1103 is changed to individually monitor device currents flowing through respective devices. The current monitoring circuit 1103 is made up of detection resistances Rmon and a measurement amplifier for measuring a voltage generated across each detection resistance Rmon. With these components, the current monitoring circuit 103 detects the currents If and outputs n detected activation current values 1109. Note that the resistance value of the detection resistance Rmon is set small enough to prevent influence on an application potential to the surface-conduction emission type electron-emitting device by a potential drop caused by the flowing device current If.

[0186] Since the arrangement of the constant current circuit 302 constituting the potential distribution circuit 1108 is changed to individually set current setting values for respective rows, the potential drop distribution at terminals Gy1 to Gyn along with the progress of activation can be more accurately reproduced by outputs By1 to Byn from the potential distribution circuit 1108. The above-described embodiments estimate current values flowing through respective devices from an activation current for one line, and control an output from the potential distribution generation circuit 108 on the assumption that activation of the devices F1 to Fn uniformly progresses and the device currents i1 to in flowing through respective devices are almost equal. In the fourth embodiment, however, a more accurate potential distribution can be reproduced by individually monitoring the activation currents of respective devices. The activation current values of respective devices are supplied as current setting values to constant current sources CI1 to CIn on each row in the potential distribution circuit 1108, and potentials in accordance with a potential distribution in an activated line are applied to the terminals Dy1 to Dyn via the outputs Sy1 to Syn of the buffer amplifier 1107. That is, the first embodiment employs the average value iave as a device current, whereas the fourth embodiment employs a device current measured for each device. Consequently, voltages applied between the terminals of the devices F1 to Fn can be made uniform regardless of the device position and the progress of activation.

[0187] Note that when an output from the buffer amplifier 1107 is not 0 V, a current value detected by the current monitoring circuit 1103 does not always coincide with a device current flowing through each device. This will be explained. Although not shown in Fig. 12, application potentials from the column-direction wiring terminals Dy1 to Dyn are applied to not only devices on an activated line but also devices on an inactivated line-because surface-conduction emission type electron-emitting devices are arranged in a simple matrix. Therefore, a current Ix of the xth row detected by the current monitoring circuit 1103 is

Ix = Device Current Flowing Through Device Fx Upon
Application of 18 V + Current Flowing Through
Inactivated Device (m-1) Connected to Terminal
Dyx Upon Application of Potential Syx

The first term is a true device current, and the current amount of the second term is an error. In practice, the difference between the potential Sy and the potential of an unselected line is small, and the current amount of the second term is small to a negligible degree. To more accurately measure the current, the following steps are executed.

(1) All the row-direction wiring terminals Dx1 to Dxm are set to 0 V, and the column-direction wiring terminals Dy1 to Dyn are driven by Sy1 to Syn. A current Ia measured at this time is the sum of (m) currents flowing through all devices connected to Dyx upon application of the potential Syx.
(2) One of the row-direction wiring terminals is selected, and the column-direction wiring terminals Dy1 to Dyn are driven by Sy1 to Syn. A current Ib measured at this time is a "device current flowing through the device Fx upon application of 18 V + a current flowing through the (m-1) inactivated devices connected to Dyx upon application of potential Syx".

[0188] By these two measurements,

Device Current Flowing Through Device Fx Upon Application of 18 V = Ib - Ia

is calculated. If a potential distribution is calculated using this value, more accurate control can be achieved.

[Fifth Embodiment]

[0189] An activation apparatus for the surface-conduction emission type electron-emitting device according to the fifth embodiment of the present invention will be described with reference to Fig. 13.
[0190] Also in Fig. 13, a surface-conduction emission type electron-emitting device substrate 1301 is the same as the substrate 101 in Fig. 1. The operation of the whole apparatus, the activation procedure, and the like are the same as in the first embodiment, and a description thereof will be omitted. The arrangement of a current monitoring circuit 1303 is the same as in the fourth embodiment. The current monitoring circuit 1303 is interposed between column-direction wiring terminals Dy1 to Dyn and a buffer amplifier 1307 to individually monitor device currents flowing through respective devices upon activation. However, the fifth embodiment is slightly different from the fourth embodiment in arrangement of a potential distribution circuit 1308. That is, a control circuit 1306 calculates a potential distribution amount from activation current values flowing through devices, and transfers a digital output value corresponding to the potential distribution obtained from the calculation result to the potential distribution generation circuit.
[0191] Similar to the first embodiment, attention is paid to a surface-conduction emission type device group on the first row to which an activation voltage is applied, a surface-conduction emission type electron-emitting device group 1401 is represented by a model including the wiring resistance, and the state in which this device group is activated will be explained with reference to Fig. 14.
[0192] Also in the fifth embodiment, the terminals Dy1 to Dyn are driven by outputs Sy1 to Syn from the buffer amplifier 1307 so as to cancel a potential distribution produced along with the progress of activation. The potential distribution circuit 1308 is constituted by n D/A converters 1402 and n latch circuits 1403. With this arrangement, digital output setting values 1310 corresponding to the n D/A converters are externally supplied to individually drive the D/A converters. The digital output setting value 1310 is set as a potential drop distribution amount calculated by the control circuit 1306. Independent potentials are set in the respective D/A converters, and all the outputs are simultaneously updated by a latch CLK 1311.
[0193] Similar to the fourth embodiment, the current monitoring circuit 1303 can individually monitor device currents flowing through respective devices. The current monitoring circuit 1303 is made up of detection resistances Rmon and a measurement amplifier for measuring a voltage generated across each detection resistance Rmon. With these components, the current monitoring circuit 103 detects the currents If and outputs n detected activation current values 1309.
[0194] In the fifth embodiment, a device potential distribution generated along with the progress of activation is calculated as follows. When device current values i1 to in flowing through devices F1 to Fn are obtained from the current monitoring circuit 1303, potentials By1 to Byn to be output to the output terminals of the potential distribution circuit 1308 are calculated using the wiring resistance values r1 to rn:

$$By1 = -r1 \times \Sigma\{k = 1 \text{ to } n\}ik$$

$$By2 = -r2 \times \Sigma\{k = 2 \text{ to } n\}ik + By1 \ ...$$

$$Byn = -rn \times in + Byn - 1 + Byn - 2 +...+ By1$$

[0195] Device currents flowing along with the progress of activation are measured. The control circuit 1306 sequentially updates the output potentials By1 to Byn by the above equations, and transfers corresponding digital output data to the latch circuits 1403 of the potential distribution circuit 1308. Upon completion of a series of operations: measurement of the device current → calculation of output data → transfer of data to the latch circuit, the control circuit 1306 applies the latch clock 1311 to all the latch circuits 1403 in order to update D/A data, and updates the data in synchronism with this. Then, the potential distribution circuit 1308 generates a potential distribution corresponding to a potential distribution amount generated at the terminals Gy1 to Gyn of the devices F1 to Fn. Note that when the number n of devices is large, a long time may be spent for a series of operations: measurement of the device current → calculation of output data data → transfer. This time can be shortened by parallel processing for respective devices.

[0196] By compensating an activation potential distribution generated in devices upon activation by the above-described method, the electron-emitting characteristics of all devices can be made uniform. Further, in the fifth embodiment, the output setting value is a digital value, and no constant current circuit or equivalent wiring resistance array is used. This can prevent a nonuniform activation voltage generated by the difference between the lines, such as the difference between a wiring resistance distribution on a line to be activated and a resistance value distribution in the equivalent wiring resistance array.

[Sixth Embodiment]

[0197] Activation for the surface-conduction emission type electron-emitting device according to the sixth embodiment of the present invention will be described with reference to Fig. 16.

[0198] Also in Fig. 16, a surface-conduction emission type electron-emitting device substrate 101 is the same as the substrate 101 in Fig. 1. The operation of the whole apparatus, the activation procedure, and the like are the same as in the first embodiment, and a description thereof will be omitted. The arrangement of a potential distribution circuit 1608 is the same as in the fifth embodiment, and a control circuit transfers a digital output value corresponding to a potential distribution to the potential distribution generation circuit. For this purpose, a control circuit 1606 outputs a latch clock 111 to the potential distribution generation circuit 1608. The remaining arrangement is the same as in the first embodiment.

[0199] In the sixth embodiment, the control circuit 1606 detects the progress of activation by a current amount flowing upon activation, i.e., an activation current 109 as output data from a current monitoring circuit 103. The control circuit 1606 starts activation in response to an activation start command, and sequentially corrects the potential distribution of devices in the column direction that changes with the progress of activation, as will be described in detail later. That is, the control circuit 1606 estimates a device current flowing through each device using an output from the current monitoring circuit 103, and calculates a potential distribution generated in devices in the column direction from the estimated value. By this driving method, a voltage distribution generated in respective devices by the activation current and row-direction wiring resistance is corrected to apply a constant voltage across all devices on an activated lines. By sequentially updating data of the potential distribution circuit 1608 in accordance with the progress of activation, the potential distribution is corrected until the end of activation.

⟨Potential Distribution Generation Circuit⟩

[0200] Fig. 17 is a circuit diagram showing the arrangement of the potential distribution generation circuit 1608 to explain the state in which a given line is activated using the potential distribution circuit 1608.

[0201] The potential distribution generation circuit 1608 generates a compensation potential amount to be applied in the column direction and outputs it to the buffer amplifier 107 in order to compensate a potential drop caused by a device current flowing through each device and a row-direction wiring resistance (r1 to rN in Fig. 40) along with the progress of activation.

[0202] In the sixth embodiment, terminals Dy1 to Dyn of the surface-conduction emission type electron-emitting device substrate 101 are driven by outputs (Sy1 to Syn) from the buffer amplifier 107 so as to cancel a potential distribution generated along with the progress of activation.

[0203] The potential distribution generation circuit 1608 is constituted by n D/A converters 302 and n latch circuits 303. Digital output setting values 110 corresponding to the n D/A converters are externally set. More specifically, the control circuit 1606 calculates a potential drop distribution amount and sets it as the digital output setting value 110. Independent potentials are set in the respective D/A converters, and all the outputs are simultaneously updated by a latch CLK 111.

〈Activation Processing〉

[0204] Subsequently, a procedure of activating the surface-conduction emission type electron-emitting device substrate 101 using the apparatus of the sixth embodiment will be described with reference to Figs. 16, 17, 5A and 5B. Activation is performed to set all device currents to a target value. This target current value is determined in advance from a necessary electron-emitting amount or the like. In the sixth embodiment, activation processing is performed while monitoring an output from the current monitoring circuit 103 so as to set the device currents of respective devices on the surface-conduction emission type electron-emitting device substrate 101 to 2 mA at last.

[0205] An activation flow will be explained.

[0206] When the control circuit 1606 receives an activation start command, it controls a timing generation circuit 105 and a power source 104 in order to perform electrification processing in units of rows.

[0207] The control circuit 1606 sets the current setting value 110 so as to set the column-direction wiring terminals Dy1 to Dyn to the ground potential, and sequentially applies pulses of the activation potential Eac to row-direction wiring terminals Dx1 to Dxm. This pulse has, e.g., a pulse width of 1 msec and a pulse height of about 18 V. Then, the pulse potentials are sequentially applied to the surface-conduction emission type electron-emitting device substrate 101 in units of rows to start activation in units of lines.

[0208] The sixth embodiment will exemplify activation when n devices on the line of the row-direction wiring terminal Dx1 are activated.

[0209] Attention is paid to a surface-conduction emission type device group on the first row to which an activation voltage is applied, a surface-conduction emission type electron-emitting device group 301 is represented by a model including the wiring resistance, and the state in which this device group is activated will be explained with reference to Fig. 17. In Fig. 17, reference symbols F1 to Fn denote surface-conduction emission type electron-emitting devices on the line of the row-direction wiring terminal Dx1; r1 to rn, wring resistances at respective portions on a row wiring EX1; and Ry, a wiring resistance from the feeding terminal of each of the wirings Dy1 to Dyn to a corresponding surface-conduction emission type electron-emitting device. Since the row wiring is designed to be formed from a material having a constant line width and thickness in the sixth embodiment, r1 to rN can be considered to be equal except for variations in the manufacture. Since the wirings are designed to be uniform, the resistances Ry of the respective wirings can be considered to be equal. Although the equivalent resistance value of the surface-conduction emission type electron-emitting device changes (decreases) before and after activation, the equivalent resistance of each device is much higher than the value Ry, and the influence of Ry is substantially negligible. The equivalent resistance value of the surface-conduction emission type electron-emitting device is designed higher than r1 to rN.

[0210] To activate the surface-conduction emission type electron-emitting device group 301, the control circuit 1606 controls a line selection circuit 102 via the timing generation circuit 105, and applies the activation potential Eac to the row-direction wiring terminal Dx1 via the power source 104 and current monitoring circuit 103. Thus, the terminal Dx1 is driven by the activation potential Eac.

[0211] On the other hand, the terminals Dy1 to Dyn as other electrode terminals of devices on the line Dx1 are driven by the buffer amplifier 107. The buffer amplifier 107 operates to sink activation currents i1 to in from the devices F1 to FN or use them as a current source, and the output potential amplitude is determined by the potential distribution generation circuit 1608.

[0212] In activation, the electrical characteristics of the device change as shown in Fig. 41. That is, the device current does not substantially flow at the start of activation, starts flowing at the same time as electrification, and saturates. At this time, the terminal potential of the device group on the row wiring Dx1 is monitored to find changes in potentials Gy1 to Gyn due to the influence of the wiring resistances r1 to rn. The potential change increases with the progress of activation and maximizes at the end of activation. For example, for an activation current of 2 mA/device, r1 to rn = 5 mΩ, and n = 1000, a potential change:

$$\Delta V = 1/2 \times 1000 \times 1001 \times 2\ \mathrm{mA} \times 5\ \mathrm{m\Omega} \fallingdotseq 5\ \mathrm{V}$$

occurs at the terminal Gyn of the device Fn farthest from the feeding terminal.

[0213] To prevent this, a potential distribution identical to this potential distribution is generated by the potential distribution generation circuit 1608, and the terminals Dy1 to Dyn are driven by outputs Sy1 to Syn from the buffer amplifier 107 so as to cancel the potential distribution produced in respective devices.

[0214] More specifically, the potential drop distribution at the terminals Gy1 to Gyn produced by currents flowing through the devices F1 to Fn along with the progress of activation is reproduced by outputs By1 to Byn from the potential distribution generation circuit 1608. If activation of the devices F1 to Fn substantially uniformly progresses, the device currents i1 to in flowing through the respective devices are almost equal, and the current value can be given using an activation current I (109) detected by the current monitoring circuit 103:

$$iave = i1 = i2 = ... = in = I/n$$

(n is the number of column-direction devices)

[0215] The control circuit 1606 calculates a potential drop amount at each device terminal using iave as a current value flowing through each device, and sets the calculated amount in the potential distribution generation circuit 1608. Accordingly, a potential drop distribution identical to the distribution at the device terminals Gy1 to Gyn of the devices F1 to Fn is realized at the outputs By1 to Byn of the potential distribution generation circuit 1608. By applying these potentials to the terminals Dy1 to Dyn via the outputs Sy1 to Syn of the buffer amplifier 107, voltages applied between the terminals of the devices F1 to Fn can be made uniform regardless of the device number and the progress of activation.

[0216] In the sixth embodiment, the potential distribution at device terminals produced along with the progress of activation is calculated as follows.

[0217] Assuming that activation substantially simultaneously progresses for respective devices, the device currents i1 to in flowing through the devices F1 to Fn are estimated from the activation current I (109) detected by the current monitoring circuit 103:

$$iave = i1 = i2 = ... = in = I/n \tag{1}$$

[0218] At this time, the potentials By1 to Byn to be output to the output terminals of the potential distribution generation circuit 1608 are calculated using the wiring resistance values r1 to rn $\fallingdotseq$ r:

$$By1 = -r1 \times \Sigma\{k = 1 \text{ to } n\}ik \fallingdotseq -r \times n \times iave \fallingdotseq -r \times I \tag{2}$$

$$By2 = -r2 \times \Sigma\{k = 2 \text{ to } n\}ik + By1 \fallingdotseq -r \times (n - 1)/n \times I + (-r \times I) ...$$

$$Byn = -rn \times in + Byn\text{-}1 + Byn\text{-}2 + ... + By1 \fallingdotseq -r \times 1/n \times I + ... -r \times (n\text{-}1)/n \times I + (-r \times I) \fallingdotseq -1/2 \times r \times (n + 1) \times I$$

[0219] Along with the progress of activation, the control circuit 1606 measures the activation current, and sequentially calculates the output potentials By1 to Byn from equation (2). The control circuit 1306 transfers digital output data corresponding to the output potentials By1 to Byn to the latch circuits 303 of the potential distribution circuit 1608. Upon completion of a series of operations: measurement of the device current →calculation of output data → transfer of data to the latch circuit, the control circuit 1606 applies the latch clock 110 to all the latch circuits 303 in order to update D/A data, and updates the data in synchronism with this. Then, the potential distribution generation circuit 1608 generates a potential distribution corresponding to a potential distribution amount generated at the terminals Gy1 to Gyn of the devices F1 to Fn.

[0220] Similar to the first embodiment, Figs. 5A and 5B show the distributions of potentials applied across the devices F1 to Fn at the start and end of activation in the sixth embodiment. Fig. 5A shows a potential distribution immediately after the start of activation. The abscissa represents device numbers F1 to Fn, which indicate device positions. The ordinate represents terminal potentials at the two terminals of each device. As described above, currents flowing through respective devices bare small immediately after the start of activation. Therefore, the activation potential Eac = 18 V is applied from the power source 104 to the terminals Gy1 to Gyn of the devices. Since almost no activation current flows, the current setting value of the potential distribution generation circuit 1608 is almost 0, and the outputs By1 to Byn of the potential distribution generation circuit 1608 and the outputs Sy1 to Syn of the buffer 107 are also at almost 0 V. For this reason, a predetermined application voltage up to 18 V is applied to the respective devices to progress activation.

[0221] Fig. 5B shows a potential distribution at the end of activation. At the end of activation, currents flowing through respective devices are almost 2 mA. The activation potential Eac (application width: 18 V) applied from the power source 104 decreases owing to the influence of a potential drop caused by the wiring resistance upon application to the terminals Gy1 to Gyn of the respective devices. At this time, if the current setting value of the potential distribution generation circuit 1608 is set to 2 mA, the outputs By1 to Byn of the potential distribution generation circuit 1608 and the outputs Sy1 to Syn of the buffer 107 have the same distribution as Gy1 to Gyn. As a result, a predetermined application voltage up to 18 V is applied to the respective devices to activate them.

[0222] More specifically, when the device current increases with the progress of activation, the potential distribution generated at the device terminal always changes due to the influence of the wiring resistance. In this case, the control circuit 1606 calculates the outputs By1 to Byn of the potential distribution generation circuit 1608 in accordance with equation (2) from the activation current values I sequentially detected by the current monitoring circuit 103 along with the progress of activation. The control circuit 1606 sequentially updates and sets values corresponding to the calculated values By1 to Byn for DD1 to DDn of the latch circuits 303 included in the potential distribution generation circuit 1608.

In this fashion, all devices are activated by a constant voltage from the start to end of activation. When the device current of each device reaches 2 mA, activation ends.

[0223] Fig. 21 shows an example of a control procedure by the control circuit 1606 when activation is performed by a procedure of completing activation in units of lines and switching lines. Fig. 21 shows a procedure for one line. Since the substrate 101 generally has a plurality of lines, this control procedure is repeatedly executed for a plurality of lines. In Fig. 21, the control circuit 1606 calculates digital values corresponding to the potentials By1 to Byn from an input value from the current monitoring circuit 103 (step S2701). The control circuit 1606 sets the calculated values in the latch circuits DD1 to DDn (step S2702). In this state, the control circuit 1606 outputs a latch clock to the potential distribution generation circuit (step S2703). This is repeatedly executed until the above-described activation end conditions are satisfied. If the conditions are satisfied, activation for this line ends (YES in step S2704). If a next line exists, the control circuit 1606 outputs a line switching signal to select the next line. If activation for the selected line has not been completed yet, the control circuit 1606 returns to step S2701 to read an activation current value with respect to the activation potential applied in step S2703 from the current monitoring circuit 103, and repeatedly executes the processing from step S2701. The clock output in step S2703 may be a signal having a predetermined frequency which is generated based on a clock for controlling the operation of the control circuit 1606 itself.

[0224] By this method, an activation voltage distribution generated upon activation can be corrected to make the electron-emitting characteristics of all devices uniform.

[0225] The above description is directed to activation of devices on the row wiring Dx1. This procedure can similarly apply to activation of devices on another line. In this way, activation of all surface-conduction emission type electron-emitting devices on the substrate 101 is completed.

[0226] When a plurality of lines are activated, after activation of devices on a given line is completed, the line selection circuit 102 is switched to activate another activation line (activation is performed in units of lines). Alternatively, a plurality of lines may be simultaneously activated while sequentially switching activation lines. In this case, the progress of activation may vary between lines. To prevent this, the average device currents of respective lines are sequentially stored in a memory or the like, and activation is performed while updating the output of the potential distribution generation circuit 1608 at a high speed using the average device current stored in the memory in switching lines. At this time, when the row-direction wiring resistances r1 to rn become slightly different between lines, these values are also stored in a memory or the like, and when the potential distributions is updated, appropriately read out together with the average device current value of each line and used for calculation.

[0227] When the number n of devices is large, a long time may be spent for a series of operations: measurement of the activation current → calculation of output data →data transfer. This time can be shortened by parallel processing for respective devices. In the sixth embodiment, the potential distribution generation circuit 1608 is constituted by D/A converters equal in number to the number n of column-direction wirings of the surface-conduction emission type electron-emitting device substrate 101. Since the compensation potential distribution profile changes gradually, as shown in Figs. 5A and 5B, the D/A converters may be thinned out, and potential values to be applied to the thinned column-direction wiring terminals may be defined by resistance division. This realizes a small number of D/A converters, a short calculation time, and low cost.

[0228] In the sixth embodiment, the power source 104 has a positive output, and activation is performed to flow a current from the terminal Dx1 to the terminals Dy1 to Dyn. Alternatively, the polarity may be inverted, and activation may be performed to flow a current from the terminals Dy1 to Dyn to the terminal Dx1. In this case, since the potential distribution is also inverted, the buffer amplifier 107 is constituted as a (-1)-time inverting buffer amplifier to source the current, thereby obtaining the same effects.

[0229] In the sixth embodiment, the influence of the column-direction wiring resistance Ry in Fig. 17 is ignored when the resistance of the column-direction wiring is much lower than the equivalent resistance of the surface-conduction emission type electron-emitting device. When, however, the resistance of the extraction wiring or the like increases to a noticeable degree, a potential drop caused by the column-direction wiring resistance may be compensated.

[0230] As described above, the activation apparatus of the sixth embodiment can make the electron-emitting characteristics of all devices uniform by monitoring activation currents and correcting the distribution of activation voltages to respective devices on one line. This electron source substrate is used to realize a high-quality image display apparatus almost free from variations in luminance or density.

[Seventh Embodiment]

[0231] An activation apparatus for the surface-conduction emission type electron-emitting device according to the seventh embodiment of the present invention will be described with reference to Fig. 18.

[0232] Also in Fig. 18, a surface-conduction emission type electron-emitting device substrate 501 is the same as the substrate 101 in Fig. 6. The operation of the whole apparatus, the activation procedure, and the like are the same as in the sixth embodiment, and a description thereof will be omitted.

[0233] The seventh embodiment is different from the sixth embodiment in method of driving a line selection circuit 502 of the surface-conduction emission type electron-emitting device substrate 501, as will be described.

[0234] The method of driving the line selection circuit 502 will be explained.

[0235] The line selection circuit 502 incorporates m switching elements (SWX1 to SWXm). Each switching element selects either one of the output potential of a power source 504 and the output potential of a variable power source 513, and the m switching elements are electrically connected to terminals Dx1 to Dxm of the surface-conduction emission type electron-emitting device substrate 501. Each switching element operates based on a control signal Vscan output from a timing generation circuit 105. In practice, the switching elements can be easily constituted by a combination of switching elements such as FETs or relays.

[0236] In Fig. 19, the first line (Sx1) is selected, the output potential of the power source 504 is applied to only the row-direction wiring Dx1, and the remaining lines (Sx2 to Sxm) are connected to the output potential of the variable power source 513. The output potential of the variable power source 513 is set by a non-selection potential setting value 512 output from a control circuit 506.

[0237] In the seventh embodiment, a non-selection potential as a potential applied to unselected lines (Sx2 to Sxm) to which no activation voltage is applied is set to a potential other than the ground level. The reason is as follows.

[0238] According to the electron source manufacturing method of the seventh embodiment, when activation is performed in units of rows, a potential drop distribution generated in the column direction on the same row is compensated by application potentials from column-direction wiring terminals Dy1 to Dyn. The application potentials from the column-direction wiring terminals Dy1 to Dyn are applied to not only devices on an activated line but also devices on an inactivated line because the surface-conduction emission type electron-emitting device substrate has a simple matrix arrangement. As a matter of course, the potentials of the column-direction wiring terminals Dy1 to Dyn are as low as several V in maximum. It is however desirable to reduce an increase in power consumption by application of potentials to devices on an inactivated line. For this purpose, inactivated lines are grouped, and the non-selection potential setting value 512 is applied to the grouped lines so as to minimize the absolute values of voltages applied across devices connected to these lines.

[0239] The non-selection potential setting value 512 is determined by the control circuit 506 as follows. The difference between maximum and minimum potentials generated at respective terminals at the output of a potential distribution circuit 508 is calculated as a potential drop amount. More specifically, in Fig. 18, the maximum potential distribution amount at outputs By1 to Byn of the potential distribution circuit 508 is calculated by

$$\text{Maximum Potential Distribution Amount} = \text{Potential By1} - \text{Potential Byn}$$

Thus, the non-selection potential setting value 512 is determined by

$$\text{Non-Selection Potential Setting Value 512: Voff} = 1/2 \times \text{Maximum Potential Distribution Amount}$$

[0240] Also in the seventh embodiment, similar to the first embodiment, the output of the potential distribution circuit 508 can be calculated using an activation current value 509 (I) of the current monitoring circuit 503 and wiring resistance values r1 to rn ≒ r:

$$By1 = -r1 \times \Sigma\{k = 1 \text{ to } n\}ik \fallingdotseq -r \times n \times iave \fallingdotseq -r \times I \ldots$$

$$Byn = -rn \times in + Byn\text{-}1 + Byn\text{-}2 + \ldots + By1 \fallingdotseq -r \times 1/n \times I + \ldots -r \times (n-1)/n \times I + (-r \times I) \fallingdotseq -1/2 \times r \times (n+1) \times I$$

[0241] Hence, the non-selection potential setting value 512 is calculated by

$$\begin{aligned} \text{Voff} &= -1/2 \times \text{Maximum Potential Distribution Amount} \\ &= -1/2\ (\text{Potential By1} - \text{Potential Byn}) \\ &= -1/4 \times r \times (n-1) \times I \end{aligned}$$

[0242] The potential of an unselected line is set in this manner to perform driving, and then voltages:
(Voff - By1) to (Voff - Byn) that is,

$$-1/4 \times r \times (n-5) \times I \text{ to } -1/4 \times r \times (n+3) \times I$$

are applied across devices on the unselected line.

[0243] When the non-selection potential setting value 512 is the ground level, voltages:
(Voff - By1) to (Voff - Byn) that is,

$$rxI \text{ to } 1/2 \times r \times (n+1) \times I$$

are applied across devices on an unselected line. By applying the non-selection potential setting value 512 to an unselected line, the absolute values of voltages applied across devices connected to the unselected line can be substantially halved (in general, n is as large as 1,000 or more).

[0244] Figs. 20A and 20B show changes in driving potential waveforms applied to each terminal of the surface-conduction emission type electron-emitting device substrate 501 at the start and end of activation.

[0245] Fig. 20A shows the driving potential waveform of each terminal immediately after the start of activation, and Fig. 20B shows the driving potential waveform at the end of activation.

[0246] As described above, each device is driven by a pulse having a driving potential of 18 in and a pulse width of 1 ms. A waveform (a) in Figs. 20A and 20B represents a driving waveform to the terminal Dx1 to be activated, which is driven by the power source 504 (driving potential: 18V, pulse width: 1 ms). A waveform (b) represents a driving waveform to the terminals Dx2 to Dxm on unselected lines which are not activated, which is driven by the variable power source 513 set by the non-selection potential setting value 512. The non-selection potential setting value 512 is represented by Voff. Waveforms (c) and (d) represent driving waveforms to the column-direction terminals of the surface-conduction emission type electron-emitting device substrate 501, which are driven by a buffer amplifier 507. The waveform (c) represents a driving waveform to the terminal Dy1 exhibiting the minimum potential drop, and the waveform (d) represents a driving waveform to the terminal Dyn exhibiting the maximum potential drop.

[0247] Immediately after the start of activation shown in Fig. 20A, almost no activation current flows. The potential drop amount caused by the wiring resistance is small, and the compensation potential amount and non-selection potential setting value Voff are also small. Activation progresses, and a large activation current flows at the end of activation. Accordingly, the potential drop amount caused by the wiring resistance increases, and the compensation potential amount and non-selection potential setting value Voff also increase, as shown in Fig 20B. That is, the compensation potential distribution changes with the progress of activation to always apply the set voltage = 18 V to each device.

[0248] Note that each device is driven by a pulse, as described above. Output of the pulse potential from the line selection circuit 502 starts after a change in pulse output from the buffer amplifier 507 for generating a potential distribution, and ends before a change in pulse output from the buffer amplifier 507. This will be explained. This time difference is represented by Δt in Figs. 20A and 20B. Δ t is about several μsec.

[0249] The time difference Δt is set to cope with a delay in output timing between channels owing to variations in buffer amplifier output between amplifiers. That is, output of the pulse voltage from the line selection circuit 502 may start before a change in pulse output from the buffer amplifier 507 for generating a potential distribution. In this case, if a delay occurs in output timing between channels, a sufficient driving voltage is instantaneously applied to only some of devices on a selected line. During this instantaneous time, all devices on the selected line are not driven to decrease a flowing activation current. The buffer amplifier applies a calculated potential on the assumption that all devices on the selected line are sufficiently driven. Therefore, a driving voltage higher than the set voltage is applied to the devices to make the characteristics nonuniform.

[0250] For this reason, output of the pulse potential from the line selection circuit 502 starts after a change in pulse output from the buffer amplifier 507 for generating a potential distribution, and ends before a change in pulse output from the buffer amplifier 507. With this setting, the influence of variations in output timing of the buffer amplifier can be avoided.

[0251] When a potential applied to an unselected line is made closer to the potential of the column wiring, as described in the seventh embodiment, the power applied in activating the surface-conduction emission type electron-emitting device substrate can be reduced. Note that the offset potential determination method is not limited to the above one, and the offset potential may be determined to minimize the power value applied to the entire surface-conduction emission type electron-emitting device substrate.

[0252] As described above, the activation apparatus of the seventh embodiment can make the electron-emitting characteristics of all devices uniform by monitoring activation currents and correcting the distribution of activation voltages to respective devices on one line. This electron source substrate is used to realize a high-quality image display apparatus almost free from variations in luminance or density.

[0253] Since a predetermined non-selection potential is applied to an inactivated line, an increase in power consumption by application of potentials to devices on an inactivated line can be reduced.

[0254] Moreover, output of the line selection pulse potential starts after a change in pulse output of the activation potential from the buffer amplifier, and ends before a change in pulse output of the activation potential from the buffer amplifier. Even if the output timing of the buffer amplifier varies, the influence can be avoided.

[Eighth Embodiment]

[0255] An activation apparatus for the surface-conduction emission type electron-emitting device according to the eighth embodiment of the present invention will be described with reference to Fig. 33.

[0256] Also in Fig. 33, a surface-conduction emission type electron-emitting device substrate 701 is the same as the substrate 101 in Fig. 1. The operation of the whole apparatus, the activation procedure, and the like are the same as in the sixth embodiment, and a description thereof will be omitted.

[0257] The eighth embodiment is different from the sixth and seventh embodiments in the absence of any current monitoring circuit connected to a line selection circuit 702 of the surface-conduction emission type electron-emitting device substrate 701. Instead, the eighth embodiment adopts a distribution value memory 712 for storing a distribution potential value to be generated in a potential distribution generation circuit 708. Data of the distribution value memory 712 can be transferred to the potential distribution circuit 708 in accordance with a command from a control circuit 706. The reason will be described.

[0258] As is apparent from changes in activation time and current in Figs. 27B, 5A, and 5B, the device current increases with electrification and saturates at last during activation processing. In the sixth and seventh embodiments, activation processing is performed while monitoring the device current by the current monitoring circuit so as to set the device current of each device on the surface-conduction emission type electron-emitting device substrate 101 to 2 mA at last. However, when the reproducibility of activation processing is high, and changes in activation time and current are almost the same in activating any device on the surface-conduction emission type electron-emitting device substrate 701, the end of activation can be determined by the electrification time of activation without monitoring the progress of activation by the current monitoring circuit.

[0259] The eighth embodiment will exemplify a method of compensating a potential drop caused in the line direction by the wiring resistance in the activation method of determining the end of activation by the electrification time of activation.

[0260] Similar to the sixth and seventh embodiments, activation was performed by applying pulses of an activation voltage having a pulse width of 1 msec, a pulse period of 10 msec, and a pulse height of 18 V. At that time, activation was performed for 30 min in order to obtain an activation device current of 2 mA/device.

[0261] Changes in activation time and current as shown in Figs. 27B, 5A, and 5B were measured for 30 min in advance. A voltage amount to be output from the potential distribution generation circuit 708 was calculated from an activation current value with the lapse of a certain activation time in accordance with equations (1) and (2) in the sixth embodiment, and stored in the distribution value correction memory 712.

[0262] The distribution value correction memory 712 is addressed by an activation time t and column-direction wiring numbers 1 to n. With the lapse of a corresponding activation time, compensation potential values to be generated at the column-direction wiring numbers 1 to n are output as output setting values 710 to set the values of corresponding D/A converters of the potential distribution generation circuit 708. Then, the independent compensation potential amounts are set in the D/A converters, and all the outputs are simultaneously updated by a latch CLK.

[0263] Fig. 34 shows an example of compensation potential values stored in the distribution value correction memory 712. In Fig. 34, compensation potential amounts are stored in the distribution value correction memory 712 every activation time t = 1 min. The compensation potential values of all the column-direction wiring numbers 1 to n are 0 V at the activation time t = 0. Compensation potentials from -0.1 V to -0.3 V are generated after 1 min, and compensation potentials from -0.5 V to -3.0 V are generated after 29 min. That is, compensation potential data for the column-direction wiring number n × 30 min are stored in the distribution value correction memory 712.

[0264] Figs. 35(a), 35(b), and 35(c) show the distributions of potentials applied across devices F1 to Fn 1 min after the start of activation and after 29 min immediately before the end when activation is performed for 30 min. The abscissa in Figs. 35(b) and 35(c) represents device numbers F1 to Fn, which indicate device positions. The ordinate represents terminal voltages at the two terminals of each device. As shown in Fig. 35(b), currents flowing through respective devices are small immediately after the start of activation, as described above. Therefore, the activation potential Eac = 18 V applied from a power source 704 is applied to terminals Gy1 to Gyn of the devices. In addition, almost no activation current flows. Respective values in the distribution value correction memory 712 are almost 0 V, the current setting value of the potential distribution generation circuit 708 is also almost 0, and outputs By1 to Byn of the potential distribution generation circuit 708 and outputs Sy1 to Syn of a buffer amplifier 707 are also almost 0 V. With the lapse of the activation time of 29 min shown in Fig 35C, respective values in the distribution value correction memory 712 generate the largest compensation potentials. Then, a predetermined application voltage up to 18 V is applied to respective devices to progress activation.

[0265] In the above description, compensation potential amounts are stored in the distribution value correction memory 712 every activation time t = 1 min. However, since a change in activation current in the unit time is not always constant in the activation time vs. activation current profile, the interval of the activation time t for addressing the distribution value correction memory 712 can be adjusted in accordance with an actual profile. More specifically, in a time range in which a change in activation current in the unit time is large, the interval of the activation time t for addressing the distribution value correction memory 712 is set small. In a time range in which a change in activation current in the unit time is small, the interval of the activation time t for addressing the distribution value correction memory 712 is set large.

With this setting, the memory capacity can be saved to realize potential compensation with high controllability.

[0266] According to the above embodiments, when a surface-conduction emission type electron-emitting device substrate on which surface-conduction emission type electron-emitting devices are arranged in a matrix is manufactured by activation, there can be realized activation which allows an electron source formed by arranging a large number of surface-conduction emission type electron-emitting devices in a simple matrix to obtain uniform electron-emitting characteristics by preventing variations in characteristics due to nonuniform voltages applied to the devices under the influence of a potential drop caused by the wiring resistance and activation current. This electron source substrate is used to realize a high-quality image display apparatus almost free from variations in luminance or density.

[0267] Further, the controllability can be improved by applying a predetermined non-selection potential to an inactivated line, and an increase in power consumption by application of voltages to devices on the unselected line can be reduced by making a potential applied to the unselected line closer to the potential of the column wiring.

[0268] Since output of the line selection pulse potential starts after a change in pulse output of the column wiring potential, and ends before a change in pulse output of the column wiring potential, the influence of variations in output (connection) timing of the potential can be avoided.

[0269] As has been described above, according to the present invention, a preferable electron-emitting device can be obtained.

[0270] As many apparently widely different embodiments of the present invention c1. An electron source manufacturing method comprising the step of applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and applying a potential to second portions of the plurality of conductive members, thereby applying a voltage to the plurality of conductive members,

an be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.

Claims

1. An electron source manufacturing method characterized by comprising the step of applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and applying a potential to second portions of the plurality of conductive members, thereby applying a voltage to the plurality of conductive members,
   wherein the potential applied to the second portions of the plurality of conductive members is set to relax a difference in voltage applied to the plurality of conductive members owing to a difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

2. The method according to claim 1, wherein the potential applied to the second portion is changed in accordance with a change in potential applied to the first portion.

3. The method according to claim 1 or 2, wherein the potential applied to the first portion is estimated.

4. The method according to claim 3, wherein the potential applied to the first portion is estimated by measuring a current flowing through the wiring.

5. The method according to claim 3, wherein the potential applied to the first portion is estimated by measuring a current flowing through a wiring connected to the second portion.

6. The method according to claim 3, wherein the potential applied to the first portion is estimated based on stored data.

7. The method according to any one of claims 1 to 6, wherein the potential to be applied to the second portion is determined by using an equivalent wiring resistance array obtained by arranging resistances substantially equal to a resistance of the wiring in an array.

8. The method according to claim 7, wherein the potential to be applied to the second portion is determined by sinking a predetermined current amount or using the predetermined current amount as a current source from portions of the equivalent wiring resistance array respectively connected to the second portions.

9. The method according to any one of claims 1 to 8, wherein one or both of the potential applied to the first portion

and the potential applied to the second portion are applied as pulses.

10. The method according to any one of claims 1 to 8, wherein a potential applied to the wiring commonly connected to the plurality of conductive members and the potential applied to the second portion are applied as pulses, and the pulse-like potential applied to the wiring commonly connected to the plurality of conductive members is applied after the pulse-like potential applied to the second portion.

11. The method according to any one of claims 1 to 10, wherein the conductive member is connected to one of a plurality of row wirings and one of a plurality of column wirings that constitute a matrix, and the voltage application step comprises the step of applying a voltage to conductive members connected to a row wiring selected from the plurality of row wirings by a potential applied to the first portions in accordance with a potential applied to the selected row wiring and a potential applied to the second portions in accordance with a potential applied to the plurality of column wirings.

12. The method according to claim 11, wherein the voltage application step comprises the step of applying, to an unselected row wiring out of the plurality of row wirings, a potential for suppressing a current flowing through the unselected row wiring owing to a potential difference from the potential applied to the column wiring.

13. The method according to claim 12, wherein one or both of the potential applied to the unselected row wiring and the potential applied to the column wiring are set to set the potential of the unselected row wiring to a potential between maximum and minimum values of the potential applied to the plurality of column wirings.

14. The method according to claim 12, wherein one or both of the potential applied to the unselected row wiring and the potential applied to the column wiring are set to set a ground potential between maximum and minimum values of the potential applied to the plurality of column wirings.

15. The method according to any one of claims 11 to 14, further comprising the step of applying the voltage while sequentially switching row wirings to be selected.

16. The method according to claim 15, wherein row wirings to be selected are switched upon completion of the step of applying the voltage to the conductive members connected to the selected row wiring.

17. The method according to claim 15, further comprising the steps of: selecting a given row wiring and applying the voltage to conductive members connected to the selected row wiring at a time interval, thereby applying the voltage; and selecting another row wiring during the time interval and applying the voltage to conductive members connected to said another row wiring.

18. A method of manufacturing an image forming apparatus having an electron source and an image forming member for forming an image upon irradiation of electrons emitted by the electron source, characterized by comprising the steps of manufacturing the electron source by the electron source manufacturing method defined in any one of claims 1 to 17, and assembling the electron source and the image forming member.

19. An electron source manufacturing apparatus characterized by comprising a first circuit for applying a potential to first portions of a plurality of conductive members serving as at least part of electron-emitting devices via a wiring commonly connected to the plurality of conductive members, and a second circuit for applying a potential to second portions of the plurality of conductive members, wherein said second circuit sets the potential applied to the second portions of the plurality of conductive members so as to relax a difference in voltage applied to the plurality of conductive members owing to a difference between potentials at portions respectively connected to the first portions of the plurality of conductive members in the wiring commonly connected to the plurality of conductive members.

20. The apparatus according to claim 19, wherein said second circuit comprises an equivalent wiring resistance array having a resistance substantially equal to a resistance of the wiring, and a control current circuit for sinking or sourcing a predetermined current.

21. The apparatus according to claim 19 or 20, further comprising a current monitoring circuit for monitoring a current flowing through the conductive member.

22. The apparatus according to claim 21 wherein said current monitoring circuit monitors a current flowing through the wiring.

23. The apparatus according to claim 21 wherein said current monitoring circuit monitors currents respectively flowing through the conductive members.

24. The apparatus according to any one of claims 19 to 23, wherein said second circuit sets the potential on the basis of a current flowing through the conductive member.

25. The apparatus according to any one of claims 21 to 24, wherein said second circuit comprises a latch circuit for storing a digital value corresponding to a current value flowing through the conductive member, and a D/A converter for converting the digital value stored in said latch circuit into a current value.

26. The apparatus according to claim 19, wherein said second circuit controls the potential applied to the second portion in accordance with an application time of the potential to the second portion.

27. The apparatus according to any one of claims 19 to 26, wherein said second circuit comprises memory means which is referred to in order to set the potential applied to the second portion.

28. The apparatus according to any one of claims 19 to 27, wherein the first circuit applies a potential from two sides of the wiring.

29. A voltage applying circuit applying a voltage to a plurality of conductive members connected with a plurality of row wirings and a plurality of column wirings which form a matrix, comprising:

first circuit supplying a predetermined potential to a row wiring selected among the plurality of row wirings; and
second circuit supplying a predetermined potential to each of the plurality of column wirings,
wherein said second circuit includes a potential distribution generating circuit having an equivalent wiring resistance array and a source of a control current, wherein the equivalent wiring resistance array has a resistance substantially equal to the resistance of the row wiring, and the source of the control current serves to sink or supply a current flowing said plurality of conductive members.

30. A circuit according to claim 29, wherein said second circuit has a circuit for superposing the potential distribution generated by said potential distribution generating circuit and an offset potential.

FIG. 1

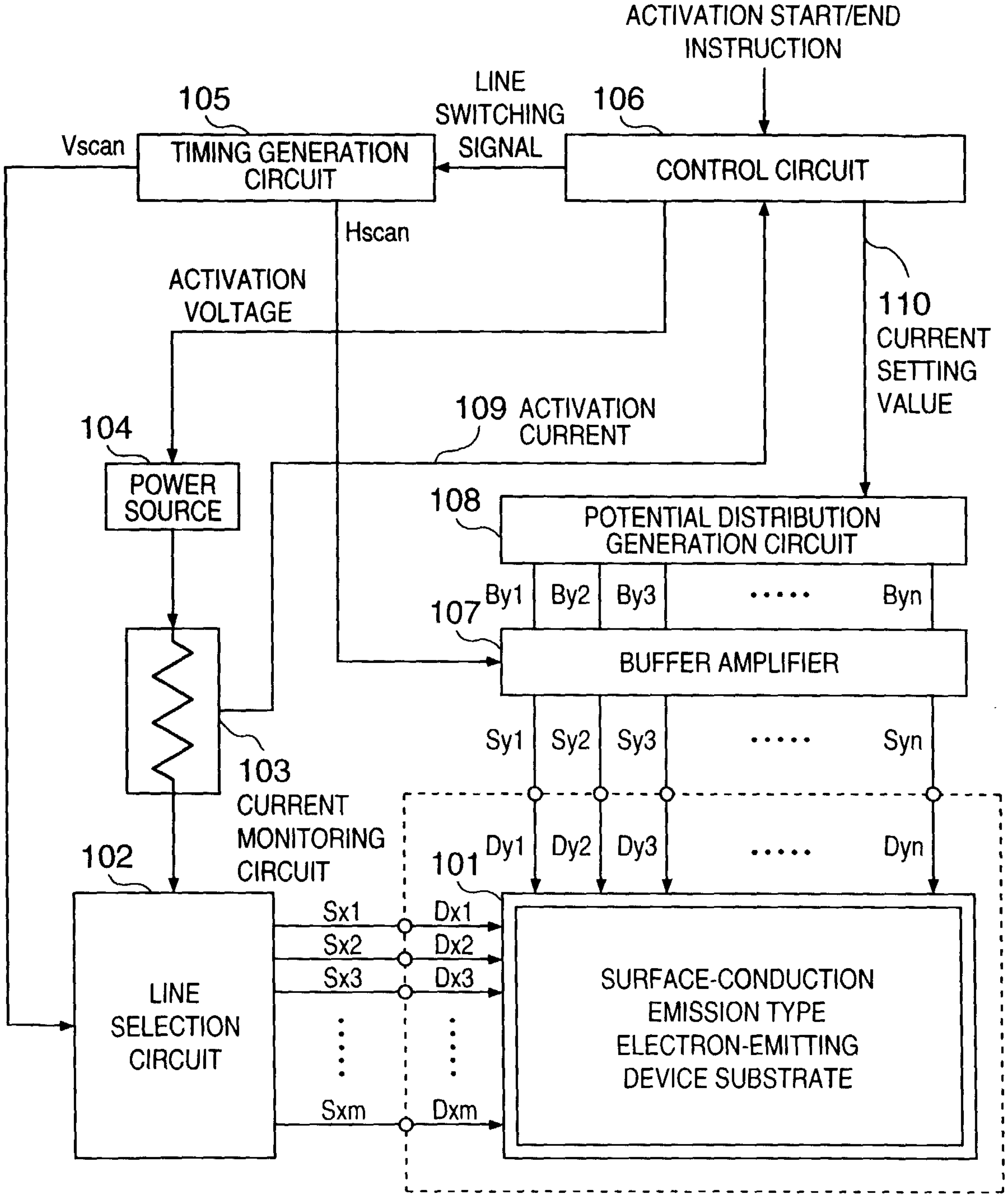

ACTIVATION START/END INSTRUCTION
LINE SWITCHING SIGNAL
105
TIMING GENERATION CIRCUIT
106
CONTROL CIRCUIT
Vscan
Hscan
ACTIVATION VOLTAGE
110
CURRENT SETTING VALUE
109 ACTIVATION CURRENT
104
POWER SOURCE
108
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
By1
By2
By3
.....
Byn
107
BUFFER AMPLIFIER
Sy1
Sy2
Sy3
.....
Syn
103
CURRENT MONITORING CIRCUIT
102
101
Dy1
Dy2
Dy3
.....
Dyn
LINE SELECTION CIRCUIT
Sx1
Sx2
Sx3
Sxm
Dx1
Dx2
Dx3
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

FIG. 2

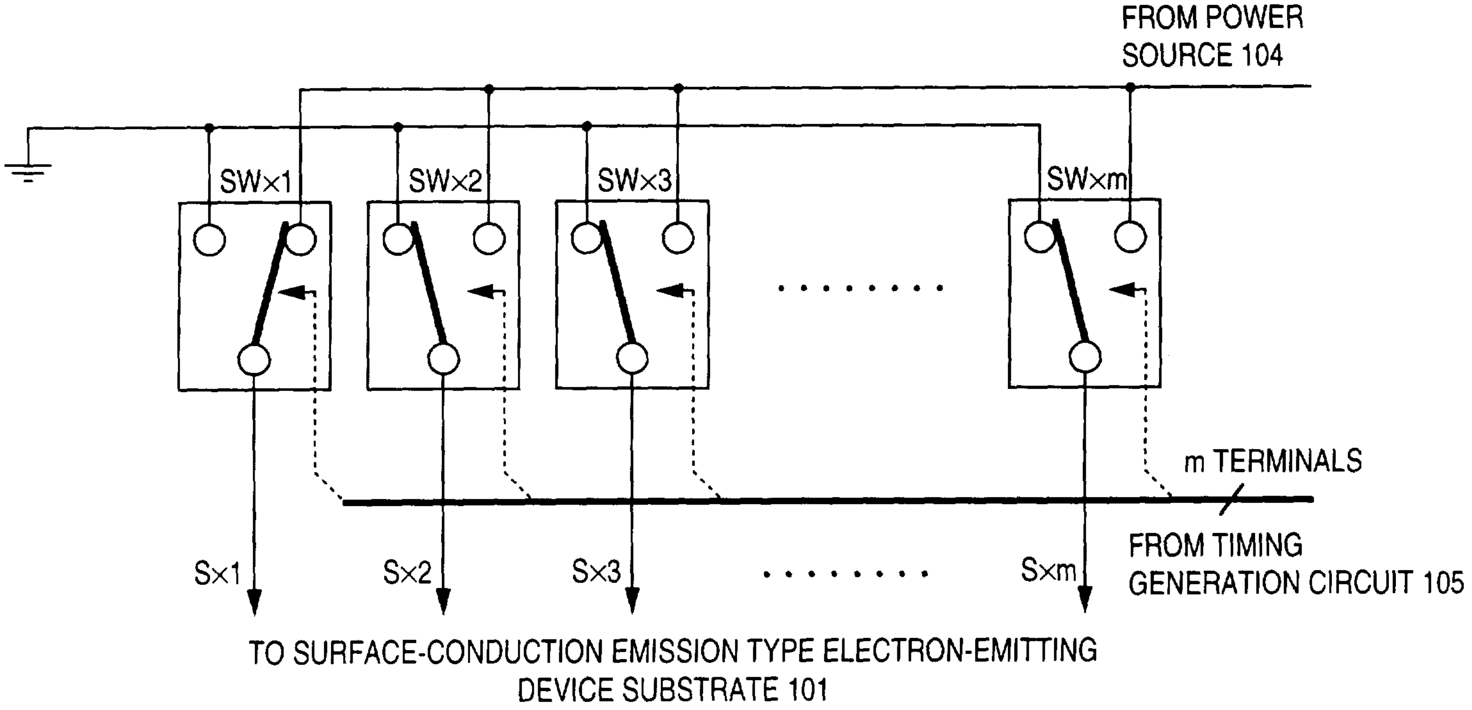
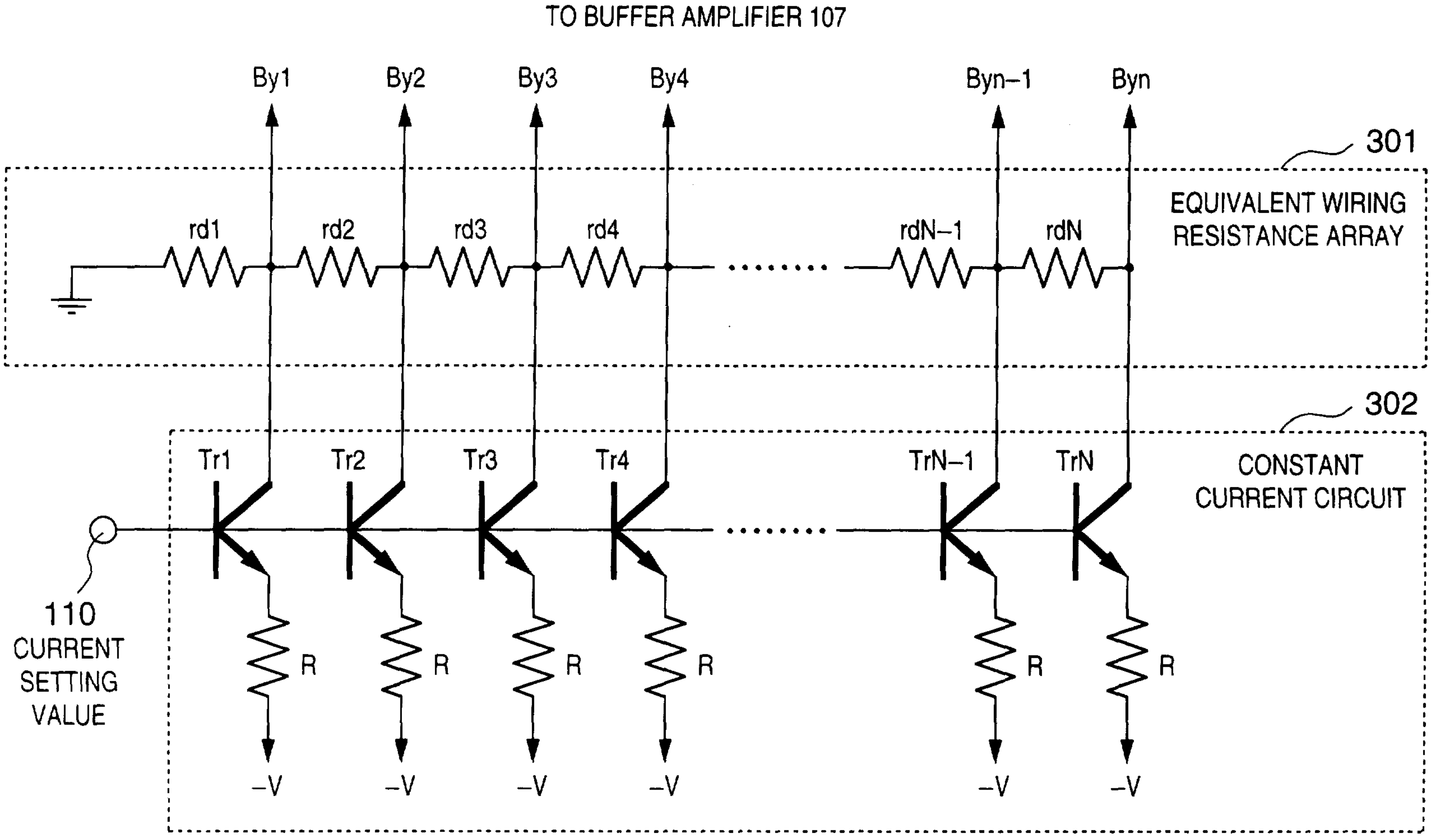

FROM POWER SOURCE 104
SW×1
SW×2
SW×3
SW×m
m TERMINALS
FROM TIMING GENERATION CIRCUIT 105
S×1
S×2
S×3
S×m
TO SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE 101

FIG. 3


TO BUFFER AMPLIFIER 107
By1
By2
By3
By4
Byn–1
Byn
301
EQUIVALENT WIRING
RESISTANCE ARRAY
rd1
rd2
rd3
rd4
rdN–1
rdN
302
CONSTANT
CURRENT CIRCUIT
Tr1
Tr2
Tr3
Tr4
TrN–1
TrN
110
CURRENT
SETTING
VALUE
R
R
R
R
R
R
–V
–V
–V
–V
–V
–V

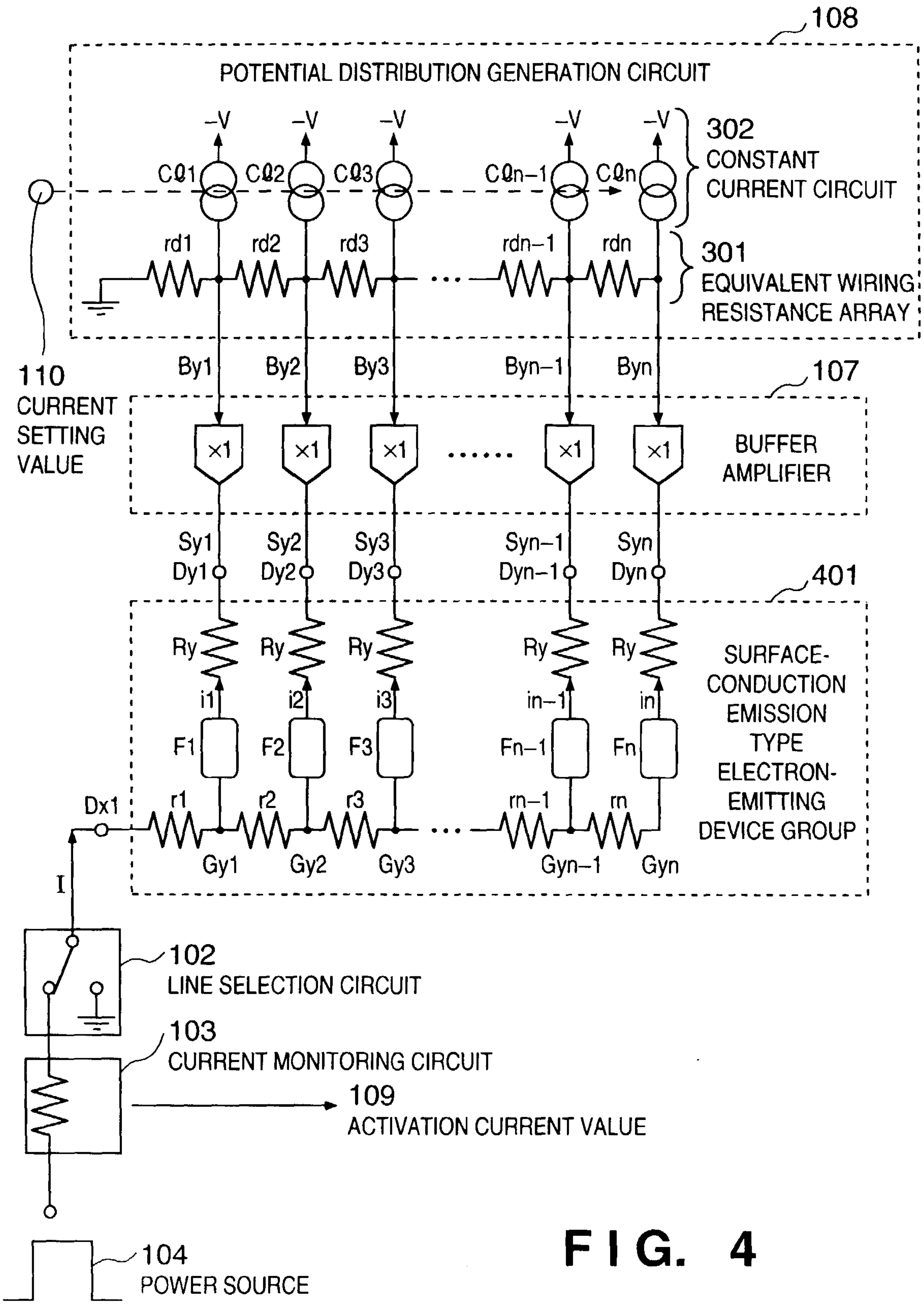

108
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
-V
-V
-V
-V
-V
302
CONSTANT CURRENT CIRCUIT
CQ1
CQ2
CQ3
CQn-1
CQn
rd1
rd2
rd3
rdn-1
rdn
301
EQUIVALENT WIRING RESISTANCE ARRAY
110
CURRENT SETTING VALUE
By1
By2
By3
Byn-1
Byn
107
×1
×1
×1
×1
×1
BUFFER AMPLIFIER
Sy1
Dy1
Sy2
Dy2
Sy3
Dy3
Syn-1
Dyn-1
Syn
Dyn
401
Ry
Ry
Ry
Ry
Ry
i1
i2
i3
in-1
in
F1
F2
F3
Fn-1
Fn
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE GROUP
Dx1
r1
r2
r3
rn-1
rn
Gy1
Gy2
Gy3
Gyn-1
Gyn
I
102
LINE SELECTION CIRCUIT
103
CURRENT MONITORING CIRCUIT
109
ACTIVATION CURRENT VALUE
104
POWER SOURCE

FIG. 4

FIG. 5A

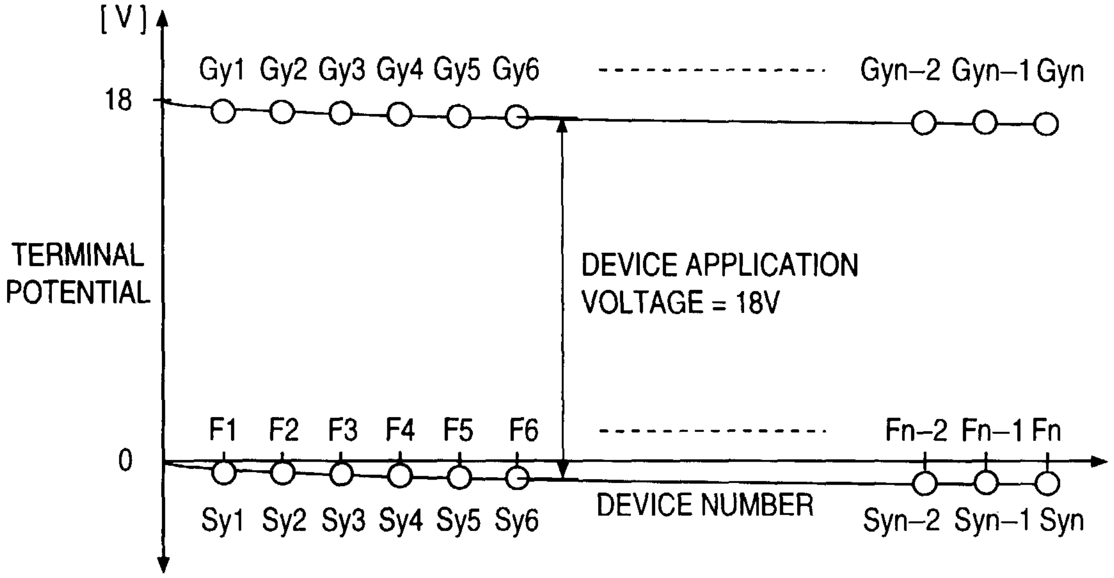

[V]
18
0
TERMINAL POTENTIAL
Gy1 Gy2 Gy3 Gy4 Gy5 Gy6
Gyn−2 Gyn−1 Gyn
DEVICE APPLICATION VOLTAGE = 18V
F1 F2 F3 F4 F5 F6
Fn−2 Fn−1 Fn
Sy1 Sy2 Sy3 Sy4 Sy5 Sy6
DEVICE NUMBER
Syn−2 Syn−1 Syn

FIG. 5B

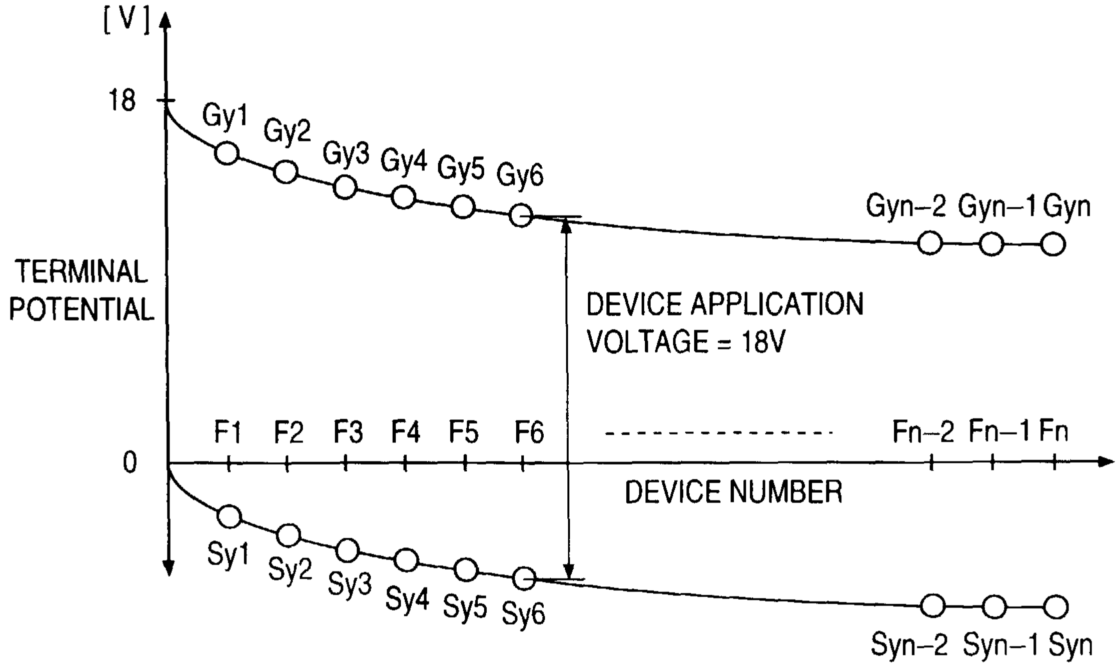

[V]
18
0
TERMINAL POTENTIAL
Gy1 Gy2 Gy3 Gy4 Gy5 Gy6
Gyn−2 Gyn−1 Gyn
DEVICE APPLICATION VOLTAGE = 18V
F1 F2 F3 F4 F5 F6
Fn−2 Fn−1 Fn
DEVICE NUMBER
Sy1 Sy2 Sy3 Sy4 Sy5 Sy6
Syn−2 Syn−1 Syn

FIG. 6

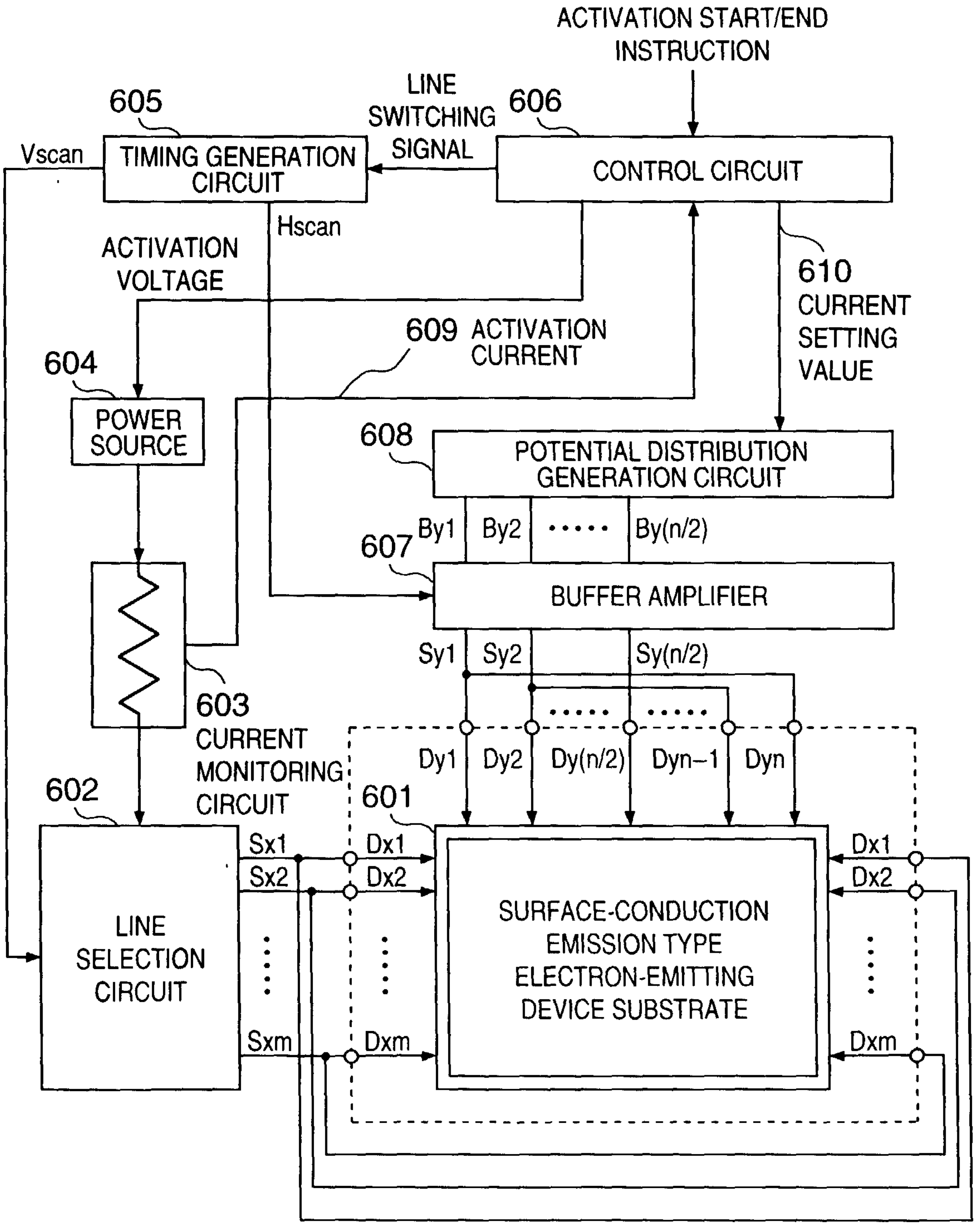

ACTIVATION START/END INSTRUCTION
605
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
606
CONTROL CIRCUIT
Vscan
Hscan
ACTIVATION VOLTAGE
610
CURRENT SETTING VALUE
609 ACTIVATION CURRENT
604
POWER SOURCE
608
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
607
By1
By2
By(n/2)
BUFFER AMPLIFIER
Sy1
Sy2
Sy(n/2)
603
CURRENT MONITORING CIRCUIT
Dy1
Dy2
Dy(n/2)
Dyn−1
Dyn
602
601
LINE SELECTION CIRCUIT
Sx1
Sx2
Sxm
Dx1
Dx2
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE
Dx1
Dx2
Dxm

FIG. 7A

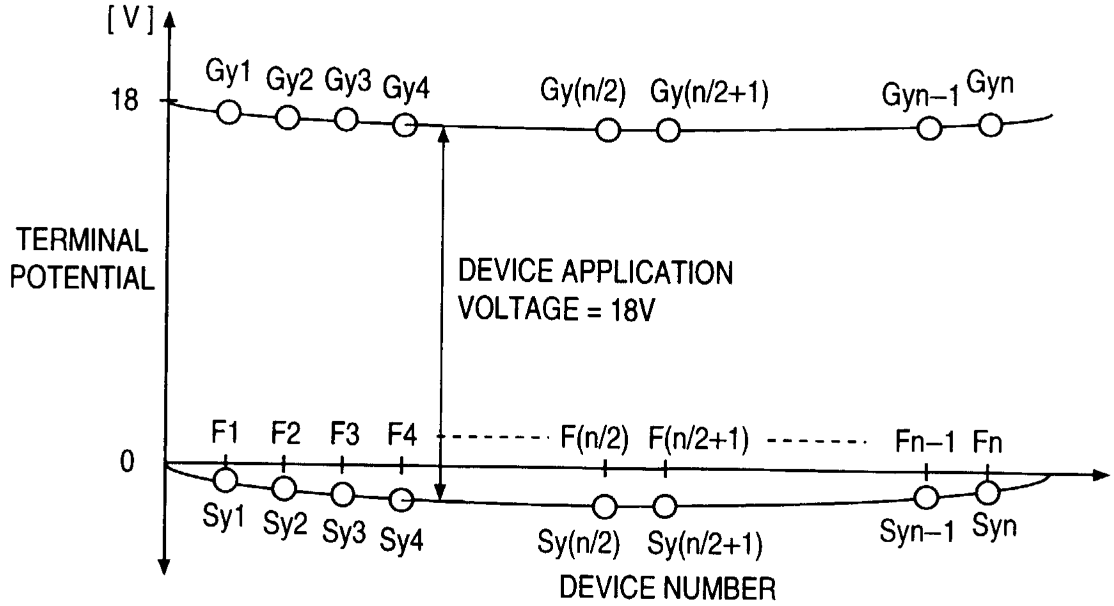

[V]
18
0
TERMINAL POTENTIAL
Gy1 Gy2 Gy3 Gy4 Gy(n/2) Gy(n/2+1) Gyn–1 Gyn
DEVICE APPLICATION VOLTAGE = 18V
F1 F2 F3 F4 F(n/2) F(n/2+1) Fn–1 Fn
Sy1 Sy2 Sy3 Sy4 Sy(n/2) Sy(n/2+1) Syn–1 Syn
DEVICE NUMBER

FIG. 7B

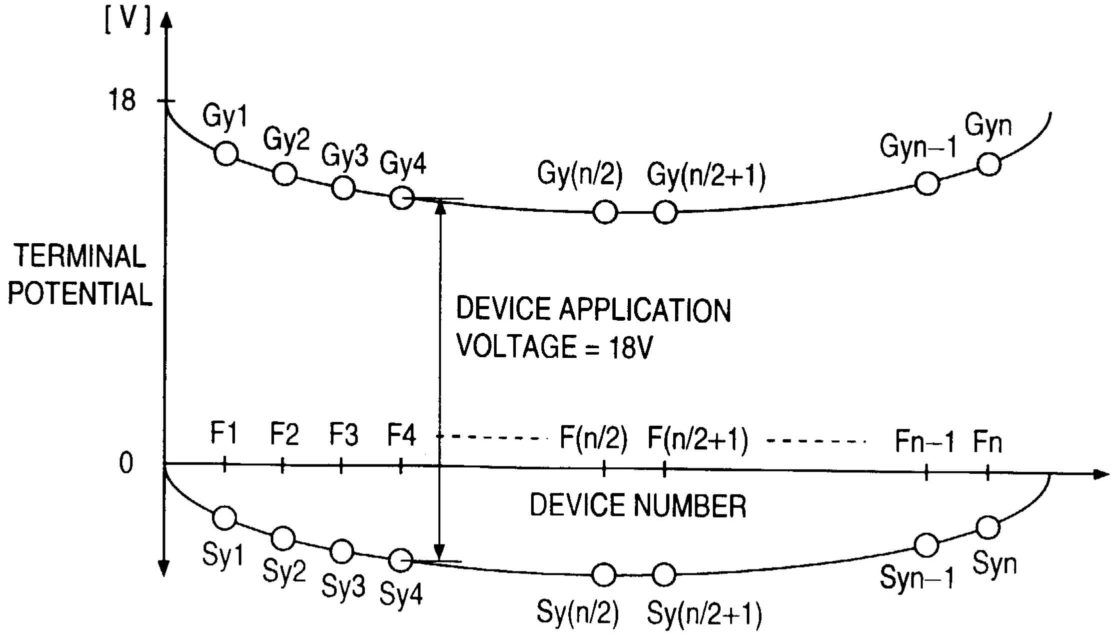
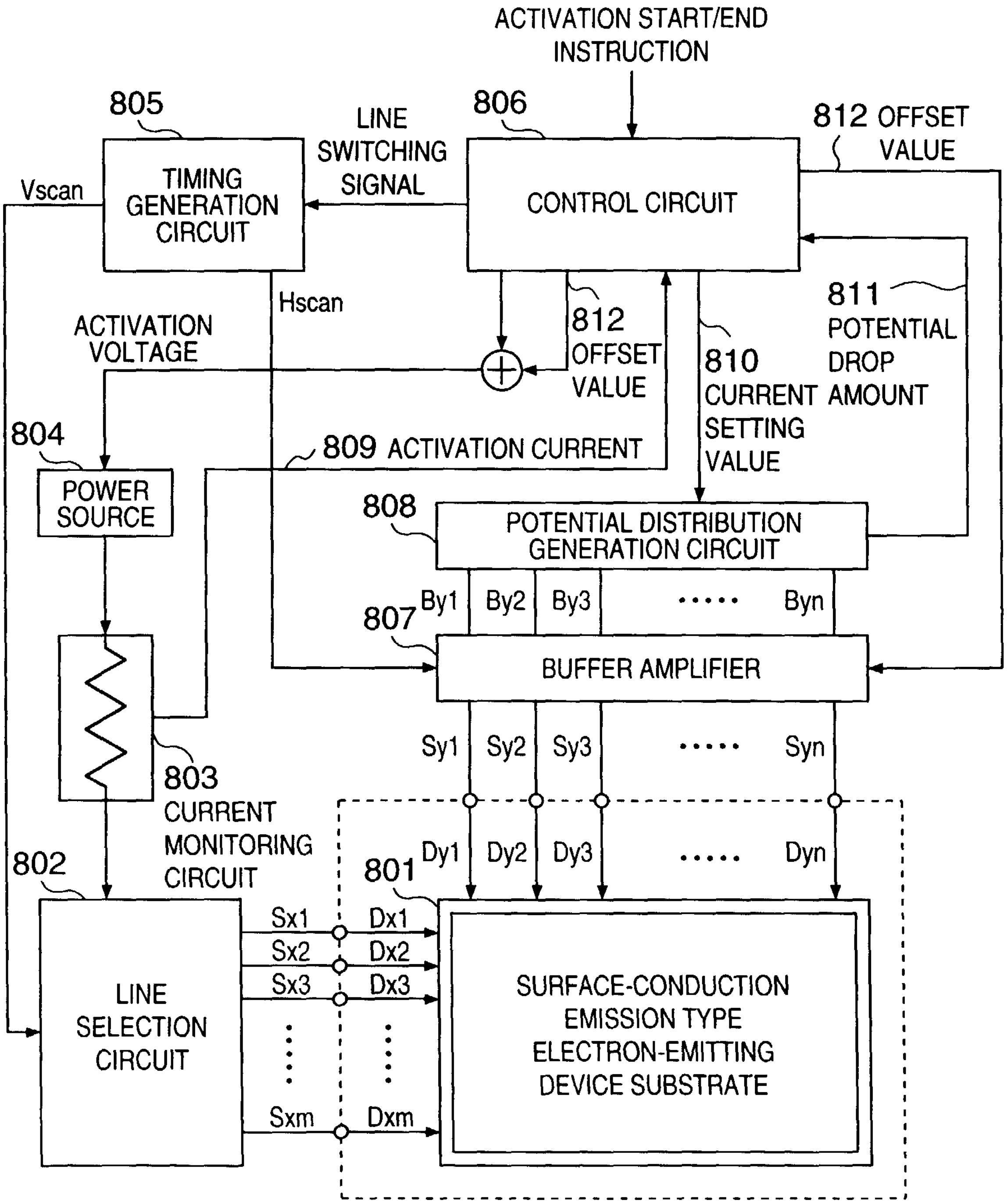

[V]
18
0
TERMINAL POTENTIAL
Gy1 Gy2 Gy3 Gy4 Gy(n/2) Gy(n/2+1) Gyn–1 Gyn
DEVICE APPLICATION VOLTAGE = 18V
F1 F2 F3 F4 F(n/2) F(n/2+1) Fn–1 Fn
DEVICE NUMBER
Sy1 Sy2 Sy3 Sy4 Sy(n/2) Sy(n/2+1) Syn–1 Syn

FIG. 8


ACTIVATION START/END INSTRUCTION
805
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
806
CONTROL CIRCUIT
812 OFFSET VALUE
Vscan
Hscan
ACTIVATION VOLTAGE
812 OFFSET VALUE
810 CURRENT SETTING VALUE
811 POTENTIAL DROP AMOUNT
804
POWER SOURCE
809 ACTIVATION CURRENT
808
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
807
By1 By2 By3 ..... Byn
BUFFER AMPLIFIER
Sy1 Sy2 Sy3 ..... Syn
803 CURRENT MONITORING CIRCUIT
802
801
Dy1 Dy2 Dy3 ..... Dyn
LINE SELECTION CIRCUIT
Sx1 Sx2 Sx3 Sxm
Dx1 Dx2 Dx3 Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

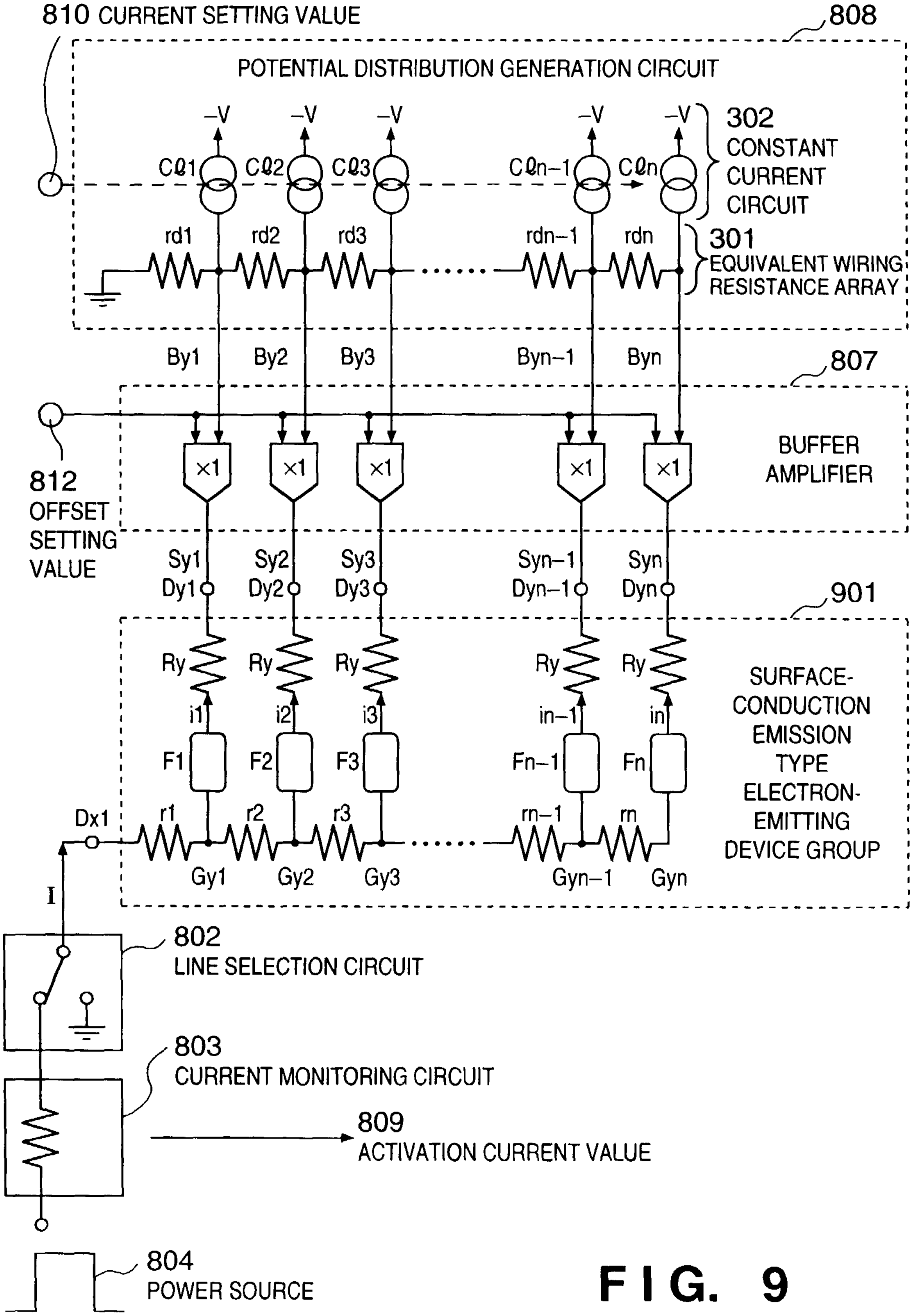

810 CURRENT SETTING VALUE
808
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
−V
−V
−V
−V
−V
302
CONSTANT CURRENT CIRCUIT
CQ1
CQ2
CQ3
CQn−1
CQn
rd1
rd2
rd3
rdn−1
rdn
301
EQUIVALENT WIRING RESISTANCE ARRAY
By1
By2
By3
Byn−1
Byn
807
×1
×1
×1
×1
×1
BUFFER AMPLIFIER
812
OFFSET SETTING VALUE
Sy1
Dy1
Sy2
Dy2
Sy3
Dy3
Syn−1
Dyn−1
Syn
Dyn
901
Ry
Ry
Ry
Ry
Ry
i1
i2
i3
in−1
in
F1
F2
F3
Fn−1
Fn
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE GROUP
Dx1
r1
r2
r3
rn−1
rn
Gy1
Gy2
Gy3
Gyn−1
Gyn
I
802
LINE SELECTION CIRCUIT
803
CURRENT MONITORING CIRCUIT
809
ACTIVATION CURRENT VALUE
804
POWER SOURCE

FIG. 9

FIG. 10A

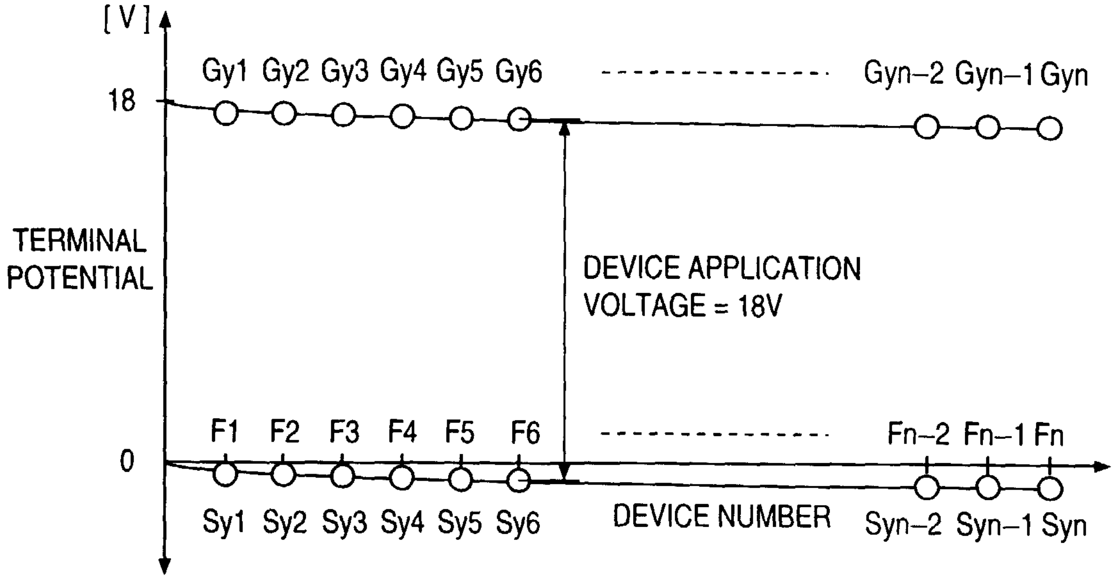
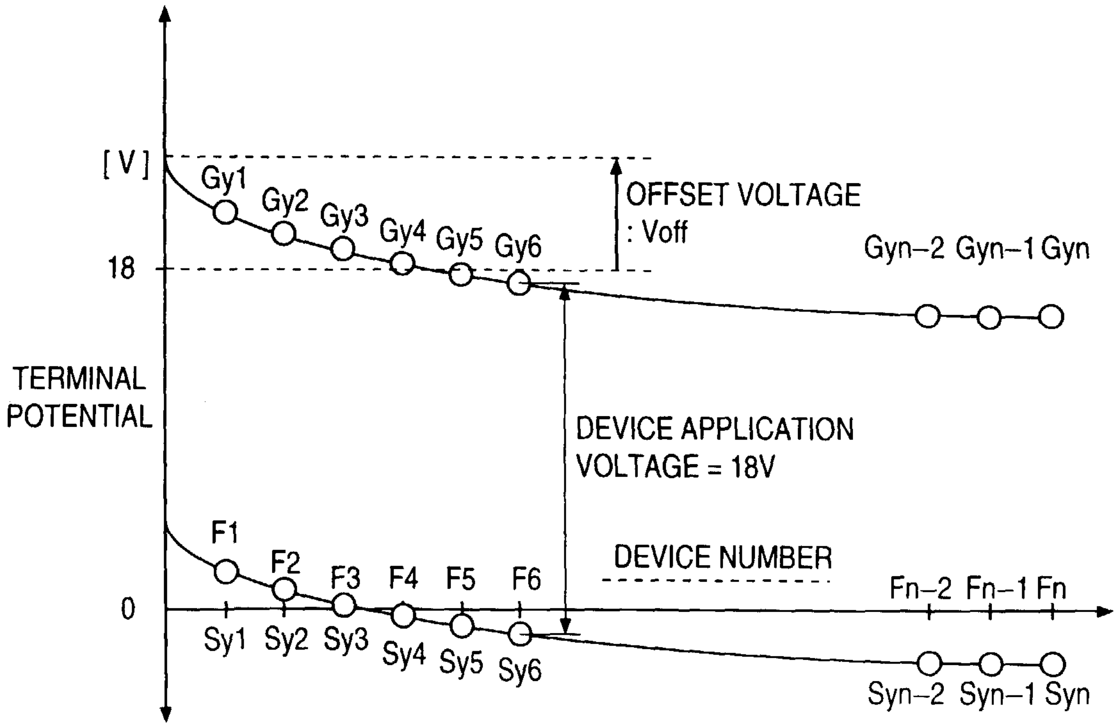
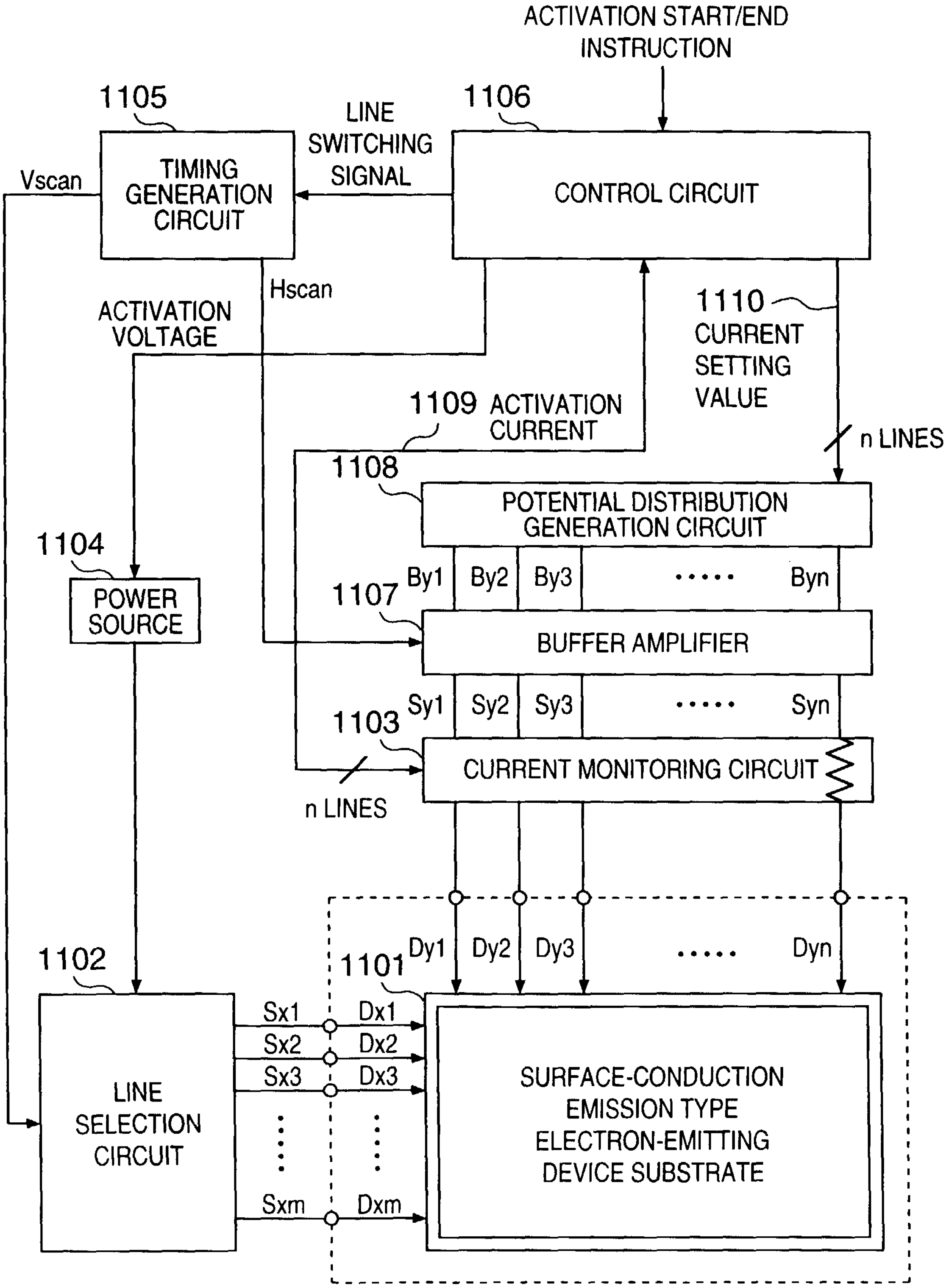


FIG. 10B



F I G. 11


ACTIVATION START/END INSTRUCTION
1105
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
1106
CONTROL CIRCUIT
Vscan
Hscan
ACTIVATION VOLTAGE
1110
CURRENT SETTING VALUE
1109
ACTIVATION CURRENT
n LINES
1108
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
1104
POWER SOURCE
1107
By1
By2
By3
.....
Byn
BUFFER AMPLIFIER
1103
Sy1
Sy2
Sy3
.....
Syn
CURRENT MONITORING CIRCUIT
n LINES
1102
1101
Dy1
Dy2
Dy3
.....
Dyn
LINE SELECTION CIRCUIT
Sx1
Sx2
Sx3
Sxm
Dx1
Dx2
Dx3
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

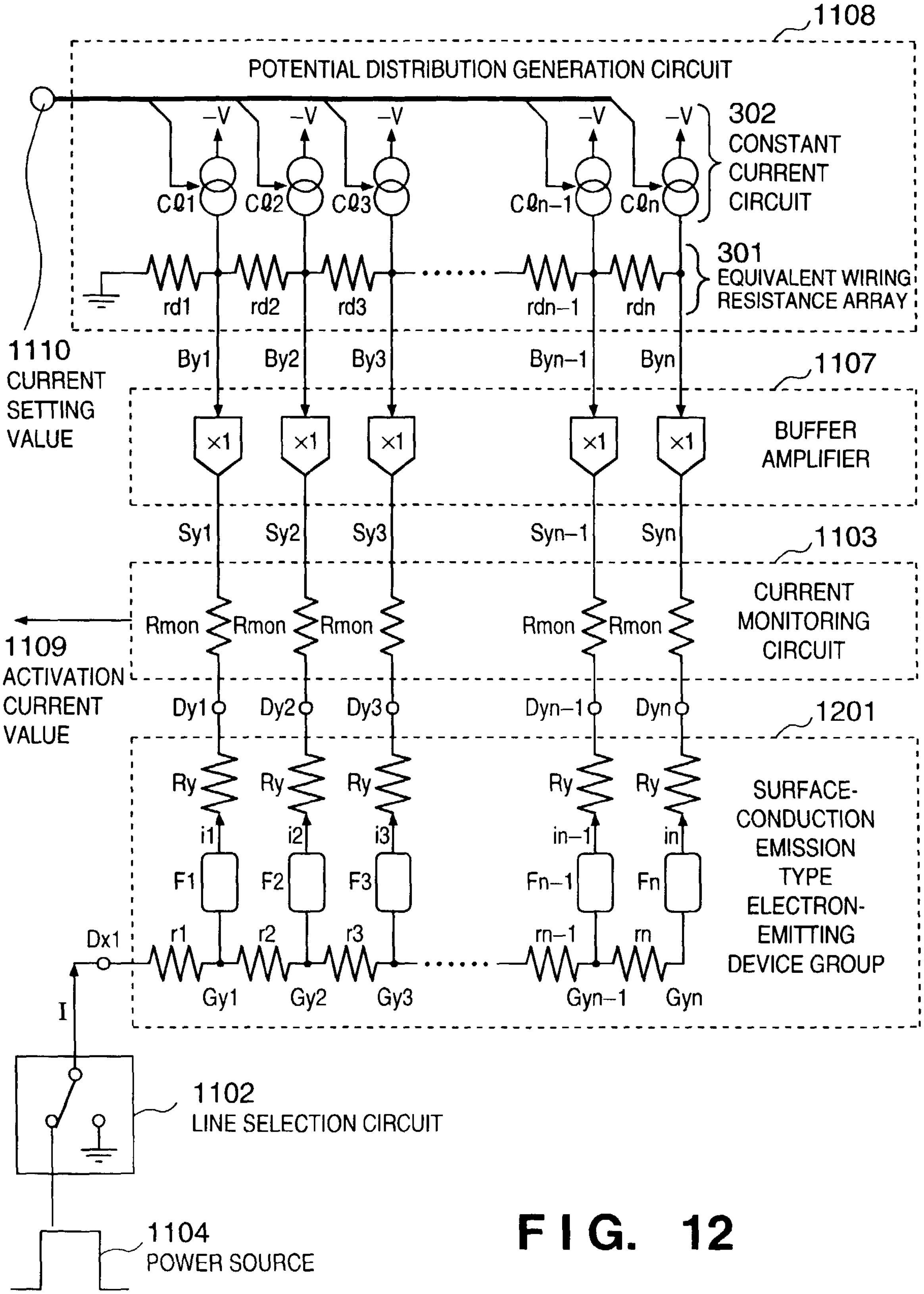
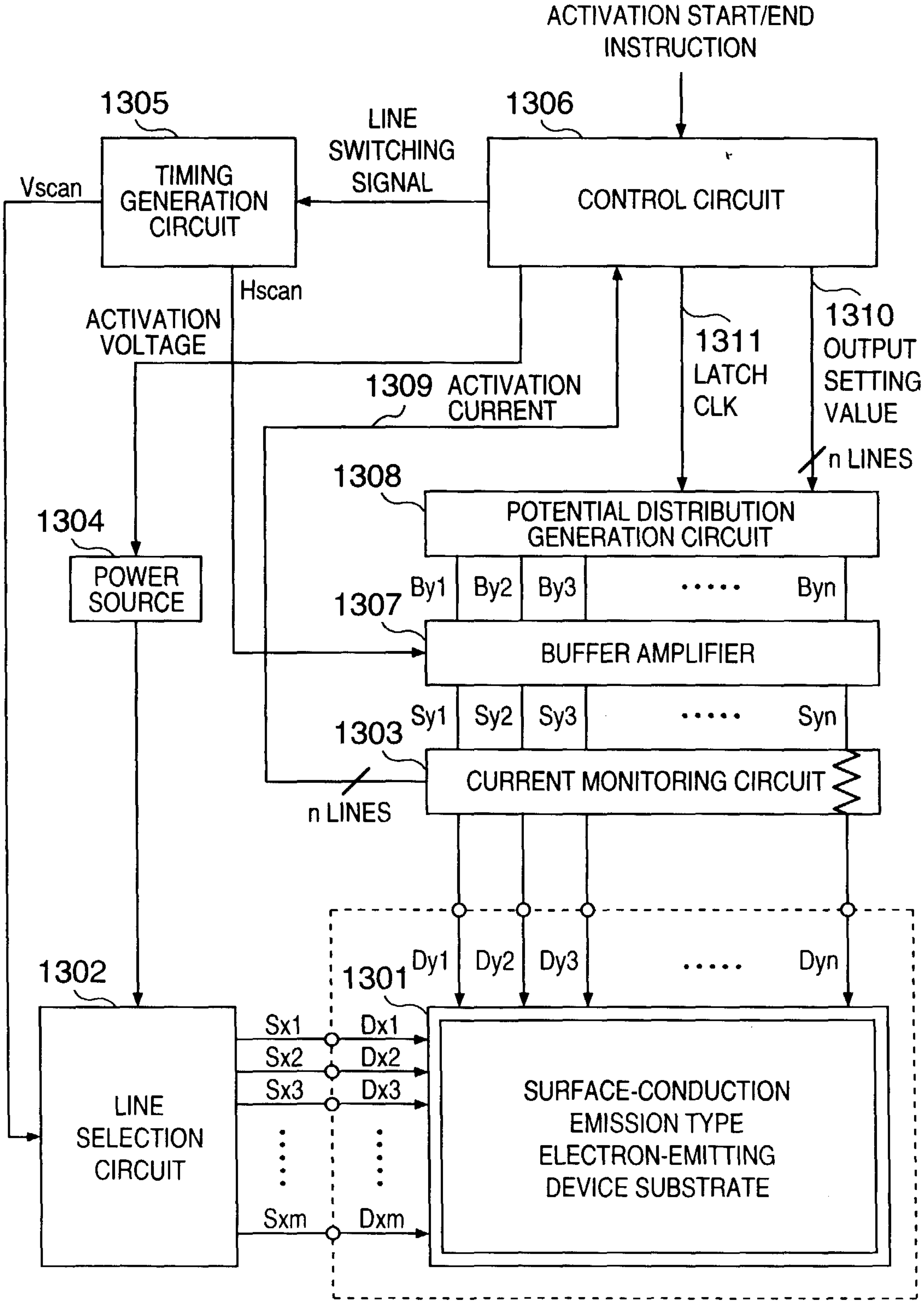

1108
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
−V
302
CONSTANT CURRENT CIRCUIT
Cℓ1
Cℓ2
Cℓ3
Cℓn−1
Cℓn
301
EQUIVALENT WIRING RESISTANCE ARRAY
rd1
rd2
rd3
rdn−1
rdn
1110
CURRENT SETTING VALUE
By1
By2
By3
Byn−1
Byn
1107
×1
BUFFER AMPLIFIER
Sy1
Sy2
Sy3
Syn−1
Syn
1103
Rmon
CURRENT MONITORING CIRCUIT
1109
ACTIVATION CURRENT VALUE
Dy1
Dy2
Dy3
Dyn−1
Dyn
1201
Ry
i1
i2
i3
in−1
in
F1
F2
F3
Fn−1
Fn
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE GROUP
Dx1
r1
r2
r3
rn−1
rn
Gy1
Gy2
Gy3
Gyn−1
Gyn
I
1102
LINE SELECTION CIRCUIT
1104
POWER SOURCE

FIG. 12

F I G. 13


ACTIVATION START/END INSTRUCTION
1305
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
1306
CONTROL CIRCUIT
Vscan
Hscan
ACTIVATION VOLTAGE
1309 ACTIVATION CURRENT
1311 LATCH CLK
1310 OUTPUT SETTING VALUE
n LINES
1308
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
1304
POWER SOURCE
1307
By1 By2 By3 ····· Byn
BUFFER AMPLIFIER
1303
Sy1 Sy2 Sy3 ····· Syn
CURRENT MONITORING CIRCUIT
n LINES
1302
1301
Dy1 Dy2 Dy3 ····· Dyn
LINE SELECTION CIRCUIT
Sx1 Sx2 Sx3 Sxm
Dx1 Dx2 Dx3 Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

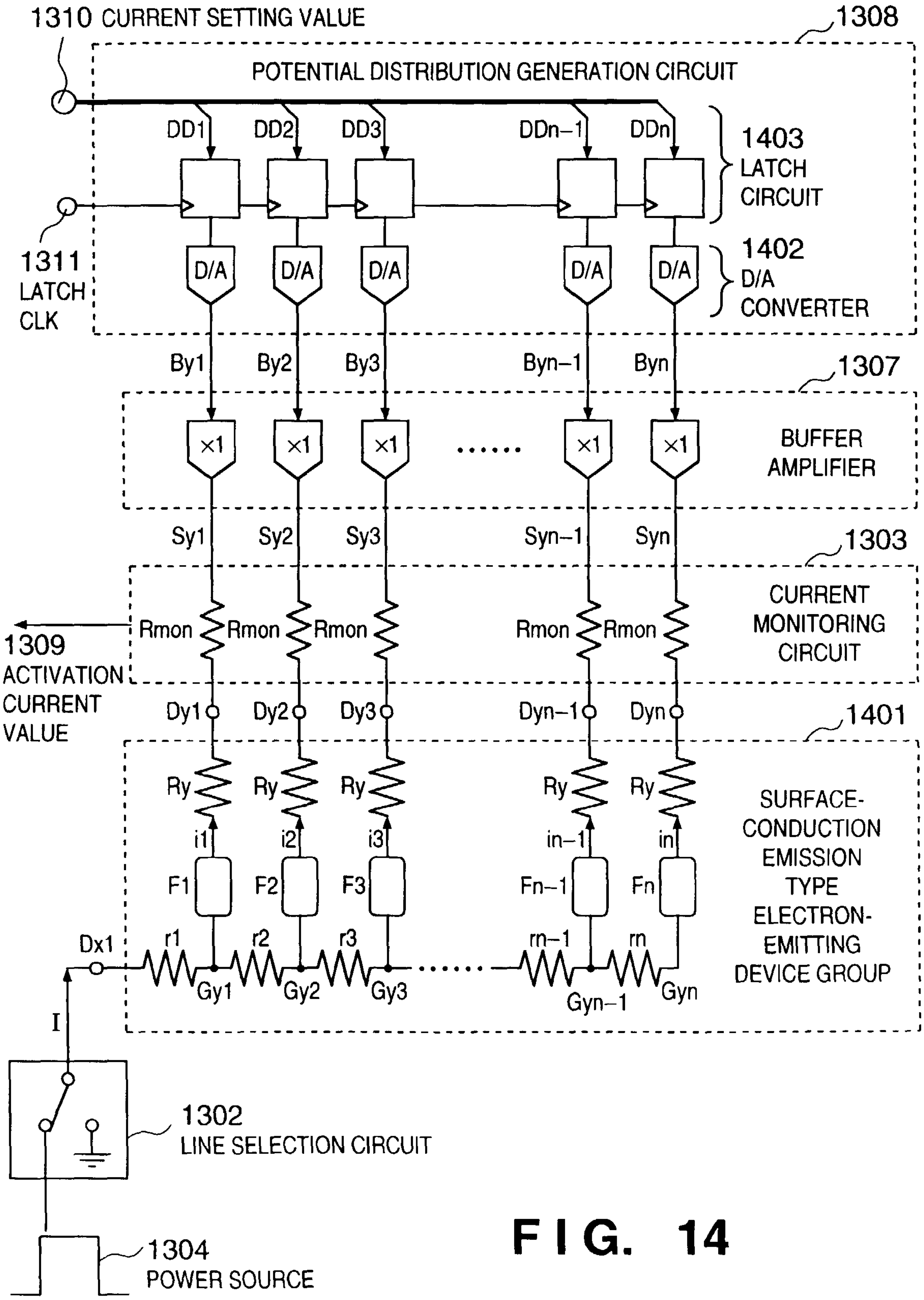

1310 CURRENT SETTING VALUE
1308
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
DD1
DD2
DD3
DDn−1
DDn
1403
LATCH
CIRCUIT
1311
LATCH
CLK
D/A
1402
D/A
CONVERTER
By1
By2
By3
Byn−1
Byn
1307
×1
BUFFER
AMPLIFIER
Sy1
Sy2
Sy3
Syn−1
Syn
1303
CURRENT
MONITORING
CIRCUIT
Rmon
1309
ACTIVATION
CURRENT
VALUE
Dy1
Dy2
Dy3
Dyn−1
Dyn
1401
Ry
i1
i2
i3
in−1
in
F1
F2
F3
Fn−1
Fn
SURFACE-
CONDUCTION
EMISSION
TYPE
ELECTRON-
EMITTING
DEVICE GROUP
Dx1
r1
r2
r3
rn−1
rn
Gy1
Gy2
Gy3
Gyn−1
Gyn
I
1302
LINE SELECTION CIRCUIT
1304
POWER SOURCE

FIG. 14

FIG. 15

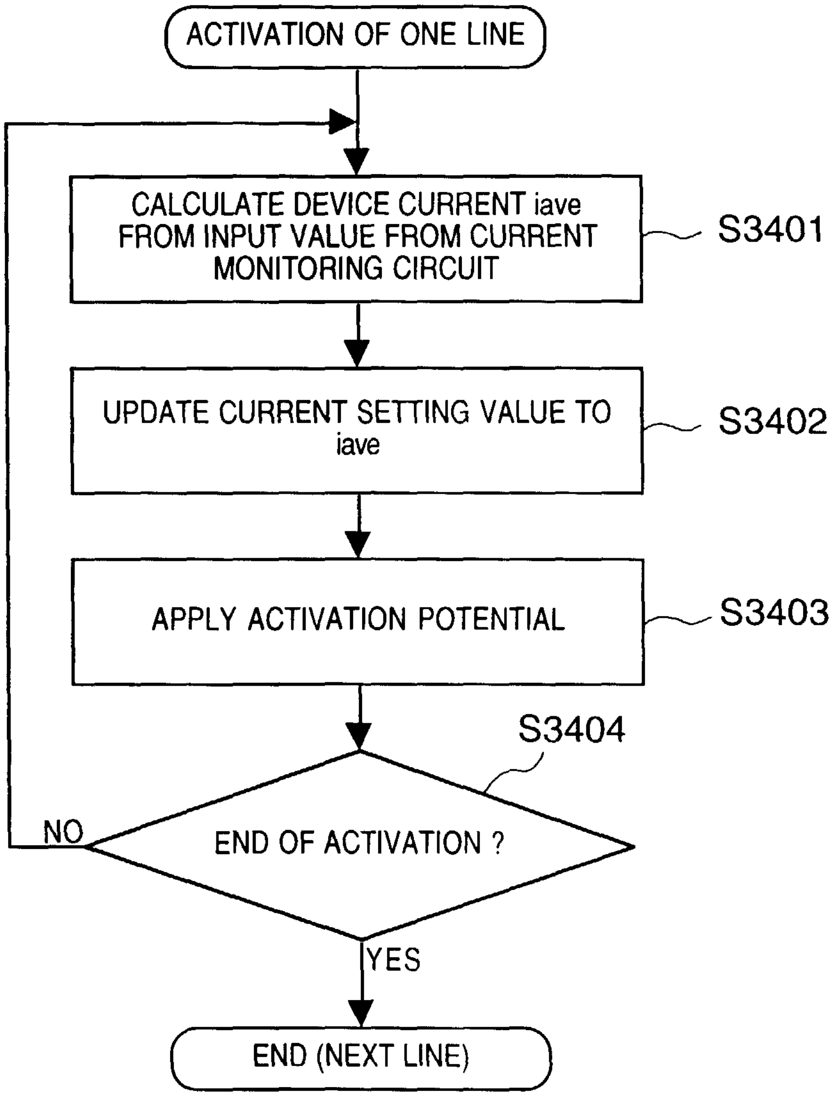
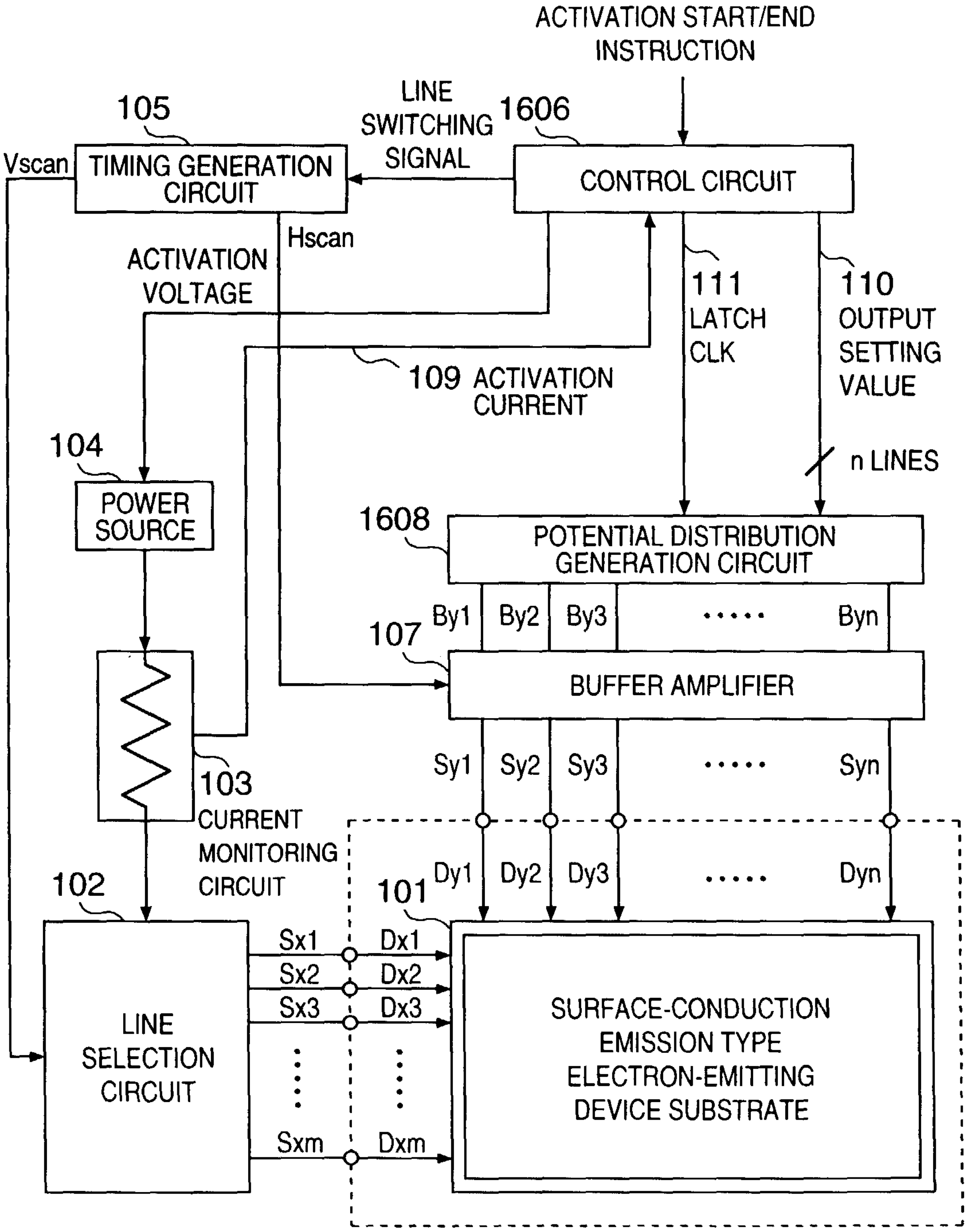

ACTIVATION OF ONE LINE
CALCULATE DEVICE CURRENT iave FROM INPUT VALUE FROM CURRENT MONITORING CIRCUIT
S3401
UPDATE CURRENT SETTING VALUE TO iave
S3402
APPLY ACTIVATION POTENTIAL
S3403
S3404
END OF ACTIVATION ?
NO
YES
END (NEXT LINE)

FIG. 16


ACTIVATION START/END INSTRUCTION
105
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
1606
CONTROL CIRCUIT
Vscan
Hscan
ACTIVATION VOLTAGE
111
LATCH CLK
110
OUTPUT SETTING VALUE
109 ACTIVATION CURRENT
n LINES
104
POWER SOURCE
1608
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
107
By1
By2
By3
.....
Byn
BUFFER AMPLIFIER
Sy1
Sy2
Sy3
.....
Syn
103
CURRENT MONITORING CIRCUIT
102
101
Dy1
Dy2
Dy3
.....
Dyn
LINE SELECTION CIRCUIT
Sx1
Sx2
Sx3
Sxm
Dx1
Dx2
Dx3
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

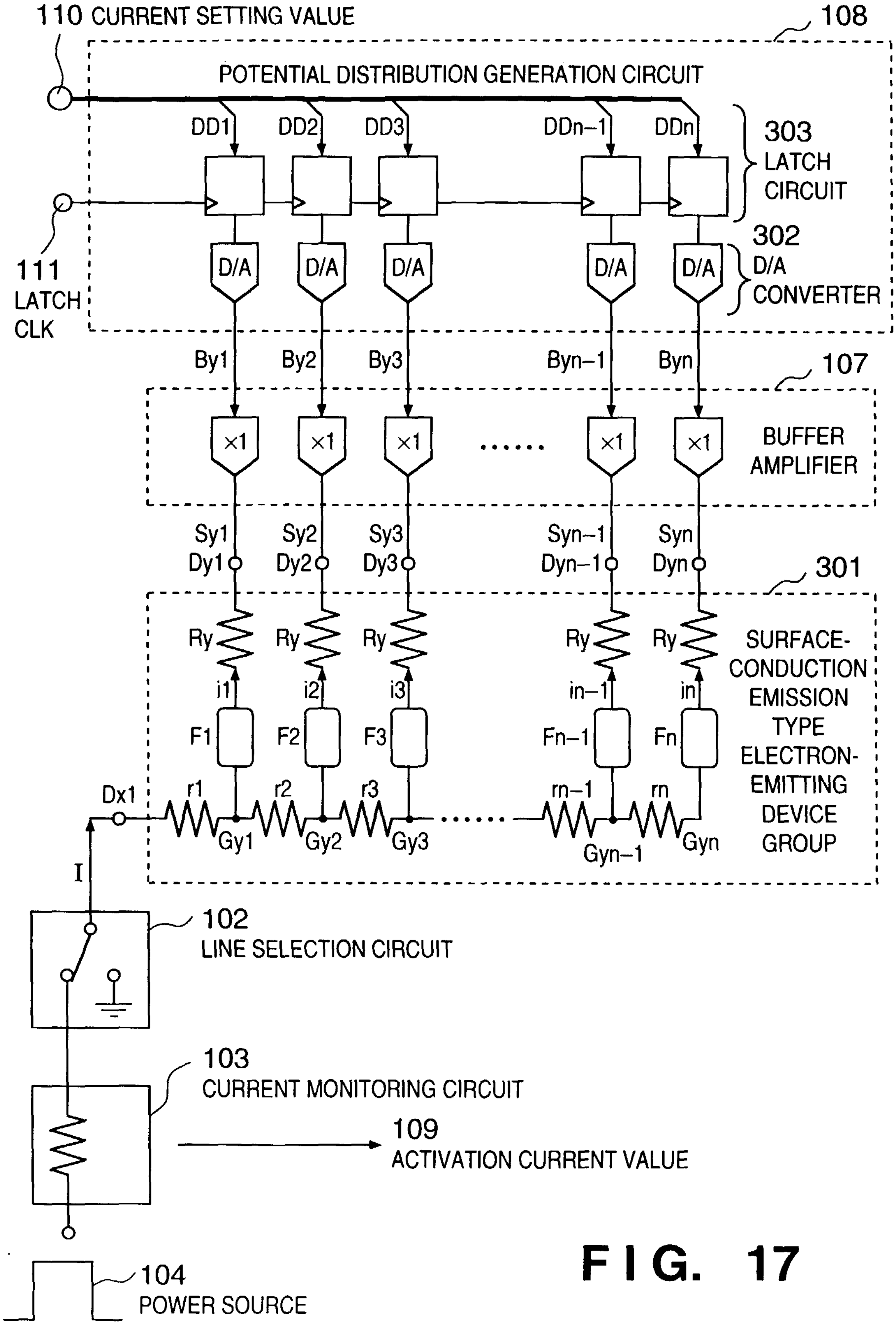

110 CURRENT SETTING VALUE
108
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
DD1
DD2
DD3
DDn−1
DDn
303 LATCH CIRCUIT
111 LATCH CLK
D/A
302 D/A CONVERTER
By1
By2
By3
Byn−1
Byn
107
×1
......
BUFFER AMPLIFIER
Sy1 Dy1
Sy2 Dy2
Sy3 Dy3
Syn−1 Dyn−1
Syn Dyn
301
Ry
i1
i2
i3
in−1
in
F1
F2
F3
Fn−1
Fn
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE GROUP
Dx1
r1
r2
r3
rn−1
rn
Gy1
Gy2
Gy3
Gyn−1
Gyn
I
102 LINE SELECTION CIRCUIT
103 CURRENT MONITORING CIRCUIT
109 ACTIVATION CURRENT VALUE
104 POWER SOURCE

FIG. 17

F I G. 18

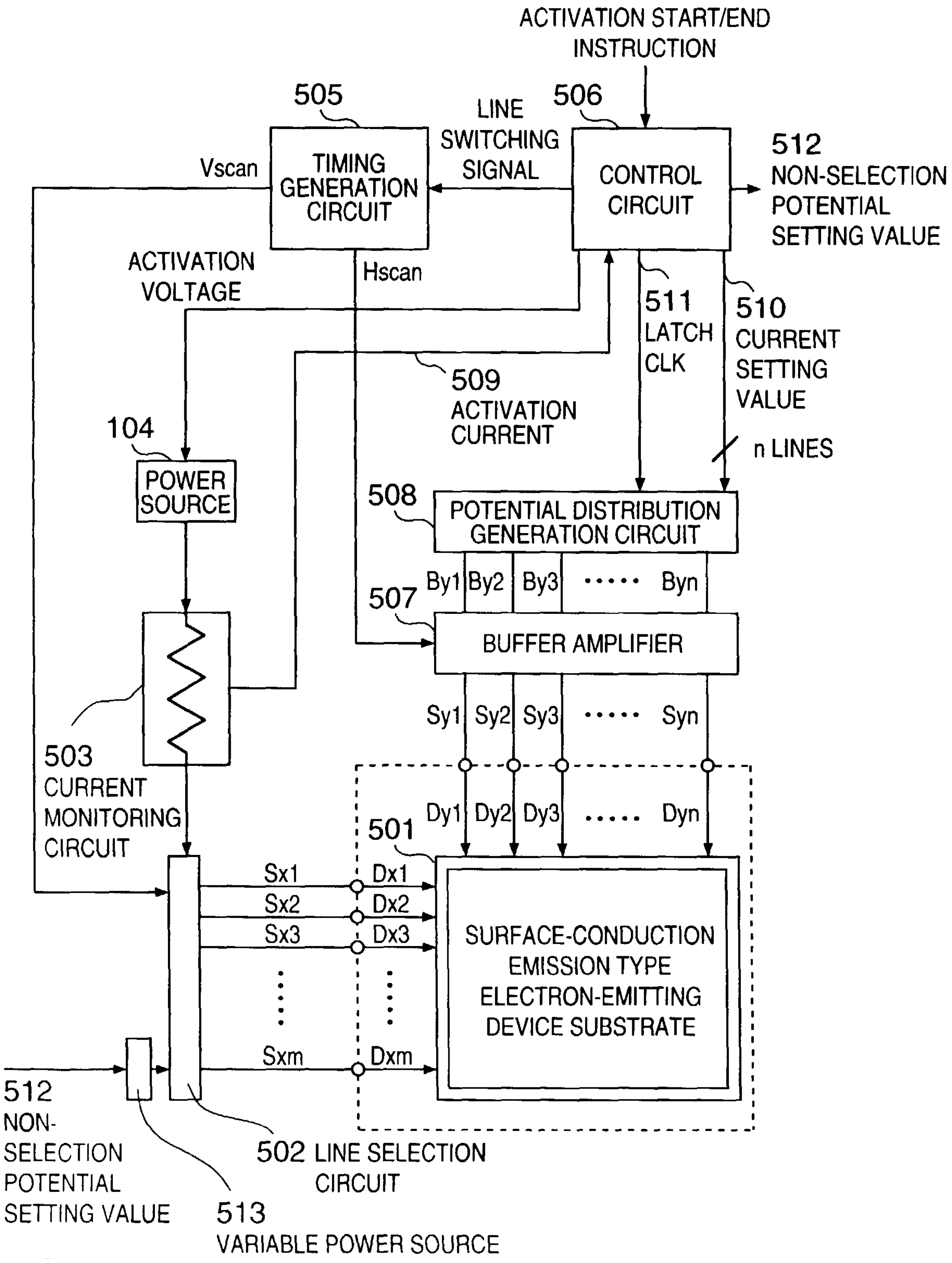

ACTIVATION START/END INSTRUCTION
505
TIMING GENERATION CIRCUIT
LINE SWITCHING SIGNAL
506
CONTROL CIRCUIT
512
NON-SELECTION POTENTIAL SETTING VALUE
Vscan
Hscan
ACTIVATION VOLTAGE
511
LATCH CLK
510
CURRENT SETTING VALUE
509
ACTIVATION CURRENT
n LINES
104
POWER SOURCE
508
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
By1
By2
By3
Byn
507
BUFFER AMPLIFIER
Sy1
Sy2
Sy3
Syn
503
CURRENT MONITORING CIRCUIT
501
Dy1
Dy2
Dy3
Dyn
Sx1
Sx2
Sx3
Sxm
Dx1
Dx2
Dx3
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE
512
NON-SELECTION POTENTIAL SETTING VALUE
502 LINE SELECTION CIRCUIT
513
VARIABLE POWER SOURCE

FIG. 19

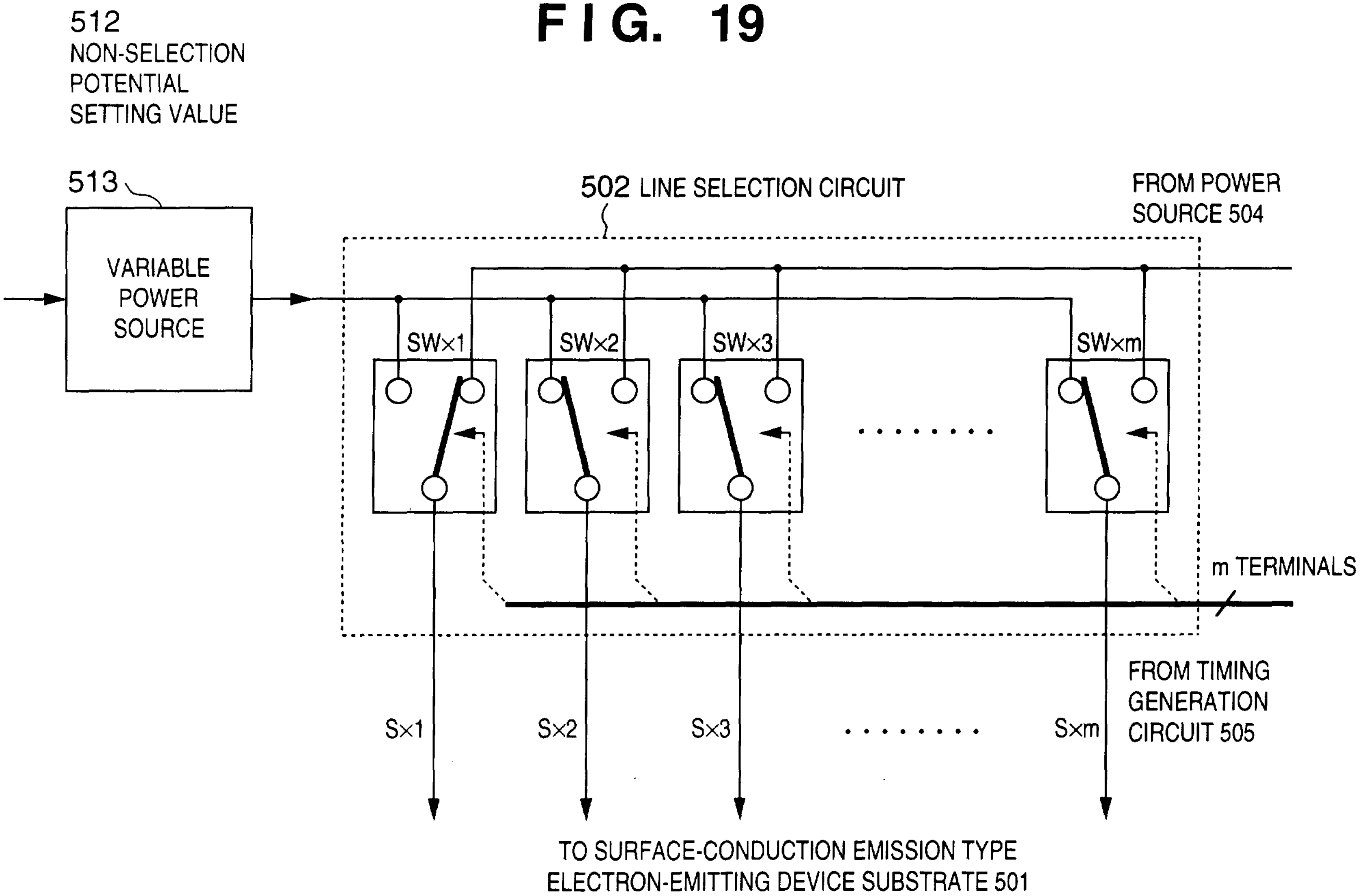

512
NON-SELECTION
POTENTIAL
SETTING VALUE
513
VARIABLE
POWER
SOURCE
502 LINE SELECTION CIRCUIT
FROM POWER
SOURCE 504
SWx1
SWx2
SWx3
SWxm
m TERMINALS
FROM TIMING
GENERATION
CIRCUIT 505
Sx1
Sx2
Sx3
Sxm
TO SURFACE-CONDUCTION EMISSION TYPE
ELECTRON-EMITTING DEVICE SUBSTRATE 501

FIG. 20A

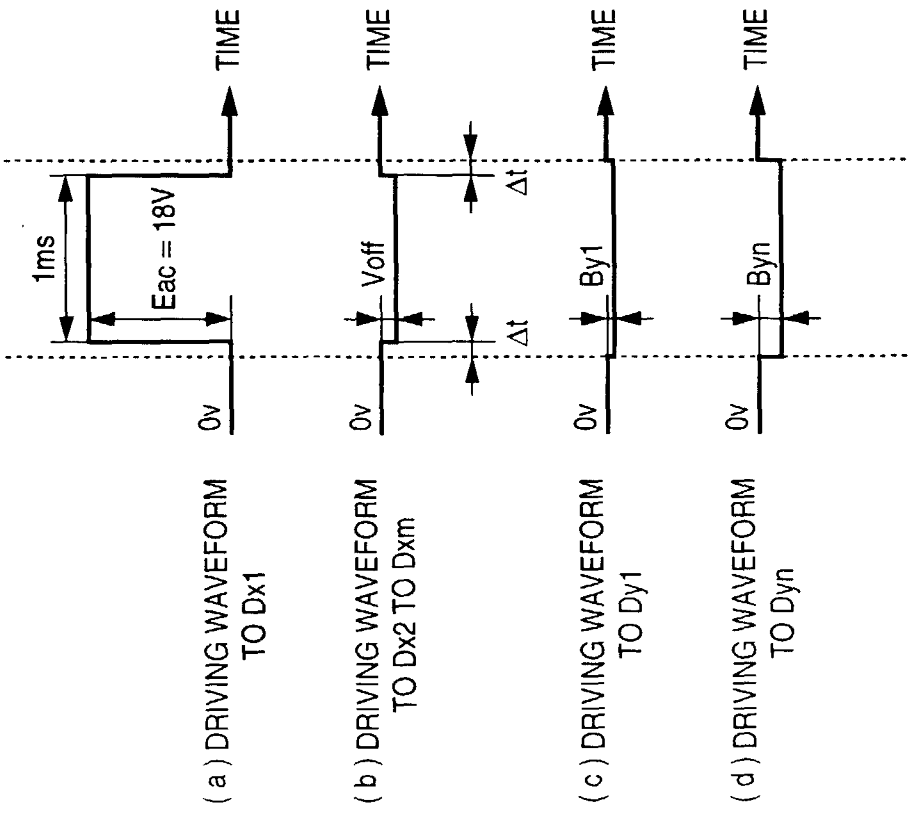


FIG. 20B

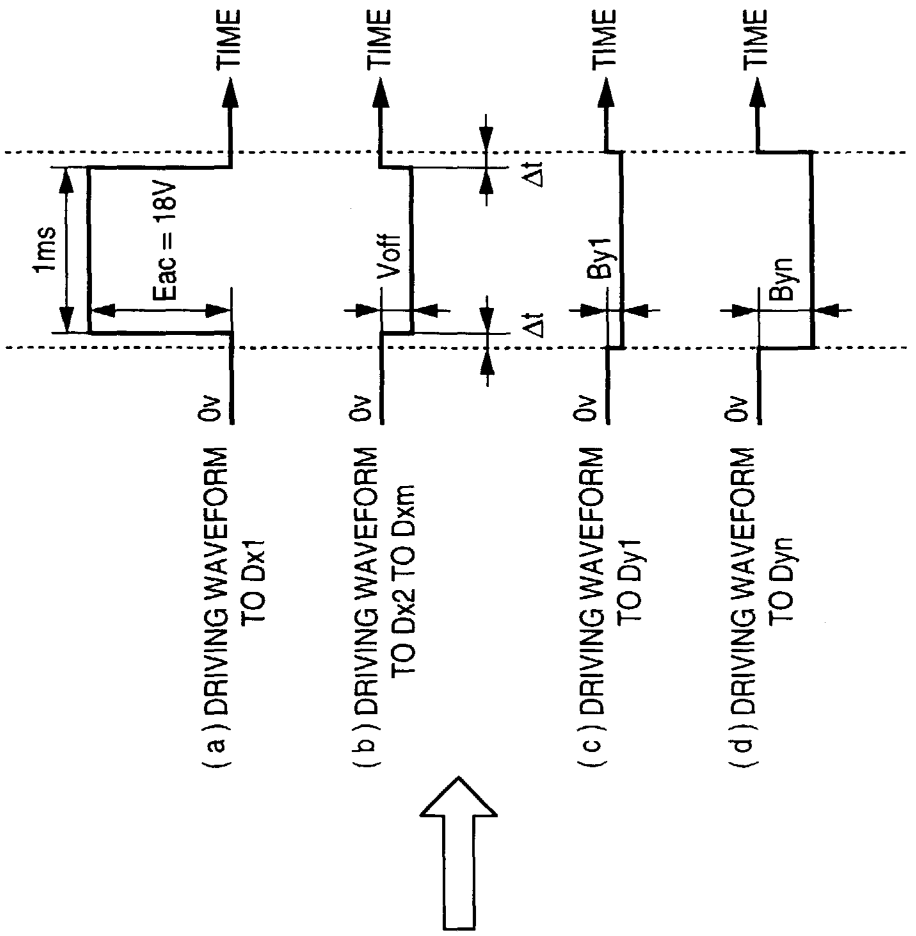


FIG. 21

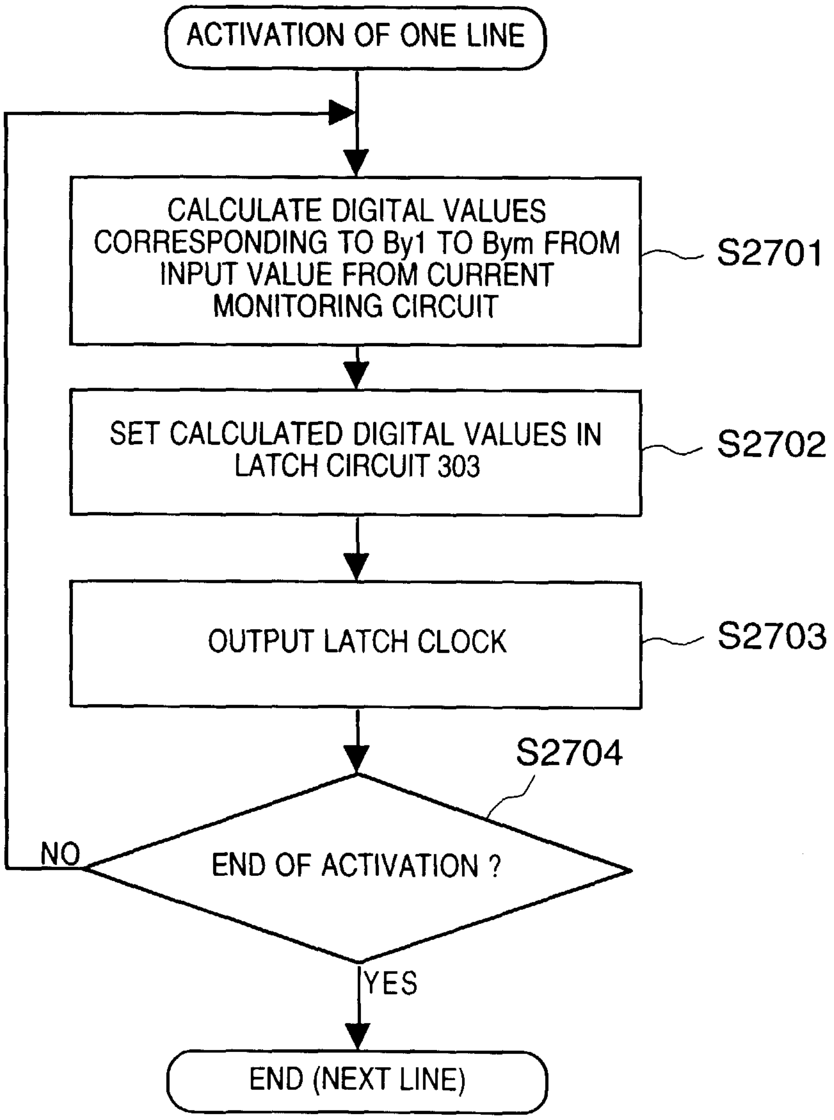
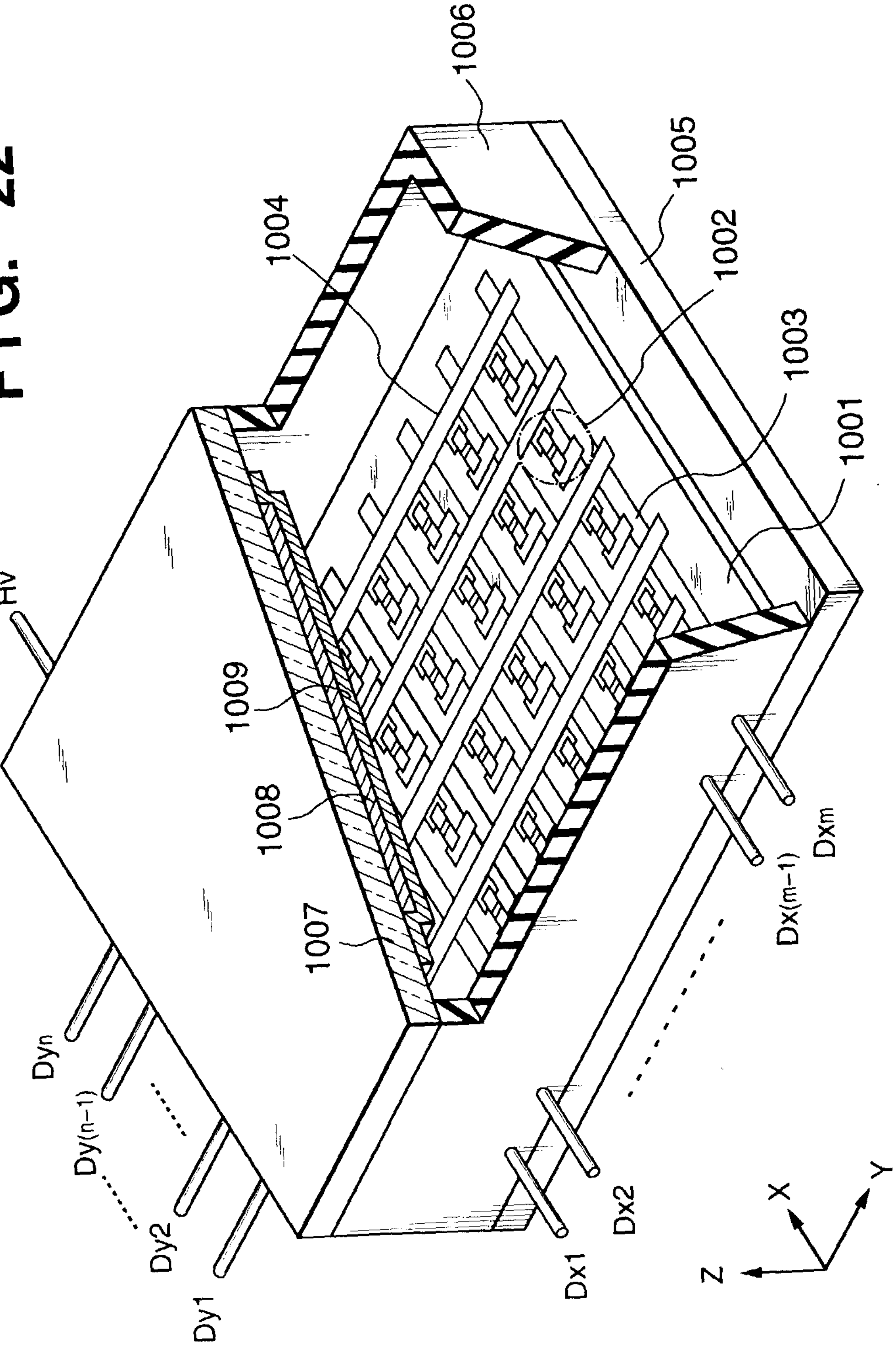
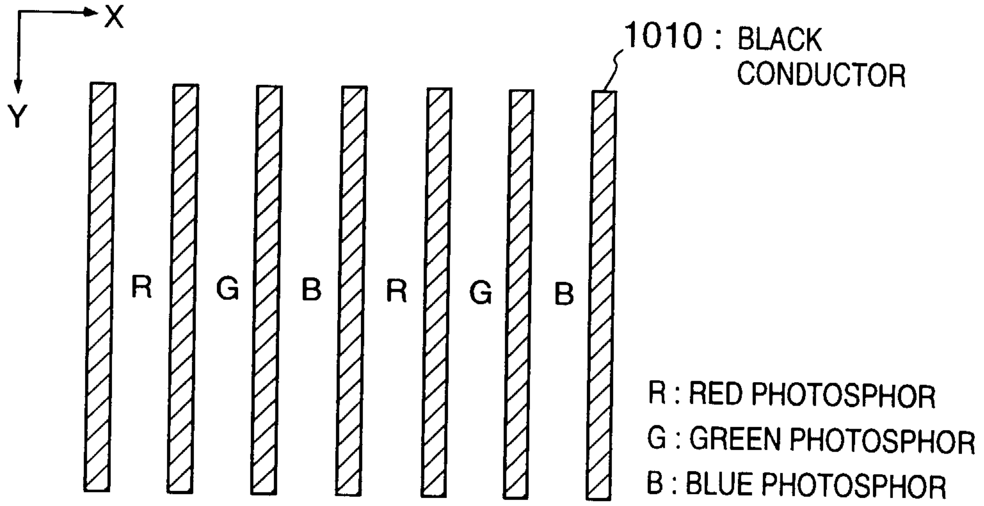

ACTIVATION OF ONE LINE
CALCULATE DIGITAL VALUES CORRESPONDING TO By1 TO Bym FROM INPUT VALUE FROM CURRENT MONITORING CIRCUIT
S2701
SET CALCULATED DIGITAL VALUES IN LATCH CIRCUIT 303
S2702
OUTPUT LATCH CLOCK
S2703
S2704
END OF ACTIVATION ?
NO
YES
END (NEXT LINE)

FIG. 22


1006
1005
1004
1002
1003
1001
Hv
1009
1008
1007
Dyn
Dy(n−1)
Dy2
Dy1
Dx1
Dx2
Dx(m−1)
Dxm
X
Y
Z

F I G. 23A



F I G. 23B

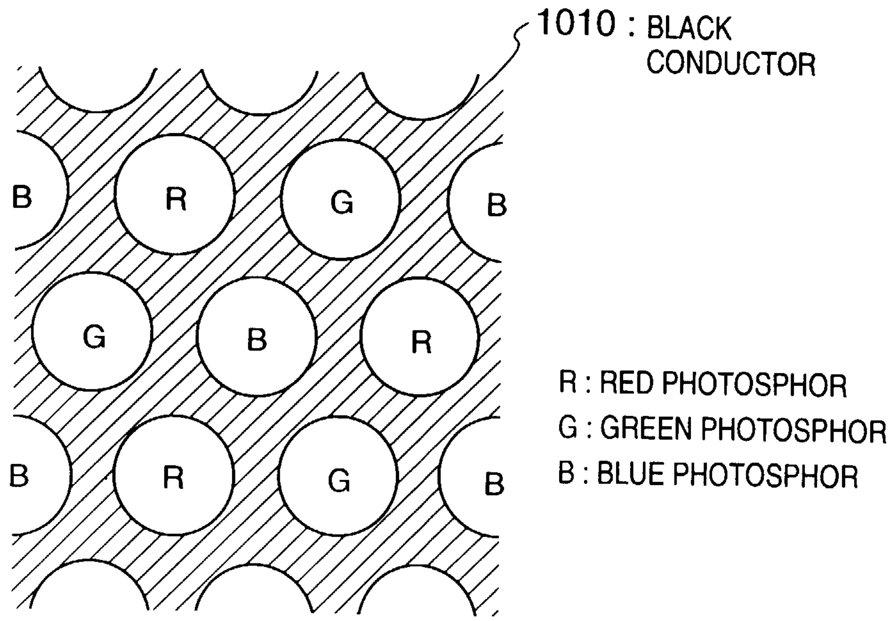


FIG. 24A

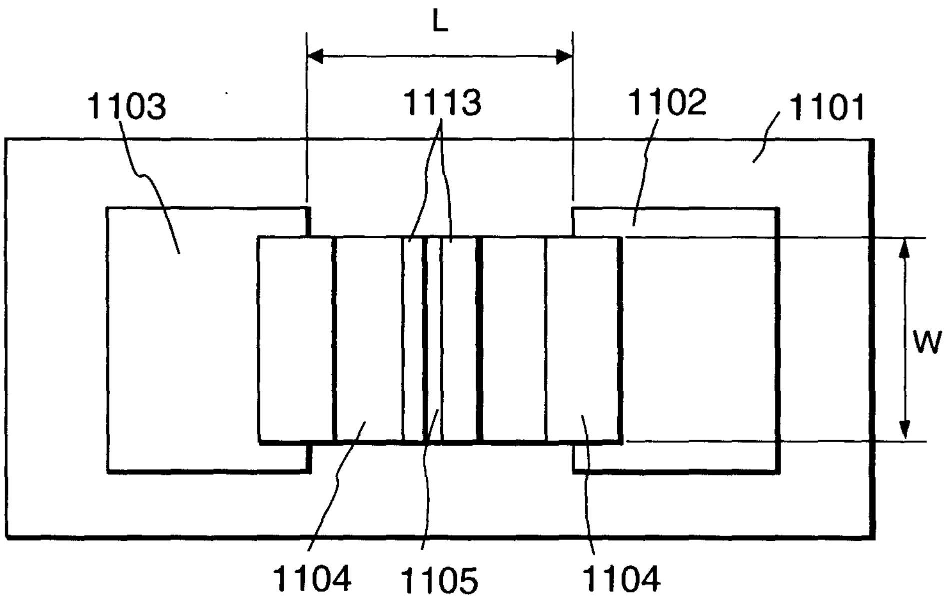


FIG. 24B

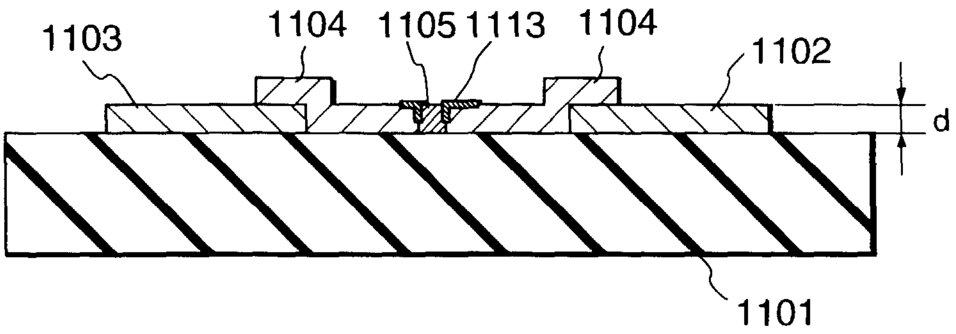


FIG. 25A

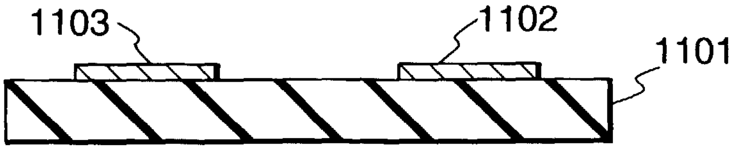


FIG. 25B

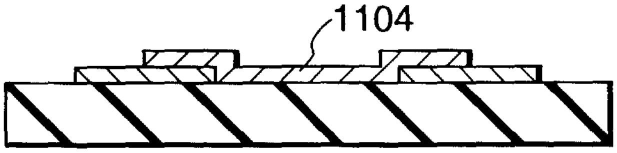


FIG. 25C

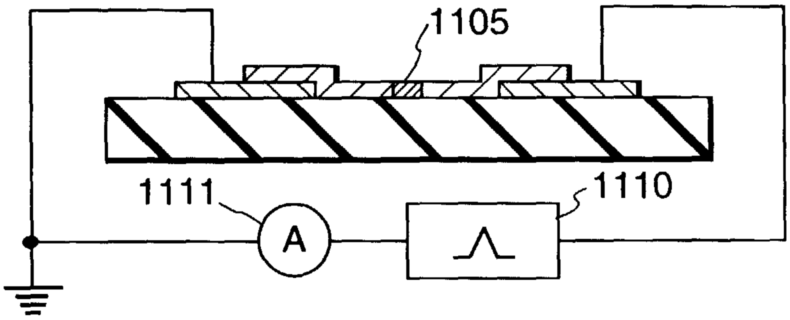


FIG. 25D

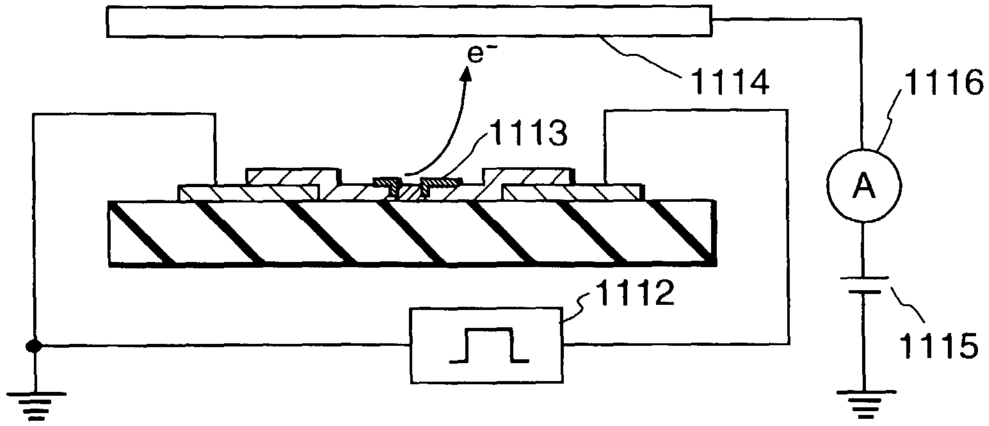
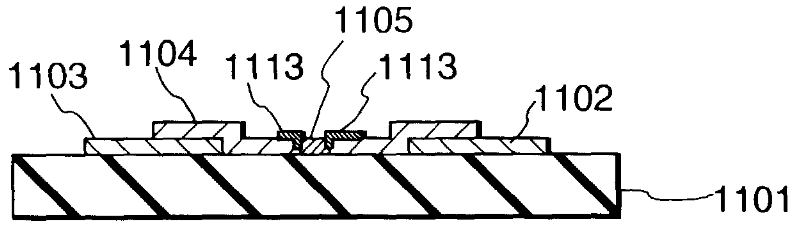


FIG. 25E



F I G. 26

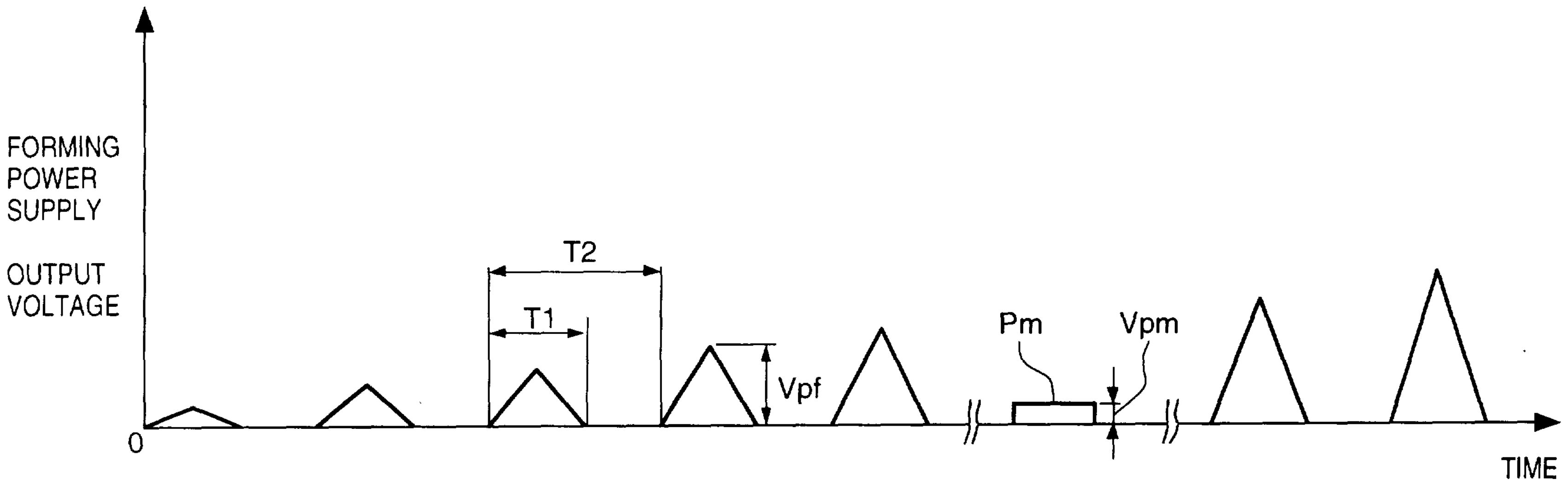


FIG. 27A

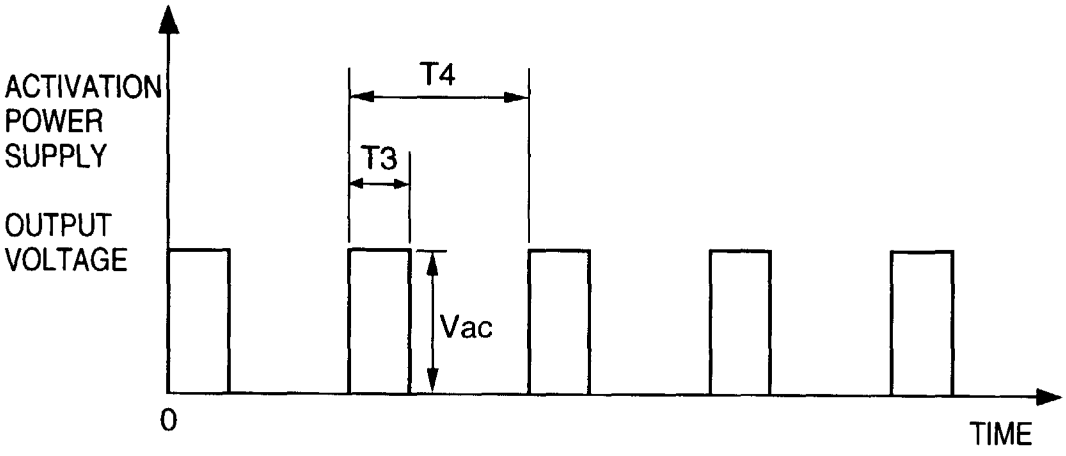
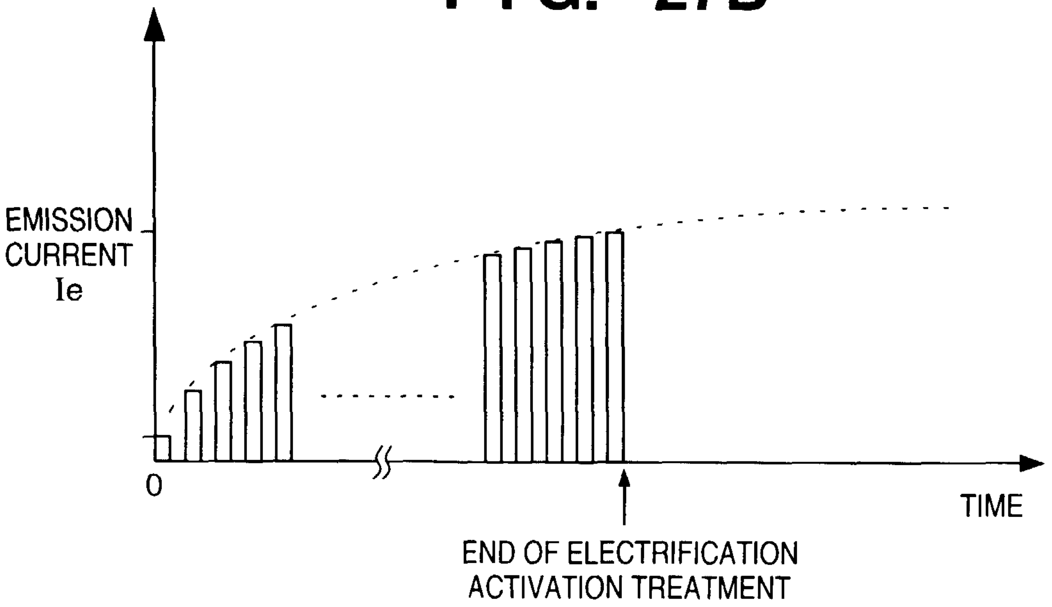


FIG. 27B



F I G. 28

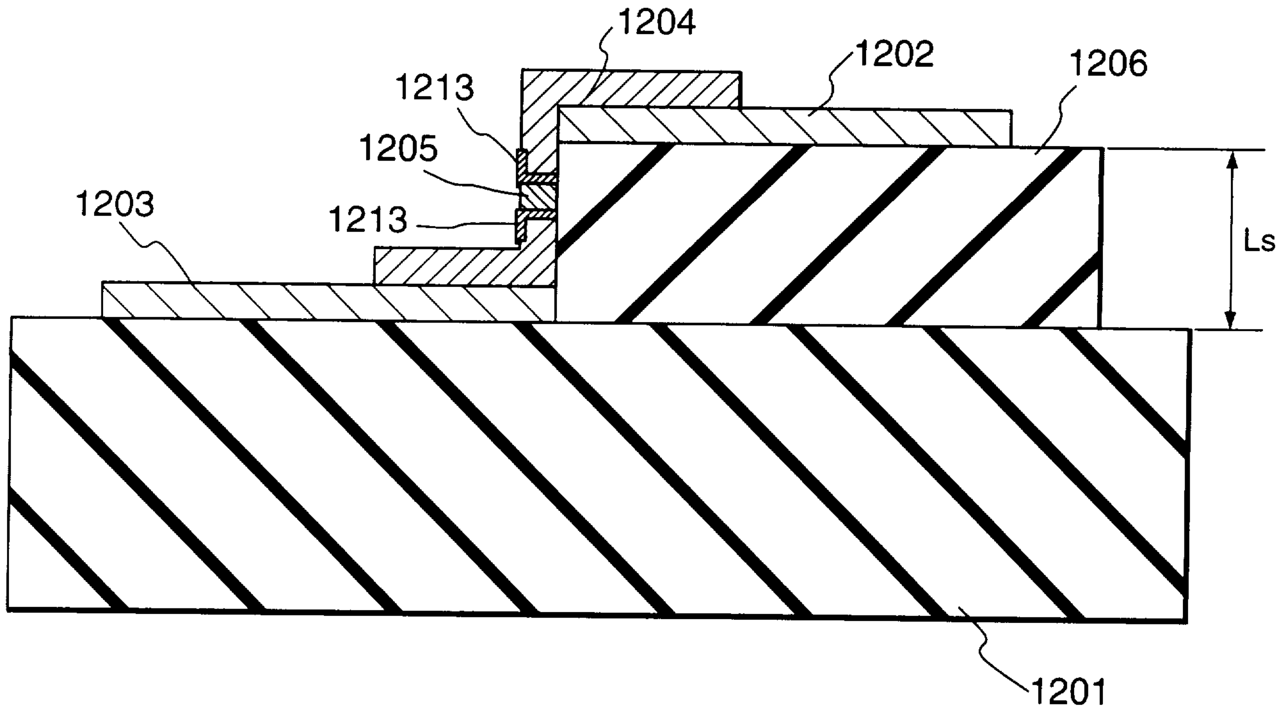


FIG. 29A

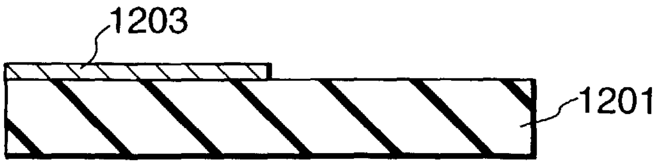


FIG. 29B

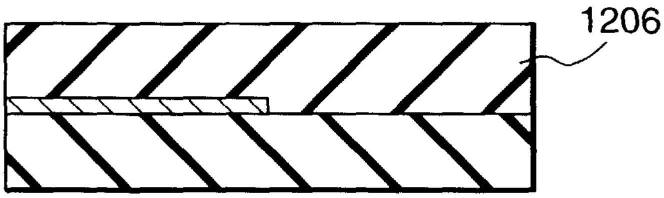


FIG. 29C

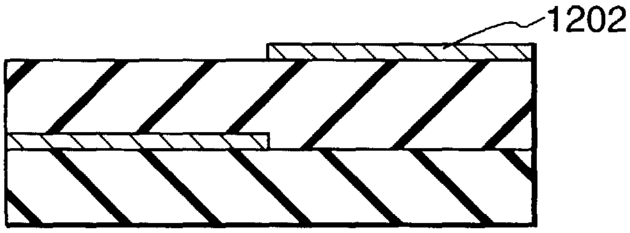


FIG. 29D

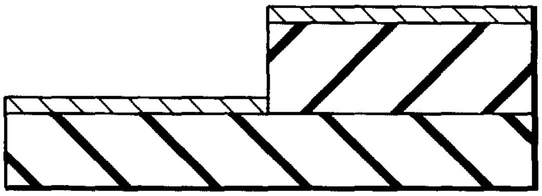


FIG. 29E

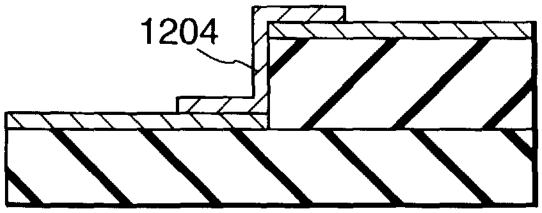


FIG. 29F

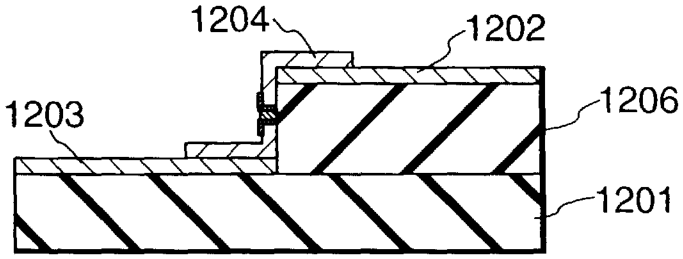


FIG. 30

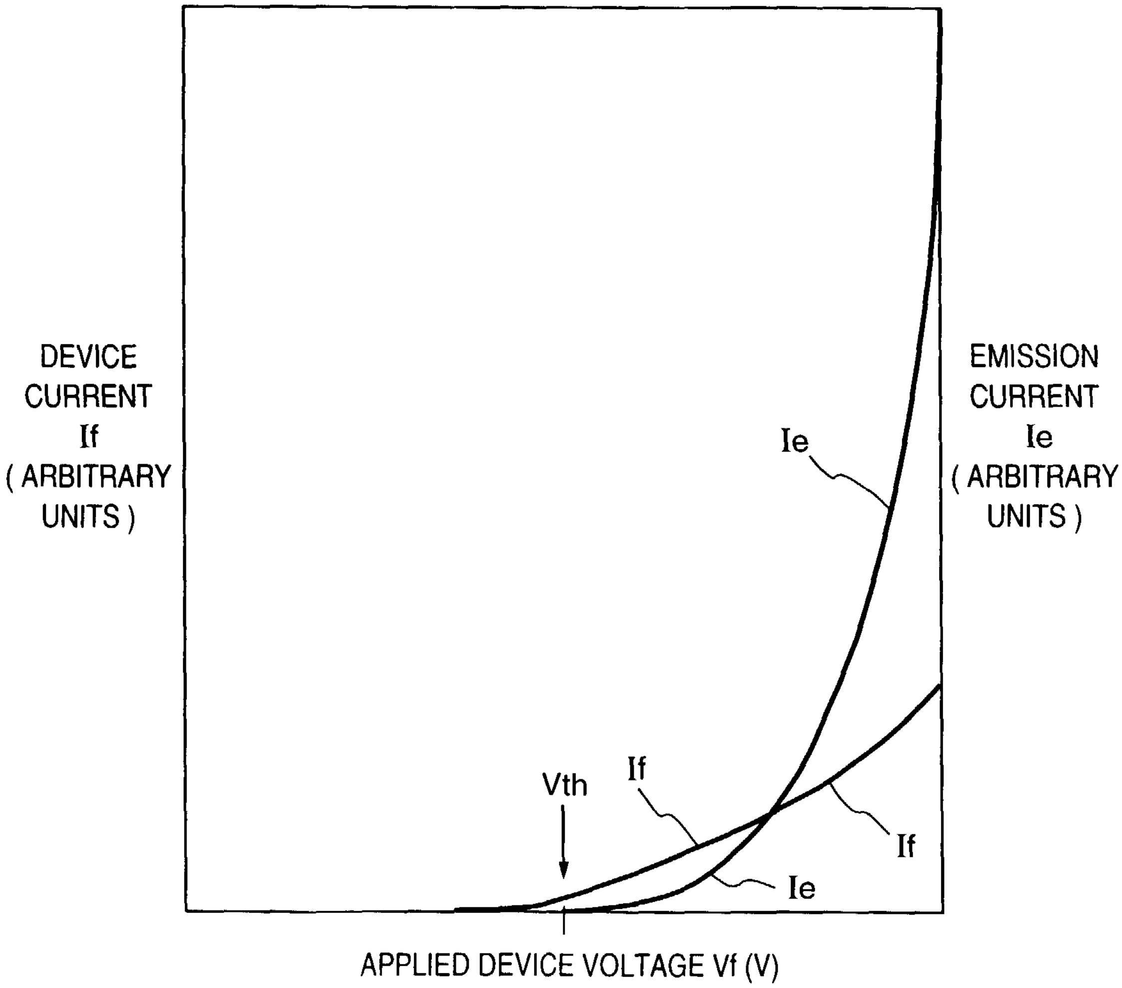

DEVICE
CURRENT
If
(ARBITRARY
UNITS)
EMISSION
CURRENT
Ie
(ARBITRARY
UNITS)
Ie
Vth
If
If
Ie
APPLIED DEVICE VOLTAGE Vf (V)

FIG. 31

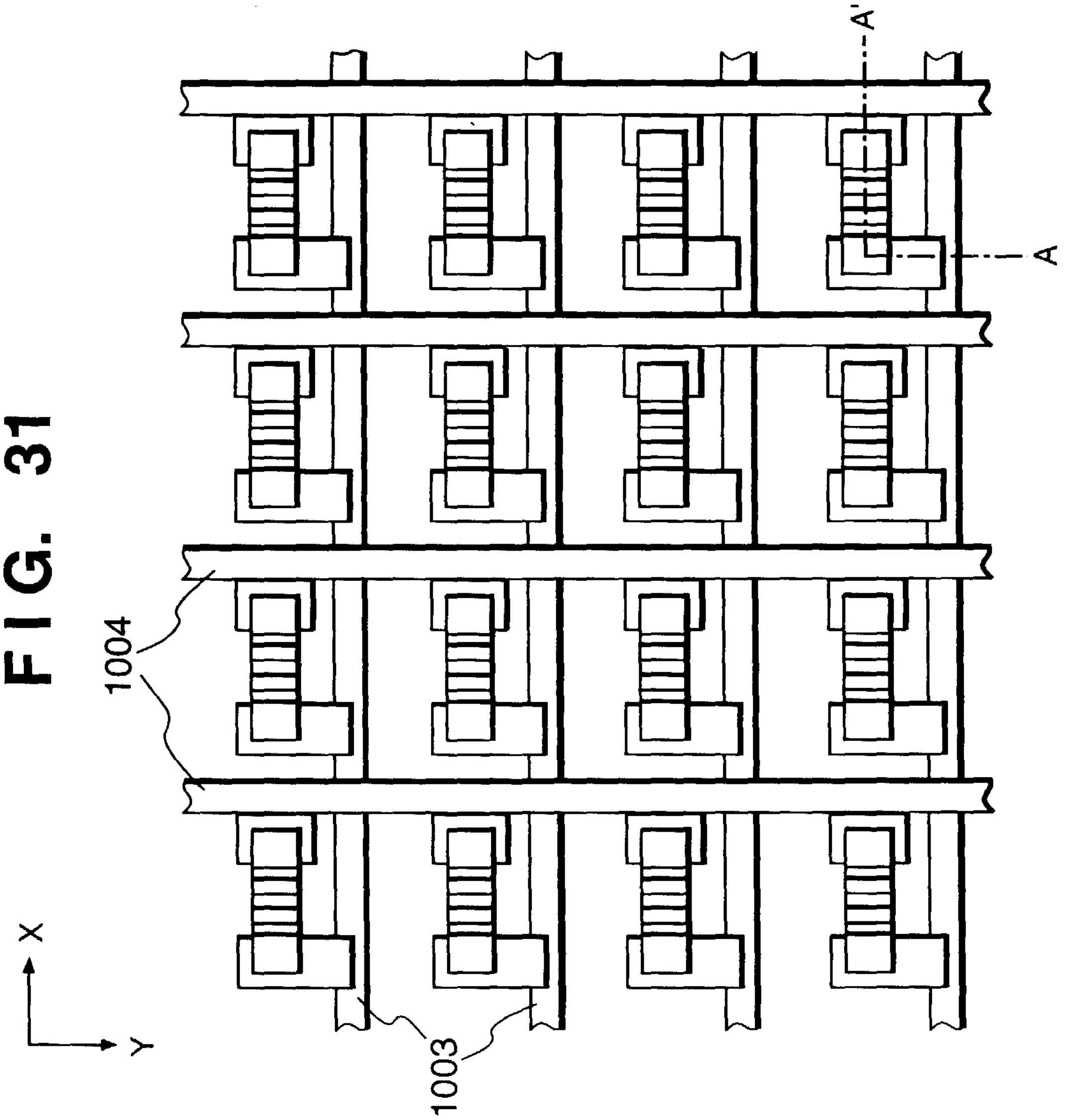
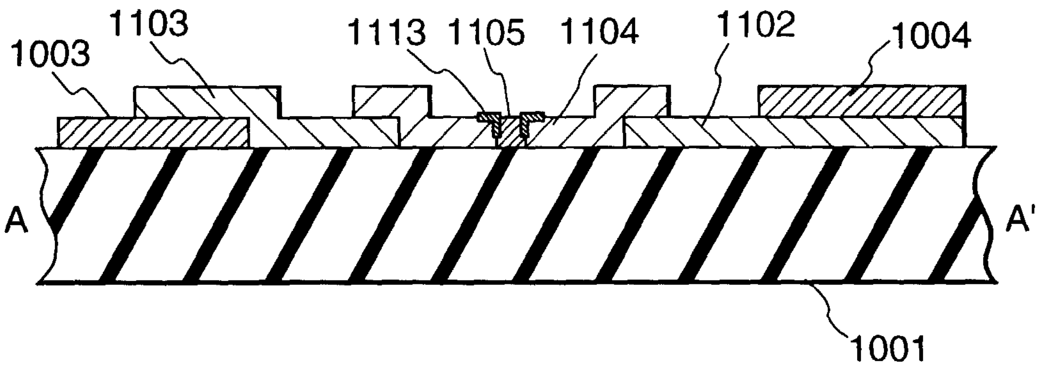
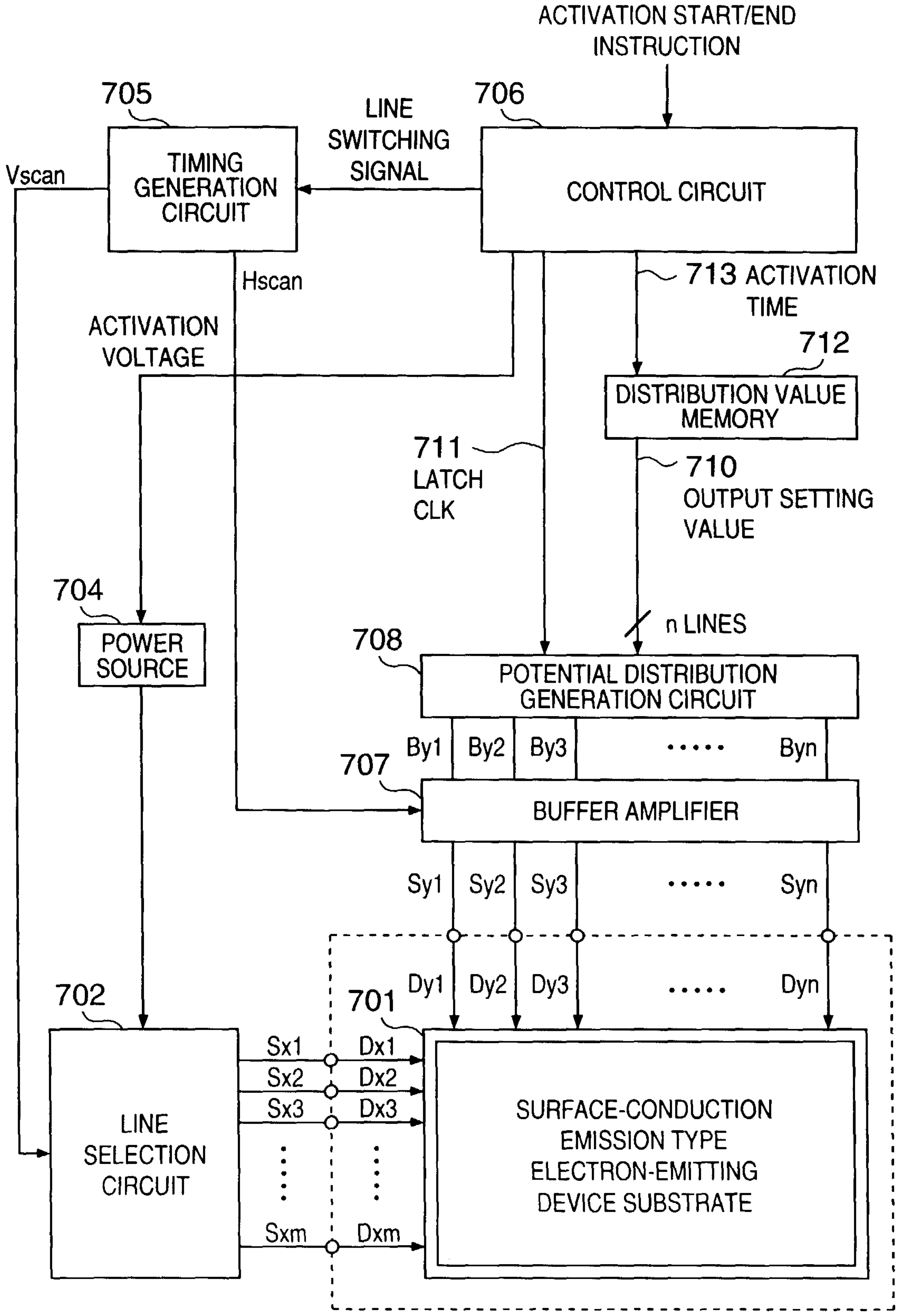


FIG. 32



F I G. 33


ACTIVATION START/END INSTRUCTION
705
TIMING GENERATION CIRCUIT
706
CONTROL CIRCUIT
LINE SWITCHING SIGNAL
Vscan
Hscan
ACTIVATION VOLTAGE
713 ACTIVATION TIME
712
DISTRIBUTION VALUE MEMORY
711
LATCH CLK
710
OUTPUT SETTING VALUE
704
POWER SOURCE
n LINES
708
POTENTIAL DISTRIBUTION GENERATION CIRCUIT
By1
By2
By3
Byn
707
BUFFER AMPLIFIER
Sy1
Sy2
Sy3
Syn
Dy1
Dy2
Dy3
Dyn
702
701
LINE SELECTION CIRCUIT
Sx1
Sx2
Sx3
Sxm
Dx1
Dx2
Dx3
Dxm
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE SUBSTRATE

F I G. 34

ADDRESS	COMPEN-SATION POTENTIAL FOR TERMINAL Dy1 (V)	COMPEN-SATION POTENTIAL FOR TERMINAL Dy2 (V)	COMPEN-SATION POTENTIAL FOR TERMINAL Dy3 (V)	.	.	.	COMPEN-SATION POTENTIAL FOR TERMINAL Dyn–1 (V)	COMPEN-SATION POTENTIAL FOR TERMINAL Dyn (V)
t = 0	0	0	0	0	0	0	0	0
t=1 MIN	–0.1	–0.1	–0.1	.	.	.	–0.3	–0.3
.	.	.	.	.	.	.	.	.
t=29 MIN	–0.5	–0.5	–0.6	.	.	.	–3.0	–3.0

FIG. 35

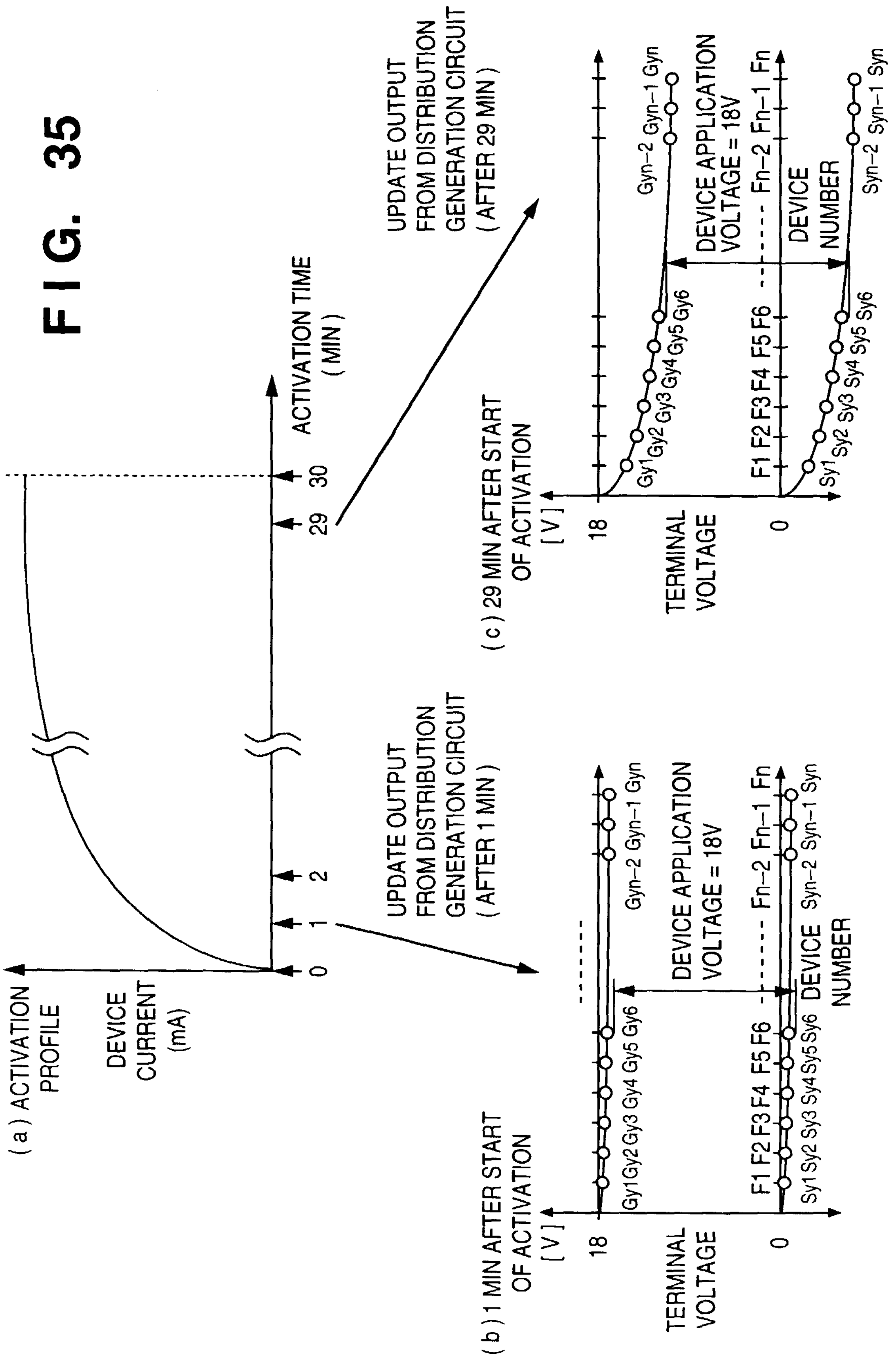
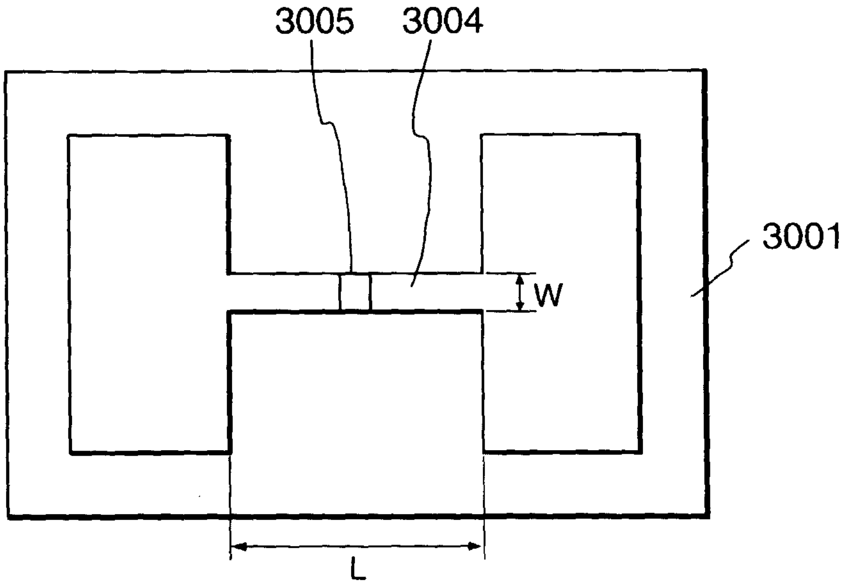

(a) ACTIVATION PROFILE
DEVICE CURRENT (mA)
ACTIVATION TIME (MIN)
0
1
2
29
30
UPDATE OUTPUT FROM DISTRIBUTION GENERATION CIRCUIT (AFTER 1 MIN)
UPDATE OUTPUT FROM DISTRIBUTION GENERATION CIRCUIT (AFTER 29 MIN)
(b) 1 MIN AFTER START OF ACTIVATION
(c) 29 MIN AFTER START OF ACTIVATION
[V]
18
0
TERMINAL VOLTAGE
DEVICE APPLICATION VOLTAGE = 18V
DEVICE NUMBER
F1 F2 F3 F4 F5 F6 Fn–2 Fn–1 Fn
Gy1 Gy2 Gy3 Gy4 Gy5 Gy6 Gyn–2 Gyn–1 Gyn
Sy1 Sy2 Sy3 Sy4 Sy5 Sy6 Syn–2 Syn–1 Syn

FIG. 36



F I G. 37

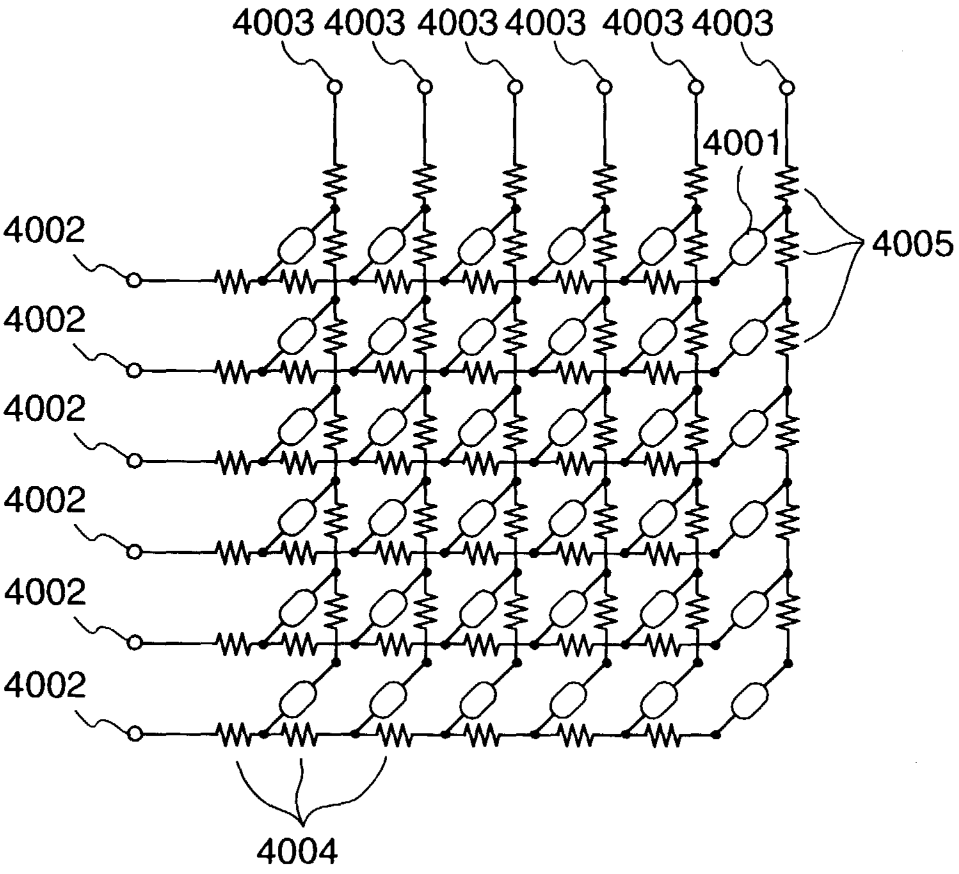
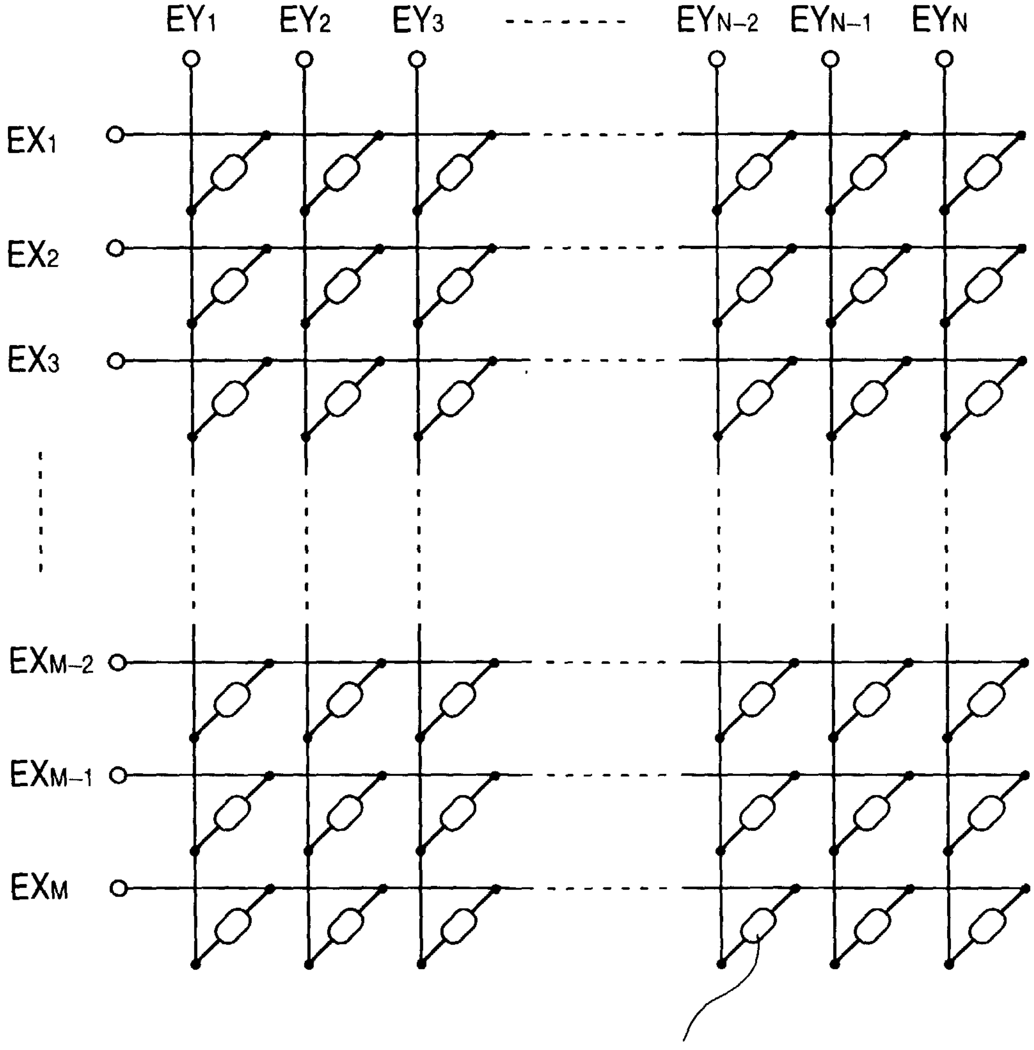

4003
4003
4003
4003
4003
4003
4001
4005
4002
4002
4002
4002
4002
4002
4004

FIG. 38


EY1
EY2
EY3
EYN-2
EYN-1
EYN
EX1
EX2
EX3
EXM-2
EXM-1
EXM
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE

F I G. 39

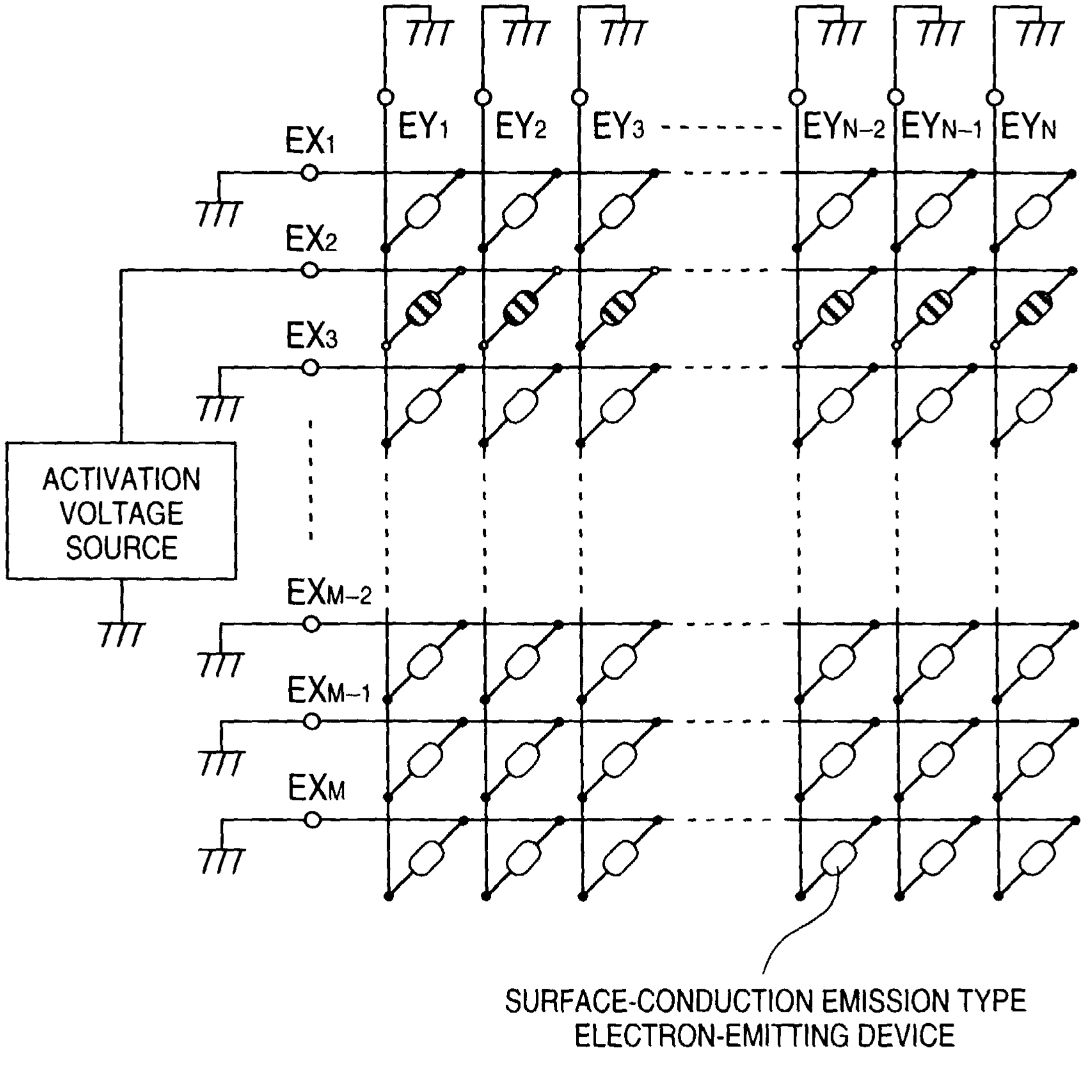

EY1
EY2
EY3
EYN-2
EYN-1
EYN
EX1
EX2
EX3
EXM-2
EXM-1
EXM
ACTIVATION VOLTAGE SOURCE
SURFACE-CONDUCTION EMISSION TYPE ELECTRON-EMITTING DEVICE

FIG. 40A

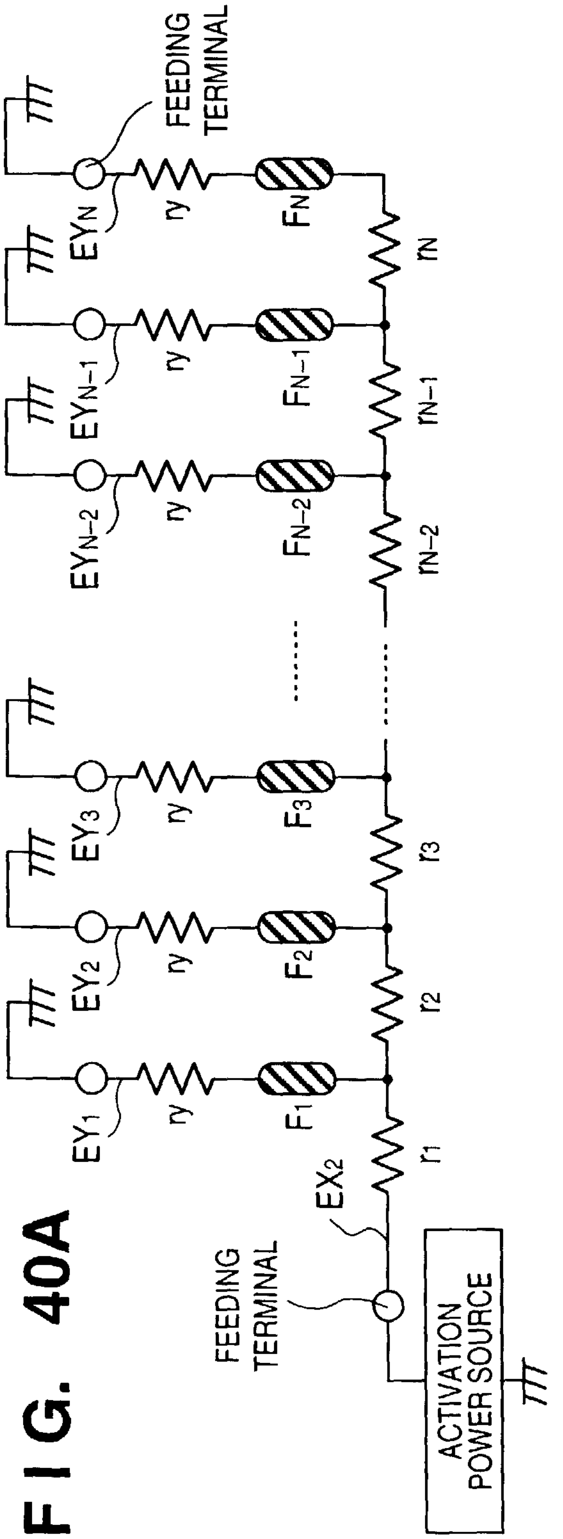
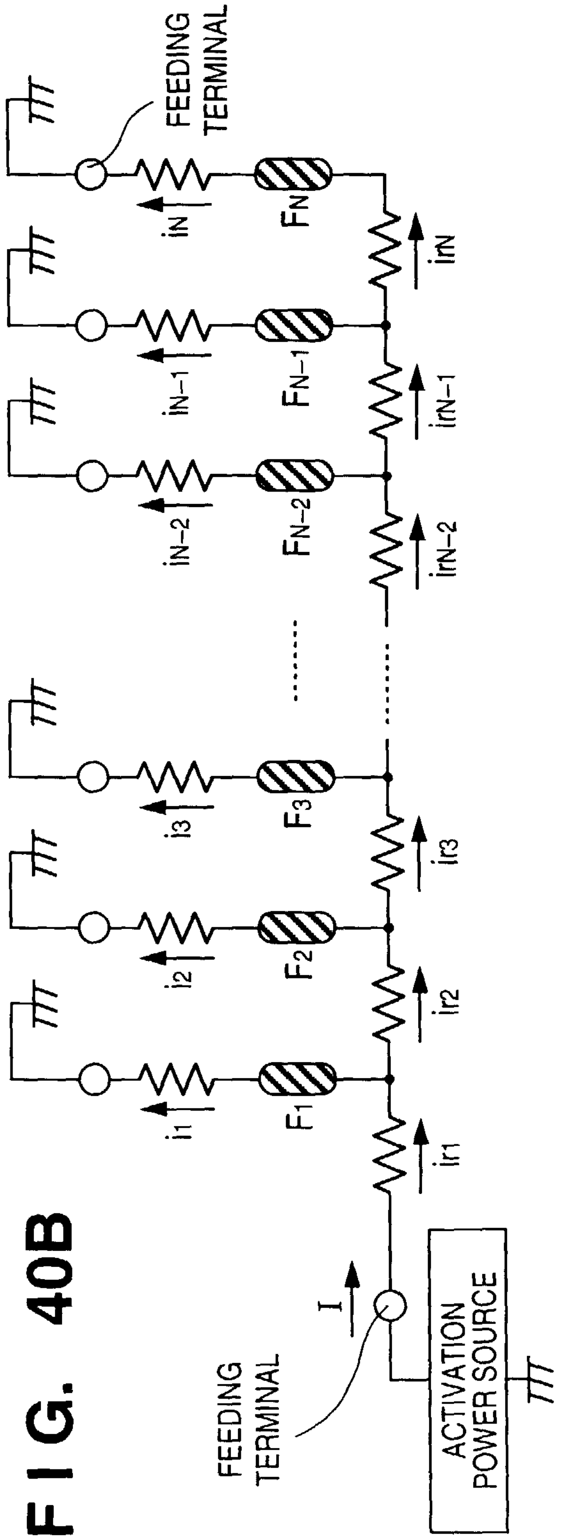
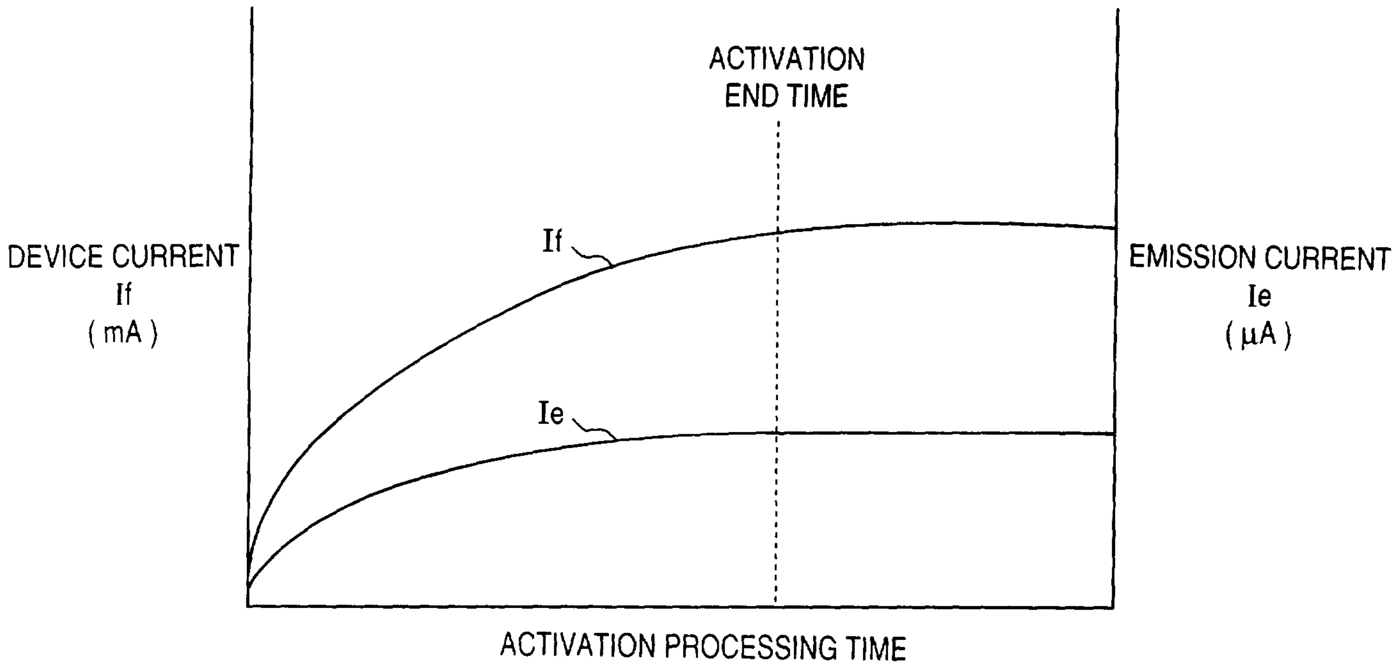


FIG. 40B



F I G. 41


ACTIVATION
END TIME
If
Ie
DEVICE CURRENT
If
(mA)
EMISSION CURRENT
Ie
(µA)
ACTIVATION PROCESSING TIME

F I G. 42

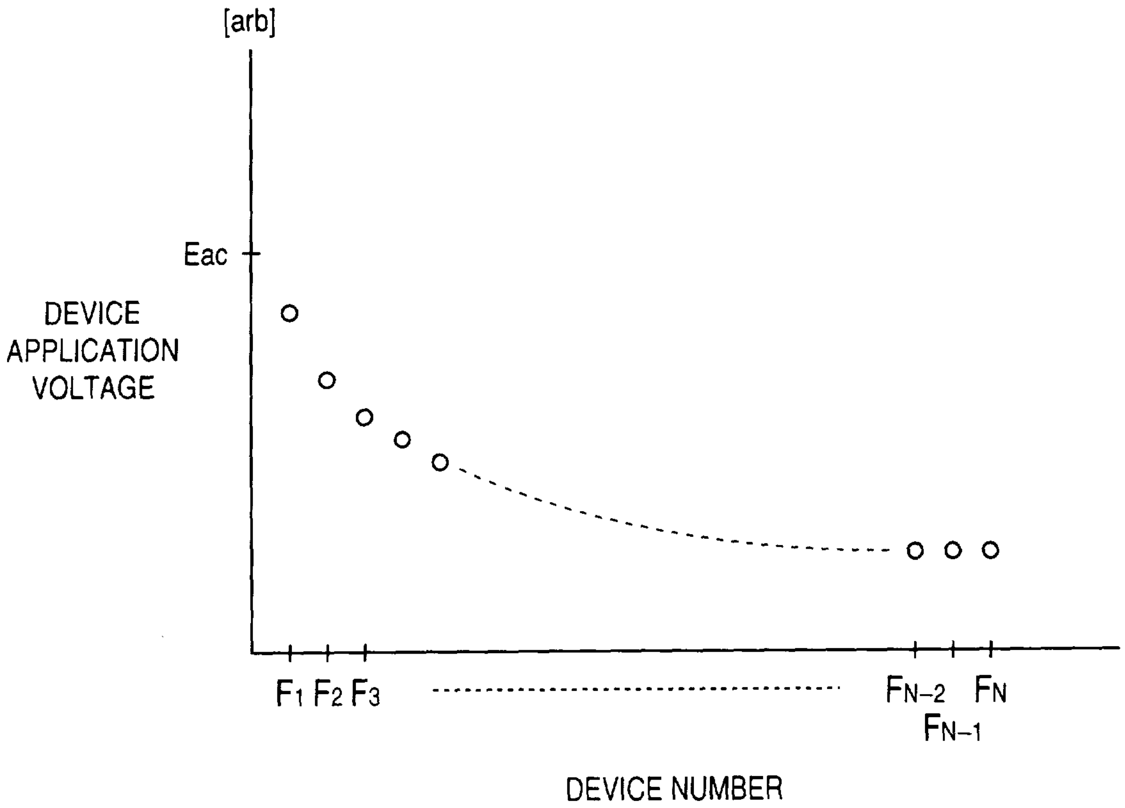

[arb]
Eac
DEVICE
APPLICATION
VOLTAGE
F_1 F_2 F_3
F_{N-2} F_N
F_{N-1}
DEVICE NUMBER

FIG. 43A

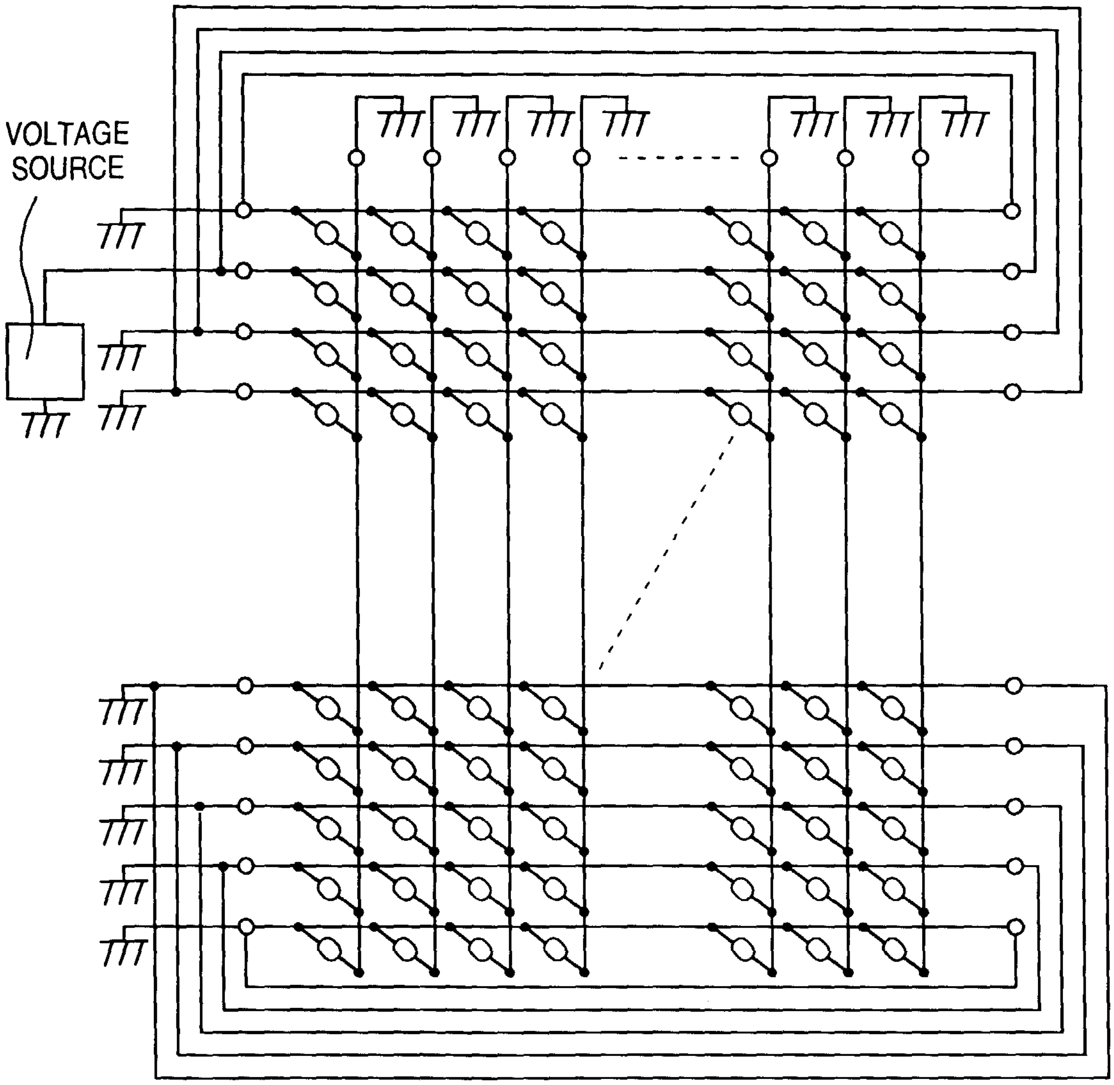


FIG. 43B