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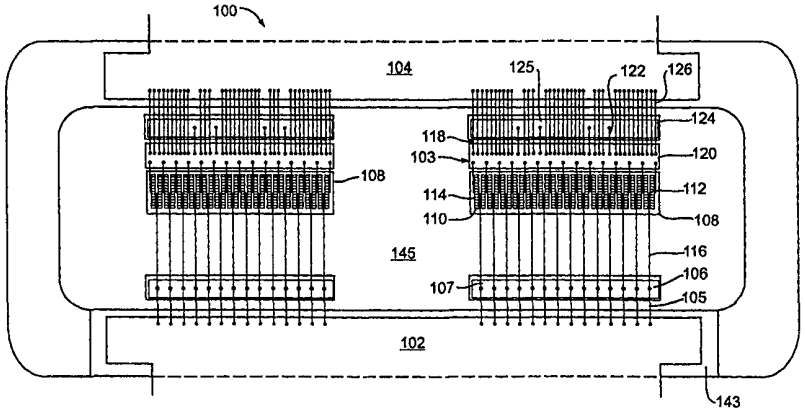
(54) Title: HIGH FREQUENCY POWER TRANSISTOR DEVICE



(57) Abstract

An output-matched LDMOS RF power transistor device (100) includes a semiconductor die (108) having a plurality of interdigitated electrodes (110) formed thereon, the electrodes each having respective input terminals (112) and output terminals (114). An input lead is coupled to a first terminal (107) of an input matching capacitor (106) by a first plurality of conductors (105) (e.g. bond wires), with a second terminal of the matching capacitor coupled to a ground (145). The first terminal of the matching capacitor is also coupled to the electrode input terminals by a second plurality of conductors (116). A conductive island (120) isolated from the ground is coupled to the electrode output terminals by a third plurality of conductors (118). Output matching of the device is provided by a shunt inductance (122) formed by a fourth plurality of conductors (122), which couple a first terminal of an output blocking capacitor (124) the conductive island, with a second terminal of the blocking capacitor coupled to the ground. An output lead is coupled to the conductive island by a fifth plurality of conductors (126). In particular, the conductive island is disposed adjacent the semiconductor die, and output blocking capacitor is disposed between the conductive island and output lead, such that transmission inductance through the respective third and fourth pluralities of conductors coupling the electrode output terminals to the blocking capacitor is sufficiently small to allow for output impedance matching of the transistor device at relatively high operating frequencies.

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DESCRIPTION

HIGH FREQUENCY POWER TRANSISTOR DEVICE

Background Of The Invention

1. Field of the Invention

The present invention pertains generally to the field of radio frequency power transistors, and more specifically to methods and apparatus for output impedance matching of an LDMOS power transistor device.

2. Background

The use of radio frequency (RF) amplifiers, for example, in wireless communication networks, is well known. With the considerable recent growth in the demand for wireless services, such as personal communication services (PCS), the operating frequency of wireless networks has increased dramatically and is now well into the gigahertz (GHz) frequencies. At such high frequencies, LDMOS transistors have been preferred for RF power amplification devices, e.g., in antenna base stations.

In a typical deployment, an LDMOS RF power transistor device generally comprises a plurality of electrodes formed on a silicon die, each electrode comprising a plurality of interdigitated transistors. The individual transistors of each electrode are connected to respective common input (gate) and output (drain) terminals for each electrode. The die is attached, by a known eutectic die attach process, atop a metallic (source) substrate, which is itself mounted to a metal flange serving as both a heat sink and a ground reference. Respective input (gate) and output (drain) lead frames are attached to the sides of the flange, electrically isolated from the metal (source) substrate, wherein the input and output lead frames are coupled to the respective electrode input and output terminals on the silicon die by multiple wires (i.e., bonded to the respective terminals and lead frames).

Impedance matching the input and output electrode terminals to the respective input and output lead frames is crucial to proper operation of the amplifier device, especially at high operating frequencies.

By way of illustration, FIG. 1 shows a simplified electrical schematic of an unmatched LDMOS device, having an input (gate) lead 12, an output (drain) lead 14 and a source 16 through an underlying substrate. Transmission inductance through the input path, e.g., a plurality of bond wires connecting the input lead 12 to the common input terminal of the respective transistor fingers, is represented by inductance 18. Output

inductance through the output path, e.g., a plurality of bond wires connecting the common output terminal of the respective transistors to the output lead 14, is represented by inductance 20.

FIG. 2 shows a known (matched) LDMOS power transistor device 40. The device 40 includes an input (gate) lead 42, output (drain) lead 44 and metallic (source) substrate 47 attached to a mounting flange 45. A first plurality of wires 48 couple the input lead 42 to a first terminal of an input matching capacitor 46. A second terminal of the input matching capacitor 46 is coupled to ground (i.e., flange 45). A second plurality of wires 52 couple the first terminal of matching capacitor 46 to the respective input terminals 49 of a plurality of interdigitated electrodes 51 formed on a semiconductor die 50 attached to the metallic substrate 47. By proper selection of the matching capacitor 46 and the series inductance of wires 48 and 52, the input impedance between the input lead 42 and electrode input terminals 49 can be effectively matched.

Respective output terminals 53 of the electrodes are coupled to the output lead 44 by a third plurality of wires 54. In order to impedance match the output of the device, a shunt inductance is used. Towards this end, the output lead 44 is coupled to a first terminal of a DC blocking capacitor 58 (i.e., an AC short) by a fourth plurality of wires 60, the blocking capacitor 58 having a substantially higher value than the input matching capacitor 46. FIG. 3 shows a schematic circuit representation of the device of FIG. 2, wherein the transmission inductance through the respective pluralities of wires is designated by the corresponding reference numbers of the wires in FIG. 2.

For "lower frequency" applications, e.g., 1500 MHz, the LDMOS device 40 of FIG. 2 may be adequately controlled, but at higher frequencies, e.g., 2 GHz, effective control of the device becomes difficult due to the relatively large series inductance generated through wires 54 to the shunt inductance 60. Further, because there is limited physical space on the electrode output terminals 53, the number of wires 54 connecting the plurality of electrodes 51 to the output lead 44.

Thus, it would be desirable to provide an LDMOS RF power transistor device in which output matching at relatively high frequencies (e.g., GHz) can be more easily accomplished.

Summary Of The Invention

In accordance with a first aspect of the present invention, an RF power transistor device comprises a semiconductor die having a plurality of electrodes formed thereon, the electrodes having respective output terminals. A conductive island is provided adjacent the semiconductor die and is coupled to the electrode output terminals by a first plurality

of conductors. A shunt inductance match is coupled from the conductive island by a second plurality of conductors to a blocking capacitor and an output lead is independently coupled to the conductive island by a third plurality of conductors.

By way of example, in a preferred embodiment, an LDMOS RF power transistor device includes a semiconductor die having a plurality of interdigitated electrodes formed thereon, the electrodes each having respective input terminals and output terminals. An input lead is coupled to a first terminal of an input matching capacitor by a first plurality of conductors (e.g., bond wires), with a second terminal of the matching capacitor coupled to a ground. The first terminal of the matching capacitor is also coupled to the electrode input terminals by a second plurality of conductors. A conductive island isolated from the ground is coupled to the electrode output terminals by a third plurality of conductors. Output matching of the device is provided by a shunt inductance formed by a fourth plurality of conductors coupling the conductive island to an output blocking capacitor, the blocking capacitor having a second terminal coupled to ground. An output lead is coupled to the conductive island by a fifth plurality of conductors.

The conductive island is preferably disposed adjacent the semiconductor die, and the output blocking capacitor is disposed between the conductive island and output lead, such that transmission inductance through the respective third and fourth pluralities of conductors coupling the electrode output terminals to the blocking capacitor is sufficiently small to allow for output impedance matching of the transistor device at relatively high operating frequencies.

As will be apparent to those skilled in the art, other and further aspects and advantages of the present invention will appear hereinafter.

Brief Description Of The Drawings

Preferred embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings, in which like reference numerals refer to like components, and in which:

FIG. 1 is a schematic circuit diagram of an unmatched LDMOS power transistor;

FIG. 2 is a partial top view of a prior art LDMOS RF power transistor device;

FIG. 3 is a schematic circuit diagram of the LDMOS transistor device of FIG. 2;

FIG. 4 is a top view of a preferred LDMOS RF power transistor device, according to the present invention; and

FIG. 5 is a schematic circuit diagram of the LDMOS transistor device of FIG. 4.

Detailed Description Of The Preferred Embodiments

Referring to FIGS. 4 and 5, a preferred LDMOS RF power transistor device 100 according to the present invention includes an input (i.e., gate) lead frame 102 and an output (i.e., drain) lead frame 104 attached to, but electrically isolated from, a conductive flange 145. By way of example, a ceramic substrate 143 may be used to isolate the respective lead frames 102 and 104 from the flange 145. Disposed on top of the flange is a metallic (i.e., source) substrate 103. In a preferred embodiment, the metallic (source) substrate comprises gold or a gold alloy.

A pair of semiconductor (e.g., silicon) dies 108 are attached to the metallic substrate 103, e.g., by ultrasonic scrubbing and/or thermal heating. Each die 108 has formed thereon a plurality of respective interdigitated electrodes 110, each electrode having respective input (gate) terminals 112 and output (drain) terminals 114. The respective input and output terminals 112 and 114 of the electrodes 110 on both dies 108 are connected to the respective lead frames 102 and 104 in the same manner. For ease in illustration, however, the remaining description will be directed to the electrodes 110 of just one of the dies 108.

Input matching of the device 100 is performed similarly to that of the prior art device 40 shown in FIG. 2. Namely, an input matching capacitor 106 is located through the (source) substrate 103 adjacent to the input lead frame 102. The input matching capacitor 106 has a first terminal 107 coupled to the input lead frame 102 by a first plurality of bonded wires 105. In particular, the wires 105 are bonded at one end to the input lead frame 102 and at the other end to the first terminal 107 of the matching capacitor 106. The matching capacitor 106 has a second terminal (not shown) coupled to the (ground) flange 145. A second plurality of wires 116 couple the first terminal 107 of the matching capacitor 106 to the respective input terminals 112 of the electrodes 110, i.e.. , wires 116 are bonded at one end to the to the matching capacitor terminal 107 and at the other end to the respective electrode input terminals 112. Input matching of the device 100 is thereby performed by selection of the desired capacitance value of matching capacitor 106 and the inductance of wires 105 and 106.

In accordance with the present invention, output matching of the device 100 is accomplished as follows:

A conductive island 120 isolated from the flange 145 by a non-conductive material (e.g., alumina) is provided adjacent the semiconductor die 108, wherein the conductive island 120 is electrically isolated from the (ground) flange 145. A third plurality of bonded wires 118 couples the respective electrode output terminals 114 to the conductive island 120. An output blocking capacitor 124 is disposed through the metallic substrate

103 between the conductive island 120 and the output lead frame 104. A shunt inductance is formed by a fourth plurality of bonded wires 122, which coupled the conductive island to a first terminal 125 of the blocking capacitor 124. A second terminal (not shown) of the blocking capacitor 124 is coupled to the (ground) flange 145. The output lead frame 104 is independently coupled to the conductive island 120 by a fifth plurality of bonded wires 126.

Notably, the output series inductance though wires 118 and 122 coupling the electrode output terminals 114 to the shunt inductance 122 is significantly reduced over that of the prior art device 40 shown in FIG. 2. Further, the conductive island 120 in device 100 allows for a significantly greater number of wires 126 to be used for coupling the island 120 to the output lead 104 than in device 40, as the longer wires are not limited by the number of electrode output terminals 114. As such, output matching of device 100 may be more readily accomplished than in device 40, especially at relatively high operating frequencies, e.g., into gigahertz frequency bandwidths.

While preferred embodiments and applications of an output-matched LDMOS Power transistor device have been shown and described, as would be apparent to those skilled in the art, many modifications and applications are possible without departing from the inventive concepts herein.

Thus, the scope of the disclosed invention is not to be restricted except in accordance with the appended claims.

Claims

1. An RF power transistor device, comprising:

a semiconductor die having a plurality of electrodes formed thereon, the electrodes having respective output terminals;

a conductive island coupled to the electrode output terminals by a first plurality of conductors;

an output blocking capacitor having a first terminal coupled to the conductive island by a second plurality of conductors and a second terminal coupled to a ground; and

an output lead coupled to the conductive island by a third plurality of conductors.

2. The transistor device of claim 1, wherein the electrodes each comprise a plurality of interdigitated electrode fingers.

3. The transistor device of claim 1, wherein the respective pluralities of conductors each comprise wires.

4. The transistor device of claim 1, wherein the conductive island is disposed adjacent the semiconductor die, and the blocking capacitor is disposed between the conductive island and output lead, such that transmission inductance through the respective first and second pluralities of conductors coupling the electrode output terminals to the blocking capacitor is sufficiently small to allow for output impedance matching of the device at relatively high operating frequencies.

5. An RF power transistor device, comprising:

a first lead;

a semiconductor die having a plurality of electrodes formed thereon, the electrodes each having respective input terminals and output terminals;

a first capacitor having a first terminal coupled to the first lead by a first plurality of conductors and coupled to the electrode input terminals by a second plurality of conductors;

a conductive island isolated from the ground and coupled to the electrode output terminals by a third plurality of conductors;

a second capacitor having a first terminal coupled to the conductive island by a fourth plurality of conductors, and a second terminal coupled to the ground; and

a second lead coupled to the conductive island by a fifth plurality of conductors.

6. The transistor device of claim 5, wherein the electrodes each comprise a plurality of interdigitated electrode fingers.

7. The transistor device of claim 5, wherein the respective pluralities of conductors each comprise wires.

8. The transistor device of claim 5, wherein the conductive island is disposed adjacent the semiconductor die, and the second capacitor is disposed between the conductive island and second lead, such that transmission inductance through the respective third and fourth pluralities of conductors coupling the electrode output terminals to the second capacitor is sufficiently small to allow for output impedance matching of the device at relatively high operating frequencies.

9. An LDMOS RF power transistor device, comprising:

an input lead frame;

a silicon die having a plurality of interdigitated electrodes formed thereon, the electrodes each having respective input terminals and output terminals;

an input matching capacitor having a first terminal coupled to the input lead by a first plurality of wires and coupled to the electrode input terminals by a second plurality of wires, the input matching capacitor having a second terminal coupled to a ground;

a conductive island isolated from the ground and coupled to the electrode output terminals by a third plurality of wires;

an output blocking capacitor having a first terminal coupled to the conductive island by a fourth plurality of wires and a second terminal coupled to the ground; and

an output lead frame coupled to the conductive island by a fifth plurality of wires,

wherein the conductive island is disposed adjacent the semiconductor die, and the output blocking capacitor is disposed between the conductive island and output lead frame , such that transmission inductance through the respective third and fourth

pluralities of wires coupling the electrode output terminals to the first terminal of the output blocking capacitor is sufficiently small to allow for output impedance matching of the device at relatively high operating frequencies.

AMENDED CLAIMS

[received by the International Bureau on 08 May 2000 (08.05.00);
original claim 1 amended; original claims 4, 5, 8 and 9 amended and renumbered
as claims 3, 4, 6 and 7; original claims 3 and 7 renumbered as claims 2 and 5 (3 pages)]

1. An RF power transistor device, comprising:

a semiconductor having a plurality of electrodes formed thereon, the electrodes having respective output terminals; each electrode comprising a plurality of interdigitated transistors;

a conductive island coupled to the electrode output terminals by a first plurality of conductors;

an input matching capacitor having a first terminal coupled to an input lead frame by a second plurality of conductors carrying an input inductance and a second terminal coupled to a ground; said first terminal coupled to said semiconductor by a third plurality of conductors;

an output blocking capacitor having a first terminal coupled to the conductive island by a fourth plurality of conductors and a second terminal coupled to the ground; and

an output lead coupled to the conductive island by a fifth plurality of conductors carrying an output inductance.

2. The transistor device of claim 1, wherein the respective pluralities of conductors each comprise wires.

3. The transistor device of claim 1, wherein the conductive island is disposed adjacent the semiconductor, and the blocking capacitor is disposed between the conductive island and the output lead, such that transmission inductance through the respective first and fourth pluralities of conductors coupling the electrode output terminals to the blocking capacitor is small to allow for output impedance matching of the device at high operating frequencies.

4. An RF power transistor device, comprising:

a first lead;

a semiconductor having a plurality of electrodes formed thereon, the electrodes each having respective input terminals and output terminals; each electrode comprising a plurality of interdigitated transistors;

a first capacitor having a first terminal coupled to the first lead by a first plurality of conductors carrying an input inductance and coupled to the electrode input terminals by a second plurality of conductors;

a conductive island isolated from a ground and coupled to the electrode output terminals by a third plurality of conductors;

a second capacitor having a first terminal coupled to the conductive island by a fourth plurality of conductors, and a second terminal coupled to the ground; and

a second lead coupled to the conductive island by a fifth plurality of conductors carrying an output inductance.

5. The transistor device of claim 4, wherein the respective pluralities of conductors each comprise wires.

6. The transistor device of claim 4, wherein the conductive island is disposed adjacent the semiconductor, and the second capacitor is disposed between the conductive island and the second lead, such that transmission inductance through the respective third and fourth pluralities of conductors coupling the electrode output terminals to the second capacitor is small to allow for output impedance matching of the device at high operating frequencies.

7. An LDMOS RF power transistor device, comprising:

an input lead frame;

a semiconductor having a plurality of electrodes formed thereon, the electrodes each having respective input terminals and output terminals, each electrode comprising a plurality of interdigitated transistors;

an input matching capacitor having a first terminal coupled to the input lead by a first plurality of wires carrying an input inductance and coupled to the electrode input terminals by a second plurality of wires, the input matching capacitor having a second terminal coupled to a ground;

a conductive island isolated from the ground and coupled to the electrode output terminals by a third plurality of wires;

an output blocking capacitor having a first terminal coupled to the conductive island by a fourth plurality of conductors and a second terminal coupled to the ground; and

an output lead frame coupled to the conductive island by a fifth plurality of wires carrying an output inductance,

wherein the conductive island is disposed adjacent the semiconductor, and the output blocking capacitor is disposed between the conductive island and the output lead frame, such that transmission inductance through the respective third and fourth pluralities of wires coupling the electrode output terminals to the first terminal of the output blocking capacitor is small to allow for output impedance matching of the device at high operating frequencies.

STATEMENT UNDER ARTICLE 19

In response to the International Search Report mailed March 6, 2000, Applicant submits herewith an Article 19 Amendment with substitute claims, which replace the original claims as filed in the international application. This Amendment is filed in order to bring the claims of the subject PCT application into conformance with the claims in the parent case, which is currently pending in the U.S. Patent and Trademark Office. Since two months were provided to reply to this International Search Report, this reply is timely filed.

Original claims 1, 4, 5, 8 and 9 have been amended. Original claims 2 and 6 have been deleted and claims 3-5 and 7-9 have been renumbered as 2-4 and 5-7 respectively. Claims 3 and 7 (now renumbered as 2 and 5) remain unchanged. No new matter has been added by way of this amendment.

Replacement sheets 6 through 8 are submitted herewith, which replace claim pages 6 through 8 as originally filed.

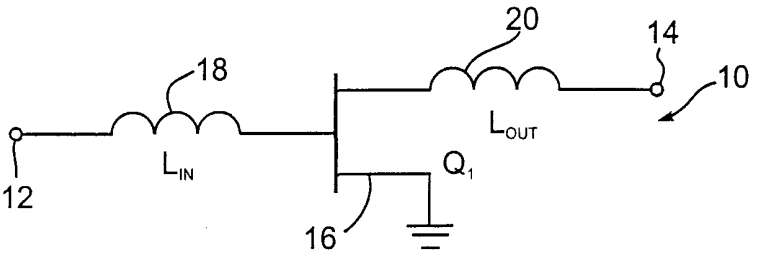

Fig. 1
PRIOR ART

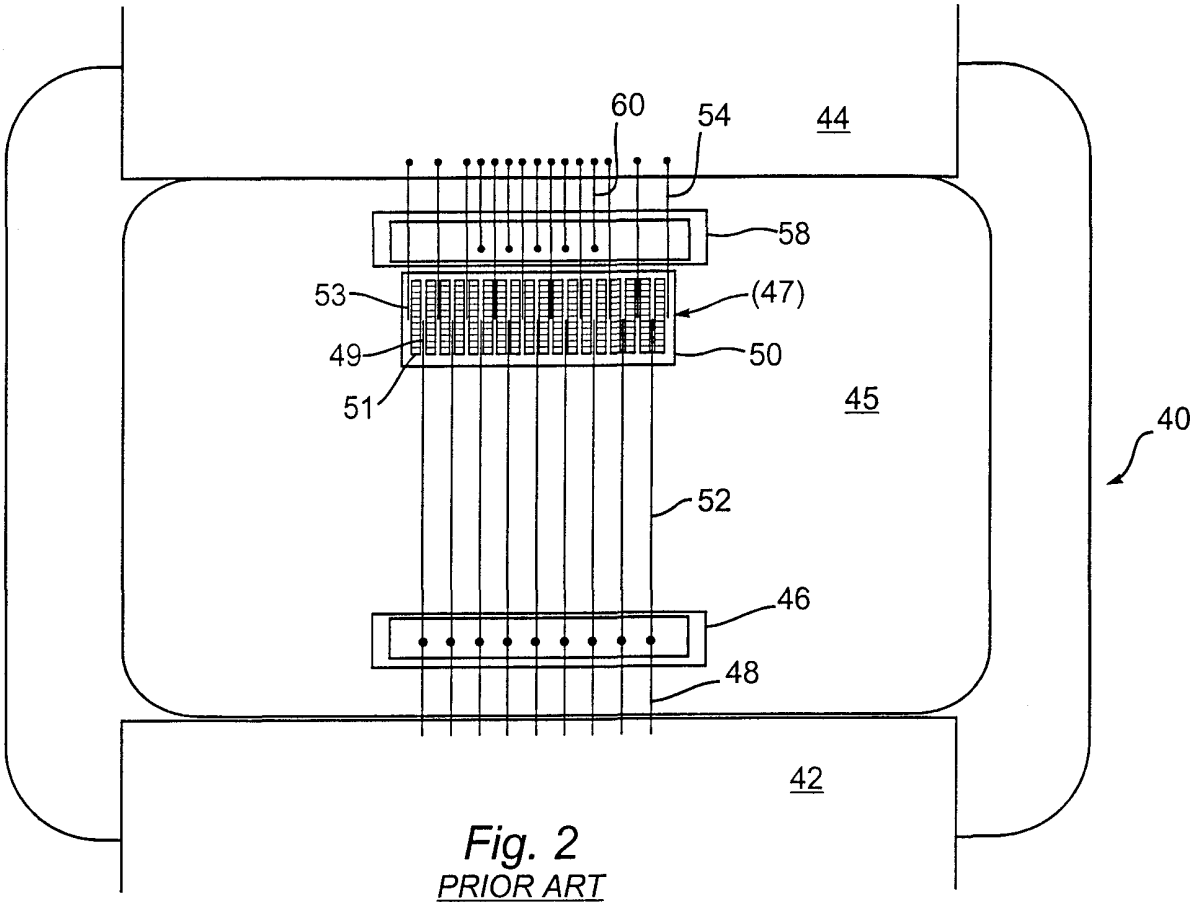

Fig. 2
PRIOR ART

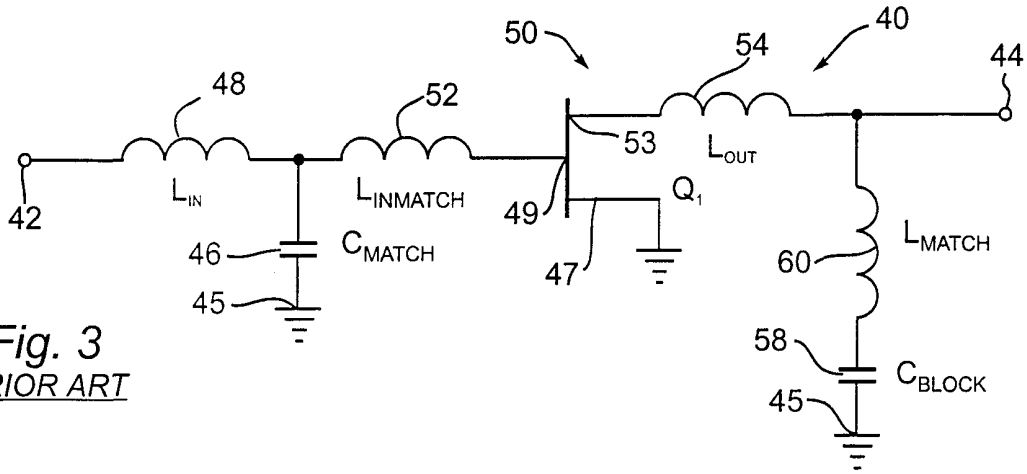

Fig. 3
PRIOR ART

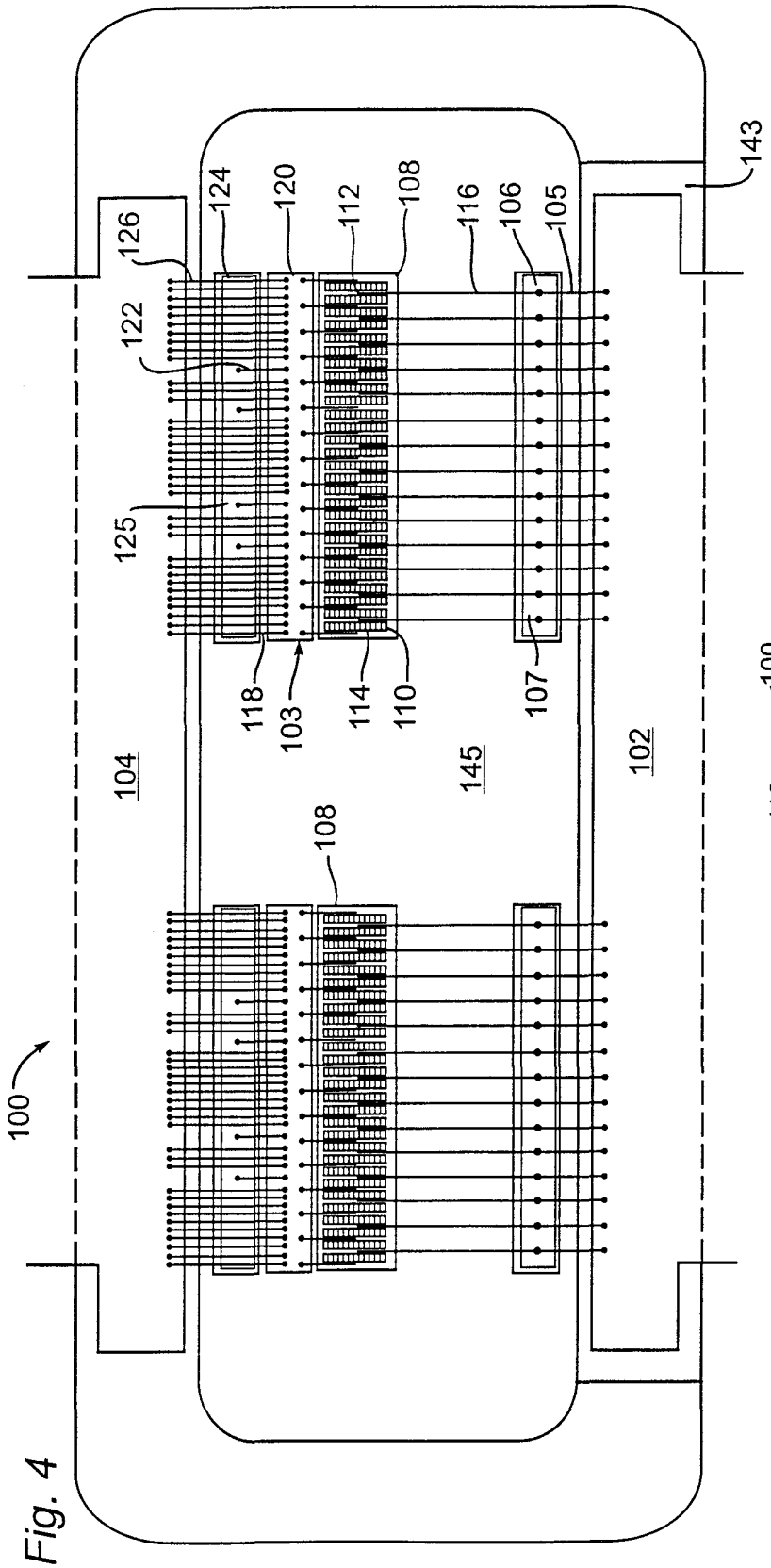
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Fig. 4

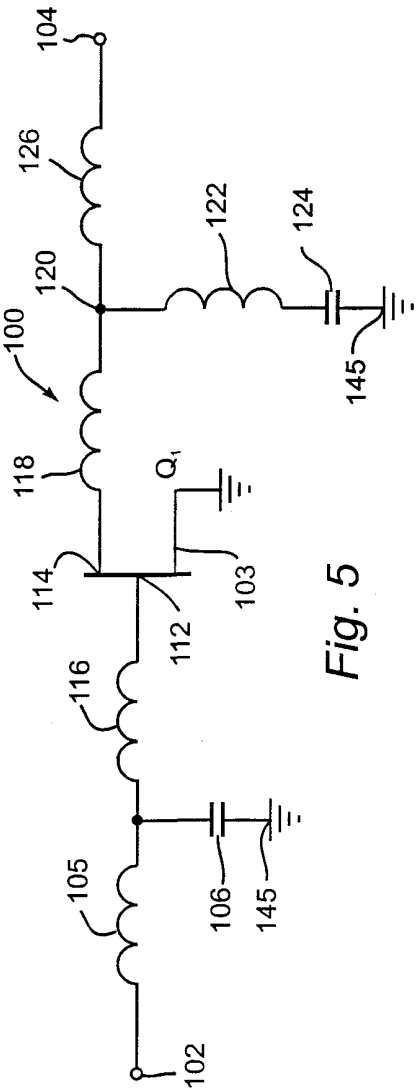
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Fig. 5

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 99/28040

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 193 083 A (MAX LEE B) 11 March 1980 (1980-03-11) claims 1,10,12; figures 1,5	1,5
X	EP 0 015 709 A (FUJITSU LTD) 17 September 1980 (1980-09-17)	5-7
A	claims 1,4,7,11; figure 8	1-3
A	GB 2 264 001 A (MITSUBISHI ELECTRIC CORP) 11 August 1993 (1993-08-11) claims 1,4; figure 2	1,3,5,7
A	US 4 393 392 A (HALE RAYMOND L) 12 July 1983 (1983-07-12) claims 1,2; figure 2	1,5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2000	06/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	De Raeve, R

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 99/28040

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 182 (E-515), 11 June 1987 (1987-06-11) & JP 62 013041 A (MITSUBISHI ELECTRIC CORP), 21 January 1987 (1987-01-21) abstract	
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
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