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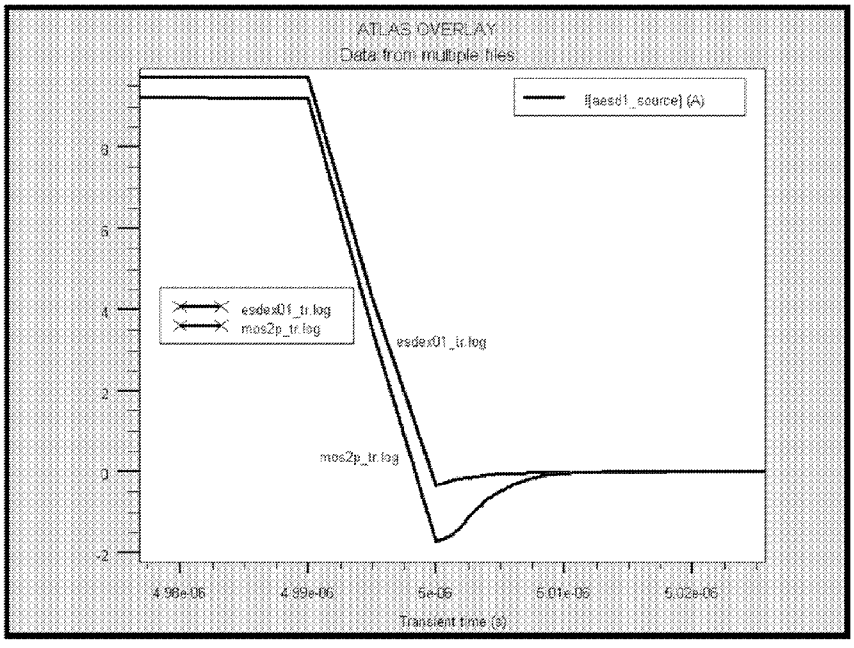
(54) **Title**: MOSFET WITH INTEGRATED FIELD EFFECT RECTIFIER

Figure 4



(57) **Abstract**: A modified MOSFET structure comprises an integrated field effect rectifier connected between the source and drain of the MOSFET to shunt current during switching of the MOSFET. The integrated FER provides faster switching of the MOSFET due to the absence of injected carriers during switching while also decreasing the level of EMI relative to discrete solutions. The integrated structure of the MOSFET and FER can be fabricated using N-, multi-epitaxial and supertrench technologies, including 0.25μm technology. Self-aligned processing can be used.

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MOSFET with Integrated Field Effect Rectifier

SPECIFICATION

RELATED APPLICATIONS

[001] This application is related to, and claims the benefit of, U.S. Patent Application U.S. Patent Application S.N. 12/238,308, filed 9/25/2008, titled "Adjustable Field Effect Rectifier" (Attached as Appendix A) and through it U.S. Provisional Patent Application S.N. 60/975,467, filed September 26, 2007, as well as U.S. Patent Application S.N. 12/359,094, filed 1/23/2009, entitled "Regenerative Building Block and Diode Bridge Rectifier," and through it U.S. Provisional Patent Application S.N. 61/022,968, filed January 23, 2008, and also provisional U.S. Patent Application S.N. 61/048,336, filed April 28, 2008, entitled "MOSFET with Integrated Field Effect Rectifier," all of which have the same inventors as the present application and are incorporated herein by reference in full for all purposes.

Field of the Invention

[002] The present invention relates generally to semiconductor transistors, and more specifically to an integration of a field effect rectifier into a MOSFET structure for improving the performance of the MOSFET, and methods therefor.

BACKGROUND OF THE INVENTION

[003] MOSFETs are commonly used for fast switching in electronic circuits. However, where the load is inductive the switching speed is limited due to the intrinsic body diode problem. When the gate

voltage is used to switch MOSFET from ON to OFF state (reverse recovery), the intrinsic p-n junction diode has to conduct current, and will inject carriers into the bulk of device. Until the injected carriers are dissipated, the MOSFET will continue to stay in the ON state. This causes slow switching of MOSFET from ON to OFF state and limits the frequency of the MOSFET operation.

[004] To overcome the slow switching of the body diode an external freewheeling diode is often added between the source and the drain of the MOSFET to prevent the injection of carriers during reverse recovery. However, the addition of the external diode can lead to increased EMI, since the current that was flowing through the MOSFET now has to flow through the external diode and connecting wires. The extra EMI emissions can also limit the switching speed of the MOSFET with freewheeling diode. While the freewheeling diode is typically put as close to MOSFET as possible, the problem of extra EMI remains.

[005] While integrating the P-N junction diode technology into the MOSFET has an initial appeal, this technology has a limited potential to improve the body diode problem, since the body diode is a P-N junction diode integral to MOSFET structure. Similarly, Schottky diode technology is practically incompatible with MOSFET technologies, since it requires specific metallization not well suited for MOSFET manufacturing.

SUMMARY OF THE INVENTION

[006] To overcome the limitations of the prior art, the present invention integrates a Field Effect Rectifier (FER) into a MOSFET to improve the switching characteristics of the MOSFET when coupled to an inductive load, thus improving switching speed without significant adverse effects on EMI.

[007] In the new design, the FER does not replace the body diode, but provides a shunt or a bypass for the current flow around the body

diode. The FER technology is compatible with MOSFET technology, permitting substantially conventional processing. Depending upon the implementation, the device of the present invention can be configured for either high voltage operation (e.g., a discrete high power device) or low voltage operation (e.g., in an integrated circuit) by adjustment of, for example, the size and resistivity of the epi, gate size, and so on. Further, unlike P-N junction diodes, the low voltage FER is a majority carrier device and prevents the body diode from injecting minority carriers that slow down the MOSFET operation. The high voltage FER will inject fewer carriers due to a particular one sided carrier injection mechanism (Rodov, Ankoudinov, Ghosh, Sol.St. Electronics 51 (2007) 714-718).

THE FIGURES

[008] Figures 1A-1B show a MOSFET with integrated Field Effect Rectifier in accordance with the invention, where Figure 1A shows a DMOS structure and Figure 1B shows a UMOS structure. The current flow between source and drain is controlled by the gate electrode. The current will flow through the FER during switching, once the Gate voltage does not allow the current flow through the MOSFET. The Adjustment area (optional) provides a control of the leakage current.

[009] Figure 2 shows in graphical form forward voltage drop vs. current for the body diode of a regular MOSFET (red) and a MOSFETR (green) in accordance with the invention. With VG=+5V the RDS,ON per MOSFET occupied area is about the same. Dark blue curve is for MOSFETR and the light blue is for MOSFET.

[0010] Figure 3 shows leakage current vs. reverse voltage for a conventional MOSFET (red), and MOSFETR with (green) and without (blue) the adjustment area in accordance with the invention. Scale (1A=2.5e-7)

[0011] Figure 4 illustrates transients for a 10A 20V MOSFETR according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0012] The present invention comprises a new MOSFET structure that has integrated therein a field effect rectifier (hereinafter sometimes referred to as a "MOSFETR"). The field effect rectifier provides the alternative path for the current flow when the gate voltage switches OFF the current flow through MOSFET. The injection of the carriers from P-N junction can be reduced or completely eliminated, leading to faster MOSFET switching without significant EMI.

[0013] Referring first to Figures 1A, the DMOS MOSFETR structure indicated generally at 100 comprises a MOSFET 100A on the left and an FER 100B on the right. In some embodiments, the FER device can be adjustable as described in U.S. Provisional Patent Application S.N. 60/975,467, filed September 26, 2007, although an FER without adjustable area also can be used in other embodiments. As shown in Figure 1, the MOSFETR 100 has three electrodes: source 105, gate 110 and drain 115. The main current flows between the source and drain electrodes through the epitaxial N- layer 125. The P-well 130 is provided to create a depletion layer when reverse bias is applied. The N++ regions 135 provide ohmic contact for the current flow. The adjustment area comprises the window 140 inside the FER gate and the P++ implantation 145. The adjustment area permits control of the current flow, and thus can be desirable in some embodiments, depending upon the implementation. The gate oxide thickness and the doping levels control the height of the potential barrier under the FER gate 165, and therefore the gate oxide under FER gate 150 can, in some embodiments, have a different thickness than the gate oxide under the MOSFET gate 155. The gate voltage controls the conductivity of the narrow channel 160 under MOS

gate 110 and switches the MOSFET between OFF and ON states. The transition from ON to OFF happens at the threshold voltage, which can be adjusted either by using a doping profile under the gate or by changing the thickness of the gate oxide 155. The gate oxide thickness for the sides of MOSFET 155 and FER gate 150 can be varied independently of one another to ensure proper operation of both components.

[0014] When the MOSFETR 100 is in the ON state (e.g., VGS=+5V), current flows through MOSFET channel 160. A forward characteristic of an embodiment of MOSFETR in accordance with the invention is shown in Figure 2, where the device is capable of operating at 10A at 20V. It can be appreciated by those skilled in the art that the MOSFETR has RDS,ON equal to 3.6 milliohm. If the right portion of the device is also a MOSFET, then simulated RDS,On is 2.0 milliohm. Notice that, for the characteristics shown in Figure 2, the area of the MOSFET is on the order of 50% of the total area of the MOSFETR. Thus RDS,On of MOSFETR per unit area is about 10% smaller. This results because part of the epitaxial layer under the diode is used for conduction during MOSFET operation. It will be appreciated that this effect will, for some embodiments, increase for higher voltage devices. The increase of RDS,ON is typically smaller for high voltage devices, since the epitaxial layer becomes thicker to withstand higher reverse voltage. For some embodiments the area covered by MOSFET can be increased to reduce RDS,On, while the reduced FER area is still effective for the stored charge reduction.

[0015] Figure 1B shows a UMOS MOSFETR structure which operates in a manner substantially identical with that shown in Figure 1A, and like elements are shown with like reference numbers, but with the most significant digit incremented by one.

[0016] When the MOSFET is turned OFF (VGS=-5V), the current will flow through the body diode of MOSFET with VF=0.76V or through the FER of the MOSFETR with VF=0.58. In at least some embodiments, VF

will preferably be kept below the knee voltage (~0.7V) of the body diode, where P-N junction starts to inject carriers. Thus, a conventional MOSFET will inject carriers during switching while a MOSFETR according to the present invention substantially eliminates this undesirable behavior.

[0017] In the OFF state, the small leakage current will flow through the AFER channel 165. In at least some embodiments, this leakage is controlled by the potential barrier height and how fast the pinch-off effect takes place. Figure 3 demonstrates that the leakage of a MOSFETR is about 500 μA at 20V, which is similar to the leakage of a MOSFET. The adjustment area of the MOSFETR plays a role to keep leakage under control, and the leakage of a MOSFETR that does not have adjustment area is on the order of twice as much, or 1μA. At higher voltages, the effect of the adjustment area can decrease.

[0018] Figure 3 illustrates the absence of injected carriers during switching with inductive load. For the example of Figure 3, VGS is set to -5V, which turns OFF the current through MOSFET channel. The electron density distribution in MOSFETR for a 10A forward current is substantially the same as the electron density distribution with no current, and thus confirms that no carrier density modulation occurs. The electron concentration in the middle of the epitaxial N- layer can be seen to be on the order of 2.9e16. In contrast, operation of a conventional MOSFET shows significant injection at 10A current: the electron concentration becomes 5.1e16, or almost double. These injected carriers significantly slow down the operation of a conventional MOSFET with inductive loads.

[0019] Figure 4 shows the simulated transient behavior of MOSFET with and without the integrated diode. The transient time and stored charge are significantly smaller for MOSFETR. The low stored charge and small dI/dt of MOSFETR demonstrate that the device of the present invention is highly suitable for fast switching applications.

[0020] In summary, the static characteristics of MOSFETR are very similar to those of the regular MOSFET, while exhibiting faster switching due to the absence of injected carriers during switching. The integrated FER diode structure is preferred over the discrete solution since it will decrease the level of EMI and allow the faster switching with low EMI.

[0021] While the embodiment of the invention described is based on an N- epitaxial layer, it will be appreciated by those skilled in the art that equivalent structures can be formed using multi-epitaxial or supertrench methods, and it is specifically intended that the present invention encompass such alternatives. Likewise, it will be appreciated that the present structure is typically integrated into the larger circuits, and can be fabricated using standard methods including, for example, 0.25μm technology with a mask alignment accuracy of approximately 20nm, as well as others.

[0022] The present invention has been described in detail, including numerous alternatives and equivalents. It is therefore to be understood that the invention is not to be limited by the embodiments specifically described herein, but only by the appended claims.

We claim:

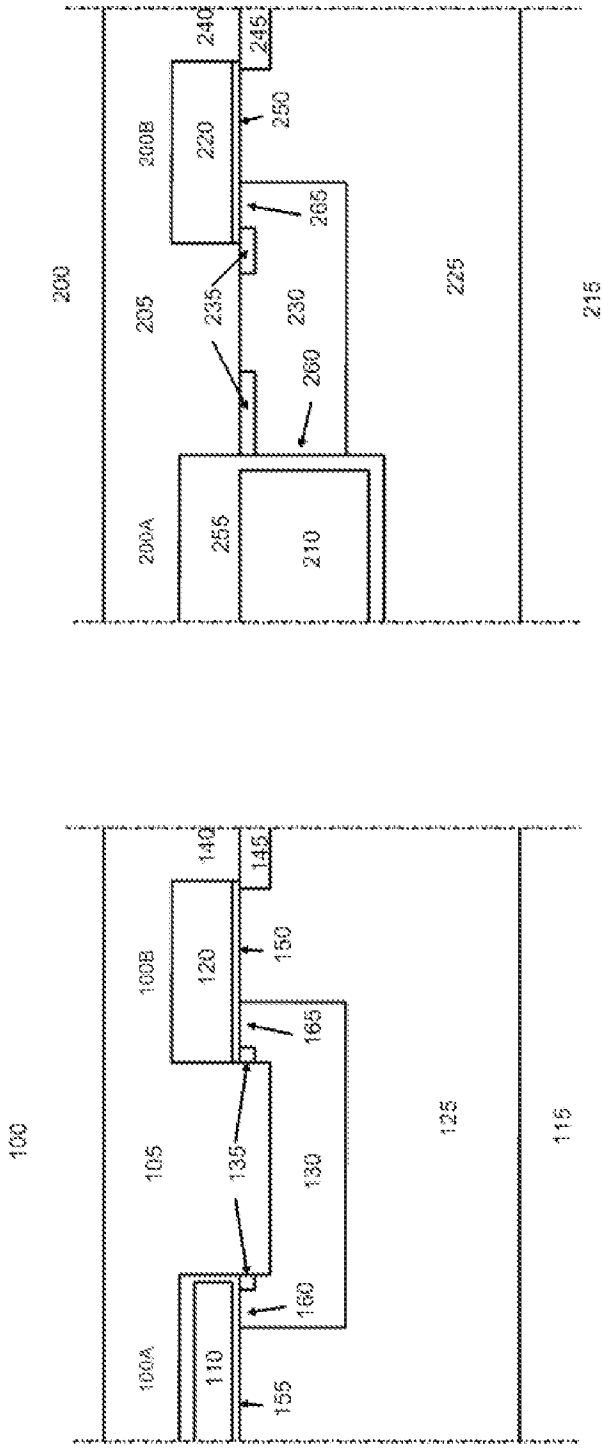
1. In a metal oxide semiconductor field effect transistor (MOSFET) structure having a gate, a source, and a drain, wherein the current flow between the source and the drain is controlled by the voltage applied to the gate, the improvement comprising

a field effect rectifier connected between the source and the drain and serving to shunt current therethrough during switching of the MOSFET.

2. The MOSFET structure of claim 1 wherein the MOSFET is a DMOS structure.
3. The MOSFET structure of claim 1 where the MOSFET is a UMOS structure.
4. The MOSFET structure of claim 1 formed using a self-aligned process.
5. The MOSFET structure of claim 1 formed using not greater than 0.25μm processing.
6. The MOSFET structure of claim 1 formed using N- epitaxial processing.
7. The MOSFET structure of claim 1 formed using multi-epitaxial processing.
8. The MOSFET structure of claim 1 formed using supertrench processing.
9. An integrated semiconductor structure comprising

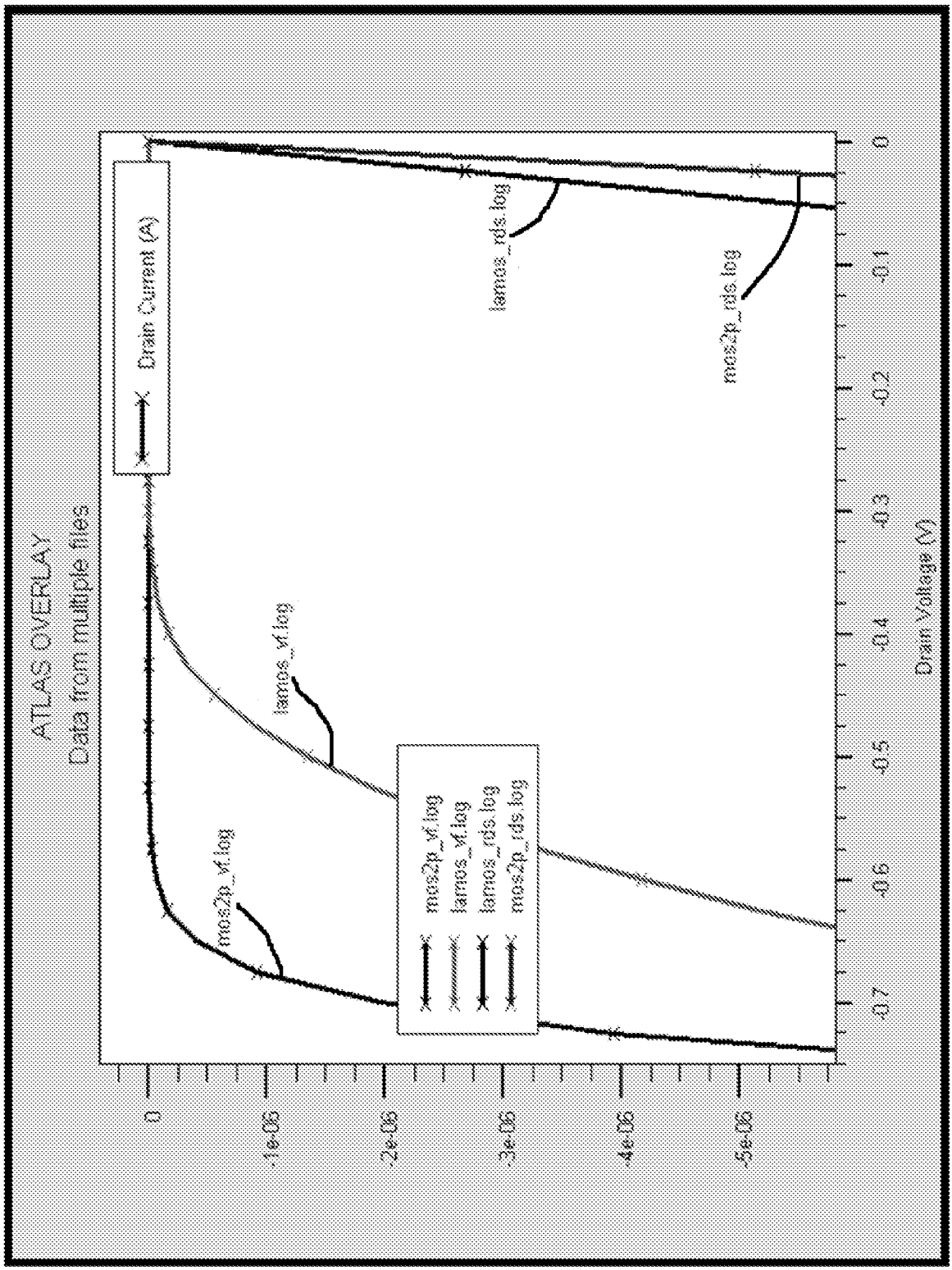
a MOSFET having a gate, a source and a drain, and

a field effect rectifier formed in the same substrate as the MOSFET and connected between the source and the drain of the MOSFET for conducting current during switching of the MOSFET.



Figures 1A-1B. MOSFET (DMOS, Figure 1A, and UMOS, Figure 1B, structures) with integrated Field Effect Rectifier. The current flow between source and drain is controlled by the gate electrode. The current will flow through FER during the switching, once the Gate voltage does not allow the current flow through MOSFET. The Adjustment area (optional) provides a control of the leakage current.

Figure 2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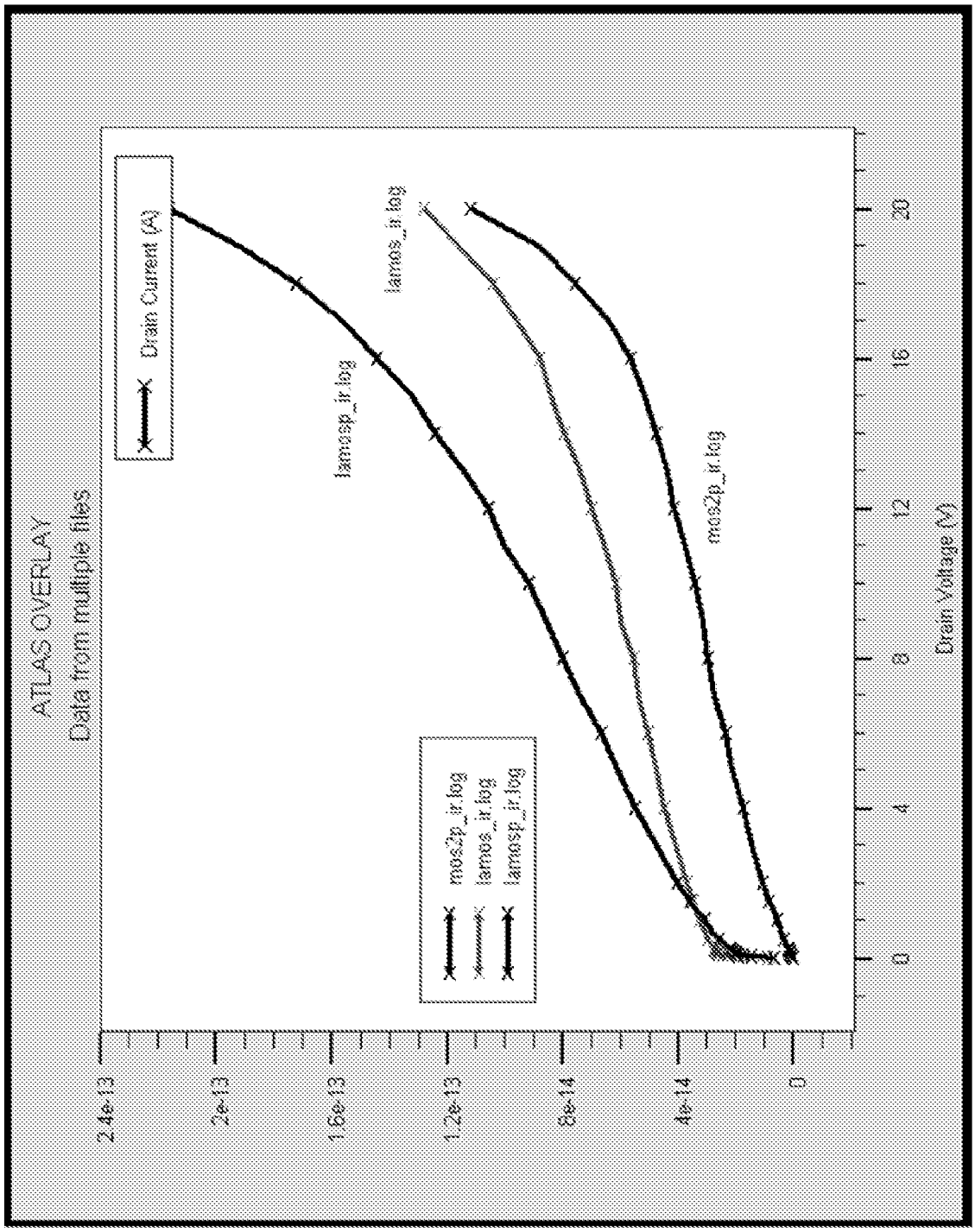
-0.3
-0.4
-0.5
-0.6
-0.7
Drain Voltage (V)

Figure 3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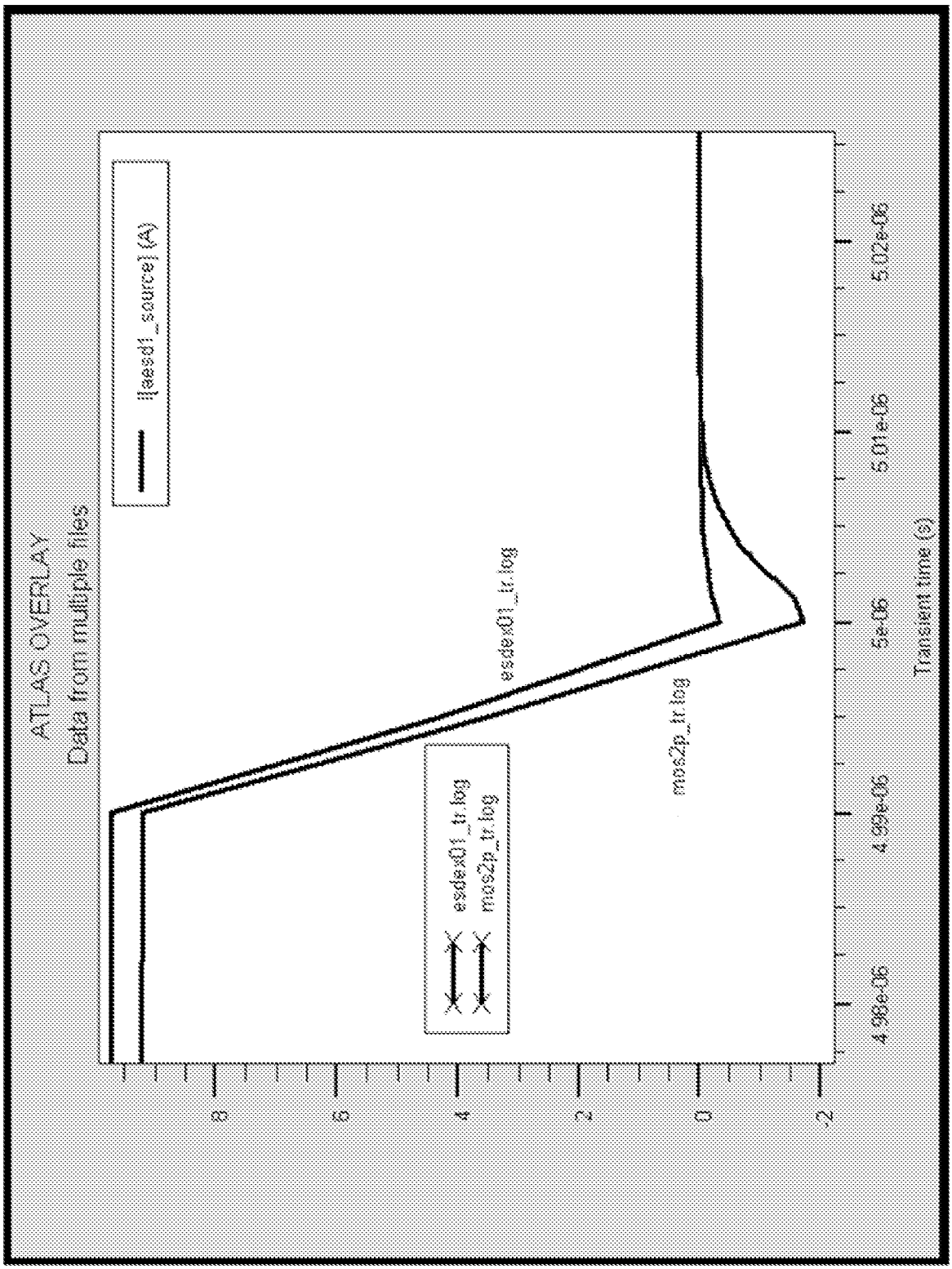
0
4
8
12
16
20
Drain Voltage (V)

Figure 4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5.02e-06
Transient time (s)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/41996

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/335 (2009.01)
USPC - 257/213, 658
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 257/213, 658; 438/142, 275

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 257/213, 658; 438/142, 275

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(USPT,PGPB,EPAB,JPAB); Google, Google Patent.
Search Terms Used: MOSFET, rectifier, shunt, current, self-aligned, epitaxial, processing, DMOS, UMOS, 0.25, multi-epitaxial, supertrench.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,929,690 A (WILLIAMS) 27 July 1999 (27.07.1999), col 8 ln 30-36, col 10 ln 25-29, col 13 ln 3740, col 17 ln 37,38, 60-67, col 18 ln 1-23, Fig. 1A, 4A, 4B, 12C, 13.	1-3, 6, 9 --- 4, 5, 7, 8
Y	US 6,100,145 A (KEPLER et al.) 08 August 2000 (08.08.2000), col 1 ln 1-55, col 2 ln 8-20.	4, 5
Y	US 6,967,374 B1 (SAITO et al.) 22 November 2005 (22.11.2005), abstract, col 3 ln 10-16, col 11 ln 20-25.	7
Y	US 6,384,456 B1 (Tihanyi) 07 May 2002 (07.05.2002), col 1 ln 47-51, col 2 ln 36-40, Fig. 1.	8

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 June 2009 (08.06.2009)	19 JUN 2009
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774