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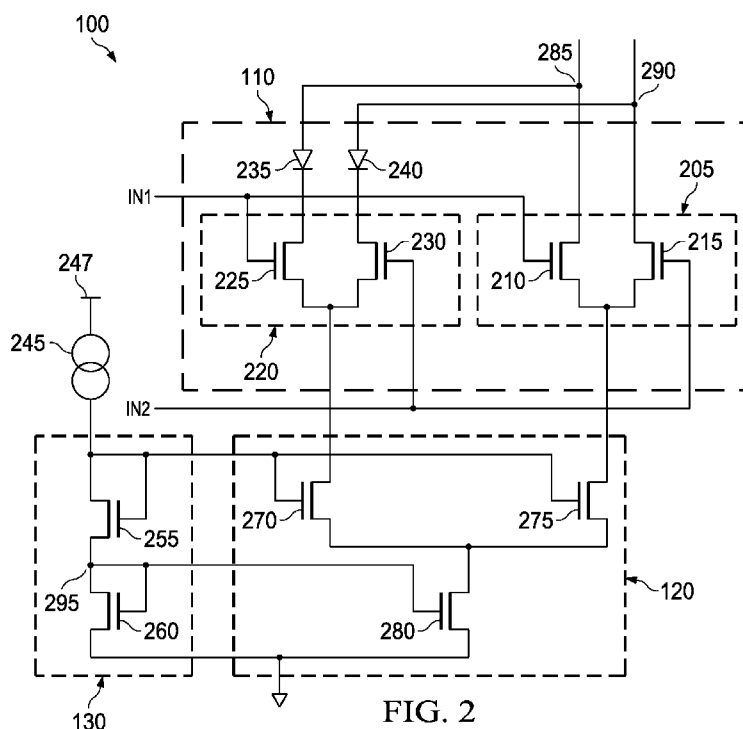


FIG. 2

(57) Abstract: In some embodiments, a differential input stage includes a first n-type metal oxide semiconductor transistor (NMOS) pair (220) coupled to a first input (IN1) and a second input (IN2), a second NMOS pair (205) coupled to the first input (IN1), a first output node (285), the second input (IN2), and a second output node (290), a first diode (235) coupled to the first NMOS pair (220) and the first output node (285), a second diode (240) coupled to the first NMOS pair (220) and the second output node (290), and a cascaded current source (120) coupled to the first NMOS pair (220) and the second NMOS pair (205).

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DIFFERENTIAL INPUT STAGES

BACKGROUND

[0001] Amplifiers are electrical circuits that receive an input signal and generate an output signal at least partially according to the input signal. Amplifiers may increase, decrease, or leave substantially unchanged a value of the output signal with respect to the input signal. To process the input signal when it is received by an amplifier, the amplifier may include an input stage.

SUMMARY

[0002] In some embodiments, a differential input stage includes a first n-type metal oxide semiconductor transistor (NMOS) pair coupled to a first input and a second input, a second NMOS pair coupled to the first input, a first output node, the second input, and a second output node, a first diode coupled to the first NMOS pair and the first output node, a second diode coupled to the first NMOS pair and the second output node, and a cascaded current source coupled to the first NMOS pair and the second NMOS pair.

[0003] In some embodiments, an amplifier includes a differential input stage and an output stage. The differential input stage includes a first NMOS pair coupled to a first input and a second input, a second NMOS pair coupled to the first input, the second input, a first output node, and a second output node, a first diode coupled between the first NMOS pair and the first output node, a second diode coupled between the first NMOS pair and the second output node, and a cascaded current source coupled between the first NMOS pair, the second NMOS pair, and a ground voltage potential. The output stage is coupled to the first output node and the second output node. The output stage includes at least one transistor configured to amplify an output of the differential input stage at the first and second output nodes to produce an amplifier output.

[0004] In some embodiments, a differential input stage includes a first diode having a first anode coupled to a first output node and a second diode having a second anode coupled to a second output node. The differential input stage further includes a first NMOS differential amplifier including a first NMOS transistor including a first gate terminal coupled to a first input, a first drain terminal coupled to a cathode of the first diode, and a first source terminal coupled to a first node. The first NMOS differential amplifier further includes a second NMOS transistor including

a second gate terminal coupled to a second input, a second drain terminal coupled to a cathode of the second diode, and a second source terminal coupled to the first node. The differential input stage further includes a second NMOS differential amplifier including a third NMOS transistor including a third gate terminal coupled to the first input, a third drain terminal coupled to the first output node, and a third source terminal coupled to a second node. The second NMOS differential amplifier further includes a fourth NMOS transistor including a fourth gate terminal coupled to the second input, a fourth drain terminal coupled to the second output node, and a fourth source terminal coupled to the second node. The differential input stage further includes a cascaded current source coupled between the first node, the second node, and a ground voltage potential.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a block diagram of an illustrative differential input stage in accordance with various embodiments.

[0006] FIG. 2 is a schematic diagram of the illustrative differential input stage in accordance with various embodiments.

[0007] FIG. 3 is a schematic diagram of an illustrative amplifier in accordance with various embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] To provide a wide input range—such as a wide common mode voltage input range—input stages of amplifiers and other electronic circuits often include both n-type metal oxide semiconductor (NMOS) transistors and p-type metal oxide semiconductor (PMOS) transistors. In at least one example, the common mode input voltage is an absolute voltage with respect to a ground voltage potential (which may be contrasted with a differential voltage that has a value with respect to another voltage level). The inclusion of the NMOS transistors and the PMOS transistors allows the wide input range because the NMOS operates at high input voltages and the PMOS operates at low input voltages. The inclusion of NMOS and PMOS transistors in such input stages, however, may result in high power consumption, high circuit complexity, and large surface areas. For example, the NMOS transistors and the PMOS transistors may require separate tail currents, outputs of the NMOS transistors and the PMOS transistors may require additional circuitry or circuit complexity to be combined at some location in a circuit that includes or is coupled to the input stage, and the PMOS transistors may be large in size in comparison to the NMOS transistors.

[0009] Described herein are embodiments that provide for a differential input stage that at least

partially mitigates the disadvantages described above. In some embodiments, the differential input stage comprises a pair of standard NMOS transistors and a pair of natural (also known as “native”) NMOS transistors. Such differential input stages improve over existing differential input stages by including the pair of standard NMOS transistors and the pair of natural NMOS transistors in lieu of a combination of NMOS transistors and PMOS transistors. For example, the improvement may include reduced size or footprint, less complex circuit design (e.g., fewer supporting components), reduced power consumption, and/or reduced cost of manufacturing. Although described herein as including a pair of standard NMOS transistors and a pair of natural NMOS transistors, the differential input stage may include any one or more types of NMOS transistors that provide for the functionality described herein. Various differential input stage embodiments and their operation are now described.

[0010] The standard NMOS transistor pair and the natural NMOS transistor pair together facilitate operation of the differential input stage for an input signal having a value of approximately zero volts to an input signal having a value of approximately a source supply voltage of the differential input stage. (The term “approximately,” as used herein, means plus or minus 10% of the stated value.) When the input signal has a low voltage level, such as approximately zero volts, only one of the standard NMOS transistor pair or the natural NMOS transistor may operate in the differential input stage to conduct a majority (or approximately all) current passing through the differential input stage. When the input signal has a high voltage level, such as approximately the source supply voltage, an opposite of the standard NMOS transistor pair or the natural NMOS transistor pair than was active when the input signal had a low voltage level may dominate, operating to conduct a majority of current passing through the differential input stage. When the input signal has neither a low nor a high voltage level, both the standard NMOS transistor pair and the natural NMOS transistor pair may operate to conduct the current passing through the differential input stage with a first of the transistor pairs conducting a first portion of the current and a second of the transistor pairs conducting a second portion of the current. The first and second portions of the current may be approximately equal or may be different such that one of the portions may be significantly larger than the other portion.

[0011] FIG. 1 is a block diagram of an illustrative differential input stage 100 in accordance with various embodiments. The differential input stage 100 may be implemented as a differential input stage of an amplifier, such as an operational amplifier and/or an operational transconductance

amplifier. In some embodiments, differential input stages 100 are implemented such that multiple amplifications are provided, where each differential input stage 100 may have a same gain or may have a different gain than other differential input stages 100. In other embodiments, the differential input stage may be implemented in devices other than amplifiers, such as any electrical device that receives a differential input signal.

[0012] In some embodiments, the differential input stage 100 comprises an input circuit 110, a cascaded current source 120, and a cascaded current mirror source 130. In some embodiments, the input circuit 110 comprises a plurality of NMOS transistor pairs (not shown) arranged in a differential configuration. While illustrated as receiving one input, in practice the input circuit 110 may receive any number of inputs, the scope of which is not limited herein. Each of the plurality of NMOS transistor pairs may receive a pair of inputs of the differential input stage 100. The inputs may be rail-to-rail inputs that may have a value ranging between approximately zero volts and approximately a source supply voltage of the differential input stage 100. For example, a first NMOS transistor of a NMOS transistor pair may receive a first input and a second NMOS transistor of the NMOS transistor pair may receive a second input. In some embodiments, a number of NMOS transistor pairs in the input circuit 100 may be at least partially determined based on a number of signals desired for the differential input stage 100 to receive and/or process.

[0013] In some embodiments, the cascaded current source 120 couples to the input circuit 110 and provides a tail current for at least some of the NMOS transistor pairs of the input circuit 110. For example, the cascaded current source 120 may provide a path to ground for current to flow from a source supply (not shown) through one or more NMOS transistor pairs of the input circuit 100 and the cascaded current source 120. The cascaded current source 120 may be at least partially controlled by the cascaded current mirror source 130. In some embodiments, the cascaded current mirror source 130 generates one or more reference signals that may bias one or more components of the cascaded current source 120. The biasing may at least partially control an amount of current flowing through components of the cascaded current source 120.

[0014] FIG. 2 is a schematic diagram of the illustrative differential input stage 100 in accordance with various embodiments. In some embodiments, the differential input stage 100 comprises a standard NMOS differential pair 205 (including standard NMOS 210 and standard NMOS 215), a natural NMOS differential pair 220 (including natural NMOS 225 and natural NMOS 230), diodes 235 and 240, constant current source 245 coupled to a voltage supply 247, a cascaded current

mirror source 130 (including NMOS 255 and NMOS 260), and cascaded current source 120 (including NMOS 270, NMOS 275, and NMOS 280). In some embodiments, the standard NMOS differential pair 205 and the natural NMOS differential pair 220 are each configured as a differential amplifier. In some embodiments, the NMOS 210 and NMOS 215 of the standard NMOS differential pair 205 may be referred to as enhancement mode NMOS. In some embodiments, the NMOS 210, NMOS 215, NMOS 225, NMOS 230, diode 235, and diode 240 may together comprise the input circuit 110 of FIG. 1.

[0015] In some embodiments, the NMOS 210 includes a drain terminal coupled to a node 285, a gate terminal configured to receive a first input signal IN1 (e.g., a first portion of a differential input signal), and the NMOS 210 further includes a source terminal coupled to a source terminal of the NMOS 215 and to a drain terminal of the NMOS 275 of the cascaded current source 120. In some embodiments, the NMOS 215 includes a drain terminal coupled to a node 290, a gate terminal configured to receive a second input signal IN2 (e.g., a second portion of the differential input signal), and a source terminal coupled to the source terminal of the NMOS 210 and the drain terminal of the NMOS 275 of the cascaded current source 120. In some embodiments, the NMOS 210 and the NMOS 215 may conduct current from their respective drain terminals to their respective source terminals when they receive voltages at their respective gate terminals that cause their gate to source voltages to exceed their respective activation thresholds. For example, such activation thresholds may be minimum differences in voltages at the respective gate terminals and the respective source terminals that, when exceeded, cause channels to form between the drain and source terminals and current to be conducted between the drain and source terminals. In some embodiments (e.g., such as for the NMOS 210 and the NMOS 215), the activation threshold is 1 volt (V).

[0016] In some embodiments, the NMOS 225 includes a drain terminal coupled to a cathode of the diode 235, a gate terminal configured to receive the first input signal IN1, and a source terminal coupled to a source terminal of the NMOS 230 and a drain terminal of the NMOS 270 of the cascaded current source 120. In some embodiments, the NMOS 230 includes a drain terminal coupled to a cathode of the diode 240, a gate terminal configured to receive the second input signal IN2, and a source terminal coupled to the source terminal of the NMOS 225 and to the drain terminal of the NMOS 270 of the cascaded current source 120. In some embodiments, an anode of the diode 235 is coupled to the node 285 and an anode of the diode 240 is coupled to the node 290.

In some embodiments, an output of the differential input stage 100 is taken across nodes 285 and 290 (e.g., such that a first output of the differential input stage 100 is taken at node 285 and a second output of the differential input stage 100 is taken at node 290). In some embodiments, the NMOS 225 and the NMOS 230 may conduct current from their respective drain terminals to their respective source terminals when they receive voltages at their respective gate terminals that cause their gate to source voltages to exceed their respective activation thresholds. For example, the activation thresholds may be differences in voltages at the respective gate terminals and the respective source terminals. In some embodiments (e.g., such as for the NMOS 225 and the NMOS 230), the activation thresholds may be 0 V. In some embodiments, the NMOS 225 and NMOS 230 of the natural NMOS differential pair 220 may be implemented as depletion mode NMOS transistors. In such embodiments, the activation threshold may be negative.

[0017] In some embodiments, the cascaded current source 120 is coupled between the standard NMOS differential pair 205, the natural NMOS differential pair 220, and a ground voltage potential such that the cascaded current source 120 provides a tail current for the standard NMOS differential pair 205 and the natural NMOS differential pair 220. In some embodiments, drain terminals of the NMOS 270 and the NMOS 275 are coupled as discussed above, a gate terminal of each of the NMOS 270 and the NMOS 275 is coupled to an output of the constant current source 245, and source terminals of the NMOS 270 and the NMOS 275 are coupled to a drain terminal of the NMOS 280. In some embodiments, a gate terminal of the NMOS 280 is coupled to a node 295, and a source terminal of the NMOS 280 is coupled to the ground voltage potential.

[0018] In some embodiments, the cascaded current source 120 may be viewed as two cascaded current sources that share a current output. For example, the NMOS 270 and the NMOS 280 may comprise a first cascaded current source and the NMOS 275 and the NMOS 280 may comprise a second cascaded current source. By implementing the differential input stage 100 using the standard NMOS differential pair 205 and the natural NMOS differential pair 220 and sharing the NMOS 280 between the NMOS 270 and the NMOS 275, the differential input stage 100 may consume less power and less surface area of an electronic circuit (e.g., semiconductor die, printed circuit board, etc.) than another differential input stage in which multiple tail currents are utilized and/or separate cascaded current sources that do not share a current output are utilized. In addition, the differential input stage 100 may be less expensive to manufacture and/or operate than another differential input stage in which multiple tail currents are utilized and/or separate cascaded current

sources that do not share a current output are utilized.

[0019] In some embodiments, the cascaded current mirror source 130 is coupled between the constant current source 245 and the ground voltage potential. In some embodiments, a drain terminal of the NMOS 255 is coupled to the output of the constant current source 245, a gate terminal of the NMOS 255 is coupled to the output of the constant current source 245, and a source terminal of the NMOS 255 is coupled to the node 295. In some embodiments, a drain terminal of the NMOS 260 is coupled to the node 295, a gate terminal of the NMOS 260 is coupled to the node 295, and a source terminal of the NMOS 260 is coupled to the ground voltage potential.

[0020] The cascaded current mirror source 130 provides one or more reference voltages to the current source 120. The reference voltages may be used by the current source 120 as bias voltages for controlling the NMOS 270, NMOS 275, and/or NMOS 280 (e.g., controlling an amount of current flowing through one or more of the NMOS 270, NMOS 275, and/or NMOS 280). In some embodiments, a value of the tail current of the current source 120 is determined at least partially according to the reference voltages provided to the current source 120 by the cascaded current mirror source 130. In some embodiments, the current source 120 provides tail currents for each of the standard NMOS differential pair 205 and the natural NMOS differential pair 220. For example, NMOS 270 and 280 together provide a tail current for the natural NMOS differential pair 220 based at least partially on the reference voltages and NMOS 275 and 280 together provide a tail current for the standard NMOS differential pair 205 based at least partially on the reference voltages. The cascaded current mirror source 130 is configured based at least partially on the cascaded current source 120. For example, the NMOS 255 is selected to have a same transistor width as the NMOS 270, or to have a transistor width that is scaled based on a transistor width of the NMOS 270 such that an approximately same density of current flows through the NMOS 255 and the NMOS 270. For example, a scaling factor of the transistor width of the NMOS 255 with respect to a transistor width of the NMOS 270 may be determined at least partially according to the current provided by the constant current source 245 and a tail current of the cascaded current source 120 (e.g., such as a current flowing through the NMOS 280). In some embodiments, a transistor length of each of the NMOS 255, NMOS 270, and NMOS 275 may be substantially the same.

[0021] In some embodiments, the cascaded current mirror source 130 is omitted from the differential input stage 100. In such embodiments, the cascaded current mirror source 130 may be

replaced, such as by a low voltage cascade circuit (not shown) operable to provide one or more reference voltages to the current source 120 and at least partially upon which the tail currents of the current source 120 may be based. In other embodiments, the cascaded current mirror source 130 may be omitted and the current source 120 may receive one or more reference voltages from any one or more other components or electrical devices, either within or external to the differential input stage 100, that may provide the one or more reference voltages to the current source 120 and at least partially upon which the tail currents of the current source 120 may be based.

[0022] In some embodiments, the NMOS 270 and NMOS 275 may each have transistor widths selected such that, when both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 are conducting current, a majority of the current flowing through the differential input stage 100 flows through the standard NMOS differential pair 205 and the NMOS 275. For example, the transistor width of the NMOS 275 may have an about twenty to one ratio to the transistor width of the NMOS 270 in some embodiments of the differential input stage 100. In such embodiments (e.g., when the twenty to one ratio exists), the NMOS 275 conducts approximately twenty times as much current as the NMOS 270 when both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 are conducting current. In some embodiments, the ratio of the transistor width of the NMOS 275 to the transistor width of the NMOS 270 may be determined according to desired operational characteristics of the differential input stage 100.

[0023] At high input signal voltages, the NMOS 225 and NMOS 230 of the natural NMOS differential pair 220 may each lose their gain characteristics and instead function substantially as resistors (e.g., as a result of a low drain to source voltage difference of the NMOS 225 and the NMOS 230). As such, at high input signal voltages the NMOS 225 and the NMOS 230 may create resistive loading on an output of the differential input stage 100. To prevent this resistive loading, the diodes 235 and 240 may isolate the resistance of the NMOS 225 and NMOS 230 at high input signal voltages from an output of the differential input stage 100. For example, the diode 235 may be coupled between the first output of the differential input stage 100 and a drain terminal of the NMOS 225 and the diode 240 may be coupled between the second output of the differential input stage 100 and a drain terminal of the NMOS 230. The diodes 235 and 240 are oriented in such a manner as to allow current to flow through the NMOS 225 and NMOS 230 (e.g., from the drain terminal to a source terminal of each respective NMOS 225 or NMOS 230) while isolating

electrical characteristics (e.g., such as resistance) or a reverse flow of current of the NMOS 225 and NMOS 230 from the outputs of the differential input stage 100.

[0024] As discussed above, based on a voltage level of an input signal received by the differential input stage 100, one, or both, of the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may be active and conducting current. This functionality enables the differential input stage to function rail-to-rail. To demonstrate this functionality, four operational states of the differential input stage 100 will be discussed below. In the following discussion, it is assumed for each of the four operational states that all characteristics of the differential input stage 100 (e.g., source supply voltage, physical characteristics of components, output of constant current source 245, etc.) remain substantially consistent other than a voltage level of the input signal(s) and/or output signal(s).

[0025] In some embodiments, the differential input stage 100 receives an input signal (e.g., a differential input signal) with a common mode voltage having a high voltage level (e.g., such as a voltage level at or near a voltage level of a source supply coupled to the differential input stage 100). When driven by the input signal having the high voltage level, NMOS 225 and NMOS 230 operate substantially linearly (e.g., in a linear region of the NMOS electrical characteristics of the NMOS 225 and the NMOS 230). This linearity results in NMOS 225 and NMOS 230 no longer imparting a gain on the input signal and instead function substantially as resistors in the differential input stage 100. The diodes 235 and 240 are oriented such that, from a perspective of the NMOS 225 and the NMOS 230, the diodes 235 and 240 are blocking diodes. As such, the diodes 235 and 240 prevent the NMOS 225 and NMOS 230 from creating a loading effect on a remainder of the differential input stage 100 and/or other components which may be coupled to the differential input stage, such as by isolating the resistance of the NMOS 225 and NMOS 230 from the nodes 285 and 290, respectively while still passing through a minimal amount of current (e.g., such as an offset current).

[0026] In such embodiments, only the standard NMOS differential pair 205 provides a gain in the differential input stage 100. Because the NMOS 275 is larger than the NMOS 270 and configured to conduct a majority of current passing through the differential input stage 100, an overall gain provided by the differential input stage 100 remains approximately unchanged despite the natural NMOS differential pair 220 functioning as resistors and providing no gain.

[0027] In other embodiments, the differential input stage 100 may receive an input signal having

a voltage level that is neither high nor low, but which may be closer to the voltage of the source supply than to the ground voltage potential (e.g., the voltage level of the input voltage signal may be greater than one half of the source supply voltage level). In such embodiments, both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may be active and may conduct current. Similarly, in such embodiments, both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may provide a gain in the differential input stage 100. However, the transistor width difference between the NMOS 270 and the NMOS 275 (e.g., where the NMOS 275 has a larger transistor width than the NMOS 270, as discussed above, and therefore conducts a greater amount of current than the NMOS 270) may cause the standard NMOS differential pair 205 to provide a majority of the gain in the differential input stage 100. For example, because of the transistor width difference in the NMOS 270 and the NMOS 275, a majority of the tail current of the differential input stage 100 will flow through the NMOS 275 to the NMOS 280 and correspondingly through the standard NMOS differential pair 205. A ratio of the tail current that flows through the NMOS 275 compared to the tail current that flows through the NMOS 270 may be approximately the same as a ratio of the transistor width of the NMOS 275 to the transistor width of the NMOS 270. For example, for an embodiment of the differential input stage 100 including an NMOS 275 having a transistor width of 20 and an NMOS 270 having a transistor width of 1, approximately 20 times as much of the tail current will flow through the NMOS 275 as flows through the NMOS 270.

[0028] In yet other embodiments, the differential input stage 100 may receive an input signal having a voltage level that is neither high nor low, but may be closer to the ground voltage potential than to the voltage of the source supply (e.g., the voltage level of the input voltage signal may be less than one half of the source supply voltage level). In such embodiments, both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may be active and may conduct current. Similarly, both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may provide a gain in the differential input stage 100.

[0029] In such embodiments, the NMOS 270 may hold the source terminal of the NMOS 275 at a voltage level based on the NMOS 270 (e.g., a gate to source voltage of the NMOS 270). This voltage level, while sufficient to cause the NMOS 275 to conduct current, may be insufficient to cause the NMOS 275 to operate in a saturation region in which a greater amount of current may flow through the NMOS 275. To compensate for the reduced current flow through the NMOS

275, which mitigates the transistor width difference between the NMOS 270 and the NMOS 275, the NMOS 270 conducts an increased amount of current. For example, the NMOS 270 and the NMOS 275 may conduct a similar amount (e.g., an approximately equal amount) of the tail current of the differential input stage 100. Both the standard NMOS differential pair 205 and the natural NMOS differential pair 220 may provide the gain in the differential input stage 100 in approximately equal proportions.

[0030] In yet other embodiments, the differential input stage 100 may receive an input signal having a low voltage level (e.g., such as a voltage level at or near the ground voltage potential that is less than the activation threshold of the NMOS 210 and NMOS 215). When driven by the input signal having the low voltage level, NMOS 210 and NMOS 215 conduct substantially no current from their respective drain terminals to their respective source terminals. For example, because the input signal has a low voltage level that is less than the activation threshold of the NMOS 210 and NMOS 215, the NMOS 210 and NMOS 215 are turned “off.” Conversely, when driven by the input signal having a low voltage level, NMOS 225 and NMOS 230 conduct current from their respective drain terminals to their respective source terminals. Because the NMOS 210 and the NMOS 215 are turned off, only the natural NMOS differential pair 220 provides a gain in the differential input stage 100 and conducts substantially all current passing through the differential input stage 100. An overall gain provided by the differential input stage 100 remains approximately unchanged despite the standard NMOS differential pair 205 being turned off and only the natural NMOS differential pair 220 providing the gain.

[0031] In some embodiments, the differential input stage 100 according to the foregoing description provides a gain for an input signal having a voltage level ranging from low to high using a single tail current, a pair of standard NMOS transistors, and a pair of natural NMOS transistors without requiring the use of PMOS transistors and/or multiple tail currents. In this way, the differential input stage 100 provides a gain for a wide range of input signals by transitioning between the pair of standard NMOS transistors and the pair of natural NMOS transistors based at least partially on the voltage level of the input signal. The differential input stage 100 switches between the standard NMOS differential pair 205 and the natural NMOS differential pair 220, at least in some embodiments, without requiring separate control circuitry to control which of the standard NMOS differential pair 205 or the natural NMOS differential pair 220 are active and providing a gain in the differential input stage 100. Through the use of the standard NMOS

differential pair 205 and the natural NMOS differential pair 220 in place of using one or more PMOS transistors, circuit complexity of the differential input stage 100 may be reduced, size (e.g., footprint or surface area consumed) of the differential input stage 100 may be reduced (e.g., because NMOS transistors have a smaller size than PMOS transistors and/or share a single tail current), and cost may be reduced (e.g., manufacturing and/or operating costs of the differential input stage 100), thereby improving the differential input stage 100 over other devices.

[0032] FIG. 3 is a schematic diagram of an illustrative amplifier 300 in accordance with various embodiments. For example, the amplifier 300 may provide amplification of a received input signal to generate an output signal and/or buffer the input signal to provide as the output signal. Although illustrated in FIG. 3 for the sake of simplicity as receiving input via a single communication line and providing an output via a single output line, the amplifier 300 may receive any number of inputs (e.g., two inputs to form a differential input) and provide any number of outputs. For example, the amplifier 300 may be an operational amplifier and/or an operational transconductance amplifier. The amplifier 300 may be implemented as a standalone device (e.g., implemented on its own die, enclosed within its own chip package, etc.) or may be implemented with other devices (e.g., on a die including other devices, enclosed in a chip package that includes other devices, etc.).

[0033] In some embodiments, the amplifier 300 comprises the differential input stage 100, discussed above with respect to FIG. 1 and FIG. 2, and an output stage 305. In some embodiments, the amplifier 300 may further comprise a plurality of output stages 305. In some embodiments, the amplifier 300 further comprises a reference stage 310. The differential input stage 100 receives an input signal and provides an output to the output stage 305. While illustrated as receiving one input, the differential input stage 100 may receive any number of inputs, the scope of which is not limited herein. The output of the differential input stage 100 is, in some embodiments, an amplification of a difference between a first input received by the differential input stage and a second input received by the differential input stage (e.g., between first and second portions of the received input signal, such as positive and negative components of a differential signal or between an input signal and a feedback signal). The output stage 305 is configured to receive and further amplify (or alternatively, buffer) the output of the differential input stage 100 for providing as an output of the amplifier 300. While illustrated as providing one output, the output stage 305 may provide any number of outputs, the scope of which is not limited herein. For example, the output stage 305 may comprise one or more transistors 315 configured to

further amplify (or buffer) the output of the differential input stage 100. Particular components included in the output stage 305, or a particular structure of the output stage 305, are not limited herein and example embodiments encompass any amplifier output stage coupled to a differential input stage 100 as described herein.

[0034] The reference stage 310, in some embodiments, comprises one or more components (e.g., resistors, capacitor, transistors, etc.) that may be configured to provide a reference signal (e.g., reference current or reference voltage) for use by either, or both, of the differential input stage 100 and/or the output stage 305. Particular components included in the reference stage 310, or a particular structure of the reference stage 310, are not limited herein and example embodiments encompass any amplifier reference stage coupled to a differential input stage 100 as described herein.

[0035] In this description, the term “couple” or “couples” means either an indirect or direct connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. Also, in this description, the phrase “ground voltage potential” includes a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of example embodiments. Unless otherwise stated, in this description, the term “about,” “approximately” or “substantially” relative to a value means +/- 10 percent of that value.

[0036] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A differential input stage comprising:
 - a first n-type metal oxide semiconductor transistor (NMOS) pair coupled to a first input and a second input;
 - a second NMOS pair coupled to the first input, a first output node, the second input, and a second output node;
 - a first diode coupled to the first NMOS pair and the first output node;
 - a second diode coupled to the first NMOS pair and the second output node; and
 - a cascaded current source coupled to the first NMOS pair and the second NMOS pair.
2. The differential input stage of claim 1, wherein the first NMOS pair comprises a first NMOS transistor and a second NMOS transistor configured as a first differential amplifier, wherein the second NMOS pair comprises a third NMOS transistor and a fourth NMOS transistor configured as a second differential amplifier, wherein the first NMOS transistor is coupled to the first input, wherein the second NMOS transistor is coupled to the second input, wherein the third NMOS is coupled to the first input and the first output node, and wherein the fourth NMOS is coupled to the second input and the second output node.
3. The differential input stage of claim 2, wherein the first diode is coupled between the first NMOS transistor and the first output node, and wherein the second diode is coupled between the second NMOS transistor and the second output node.
4. The differential input stage of claim 1, wherein the cascaded current source comprises a fifth NMOS transistor coupled to the first NMOS pair, a sixth NMOS transistor coupled to the second NMOS pair, and a seventh NMOS transistor coupled between the fifth NMOS transistor, the sixth NMOS transistor, and a ground voltage potential.
5. The differential input stage of claim 4, wherein the seventh NMOS transistor is configured to sink a tail current of the first NMOS pair and the second NMOS pair to the ground voltage potential.
6. The differential input stage of claim 4, wherein a transistor width of the sixth NMOS transistor is larger than a transistor width of the fifth NMOS transistor.
7. The differential input stage of claim 6, further comprising a constant current source and a second cascaded current source, wherein the second cascaded current source is coupled between

the constant current source and the ground voltage potential, and wherein the second cascaded current source is further coupled to the cascaded current source and is configured to provide a reference value to the cascaded current source to at least partially control the cascaded current source.

8. The differential input stage of claim 7, wherein the second cascaded current source comprises an eighth NMOS transistor and a ninth NMOS transistor, wherein the eighth NMOS transistor is coupled between the constant current source and the ninth NMOS transistor, and wherein the ninth NMOS transistor is coupled between the eighth NMOS transistor and the ground voltage potential.

9. The differential input stage of claim 8, wherein a transistor width of the eighth NMOS transistor is based on the transistor width of the fifth NMOS transistor to configure the eighth NMOS transistor and the fifth NMOS transistor.

10. The differential input stage of claim 1, wherein the differential input stage is configured to output a signal based on a received input signal, wherein the output signal has a gain determined by the differential input stage, wherein the first NMOS pair contributes a majority of the gain at low input voltage levels, and wherein the second NMOS pair contributes the majority of the gain at high input voltage levels.

11. An amplifier comprising:

a differential input stage comprising: a first n-type metal oxide semiconductor transistor (NMOS) pair coupled to a first input and a second input; a second NMOS pair coupled to the first input, the second input, a first output node, and a second output node; a first diode coupled between the first NMOS pair and the first output node; a second diode coupled between the first NMOS pair and the second output node; and a cascaded current source coupled between the first NMOS pair, the second NMOS pair, and a ground voltage potential; and

an output stage coupled to the first output node and the second output node and comprising at least one transistor configured to amplify an output of the differential input stage present at the first and second output nodes to produce an amplifier output.

12. The amplifier of claim 11, wherein the cascaded current source comprises a first NMOS transistor coupled to the first NMOS pair, a second NMOS transistor coupled to the second NMOS pair, and a third NMOS transistor coupled between the first NMOS transistor, the second NMOS transistor, and the ground voltage potential.

13. The amplifier of claim 12, wherein the first NMOS pair comprises:
a fourth NMOS transistor coupled between the first diode and the first NMOS transistor and to the first input; and
a fifth NMOS transistor coupled between the second diode and the first NMOS transistor and to the second input; and
wherein the second NMOS pair comprises: a sixth NMOS transistor coupled between the first output node and the second NMOS transistor and to the first input; and a seventh NMOS transistor coupled between the second output node and the second NMOS transistor and to the second input.
14. The amplifier of claim 12, wherein the second NMOS transistor has a larger transistor width than the first NMOS transistor.
15. The amplifier of claim 11, wherein the differential input stage further comprises a constant current source and a second cascaded current source comprising an eighth NMOS transistor and a ninth NMOS transistor.
16. The amplifier of claim 15, wherein the constant current source is coupled between a source voltage and the eighth NMOS transistor, and wherein the ninth NMOS transistor is coupled between the eighth NMOS transistor and the ground voltage potential.
17. The amplifier of claim 16, wherein the second cascaded current source is coupled to the cascaded current source and configured to provide a reference value to the cascaded current source to at least partially control the cascaded current source.
18. A differential input stage comprising:
a first diode having a first anode coupled to a first output node;
a second diode having a second anode coupled to a second output node;
a first n-type metal oxide semiconductor (NMOS) differential amplifier comprising:
a first NMOS transistor comprising: a first gate terminal coupled to a first input; a first drain terminal coupled to a cathode of the first diode; and a first source terminal coupled to a first node; and
a second NMOS transistor comprising: a second gate terminal coupled to a second input; a second drain terminal coupled to a cathode of the second diode; and a second source terminal coupled to the first node;

a second NMOS differential amplifier comprising:

- a third NMOS transistor comprising: a third gate terminal coupled to the first input; a third drain terminal coupled to the first output node; and a third source terminal coupled to a second node; and
- a fourth NMOS transistor comprising: a fourth gate terminal coupled to the second input; a fourth drain terminal coupled to the second output node; and a fourth source terminal coupled to the second node; and
- a cascaded current source coupled between the first node, the second node, and a ground voltage potential.

19. The differential input stage of claim 18, wherein the cascaded current source comprises:

- a fifth NMOS transistor comprising: a fifth gate terminal coupled to a third node; a fifth drain terminal coupled to the first node; and a fifth source terminal coupled to a fourth node;

- a sixth NMOS transistor comprising: a sixth gate terminal coupled to the third node; a sixth drain terminal coupled to the second node; and a sixth source terminal coupled to the fourth node; and

- a seventh NMOS transistor comprising: a seventh gate terminal coupled to a fifth node; a seventh drain terminal coupled to the fourth node; and a seventh source terminal coupled to the ground voltage potential.

20. The differential input stage of claim 19, further comprising:

- a constant current source coupled between a voltage source and the third node; and

- a second cascaded current source comprising:

- an eighth NMOS transistor comprising: an eighth gate terminal coupled to the third node; an eighth drain terminal coupled to the third node; and an eighth source terminal coupled to the fifth node; and

- a ninth NMOS transistor comprising: a ninth gate terminal coupled to the fifth node; a ninth drain terminal coupled to the fifth node; and a ninth source terminal coupled to the ground voltage potential.

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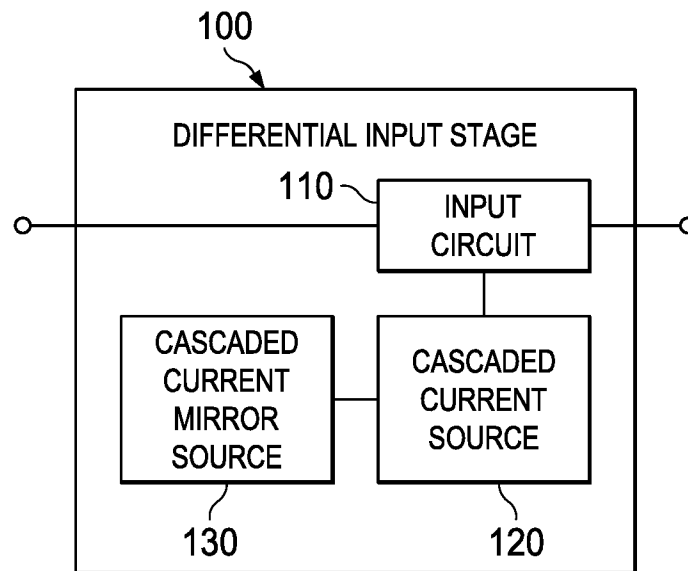


FIG. 1

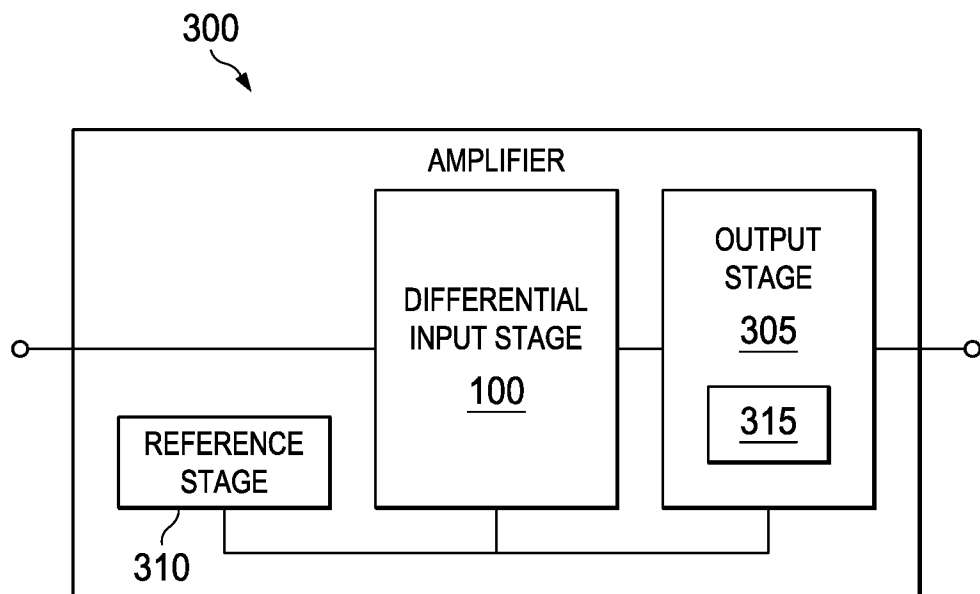
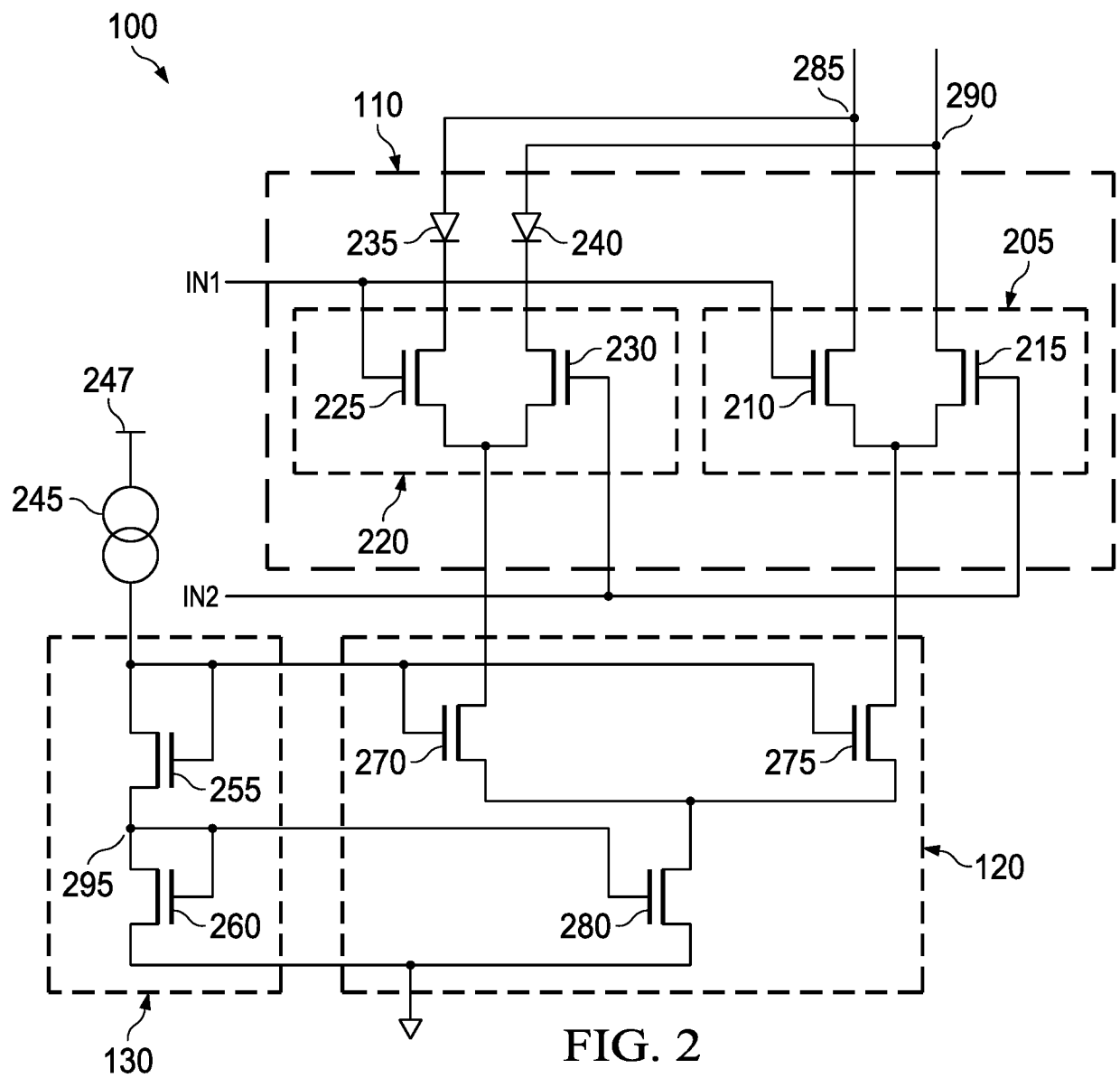


FIG. 3

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2018/059601

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H03F 3/45 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H03F 3/00, 3/45		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8928409 B1 (ION E. OPRIS) 06.01.2015	1-20
A	JP 2010-041131 A (TOSHIBA) 18.02.2010	1-20
A	US 2004/0080369 A1 (PRAVAS PRADHAN et al) 29.04.2004	1-20
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Date of the actual completion of the international search	Date of mailing of the international search report	
19 February 2019 (19.02.2019)	28 February 2019 (28.02.2019)	
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