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(54) Title: VERTICAL SEMICONDUCTOR DEVICES INCLUDING SUPERLATTICE PUNCH THROUGH STOP LAYER AND RELATED METHODS

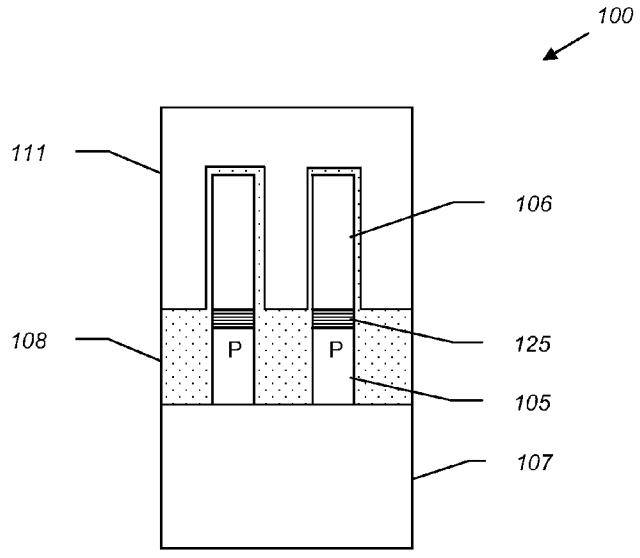

FIG. 6

(57) Abstract: A semiconductor device may include a substrate, and a plurality of fins spaced apart on the substrate. Each of the fins may include a lower semiconductor fin portion extending vertically upward from the substrate, and at least one superlattice punch-through layer on the lower fin portion. The superlattice punch-through layer may include a plurality of stacked groups of layers, with each group of layers of the superlattice punch-through layer comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. Each fin may also include an upper semiconductor fin portion on the at least one superlattice punch-through layer and extending vertically upward therefrom. The semiconductor device may also include source and drain regions at opposing ends of the fins, and a gate overlying the fins.

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VERTICAL SEMICONDUCTOR DEVICES INCLUDING SUPERLATTICE PUNCH THROUGH STOP LAYER AND RELATED METHODS

Field of the Invention

[0001] The present invention relates to the field of semiconductors, and, more particularly, to semiconductor devices comprising superlattices and associated methods.

Background of the Invention

[0002] Structures and techniques have been proposed to enhance the performance of semiconductor devices, such as by enhancing the mobility of the charge carriers. For example, U.S. Patent Application No. 2003/0057416 to Currie et al. discloses strained material layers of silicon, silicon-germanium, and relaxed silicon and also including impurity-free zones that would otherwise cause performance degradation. The resulting biaxial strain in the upper silicon layer alters the carrier mobilities enabling higher speed and/or lower power devices. Published U.S. Patent Application No. 2003/0034529 to Fitzgerald et al. discloses a CMOS inverter also based upon similar strained silicon technology.

[0003] U.S. Patent No. 6,472,685 B2 to Takagi discloses a semiconductor device including a silicon and carbon layer sandwiched between silicon layers so that the conduction band and valence band of the second silicon layer receive a tensile strain. Electrons having a smaller effective mass, and which have been induced by an electric field applied to the gate electrode, are confined in the second silicon layer, thus, an n-channel MOSFET is asserted to have a higher mobility.

[0004] U.S. Patent No. 4,937,204 to Ishibashi et al. discloses a superlattice in which a plurality of layers, less than eight monolayers, and containing a fractional or binary or a binary compound semiconductor layer, are alternately and epitaxially grown. The direction of main current flow is perpendicular to the layers of the superlattice.

[0005] U.S. Patent No. 5,357,119 to Wang et al. discloses a Si-Ge short period superlattice with higher mobility achieved by reducing alloy scattering in the superlattice. Along these lines, U.S. Patent No. 5,683,934 to Candelaria discloses an

enhanced mobility MOSFET including a channel layer comprising an alloy of silicon and a second material substitutionally present in the silicon lattice at a percentage that places the channel layer under tensile stress.

[0006] U.S. Patent No. 5,216,262 to Tsu discloses a quantum well structure comprising two barrier regions and a thin epitaxially grown semiconductor layer sandwiched between the barriers. Each barrier region consists of alternate layers of SiO_2/Si with a thickness generally in a range of two to six monolayers. A much thicker section of silicon is sandwiched between the barriers.

[0007] An article entitled “Phenomena in silicon nanostructure devices” also to Tsu and published online September 6, 2000 by Applied Physics and Materials Science & Processing, pp. 391-402 discloses a semiconductor-atomic superlattice (SAS) of silicon and oxygen. The Si/O superlattice is disclosed as useful in a silicon quantum and light-emitting devices. In particular, a green electromuminescence diode structure was constructed and tested. Current flow in the diode structure is vertical, that is, perpendicular to the layers of the SAS. The disclosed SAS may include semiconductor layers separated by adsorbed species such as oxygen atoms, and CO molecules. The silicon growth beyond the adsorbed monolayer of oxygen is described as epitaxial with a fairly low defect density. One SAS structure included a 1.1 nm thick silicon portion that is about eight atomic layers of silicon, and another structure had twice this thickness of silicon. An article to Luo et al. entitled “Chemical Design of Direct-Gap Light-Emitting Silicon” published in Physical Review Letters, Vol. 89, No. 7 (August 12, 2002) further discusses the light emitting SAS structures of Tsu.

[0008] Published International Application WO 02/103,767 A1 to Wang, Tsu and Lofgren, discloses a barrier building block of thin silicon and oxygen, carbon, nitrogen, phosphorous, antimony, arsenic or hydrogen to thereby reduce current flowing vertically through the lattice more than four orders of magnitude. The insulating layer/barrier layer allows for low defect epitaxial silicon to be deposited next to the insulating layer.

[0009] Published Great Britain Patent Application 2,347,520 to Mears et al. discloses that principles of Aperiodic Photonic Band-Gap (APBG) structures may be adapted for electronic bandgap engineering. In particular, the application discloses that material parameters, for example, the location of band minima, effective mass,

etc, can be tailored to yield new aperiodic materials with desirable band-structure characteristics. Other parameters, such as electrical conductivity, thermal conductivity and dielectric permittivity or magnetic permeability are disclosed as also possible to be designed into the material.

[0010] Despite the advantages provided by such structures, further developments may be desirable for integrating advanced semiconductor materials in various semiconductor devices.

Summary

[0011] A method for making a semiconductor device may include forming a plurality of fins on a substrate. The fins may be formed by forming a plurality of spaced apart lower semiconductor fin portions extending vertically upward from the substrate, and forming at least one respective superlattice punch-through stop layer on each of the lower fin portions. Each superlattice punch-through stop layer may include a plurality of stacked groups of layers, with each group of layers of the superlattice punch-through stop layer comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. A respective upper semiconductor fin portion may be formed above each of the at least one superlattice punch-through stop layers and extending vertically upward therefrom. The method may also include forming source and drain regions at opposing ends of the fins, and forming a gate overlying the fins.

[0012] More particularly, forming the at least one respective superlattice punch-through stop layer may include forming a respective plurality of vertically stacked superlattice punch-through stop layers on each of the lower fin portions with a respective semiconductor layer between each of the superlattice punch-through stop layers. The method may also include forming an insulating layer on the substrate surrounding the lower semiconductor fin portions.

[0013] By way of example, forming the plurality of fins may further include forming a superlattice layer on the substrate, epitaxially growing a bulk semiconductor layer on the superlattice layer, and etching a plurality of spaced apart trenches extending through the bulk semiconductor layer, the superlattice layer, and into the substrate to define the respective lower semiconductor fin portions, superlattice punch-through stop layers, and upper semiconductor fin portions. The

method may further include performing a thermal anneal after forming the plurality of fins.

[0014] Each base semiconductor portion may comprise silicon, germanium, etc. The at least one non-semiconductor monolayer may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen, for example. Furthermore, the gate may include an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer. Moreover, at least some semiconductor atoms from opposing base semiconductor portions may be chemically bound together through the non-semiconductor layer therebetween.

[0015] A related semiconductor device may include a substrate, and a plurality of fins spaced apart on the substrate. Each of the fins may include a lower semiconductor fin portion extending vertically upward from the substrate, and at least one superlattice punch-through stop layer on the lower fin portion. The superlattice punch-through stop layer may include a plurality of stacked groups of layers, with each group of layers of the superlattice punch-through stop layer comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. Each fin may also include an upper semiconductor fin portion above the at least one superlattice punch-through stop layer and extending vertically upward therefrom. The semiconductor device may also include source and drain regions at opposing ends of the fins, and a gate overlying the fins.

Brief Description of the Drawings

[0016] FIG. 1 is a greatly enlarged schematic cross-sectional view of a superlattice for use in a semiconductor device in accordance with the present invention.

[0017] FIG. 2 is a perspective schematic atomic diagram of a portion of the superlattice shown in FIG. 1.

[0018] FIG. 3 is a greatly enlarged schematic cross-sectional view of another embodiment of a superlattice in accordance with the invention.

[0019] FIG. 4A is a graph of the calculated band structure from the gamma point (G) for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. 1-2.

[0020] FIG. 4B is a graph of the calculated band structure from the Z point for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. 1-2.

[0021] FIG. 4C is a graph of the calculated band structure from both the gamma and Z points for both bulk silicon as in the prior art, and for the 5/1/3/1 Si/O superlattice as shown in FIG. 3.

[0022] FIG. 5 is a top plan view of a semiconductor device in accordance with an example embodiment including superlattice punch through stop layers.

[0023] FIGS. 6 is a cross-sectional view of the semiconductor device of FIG. 5 taken along the line A-A'.

[0024] FIG. 7 is a cross-sectional view of another example semiconductor device similar to that of FIG. 5 and taken along the line B-B'.

[0025] FIG. 8 is a cross-sectional view of yet another semiconductor device similar to that of FIG. 5 and taken along the line A-A'.

[0026] FIG. 9a is a flow diagram illustrating a method for making a semiconductor device similar to that of FIG. 5.

[0027] FIGS. 9b(i)-9b(iv) are a series of cross-sectional diagrams corresponding to the method steps illustrated in FIG. 9a.

Detailed Description

[0028] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout, and prime notation is used to indicate similar elements in different embodiments.

[0029] The present invention relates to controlling the properties of semiconductor materials at the atomic or molecular level. Further, the invention

relates to the identification, creation, and use of improved materials for use in semiconductor devices.

[0030] Applicants theorize, without wishing to be bound thereto, that certain superlattices as described herein reduce the effective mass of charge carriers and that this thereby leads to higher charge carrier mobility. Effective mass is described with various definitions in the literature. As a measure of the improvement in effective mass Applicants use a "conductivity reciprocal effective mass tensor", $\mathbf{M}_e^{-1}$ and $\mathbf{M}_h^{-1}$ for electrons and holes respectively, defined as:

$$\mathbf{M}_{e,ij}^{-1}(E_F,T) = \frac{\sum_{E>E_F} \int_{B.Z.} \left(\nabla_{\mathbf{k}} E(\mathbf{k},n)\right)_i \left(\nabla_{\mathbf{k}} E(\mathbf{k},n)\right)_j \frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E} d^3\mathbf{k}}{\sum_{E>E_F} \int_{B.Z.} f(E(\mathbf{k},n),E_F,T)\, d^3\mathbf{k}}$$

for electrons and:

$$\mathbf{M}_{h,ij}^{-1}(E_F,T) = \frac{-\sum_{E<E_F} \int_{B.Z.} \left(\nabla_{\mathbf{k}} E(\mathbf{k},n)\right)_i \left(\nabla_{\mathbf{k}} E(\mathbf{k},n)\right)_j \frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E} d^3\mathbf{k}}{\sum_{E<E_F} \int_{B.Z.} (1-f(E(\mathbf{k},n),E_F,T))\, d^3\mathbf{k}}$$

for holes, where *f* is the Fermi-Dirac distribution, E_F is the Fermi energy, T is the temperature, E(**k**,n) is the energy of an electron in the state corresponding to wave vector **k** and the n^{th} energy band, the indices i and j refer to Cartesian coordinates x, y and z, the integrals are taken over the Brillouin zone (B.Z.), and the summations are taken over bands with energies above and below the Fermi energy for electrons and holes respectively.

[0031] Applicants' definition of the conductivity reciprocal effective mass tensor is such that a tensorial component of the conductivity of the material is greater for greater values of the corresponding component of the conductivity reciprocal effective mass tensor. Again Applicants theorize without wishing to be bound thereto that the superlattices described herein set the values of the conductivity reciprocal effective mass tensor so as to enhance the conductive

properties of the material, such as typically for a preferred direction of charge carrier transport. The inverse of the appropriate tensor element is referred to as the conductivity effective mass. In other words, to characterize semiconductor material structures, the conductivity effective mass for electrons/holes as described above and calculated in the direction of intended carrier transport is used to distinguish improved materials.

[0032] Applicants have identified improved materials or structures for use in semiconductor devices. More specifically, the Applicants have identified materials or structures having energy band structures for which the appropriate conductivity effective masses for electrons and/or holes are substantially less than the corresponding values for silicon. In addition to the enhanced mobility characteristics of these structures, they may also be formed or used in such a manner that they provide piezoelectric, pyroelectric, and/or ferroelectric properties that are advantageous for use in a variety of different types of devices, as will be discussed further below.

[0033] Referring now to FIGS. 1 and 2, the materials or structures are in the form of a superlattice **25** whose structure is controlled at the atomic or molecular level and may be formed using known techniques of atomic or molecular layer deposition. The superlattice **25** includes a plurality of layer groups **45a-45n** arranged in stacked relation, as perhaps best understood with specific reference to the schematic cross-sectional view of FIG. 1.

[0034] Each group of layers **45a-45n** of the superlattice **25** illustratively includes a plurality of stacked base semiconductor monolayers **46** defining a respective base semiconductor portion **46a-46n** and an energy band-modifying layer **50** thereon. The energy band-modifying layers **50** are indicated by stippling in FIG. 1 for clarity of illustration.

[0035] The energy band-modifying layer **50** illustratively includes one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. By “constrained within a crystal lattice of adjacent base semiconductor portions” it is meant that at least some semiconductor atoms from opposing base semiconductor portions **46a-46n** are chemically bound together through the non-semiconductor monolayer **50** therebetween, as seen in FIG. 2. Generally speaking, this configuration is made possible by controlling the amount of

non-semiconductor material that is deposited on semiconductor portions **46a-46n** through atomic layer deposition techniques so that not all (i.e., less than full or 100% coverage) of the available semiconductor bonding sites are populated with bonds to non-semiconductor atoms, as will be discussed further below. Thus, as further monolayers **46** of semiconductor material are deposited on or over a non-semiconductor monolayer **50**, the newly deposited semiconductor atoms will populate the remaining vacant bonding sites of the semiconductor atoms below the non-semiconductor monolayer.

[0036] In other embodiments, more than one such non-semiconductor monolayer may be possible. It should be noted that reference herein to a non-semiconductor or semiconductor monolayer means that the material used for the monolayer would be a non-semiconductor or semiconductor if formed in bulk. That is, a single monolayer of a material, such as silicon, may not necessarily exhibit the same properties that it would if formed in bulk or in a relatively thick layer, as will be appreciated by those skilled in the art.

[0037] Applicants theorize without wishing to be bound thereto that energy band-modifying layers **50** and adjacent base semiconductor portions **46a-46n** cause the superlattice **25** to have a lower appropriate conductivity effective mass for the charge carriers in the parallel layer direction than would otherwise be present. Considered another way, this parallel direction is orthogonal to the stacking direction. The band modifying layers **50** may also cause the superlattice **25** to have a common energy band structure, while also advantageously functioning as an insulator between layers or regions vertically above and below the superlattice.

[0038] Moreover, this superlattice structure may also advantageously act as a barrier to dopant and/or material diffusion between layers vertically above and below the superlattice **25**. These properties may thus advantageously allow the superlattice **25** to provide an interface for high-K dielectrics which not only reduces diffusion of the high-K material into the channel region, but which may also advantageously reduce unwanted scattering effects and improve device mobility, as will be appreciated by those skilled in the art.

[0039] It is also theorized that semiconductor devices including the superlattice **25** may enjoy a higher charge carrier mobility based upon the lower conductivity effective mass than would otherwise be present. In some embodiments,

and as a result of the band engineering achieved by the present invention, the superlattice **25** may further have a substantially direct energy bandgap that may be particularly advantageous for opto-electronic devices, for example.

[0040] The superlattice **25** also illustratively includes a cap layer **52** on an upper layer group **45n**. The cap layer **52** may comprise a plurality of base semiconductor monolayers **46**. The cap layer **52** may have between 2 to 100 monolayers of the base semiconductor, and, more preferably between 10 to 50 monolayers.

[0041] Each base semiconductor portion **46a-46n** may comprise a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors. Of course, the term Group IV semiconductors also includes Group IV-IV semiconductors, as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example.

[0042] Each energy band-modifying layer **50** may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, carbon and carbon-oxygen, for example. The non-semiconductor is also desirably thermally stable through deposition of a next layer to thereby facilitate manufacturing. In other embodiments, the non-semiconductor may be another inorganic or organic element or compound that is compatible with the given semiconductor processing as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example

[0043] It should be noted that the term monolayer is meant to include a single atomic layer and also a single molecular layer. It is also noted that the energy band-modifying layer **50** provided by a single monolayer is also meant to include a monolayer wherein not all of the possible sites are occupied (i.e., there is less than full or 100% coverage). For example, with particular reference to the atomic diagram of FIG. 2, a 4/1 repeating structure is illustrated for silicon as the base semiconductor material, and oxygen as the energy band-modifying material. Only half of the possible sites for oxygen are occupied in the illustrated example.

[0044] In other embodiments and/or with different materials this one-half occupation would not necessarily be the case as will be appreciated by those skilled

in the art. Indeed it can be seen even in this schematic diagram, that individual atoms of oxygen in a given monolayer are not precisely aligned along a flat plane as will also be appreciated by those of skill in the art of atomic deposition. By way of example, a preferred occupation range is from about one-eighth to one-half of the possible oxygen sites being full, although other numbers may be used in certain embodiments.

[0045] Silicon and oxygen are currently widely used in conventional semiconductor processing, and, hence, manufacturers will be readily able to use these materials as described herein. Atomic or monolayer deposition is also now widely used. Accordingly, semiconductor devices incorporating the superlattice **25** in accordance with the invention may be readily adopted and implemented, as will be appreciated by those skilled in the art.

[0046] It is theorized without Applicants wishing to be bound thereto that for a superlattice, such as the Si/O superlattice, for example, that the number of silicon monolayers should desirably be seven or less so that the energy band of the superlattice is common or relatively uniform throughout to achieve the desired advantages. The 4/1 repeating structure shown in FIGS. 1 and 2, for Si/O has been modeled to indicate an enhanced mobility for electrons and holes in the X direction. For example, the calculated conductivity effective mass for electrons (isotropic for bulk silicon) is 0.26 and for the 4/1 SiO superlattice in the X direction it is 0.12 resulting in a ratio of 0.46. Similarly, the calculation for holes yields values of 0.36 for bulk silicon and 0.16 for the 4/1 Si/O superlattice resulting in a ratio of 0.44.

[0047] While such a directionally preferential feature may be desired in certain semiconductor devices, other devices may benefit from a more uniform increase in mobility in any direction parallel to the groups of layers. It may also be beneficial to have an increased mobility for both electrons or holes, or just one of these types of charge carriers as will be appreciated by those skilled in the art.

[0048] The lower conductivity effective mass for the 4/1 Si/O embodiment of the superlattice **25** may be less than two-thirds the conductivity effective mass than would otherwise occur, and this applies for both electrons and holes. Of course, the superlattice **25** may further comprise at least one type of conductivity dopant therein, as will also be appreciated by those skilled in the art.

[0049] Indeed, referring now additionally to FIG. 3, another embodiment of a superlattice **25'** in accordance with the invention having different properties is now described. In this embodiment, a repeating pattern of 3/1/5/1 is illustrated. More particularly, the lowest base semiconductor portion **46a'** has three monolayers, and the second lowest base semiconductor portion **46b'** has five monolayers. This pattern repeats throughout the superlattice **25'**. The energy band-modifying layers **50'** may each include a single monolayer. For such a superlattice **25'** including Si/O, the enhancement of charge carrier mobility is independent of orientation in the plane of the layers. Those other elements of FIG. 3 not specifically mentioned are similar to those discussed above with reference to FIG. 1 and need no further discussion herein.

[0050] In some device embodiments, all of the base semiconductor portions of a superlattice may be a same number of monolayers thick. In other embodiments, at least some of the base semiconductor portions may be a different number of monolayers thick. In still other embodiments, all of the base semiconductor portions may be a different number of monolayers thick.

[0051] In FIGS. 4A-4C, band structures calculated using Density Functional Theory (DFT) are presented. It is well known in the art that DFT underestimates the absolute value of the bandgap. Hence all bands above the gap may be shifted by an appropriate "scissors correction." However the shape of the band is known to be much more reliable. The vertical energy axes should be interpreted in this light.

[0052] FIG. 4A shows the calculated band structure from the gamma point (G) for both bulk silicon (represented by continuous lines) and for the 4/1 Si/O superlattice **25** shown in FIG. 1 (represented by dotted lines). The directions refer to the unit cell of the 4/1 Si/O structure and not to the conventional unit cell of Si, although the (001) direction in the figure does correspond to the (001) direction of the conventional unit cell of Si, and, hence, shows the expected location of the Si conduction band minimum. The (100) and (010) directions in the figure correspond to the (110) and (-110) directions of the conventional Si unit cell. Those skilled in the art will appreciate that the bands of Si on the figure are folded to represent them on the appropriate reciprocal lattice directions for the 4/1 Si/O structure.

[0053] It can be seen that the conduction band minimum for the 4/1 Si/O structure is located at the gamma point in contrast to bulk silicon (Si), whereas the

valence band minimum occurs at the edge of the Brillouin zone in the (001) direction which we refer to as the Z point. One may also note the greater curvature of the conduction band minimum for the 4/1 Si/O structure compared to the curvature of the conduction band minimum for Si owing to the band splitting due to the perturbation introduced by the additional oxygen layer.

[0054] FIG. 4B shows the calculated band structure from the Z point for both bulk silicon (continuous lines) and for the 4/1 Si/O superlattice **25** (dotted lines). This figure illustrates the enhanced curvature of the valence band in the (100) direction.

[0055] FIG. 4C shows the calculated band structure from both the gamma and Z point for both bulk silicon (continuous lines) and for the 5/1/3/1 Si/O structure of the superlattice **25'** of FIG. 3 (dotted lines). Due to the symmetry of the 5/1/3/1 Si/O structure, the calculated band structures in the (100) and (010) directions are equivalent. Thus the conductivity effective mass and mobility are expected to be isotropic in the plane parallel to the layers, i.e. perpendicular to the (001) stacking direction. Note that in the 5/1/3/1 Si/O example the conduction band minimum and the valence band maximum are both at or close to the Z point.

[0056] Although increased curvature is an indication of reduced effective mass, the appropriate comparison and discrimination may be made via the conductivity reciprocal effective mass tensor calculation. This leads Applicants to further theorize that the 5/1/3/1 superlattice **25'** should be substantially direct bandgap. As will be understood by those skilled in the art, the appropriate matrix element for optical transition is another indicator of the distinction between direct and indirect bandgap behavior.

[0057] Using the above-described measures, one can select materials having improved band structures for specific purposes. Referring more particularly to FIGS. 5 and 6, a first example would be a superlattice material layer **125** in a vertical semiconductor device **100**, such as a FINFET, in which the superlattice material layer is used for dopant blocking within each semiconductor fin **104**. More particularly, it may generally be desirable to dope a bottom portion **105** of a fin **104** to help reduce leakage (a P-type dopant is used in the illustrated NMOS embodiment, but an N-type dopant may be used for a PMOS device, as will be discussed further below). However, it may also be desirable to have an upper channel portion **106** of the fin **104** remain undoped, but it may be difficult to prevent dopant creep from the

bottom of the fin **105** into the upper channel portion of the fin. The superlattice layer **125** may advantageously provide a self-aligned punch-through stop layer for preventing dopant from the lower portion **105** of the fin **104** from creeping into the upper undoped portion **106** of the fin, in addition to the leakage reduction properties of the superlattice itself, as described above. The upper (undoped) portion **106** of each fin **104** may advantageously be epitaxially grown on top of a respective superlattice layer **125**, as also described above.

[0058] The fins **104** are formed on a substrate **107** (e.g., silicon substrate), and a source and drain regions **109**, **110** are formed at opposing ends of the fins **104** (see FIG. 5). An insulating layer **108** (e.g., SiO_2) is formed over the fins **104** and source and drain regions **109**, **110**. Moreover, a gate **111** is formed overlying the fins **104** and the insulating layer **108**.

[0059] A second related example embodiment is shown in FIG. 7, in which a vertical device **100'** includes a "quasi-BOX" structure below the upper channel portion **106'**, in which a series of vertically spaced-apart superlattice layers **125'** have regions or layers **112'**, **113'** of a bulk semiconductor (e.g., Si) stacked therebetween and with alternating dopant types. In the illustrated example, the stack includes a bottom superlattice layer **125'** on the Si substrate **107'**, an N-type Si layer **112'** on the bottom superlattice layer, an intermediate superlattice layer on the N-type Si layer, a P-type Si layer **113'** on the intermediate superlattice layer, and an upper superlattice layer on the P-type Si layer. The Si channel **106'** may advantageously be grown on top of the upper superlattice layer **125'**, as noted above. However, in some embodiments the channel may reside partially or completely in the upper superlattice layer **125'**, if desired. This quasi-BOX structure may conceptually be considered to perform a similar function to a buried oxide (BOX) layer, but here the quasi-BOX stack provides an added benefit of an embedded P-N junction to provide further isolation of the channel region, as will be appreciated by those skilled in the art.

[0060] In accordance with a third example as described with reference to FIG. 8, a "quasi-planar" semiconductor device **100''** is similar to the FINFET embodiment described above with respect to FIG. 6, but with a shorter and wider profile for the fins. This embodiment may be advantageous in certain implementations, as it may help relax fin patterning requirements, for example.

[0061] An example method for making a CMOS version of the semiconductor device **100** will now be described with reference to FIGS. 9a and 9b. Beginning at Block **201**, a blanket superlattice layer **125** may be formed on a silicon substrate **107**, followed by an epitaxial silicon growth above the superlattice layer (FIG. 9b, (i)). Deep punch-through stop implants (e.g., N-type for PMOS, P-type for NMOS) may then be performed at Block **202** (FIG. 9b, (ii)), followed by a fin **104** patterning/isolation processing module, at Block **203** (FIG. 9b, (iii)). Gate **111** and source/drain **109**, **110** processing may then be performed using typical steps for FINFET processing, for example, at Blocks **204**-**205** (FIG. 9b, (iv)).

[0062] Many modifications and other embodiments will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

THAT WHICH IS CLAIMED IS:

1. A method for making a semiconductor device comprising:

forming a plurality of fins on a substrate by

forming a plurality of spaced apart lower semiconductor fin portions extending vertically upward from the substrate,

forming at least one respective superlattice punch-through stop layer on each of the lower fin portions, each superlattice punch-through stop layer including a plurality of stacked groups of layers, each group of layers of the superlattice punch-through stop layer comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions, and

forming a respective upper semiconductor fin portion on each of the at least one superlattice punch-through stop layers and extending vertically upward therefrom;

forming source and drain regions at opposing ends of the fins; and

forming a gate overlying the fins.

2. The method of Claim 1 wherein forming the at least one respective superlattice punch-through stop layer comprises forming a respective plurality of vertically stacked superlattice punch-through stop layers on each of the lower fin portions with a respective semiconductor layer between each of the superlattice punch-through stop layers.

3. The method of Claim 1 further comprising forming an insulating layer on the substrate surrounding the lower semiconductor fin portions.

4. The method of Claim 1 wherein forming the plurality of fins further comprises:

forming a superlattice layer on the substrate;

epitaxially growing a bulk semiconductor layer on the superlattice layer; and

etching a plurality of spaced apart trenches extending through the bulk semiconductor layer, the superlattice layer, and into the substrate to simultaneously

define the respective lower semiconductor fin portions, superlattice punch-through stop layers, and upper semiconductor fin portions.

5. The method of Claim 1 further comprising performing a thermal anneal after forming the plurality of fins.

6. The method of Claim 1 wherein each base semiconductor portion comprises silicon.

7. The method of Claim 1 wherein each base semiconductor portion comprises germanium.

8. The method of Claim 1 wherein the at least one non-semiconductor layer comprises oxygen.

9. The method of Claim 1 wherein the at least one non-semiconductor monolayer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

10. The method of Claim 1 wherein the gate comprises an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer.

11. The method of Claim 1 wherein at least some semiconductor atoms from opposing base semiconductor portions are chemically bound together through the non-semiconductor layer therebetween.

12. A semiconductor device comprising:

a substrate;

a plurality of fins spaced apart on said substrate, each of said fins comprising

a lower semiconductor fin portion extending vertically upward from the substrate,

at least one superlattice punch-through stop layer on the lower fin portion, said superlattice punch-through stop layer including a plurality of stacked groups of layers, each group of layers of the superlattice punch-through stop layer comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions, and

an upper semiconductor fin portion on said at least one superlattice punch-through stop layer and extending vertically upward therefrom;

source and drain regions at opposing ends of the fins; and

a gate overlying the fins.

13. The semiconductor device of Claim 12 wherein the at least one respective superlattice punch-through stop layer comprises a respective plurality of vertically stacked superlattice punch-through stop layers on each of the lower fin portions with a respective bulk semiconductor layer between each of the superlattice punch-through stop layers.

14. The semiconductor device of Claim 12 further comprising an insulating layer on the substrate surrounding the lower semiconductor fin portions.

15. The semiconductor device of Claim 12 wherein each base semiconductor portion comprises silicon.

16. The semiconductor device of Claim 12 wherein each base semiconductor portion comprises germanium.

17. The semiconductor device of Claim 12 wherein the at least one non-semiconductor layer comprises oxygen.

18. The semiconductor device of Claim 12 wherein the at least one non-semiconductor monolayer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

19. The semiconductor device of Claim 12 wherein the gate comprises an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer.

20. The semiconductor device of Claim 12 wherein at least some semiconductor atoms from opposing base semiconductor portions are chemically bound together through the non-semiconductor layer therebetween.

21. A semiconductor device comprising:

a substrate;

a plurality of fins spaced apart on said substrate, each of said fins comprising

a lower semiconductor fin portion extending vertically upward from the substrate,

at least one superlattice punch-through stop layer on the lower fin portion, said superlattice punch-through stop layer including a plurality of stacked groups of layers, each group of layers of the superlattice punch-through stop layer comprising a plurality of stacked base silicon monolayers defining a base silicon portion and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions, and

an upper semiconductor fin portion on said at least one superlattice punch-through stop layer and extending vertically upward therefrom;

source and drain regions at opposing ends of the fins; and

a gate overlying the fins.

22. The semiconductor device of Claim 12 wherein the at least one respective superlattice punch-through stop layer comprises a respective plurality of vertically stacked superlattice punch-through stop layers on each of the lower fin portions with a respective bulk semiconductor layer between each of the superlattice punch-through stop layers.

23. The semiconductor device of Claim 12 further comprising an insulating layer on the substrate surrounding the lower semiconductor fin portions.

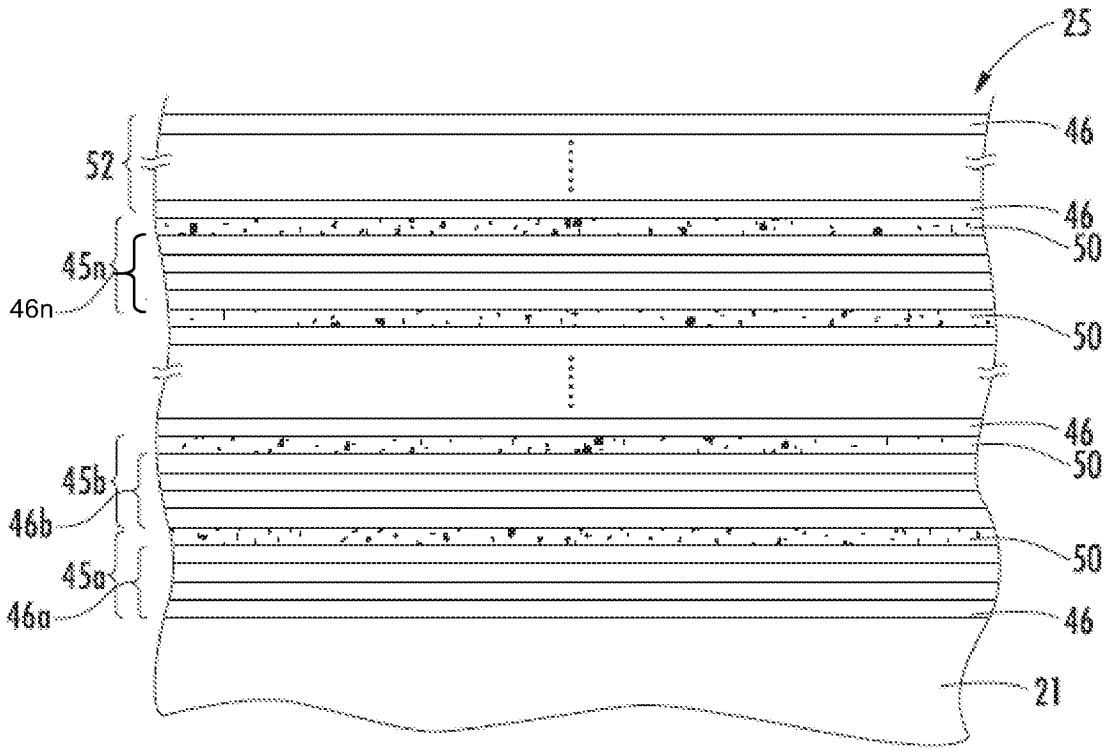

FIG. 1

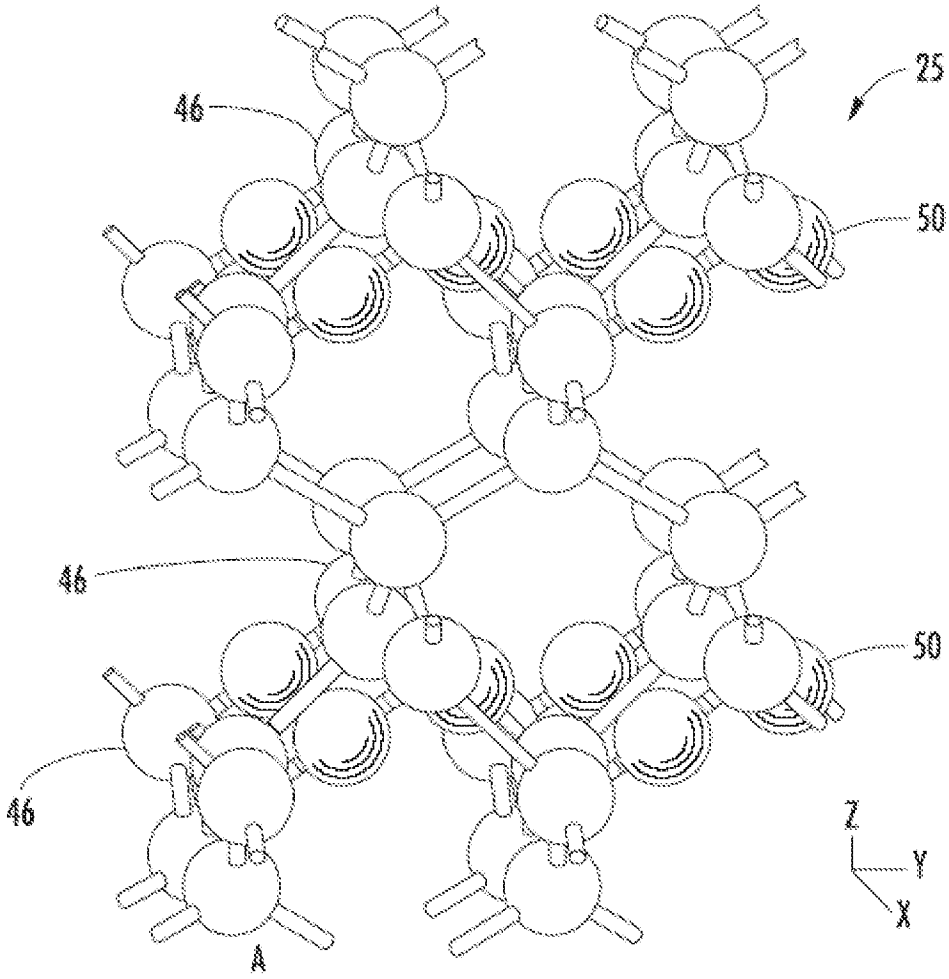

FIG. 2

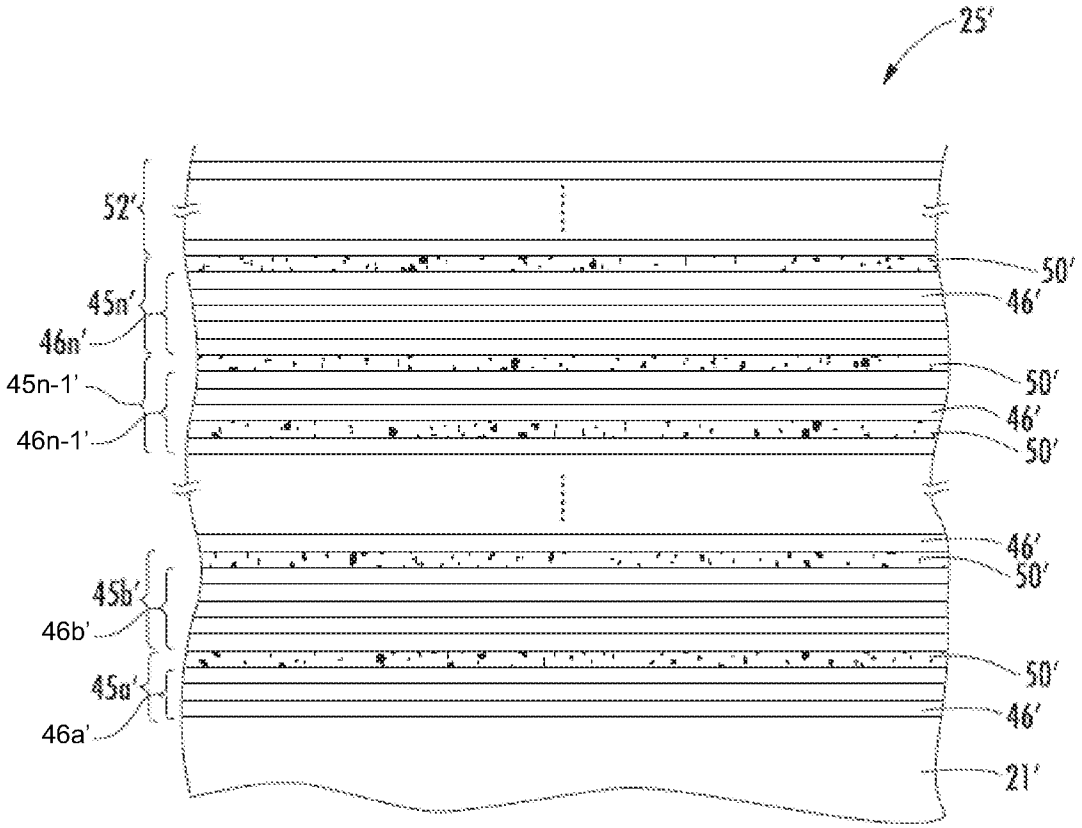
25'
52'
45n'
46n'
45n-1'
46n-1'
50'
46'
50'
46'
50'
46'
50'
45b'
46b'
45a'
46a'
50'
46'
21'

FIG. 3

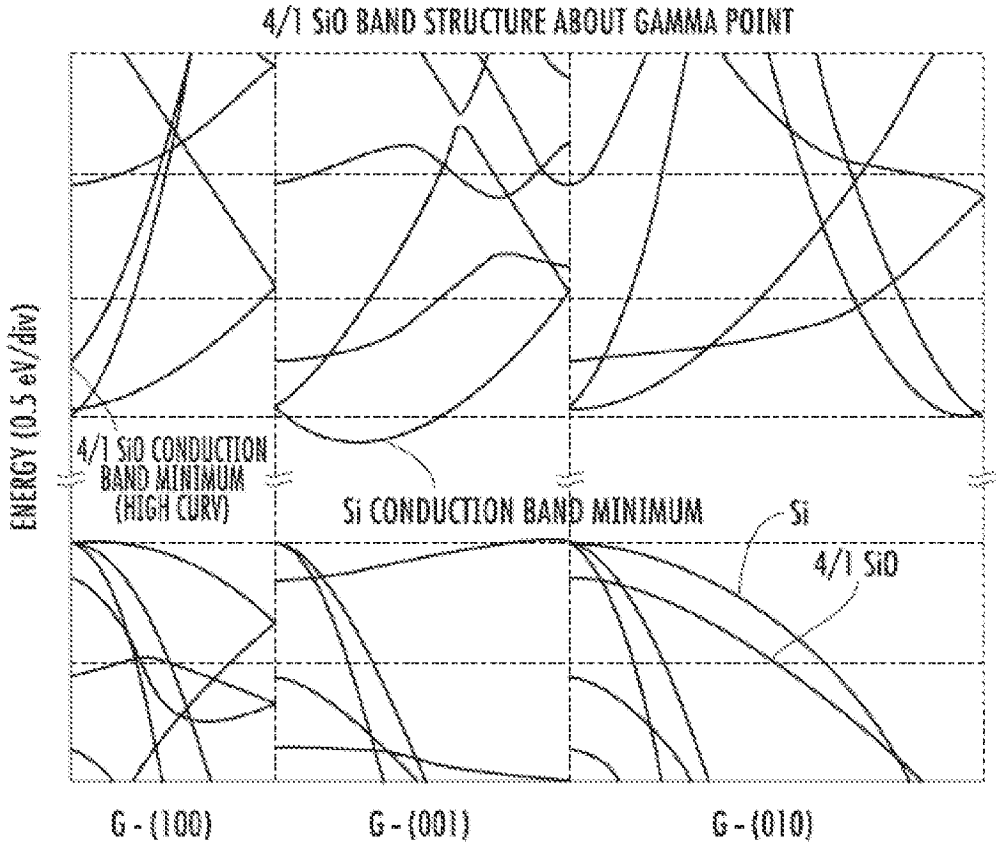
4/1 SiO BAND STRUCTURE ABOUT GAMMA POINT
ENERGY (0.5 eV/div)
4/1 SiO CONDUCTION BAND MINIMUM (HIGH CURV)
Si CONDUCTION BAND MINIMUM
Si
4/1 SiO
G - (100)
G - (001)
G - (010)

FIG. 4A

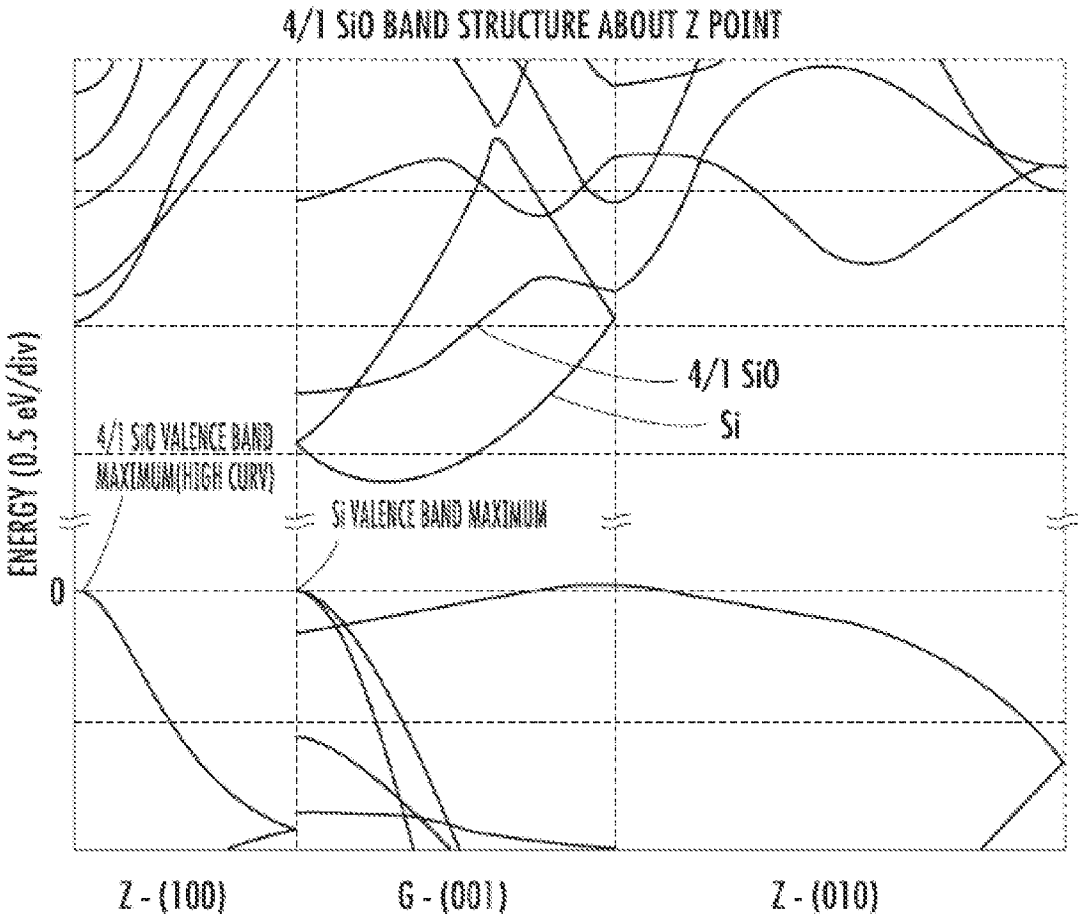
4/1 SiO BAND STRUCTURE ABOUT Z POINT
ENERGY (0.5 eV/div)
0
4/1 SiO
Si
4/1 SiO VALENCE BAND MAXIMUM(HIGH CURV)
Si VALENCE BAND MAXIMUM
Z - (100)
G - (001)
Z - (010)

FIG. 4B

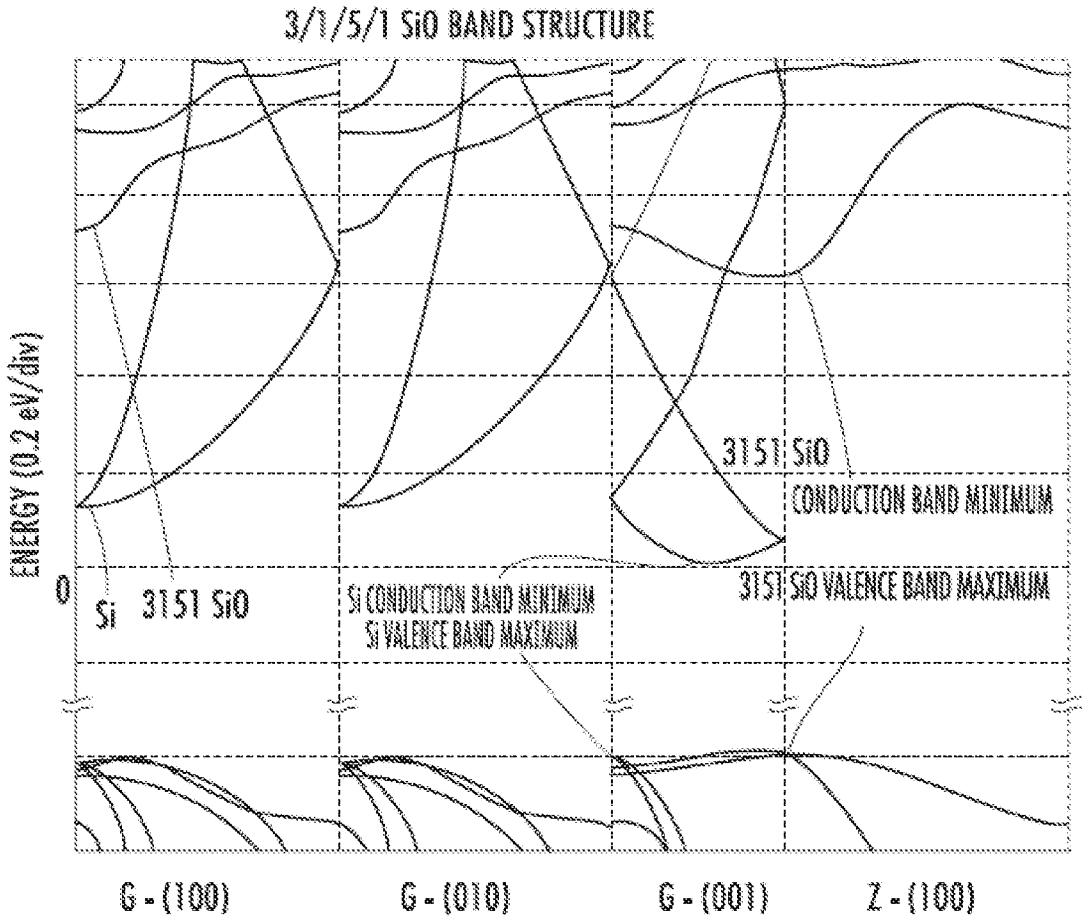
3/1/5/1 SiO BAND STRUCTURE
ENERGY (0.2 eV/div)
0
Si
3151 SiO
Si CONDUCTION BAND MINIMUM
Si VALENCE BAND MAXIMUM
3151 SiO
CONDUCTION BAND MINIMUM
3151 SiO VALENCE BAND MAXIMUM
G - (100)
G - (010)
G - (001)
Z - (100)

FIG. 4C

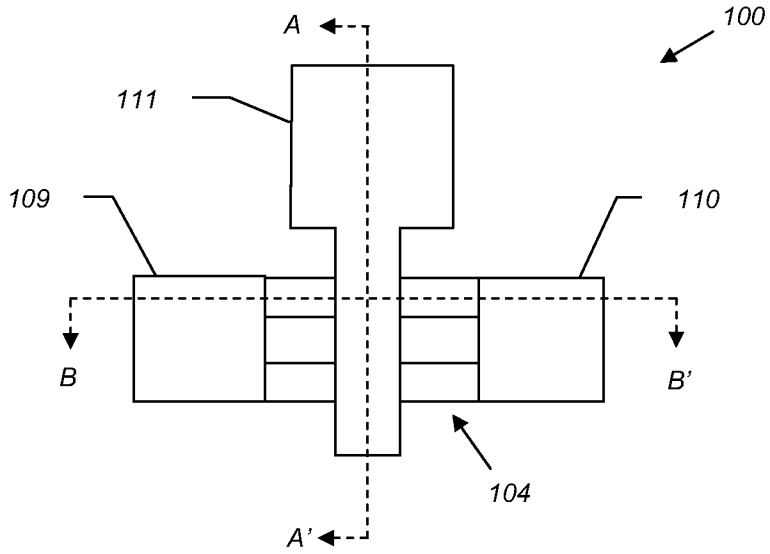

FIG. 5

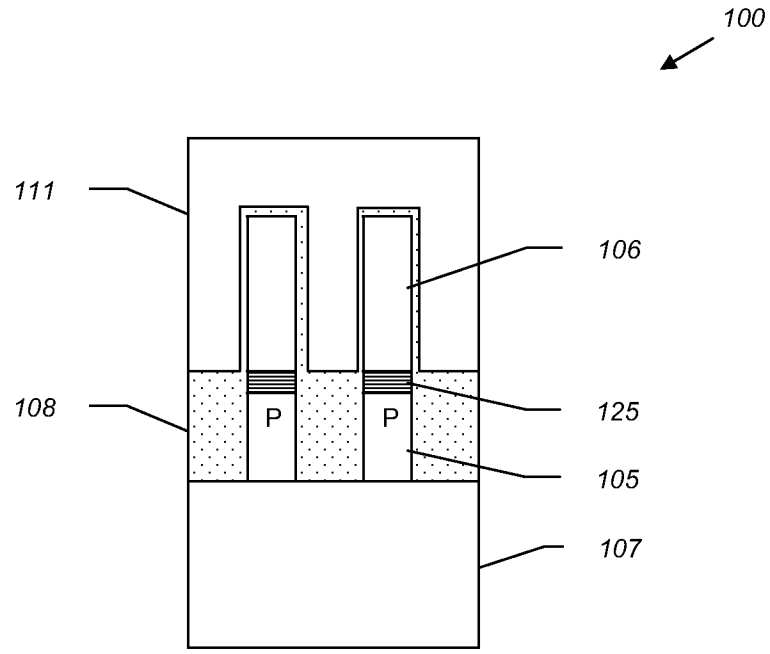

FIG. 6

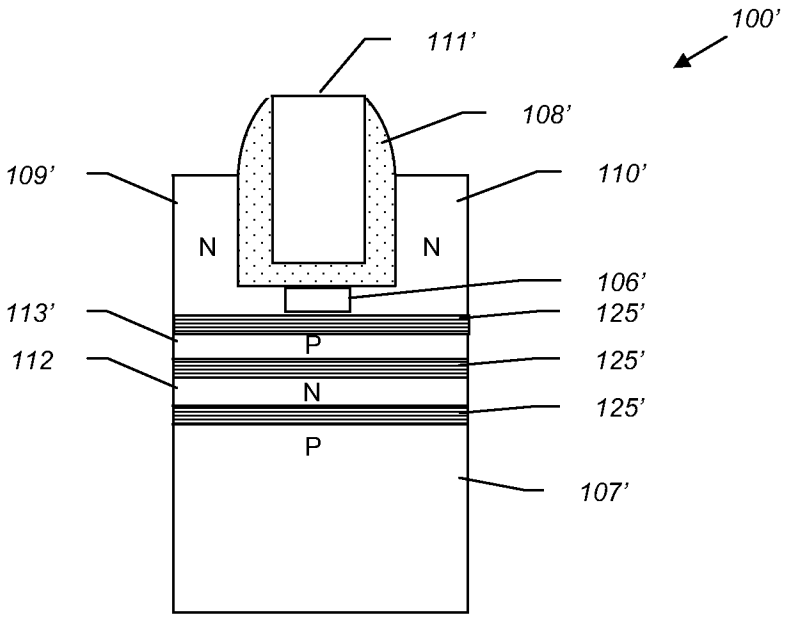
100'
111'
108'
109'
110'
N
N
106'
113'
125'
P
112
125'
N
125'
P
107'

FIG. 7

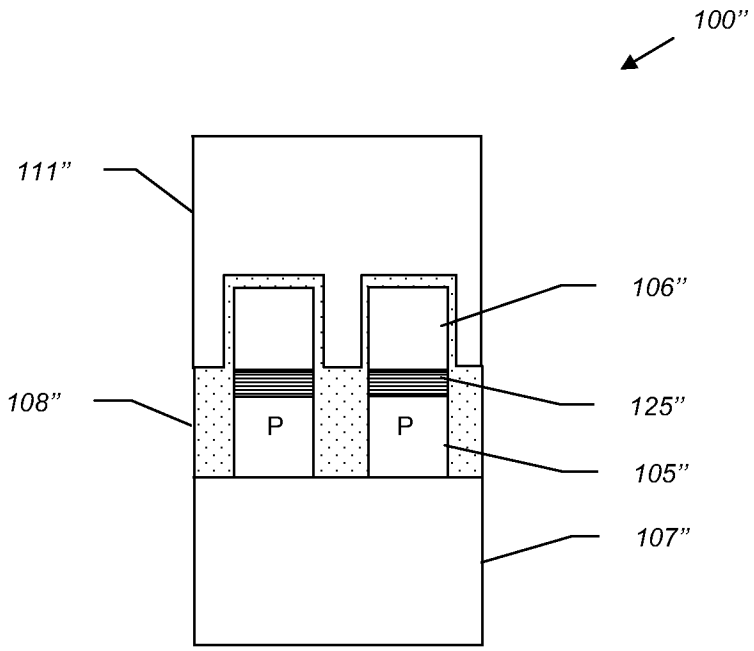
100"
111"
106"
108"
125"
P
P
105"
107"

FIG. 8

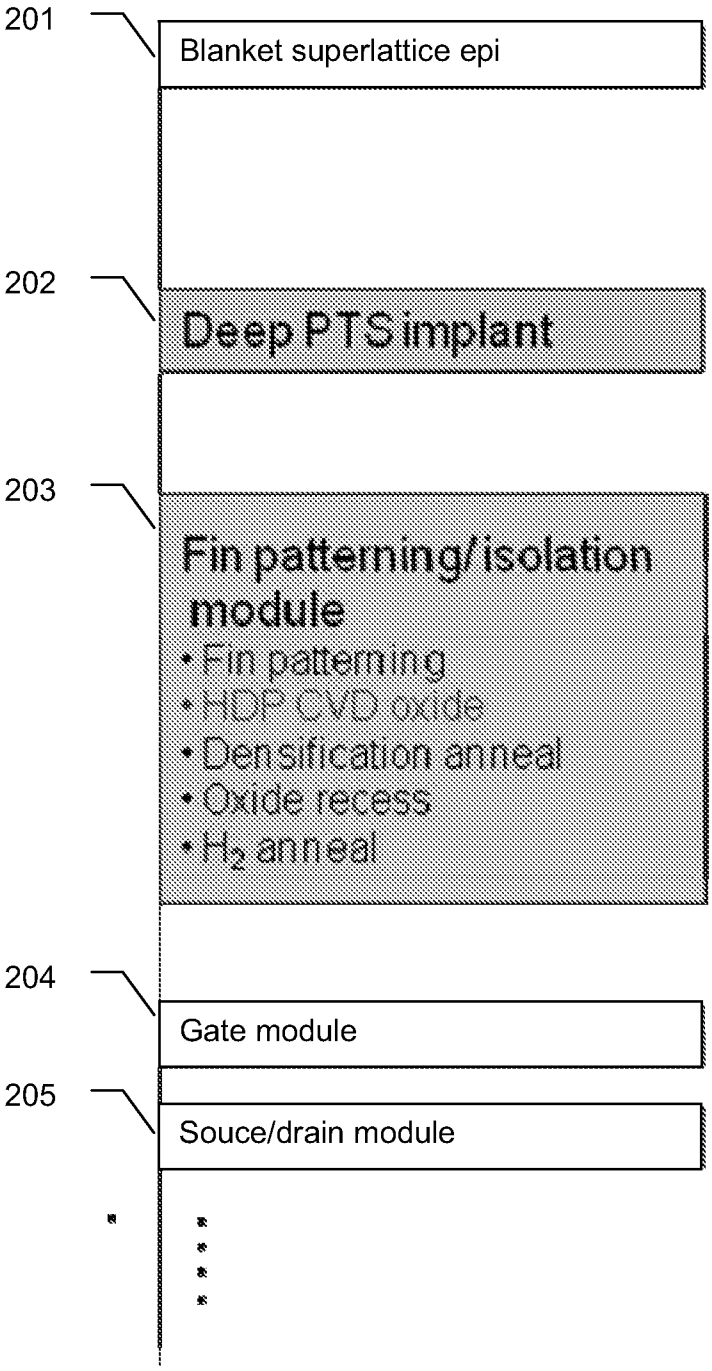
201
Blanket superlattice epi
202
Deep PTS implant
203
Fin patterning/isolation module
• Fin patterning
• HDP CVD oxide
• Densification anneal
• Oxide recess
• H_2 anneal
204
Gate module
205
Souce/drain module

FIG. 9a

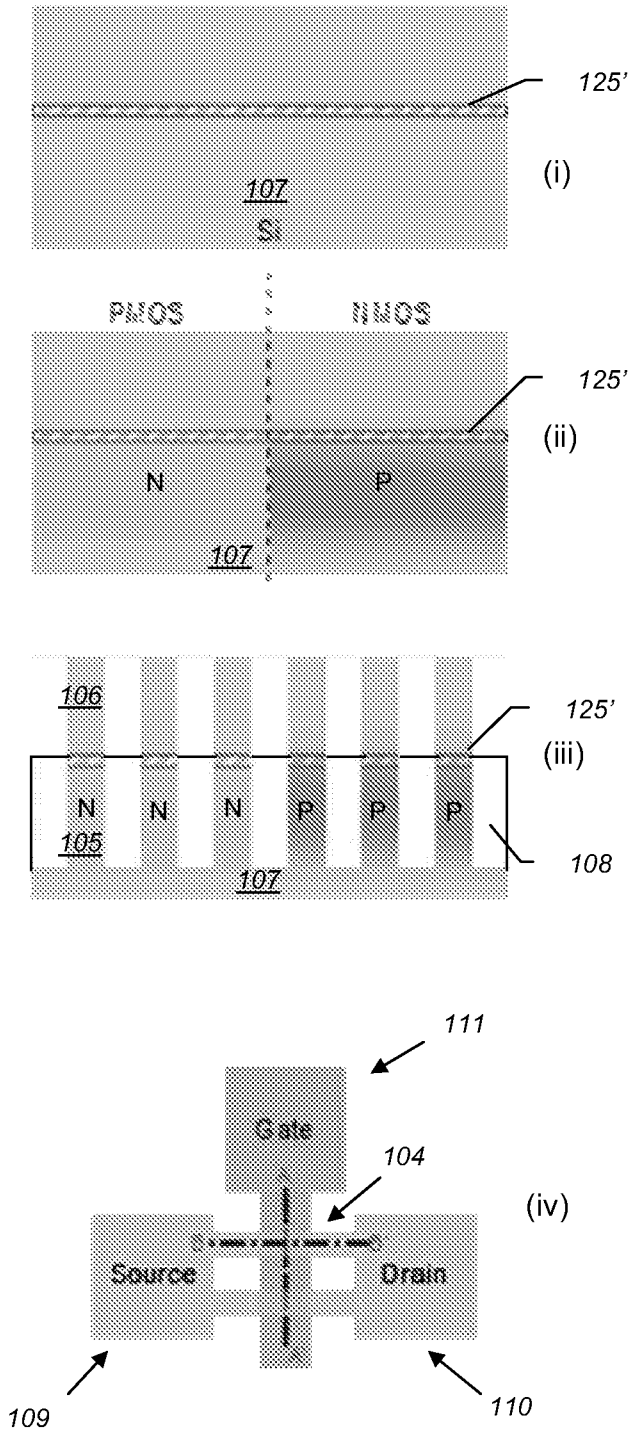
125'
107
Si
(i)
PMOS
NMOS
125'
N
P
107
(ii)
106
125'
N
N
N
P
P
P
105
107
108
(iii)
111
Gate
104
(iv)
Source
Drain
109
110

FIG. 9b

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/066873

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/66 H01L29/78 H01L29/10
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 2006/220118 A1 (STEPHENSON ROBERT J [US] ET AL) 5 October 2006 (2006-10-05) paragraph [0031] - paragraph [0034]	1-23
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 February 2015	04/03/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/066873

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	XU N ET AL: "MOSFET performance and scalability enhancement by insertion of oxygen layers", 2012 INTERNATIONAL ELECTRON DEVICES MEETING (IEDM 2012) : SAN FRANCISCO, CALIFORNIA, USA, 10 - 13 DECEMBER 2012, IEEE, PISCATAWAY, NJ, 10 December 2012 (2012-12-10), pages 6.4.1-6.4.4, XP032341682, DOI: 10.1109/IEDM.2012.6478990 ISBN: 978-1-4673-4872-0 the whole document	1-23
A	HUIMING BU: "FINFET technology a substrate perspective", SOI CONFERENCE (SOI), 2011 IEEE INTERNATIONAL, IEEE, 3 October 2011 (2011-10-03), pages 1-27, XP032011594, DOI: 10.1109/SOI.2011.6081712 ISBN: 978-1-61284-761-0 page 19	1-23

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/066873

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