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(71) Applicant: INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) Applicants (for MG only): IBM UNITED KINGDOM LIMITED [GB/GB]; PO Box 41, North Harbour, Portsmouth Hampshire PO6 3AU (GB). IBM (CHINA) INVESTMENT COMPANY LIMITED [CN/CN]; 25/F, Pangu Plaza, No.27, Central North 4th Ring Road, Chaoyang District, Beijing 100101 (CN).

(72) Inventors: ANDERSON, Brent, Alan; Ibm Corporation, Mail Drop 972c, 1000 River St, Essex Junction, Vermont 05452-4299 (US). NOWAK, Edward; Ibm Corporation, 1000 River St, Essex Junction, Vermont 05452-4299 (US).

(74) Agent: LITHERLAND, David; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester Hampshire SO21 2JN (GB).

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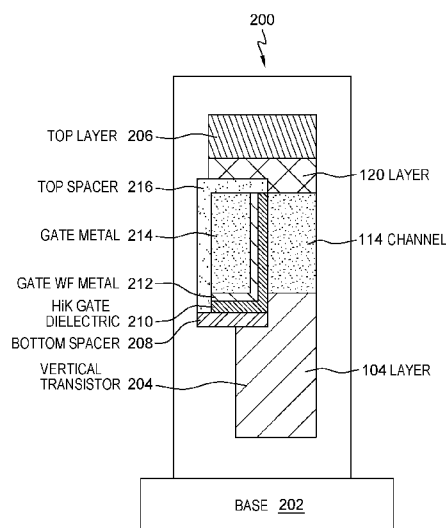


FIG. 2A

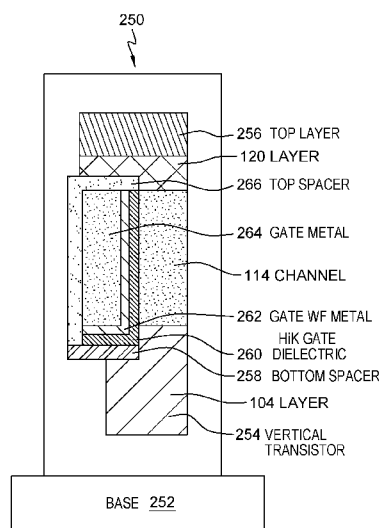


FIG. 2B

(57) **Abstract:** A method for fabricating a vertical FET structure includes prior to depositing a gate on a first vertical FET on a semiconductor substrate, depositing a first layer on the first vertical FET on the semiconductor substrate. The method further includes prior to depositing a gate on a second vertical FET on the semiconductor substrate, depositing a second layer on the second vertical FET on the semiconductor substrate. The method further includes etching the first layer on the first vertical FET to a lower height than the second layer on the second vertical FET. The method further includes depositing a gate material on both the first vertical FET and the second vertical FET. The method further includes etching the gate material on both the first vertical FET and the second vertical FET to a co-planar height.

VARIABLE GATE LENGTHS FOR VERTICAL TRANSISTORS

BACKGROUND

[0001] The present invention relates generally to the field of semiconductor devices, and more particularly to the formation of modified gate lengths.

[0002] The fabrication of semiconductor devices involves forming electronic components in and on semiconductor substrates, such as silicon wafers. These electronic components may include one or more conductive layers, one or more insulation layers, and doped regions formed by implanting various dopants into portions of a semiconductor substrate to achieve specific electrical properties. Semiconductor devices include transistors, resistors, capacitors, and the like, with intermediate and overlying metallization patterns at varying levels, separated by dielectric materials, which interconnect the semiconductor devices to form integrated circuits.

[0003] Field-effect transistors (FETs), such as metal-oxide-semiconductor FETs (MOSFETs), are a commonly used semiconductor device. Generally, a FET has three terminals, i.e., a gate structure (or gate stack), a source region, and a drain region. In some instances, the body of the semiconductor may be considered a fourth terminal. The gate stack is a structure used to control output current, i.e., flow of carriers in the channel portion of a FET, through electrical or magnetic fields. The channel portion of the substrate is the region between the source region and the drain region of a semiconductor device that becomes conductive when the semiconductor device is turned on. The source region is a doped region in the semiconductor device from which majority carriers are flowing into the channel portion. The drain region is a doped region in the semiconductor device located at the end of the channel portion, in which carriers are flowing into from the source region via the channel portion and out of the semiconductor device through the drain region. A conductive plug, or contact, is electrically coupled to each terminal. One contact is made to the source region, one contact is made to the drain region, and one contact is made to the gate stack.

[0004] A multigate device or multiple gate field-effect transistor (MuGFET) refers to a MOSFET (metal-oxide-semiconductor field-effect transistor) which incorporates more than

one gate into a single device. The multiple gates may be controlled by a single gate electrode, wherein the multiple gate surfaces act electrically as a single gate, or by independent gate electrodes. A multigate device employing independent gate electrodes is sometimes called a Multiple Independent Gate Field Effect Transistor (MIGFET).

SUMMARY

[0005] One aspect of the present invention discloses a method for fabrication of a field-effect transistor (FET) structure. The method includes prior to depositing a gate on a first vertical FET on a semiconductor substrate, depositing a first layer on the first vertical FET on the semiconductor substrate. The method further includes prior to depositing a gate on a second vertical FET on the semiconductor substrate, depositing a second layer on the second vertical FET on the semiconductor substrate. The method further includes etching the first layer on the first vertical FET to a lower height than the second layer on the second vertical FET. The method further includes depositing a gate material on both the first vertical FET and the second vertical FET. The method further includes etching the gate material on both the first vertical FET and the second vertical FET to a co-planar height.

[0006] Another aspect of the present invention discloses a method for fabrication of a field-effect transistor (FET) structure. The method includes depositing a first layer of gate materials on a first vertical FET on a semiconductor substrate. The method further includes depositing a second layer of gate materials on a second vertical FET on the semiconductor substrate. The method further includes wherein the bottom of the first layer and the bottom of the second layer are co-planar. The method further includes etching the first layer of gate materials on the first vertical FET. The method further includes etching the second layer of gate materials on the second vertical FET. The method further includes wherein the top of the first layer of gate materials and the top of the second layer of gate materials are not co-planar.

[0007] Another aspect of the present invention discloses a field-effect transistor (FET) structure. The FET structure comprises a first vertical field effect transistor (FET) formed on a semiconductor substrate and a second vertical FET formed on the semiconductor substrate. The structure further comprises the first vertical FET with a gate height co-planar to a gate height of

the second vertical FET. The structure further comprises the first vertical FET comprising a first layer below a gate on the first vertical FET. The structure further comprises the second vertical FET comprising second layer below a gate on the second vertical FET. The structure further comprises wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET are comprised of a first semiconductor material. The structure further comprises wherein the layer below the gate on the second vertical FET is not co-planar with the layer below the gate on the first vertical FET. The structure further comprises wherein the bottom of the gate on the first vertical FET is not co-planar with the bottom of the gate on the second vertical FET.

[0008] Another aspect of the present invention discloses a field-effect transistor (FET) structure. The FET structure comprises a first vertical field effect transistor (FET) formed on a semiconductor substrate and a second vertical FET formed on the semiconductor substrate. The structure further comprises the first vertical FET with a gate height that is not co-planar to a gate height of the second vertical FET. The method further comprises the first vertical FET comprising a first layer above a gate on the first vertical FET. The method further comprises the second vertical FET comprising a second layer above a gate on the second vertical FET. The method further comprises wherein the bottom of the gate on the first vertical FET is co-planar with the bottom of the gate on the second vertical FET.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The following detailed description, given by way of example and not intended to limit the disclosure solely thereto, will best be appreciated in conjunction with the accompanying drawings, in which:

Figure 1 depicts a cross section view of a vertical transistor, in accordance with embodiments of the invention.

Figure 2A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 2B depicts a cross section view of one quarter of a vertical transistor in which the bottom S/D has been etched for a longer period, in accordance with embodiments of the present invention.

Figure 3A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 3B depicts a cross section view of one quarter of a vertical transistor in which the bottom spacer has been etched for a longer period, in accordance with embodiments of the present invention.

Figure 4A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 4B depicts a cross section view of one quarter of a vertical transistor in which the HiK foot and/or WF metal has been etched for a longer period, in accordance with embodiments of the present invention.

Figure 5A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 5B depicts a cross section view of one quarter of a vertical transistor in which the gate top and/or WF metal has been etched for a longer period, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0010] Detailed embodiments of the claimed structures and methods are disclosed herein; however, it is to be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. In addition, each of the examples given in connection with the various embodiments is intended to be illustrative and not restrictive. Further, the Figures are not necessarily to scale, some features may be exaggerated to show details of particular components. Therefore, specific structural and functional details disclosed herein are not to be interpreted as limiting but merely as a representative basis for teaching one skilled in the art to variously employ the methods and structures of the present disclosure.

[0011] References in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in

the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0012] For purposes of the description hereinafter, the terms "upper," "lower," "right," "left," "vertical," "horizontal," "top," "bottom," and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. The terms "overlying," "atop," "on," "positioned on," or "positioned atop" mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure may be present between the first element and the second element. The term "direct contact" means that a first element and a second element are connected without any intermediary conducting, insulating, or semiconductor layers at the interface of the two elements.

[0013] Embodiments of the present invention recognize that multiple gate lengths is a popular feature to allow different Ion (on-state current) vs. Ioff (off-state current) device points. Embodiments of the present invention recognize that supporting multiple gate lengths is extremely difficult at the 7nm node and beyond with lateral transistors due to poor Ioff with shorter gates and longer gates resulting in increased contacts resistance. Embodiments of the present invention recognize that moving to a vertical transistor allows for room to support multiple gate lengths.

[0014] Implementation of embodiments of the invention may take a variety of forms, and exemplary implementation details are discussed subsequently with reference to the Figures.

[0015] Figure 1 depicts a cross section view of an embodiment of vertical transistor 100, in accordance with the present invention. Vertical transistor 100 may include more or less layers than depicted and is shown to represent a generic vertical transistor as known in the art. In some embodiments, vertical transistor 100 may include a single gate design, a multiple gate design, or a wraparound gate design. Layer 102 represents the base of the structure. In some embodiments, layer 102 may be a silicon wafer or any other base structure known in the art. Layer 104 represents the bottom source or drain of vertical transistor 100. In some embodiments, a designer of vertical transistor 100 may require a source or a drain at the bottom

of vertical transistor 100 depending on the desired direction of flow across the channel (e.g., channel 114). In an embodiment, layer 104 may be a heavily doped source or drain. Layer 120 may be composed of a first semiconductor layer material with the same doping polarity as the device polarity. In some examples, the source/drain layer, (e.g. layer 120) may comprise a number of base semiconductor material as well as dopants. For example, layer 120 may comprise silicon, tellurium, selenium, or other n-type doping materials. In another example, layer 120 may comprise p-type doping materials. In yet another example, layer 120 may be doped using conventional methods, such as ion implantation or any other method known by a person skilled in the art.

[0016] Layer 106 may be a bottom spacer utilized to insulate the gate from the bottom source or drain to prevent shorting. In an example, a spacer may be a dielectric material, such as SiN (Silicon Nitride), a nitride compound dielectric material, or an oxide, such as SiO₂. In some embodiments, layer 106 may be etched smaller or not deposited, which may allow for an increase in the gate length (e.g., gate 112). In some embodiments, layer 108 may be a HiK (high K) dielectric (e.g., high K dielectric may be deposited chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or other similar deposition methods). Some examples of HiK materials may include HfO₂, ZrO₂, Al₂O₃, TiO₂, LaAlO₃, HfSiO₂, Y₂O₃, etc. In some embodiments, layer 108 may be etched to reduce or remove the bottom portion of layer 108. In some embodiments, vertical transistor 100 may include an additional gate dielectric between layer 108 and channel 114, such as layer 110. In an example, layer 110 may include a dielectric material, such as SiN (Silicon Nitride), a nitride compound dielectric material, or an oxide, such as SiO₂.

[0017] In some embodiments, gate 112 may include a work function metal and a low resistance metal. In an example, the work function metal may comprise the inner surface of gate 112 where gate 112 contacts the HiK layer of 108. In some embodiments, gate 112 may be etched to reach a desired gate height. Some examples of materials utilized in gate 112 may include TiN, W, Ta, TaN, Au, etc. An example of a work function metal utilized in gate 112 may include TiN, TiC, TiAlC, etc.

[0018] In some embodiments, channel 114 is a highly conductive region between the source and the drain (e.g., layer 104 and layer 120) of vertical transistor 100. In some embodiments, channel 114 may be a low bandgap channel utilizing materials, such as SiGe, GaAs, InAs, or an alloy of InGaAs, or another group IV semiconductor commonly used in the art. In various embodiments, layer 116 is a top spacer similar to layer 106. In an example, layer 116 may include a dielectric material, such as SiN (Silicon Nitride), a nitride compound dielectric material, or an oxide, such as SiO₂. In some embodiments, layer 120 is a top source or drain, such as a heavily doped source or drain. Layer 120 may be composed of a first semiconductor layer material with the same doping polarity as the device polarity. For example, layer 120 may comprise silicon, tellurium, selenium, or other n-type doping materials. In another example, layer 120 may comprise p-type doping materials. In yet another example, layer 120 may be doped using conventional methods, such as ion implantation or any other method known by a person skilled in the art. In an example, layer 104 is a source; and therefore, layer 120 is a drain. In another example, layer 104 is a drain; and therefore, layer 120 is a source. In various embodiments, layer 122 is a dielectric material, such as SiN or SiO₂, that enables the source to be contained above the gate (e.g., gate 112) and channel (e.g., channel 114) in vertical transistor 100.

[0019] Figures 2A and 2B represent devices 200 and 250 located on the same wafer. Figure 2A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 2B depicts a cross section view of one quarter of a vertical transistor in which the bottom S/D has been etched for a longer period, in accordance with embodiments of the present invention. In some embodiments, etching may be performed by utilizing reactive ion etching (RIE) or other methods known by a person skilled in the art.

[0020] Figure 2A is representative of a cross section of a vertical transistor. In some embodiments, Figure 2A may be a generic representation of vertical transistor 100. Figure 2A includes a base 202, which is the semiconductor substrate (e.g., silicon) the vertical transistor is constructed on. Figure 2A also includes a bottom source or drain located within vertical transistor 204 and a top source or drain located in top layer 206. Figure 2A includes bottom spacer 208 which corresponds to layer 106 from Figure 1. Figure 2A further includes HiK gate dielectric 210 that corresponds to layer 108 in Figure 1, gate WF (work function) metal 212 and

gate metal 214 that corresponds to gate 112 in Figure 1, and top spacer 216 that corresponds to layer 116 in Figure 1.

[0021] Figure 2B depicts a cross section view representing the difference between a standard vertical transistor (e.g., 200 from Figure 2A) and a modified vertical transistor (e.g., 250 from Figure 2B) to adjust the gate length. In Figure 2B, the bottom source or drain represented at the bottom portion of vertical transistor 254, and also corresponding to layer 104 in Figure 1, can be etched to different lengths. In an example, device 200 of Figure 2A is masked and device 250 of Figure 2B is selectively etched. By masking the device 200 of Figure 2A prior to the selective etching, device 200 remains unchanged while device 250 is etched. By etching the bottom source or drain (e.g., the lower portion of vertical transistor 254) the gate length can be extended while keeping the same overall height for Figure 2B as in Figure 2A (e.g., the tops of gate metals 214 and 264 are co-planar). In an embodiment, the bottom source or drain of device 250 is selectively etched. After a spacer and HiK gate dielectric are added, gate materials are then added to both devices 200 and 250, which are subsequently etched to the same gate height resulting in a longer gate for device 250.

[0022] In an example, the bottom source or drain of vertical transistor 254 has been etched lower relative to the bottom source or drain of vertical transistor 204. Bottom spacer 258 is added via process that grows, coats, or otherwise transfers a material onto the wafer, such as PVD, CVD, etc., in the same amount as bottom spacer 208 in Figure 2A. HiK gate dielectric 260 is added similar to HiK gate dielectric 210 in Figure 2A; however, HiK gate dielectric 260 and HiK gate dielectric 210 are etched to a co-planar level. In an example, HiK gate dielectric 210 and HiK gate dielectric 260 are added to devices 200 and 250 in an “overflow” amount, and then etched back to a desired co-planar level. Gate WF metal 262 and gate metal 264 are added in the same manner as gate WF metal 212 and gate metal 214 in Figure 2A; however, gate WF metal 212 and gate WF metal 262 are etched to a co-planar level. In an example, gate WF metal 212 and gate WF metal 262 are added to devices 200 and 250 in an “overflow” amount and then etched back to a desired co-planar level. Top spacer 266 is added to cover the top of the gates as in top spacer 216 in Figure 2A; however, top spacer 216 and top spacer 266 are etched to a co-planar level. In an example, top spacer 216 and top spacer 266 are added to devices 200 and 250 in an “overflow” amount and then etched back to a desired co-planar level.

Top layer 256 represents the top source or drain in Figure 2B, which is the same size as top layer 206 in Figure 2A.

[0023] Figures 3A and 3B represent devices 300 and 350 located on the same wafer. Figure 3 depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 3B depicts a cross section view of one quarter of a vertical transistor in which the bottom spacer has been etched for a longer period, in accordance with embodiments of the present invention. In some embodiments, etching may be performed by utilizing reactive ion etching (RIE) or other methods known by a person skilled in the art.

[0024] Figure 3A is representative of a cross section of a vertical transistor. In some embodiments, Figure 3A may be a generic representation of vertical transistor 100. Figure 3A includes a base 302, which is the semiconductor substrate (e.g., silicon) the vertical transistor is constructed on. Figure 3A also includes a bottom source or drain located within vertical transistor 304 and a top source or drain located in top layer 306. Figure 3A includes bottom spacer 308 which corresponds to layer 106 from Figure 1. Figure 3A further includes HiK gate dielectric 310 that corresponds to layer 108 in Figure 1, gate WF (work function) metal 312 and gate metal 314 that corresponds to gate 112 in Figure 1, and top spacer 316 that corresponds to layer 116 in Figure 1.

[0025] Figure 3B depicts a cross section view representing the difference between a standard vertical transistor (e.g., device 300 from Figure 3A) and a modified vertical transistor (e.g., device 350 from Figure 3B) to adjust the gate length. In Figure 3B, the bottom source or drain represented at the bottom portion of vertical transistor 354, and also corresponding to layer 104 in Figure 1, which is maintained as the same size as in Figure 3A. In an embodiment, by etching the bottom spacer (e.g., bottom spacer not shown because it has been etched to completely remove the spacer in Figure 3B or layer 106 in Figure 1) the gate length can be extended while keeping the same overall height for Figure 3B as in Figure 3A. In an embodiment, the bottom spacer of device 350 from Figure 3B is etched more. In an example, the bottom spacer (e.g., bottom spacer 358) of device 300 of Figure 3A is masked and device 350 of Figure 3B is selectively etched. By masking device 300 of Figure 3A prior to the

selective etching, device 300 remains unchanged while device 350 is etched. By etching the bottom spacer (e.g., bottom spacer 358) the gate length can be extended while keeping the same overall height for Figure 3B as in Figure 3A (e.g., the tops of gate metals 314 and 364 are co-planar). In an embodiment, the bottom spacer of Figure 3B, device 350 is selectively etched. Gate materials are then added to both devices 300 and 350, which are subsequently etched to the same gate height resulting in a longer gate for device 350.

[0026] In an example, bottom spacer 358 has been etched lower relative to bottom spacer 308. In another example, bottom spacer 358 may not be added or bottom spacer 358 is etched (e.g., RIE etched) to remove bottom spacer 358 completely. HiK gate dielectric 360 is added similar to HiK gate dielectric 310 in Figure 3A; however, HiK gate dielectric 360 and HiK gate dielectric 310 are etched to a co-planar level. In an example, HiK gate dielectric 310 and HiK gate dielectric 360 are added to devices 300 and 350 in an “overflow” amount and then etched back to a desired co-planar level. Gate WF metal 362 and gate metal 364 are added in the same manner as gate WF metal 312 and gate metal 314 in Figure 3A; however, gate WF metal 312 and gate WF metal 362 are etched to a co-planar level. In an example, gate WF metal 312 and gate WF metal 362 are added to devices 300 and 350 in an “overflow” amount and then etched back to a desired co-planar level. Top spacer 366 is added by the same method to cover the top of the gates as in top spacer 316 in Figure 3A; however, top spacer 316 and top spacer 366 are etched to a co-planar level. In an example, top spacer 316 and top spacer 366 are added to devices 300 and 350 in an “overflow” amount and then etched back to a desired co-planar level. Top layer 356 represents the top source or drain in Figure 3B, which is the same size as top layer 306 in Figure 3A.

[0027] Figures 4A and 4B represent devices 400 and 450 located on the same wafer. Figure 4A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 4B depicts a cross section view of one quarter of a vertical transistor in which the HiK gate dielectric has been etched for a longer period, in accordance with embodiments of the present invention. In some embodiments, etching may be performed by utilizing reactive ion etching (RIE) or other methods known by a person skilled in the art.

[0028] Figure 4A is representative of a cross section of a vertical transistor. In some embodiments, Figure 4A may be a generic representation of vertical transistor 100. Figure 4A includes a base 402, which is the semiconductor substrate (e.g., silicon) the vertical transistor is constructed on. Figure 4A also includes a bottom source or drain located within vertical transistor 404 and a top source or drain located in top layer 406. Figure 4A includes bottom spacer 408 which corresponds to layer 106 from Figure 1. Figure 4A further includes HiK gate dielectric 410 that corresponds to layer 108 in Figure 1, gate WF (work function) metal 412 and gate metal 414 that corresponds to gate 112 in Figure 1, and top spacer 416 that corresponds to layer 116 in Figure 1.

[0029] Figure 4B depicts a cross section view representing the difference between a standard vertical transistor (e.g., device 400 from Figure 4A) and a modified vertical transistor (e.g., device 450 from Figure 4B) to adjust the gate length. In Figure 4B, the bottom source or drain represented at the bottom portion of vertical transistor 454, and also corresponding to layer 104 in Figure 1, which is maintained as the same size as in Figure 4A. Bottom spacer 458 is added in the same amount as bottom spacer 408 in Figure 4A. In an embodiment, by etching the HiK gate dielectric (e.g., HiK gate dielectric 460 in Figure 4B or layer 108 in Figure 1) the gate length can be extended while keeping the same overall height for Figure 4B as in Figure 4A. In an embodiment, the HiK gate dielectric of Figure 4B is etched more. In an example, the HiK gate dielectric (e.g., HiK gate dielectric 410) of device 400 of Figure 4A is masked and device 450 of Figure 4B is selectively etched. By masking device 400 of Figure 4A prior to the selective etching, device 400 remains unchanged while device 450 is etched. By etching the HiK gate dielectric (e.g., HiK gate dielectric 460) the gate length can be extended while keeping the same overall height for Figure 4B as in Figure 4A (e.g., the tops of gate metals 414 and 464 are co-planar). In an embodiment, the HiK gate dielectric of Figure 4B device 450 is selectively etched. Gate materials are then added to both devices 400 and 450, which are subsequently etched to the same gate height resulting in a longer gate for device 450.

[0030] In an example, HiK gate dielectric 460 has been etched lower relative to HiK gate dielectric 410. In another example, HiK gate dielectric 460 may not be added or etched to remove bottom portion of HiK gate dielectric 460 completely. Gate WF metal 462 and gate metal 464 are added in the same manner as gate WF metal 412 and gate metal 414 in Figure

4A; however, gate WF metal 412 and gate WF metal 462 are etched to a co-planar level. In an example, gate WF metal 412 and gate WF metal 462 are added to devices 400 and 450 in an “overflow” amount and then etched back to a desired co-planar level. Top spacer 466 is added by the same method to cover the top of the gates as in top spacer 416 in Figure 4A; however, top spacer 416 and top spacer 466 are etched to a co-planar level. In an example, top spacer 416 and top spacer 466 are added to devices 400 and 450 in an “overflow” amount and then etched back to a desired co-planar level. Top layer 456 represents the top source or drain in Figure 4B, which is the same size as top layer 406 in Figure 4A.

[0031] Figures 5A and 5B represent devices 500 and 550 located on the same wafer. Figure 5A depicts a cross section view of one quarter of a vertical transistor, in accordance with an embodiment of the present invention. Figure 5B depicts a cross section view of one quarter of a vertical transistor in which the gate metal has been etched for a longer period, in accordance with embodiments of the present invention. In some embodiments, etching may be performed by utilizing reactive ion etching (RIE) or other methods known by a person skilled in the art.

[0032] Figure 5A is representative of a cross section of a vertical transistor. In some embodiments, Figure 5A may be a generic representation of vertical transistor 100. Figure 5A includes a base 502, which is the semiconductor substrate (e.g., silicon) the vertical transistor is constructed on. Figure 5A also includes a bottom source or drain located within vertical transistor 504 and a top source or drain located in top layer 506. Figure 5A includes bottom spacer 508 which corresponds to layer 106 from Figure 1. Figure 5A further includes HiK gate dielectric 510 that corresponds to layer 108 in Figure 1, gate WF (work function) metal 512 and gate metal 514 that corresponds to gate 112 in Figure 1, and top spacer 516 that corresponds to layer 116 in Figure 1.

[0033] Figure 5B depicts a cross section view representing the difference between a standard vertical transistor (e.g., device 500 from Figure 5A) and a modified vertical transistor (e.g., device 550 from Figure 5B) to adjust the gate length. In Figure 5B, the bottom source or drain represented at the bottom portion of vertical transistor 554, and also corresponding to layer 104 in Figure 1, which is maintained as the same size as in Figure 5A. Bottom spacer 558 is added in the same amount as bottom spacer 508 in Figure 5A. HiK gate dielectric 560 is added

similar to HiK gate dielectric 510 in Figure 5A. In an embodiment, by etching the gate WF metal (e.g., gate WF metal 562 in Figure 5 or gate 112 in Figure 1) and/or gate metal (e.g., gate metal 564 in Figure 5 or gate 112 in Figure 1) the gate length can be shortened while keeping the same overall height for Figure 5B as in Figure 5A. In an embodiment, gate WF metal 562 and/or gate metal 564 of Figure 5B are etched more. In an example, the gate WF metal and/or gate metal (e.g., gate WF metal 512 and/or gate metal 514) of device 500 of Figure 5A is masked and device 550 of Figure 5B is selectively etched. By masking device 500 of Figure 5A prior to the selective etching, device 500 remains unchanged while device 550 is etched. By etching the gate WF metal and/or gate metal (e.g., gate WF metal 562 and/or gate metal 564) the gate length can be shortened while keeping the same overall height for Figure 5B as in Figure 5A (e.g., the tops of gate metals 514 and 564 are co-planar).

[0034] In an example, gate metal 564 has been etched lower relative to gate metal 514. In another example, gate WF metal 562 has been etched lower relative to gate WF metal 512. In yet another example, both gate metal 564 and gate WF metal 562 have been etched lower. Top spacer 566 is added by the same method to cover the top of the gates as in top spacer 516 in Figure 4A; however, top spacer 516 and top spacer 566 are etched to a co-planar level. In an example, top spacer 516 and top spacer 566 are added to devices 500 and 550 in an “overflow” amount and then etched back to a desired co-planar level. Top layer 556 represents the top source or drain in Figure 5B, which is the same size as top layer 506 in Figure 5A.

[0035] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The terminology used herein was chosen to best explain the principles of the embodiment, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A semiconductor structure comprising:
 - a first vertical field effect transistor (FET) formed on a semiconductor substrate and a second vertical FET formed on the semiconductor substrate;
 - the first vertical FET with a gate height co-planar to a gate height of the second vertical FET;
 - the first vertical FET comprising a first layer below a gate on the first vertical FET;
 - the second vertical FET comprising second layer below a gate on the second vertical FET;
 - wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET are comprised of a first semiconductor material;
 - wherein the layer below the gate on the second vertical FET is not co-planar with the layer below the gate on the first vertical FET; and
 - wherein the bottom of the gate on the first vertical FET is not co-planar with the bottom of the gate on the second vertical FET.
2. The structure of claim 1, wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET comprise a source, wherein the top of the source under the gate of the first vertical FET and the top of the source under the gate of the second vertical FET are not co-planar.
3. The structure of claim 1, wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET comprise a drain, wherein the top of the drain under the gate of the first vertical FET and the top of the drain under the gate of the second vertical FET are not co-planar.
4. The structure of claim 1, wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET comprise a spacer, wherein the spacer of the first vertical FET and the spacer of the second vertical FET are a different thickness.

5. The structure of claim 1, wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET comprise a high K dielectric, wherein the high K dielectric of the first vertical FET and the high K dielectric of the second vertical FET are a different thickness.

6. The structure of claim 1, wherein the first layer below the gate on the first vertical FET and the second layer below the gate on the second vertical FET comprise a high K dielectric, wherein the high K dielectric of the first vertical FET includes a vertical portion and a horizontal portion, and the high K dielectric of the second vertical FET includes a vertical portion.

7. A semiconductor structure comprising:
a first vertical field effect transistor (FET) formed on a semiconductor substrate and a second vertical FET formed on the semiconductor substrate;
the first vertical FET with a gate height that is not co-planar to a gate height of the second vertical FET;
the first vertical FET comprising a first layer above a gate on the first vertical FET; and
the second vertical FET comprising a second layer above a gate on the second vertical FET; and
wherein the bottom of the gate on the first vertical FET is co-planar with the bottom of the gate on the second vertical FET.

8. The structure of claim 7, wherein the first layer above the gate on the first vertical FET and the second layer above the gate on the second vertical FET comprise a spacer, wherein the spacer of the first vertical FET and the spacer of the second vertical FET are a different thickness.

9. A method for fabricating a vertical field-effect transistor (FET) structure, the method comprising:
prior to depositing a gate on a first vertical FET on a semiconductor substrate,
depositing a first layer on the first vertical FET on the semiconductor substrate;

prior to depositing a gate on a second vertical FET on the semiconductor substrate,
depositing a second layer on the second vertical FET on the semiconductor substrate;

etching the first layer on the first vertical FET to a lower height than the second layer on the second vertical FET;

depositing a gate material on both the first vertical FET and the second vertical FET;
and

etching the gate material on both the first vertical FET and the second vertical FET to a co-planar height.

10. The method of claim 9, wherein the first layer and the second layer comprise a source.

11. The method of claim 9, wherein the first layer and the second layer comprise a drain.

12. The method of claim 9, wherein the first layer and the second layer comprises a spacer.

13. The method of claim 12, wherein etching the first layer on the first vertical FET comprises etching the first layer to remove the first layer.

14. The method of claim 12, wherein etching the first layer on the first vertical FET comprises etching the first layer to remove a portion of spacer layer respective the second layer.

15. The method of claim 9, wherein the first layer and the second layer comprises a high K gate dielectric.

16. The method of claim 15, wherein the first layer and the second layer comprise a vertical part and a horizontal part.

17. The method of claim 16, wherein etching the first layer on the first vertical FET comprises etching the first layer to remove the horizontal part of the first layer.

18. The method of claim 16, wherein etching the layer on the first vertical FET comprises etching the layer to remove a portion of the horizontal part of the first layer.

19. A method for fabricating a vertical field-effect transistor (FET) structure, the method comprising:

depositing a first layer of gate materials on a first vertical FET on a semiconductor substrate;

depositing a second layer of gate materials on a second vertical FET on the semiconductor substrate;

wherein the bottom of the first layer and the bottom of the second layer are co-planar;

etching the first layer of gate materials on the first vertical FET;

etching the second layer of gate materials on the second vertical FET; and

wherein the top of the first layer of gate materials and the top of the second layer of gate materials are not co-planar.

20. The method of claim 19, further comprising:

depositing a first spacer on the first vertical FET and a second spacer on the second vertical FET; and

etching the first spacer and the second spacer to a co-planar height.

21. The method of claim 19, wherein depositing a first layer and second layer comprises depositing a gate work function metal and a gate metal.

22. The method of claim 21, wherein etching the first layer comprises etching at least a portion of the gate metal.

23. The method of claim 21, wherein etching the first layer and etching the second layer comprises etching at least a portion of the gate work function metal.

24. The method of claim 21, wherein etching the first layer and etching the second layer comprises etching at least a portion of the gate metal and the gate work function metal.

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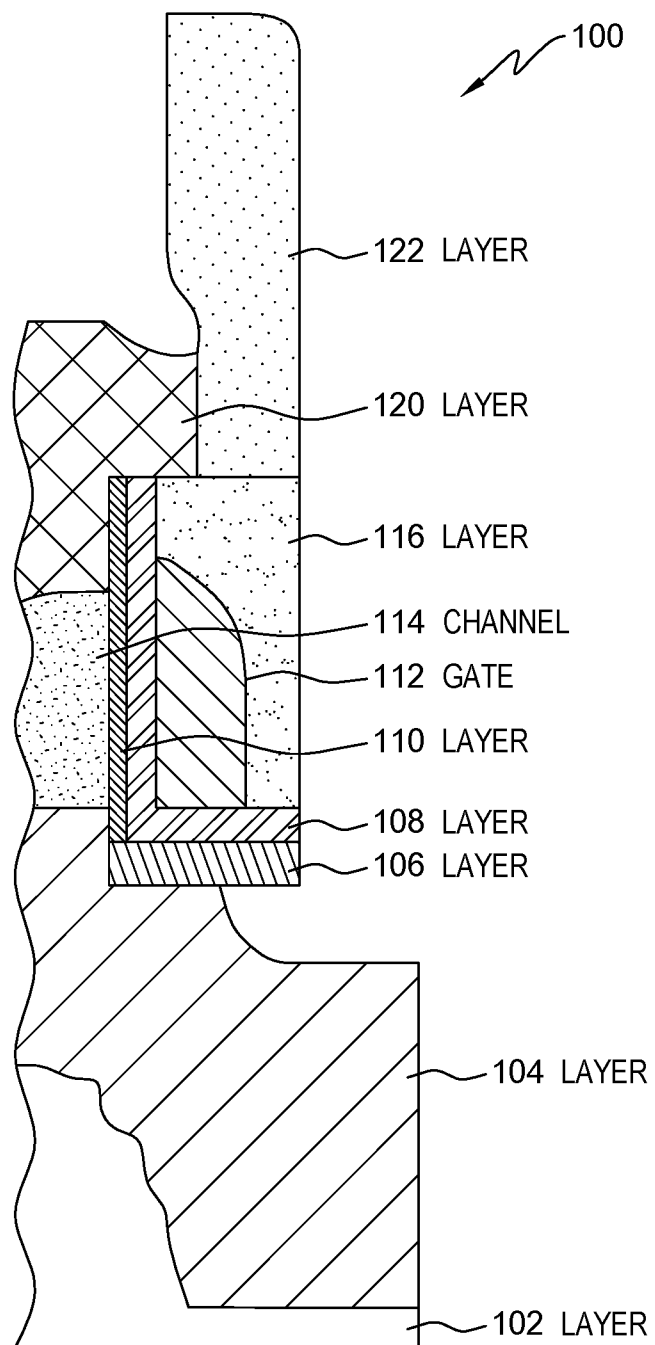


FIG. 1

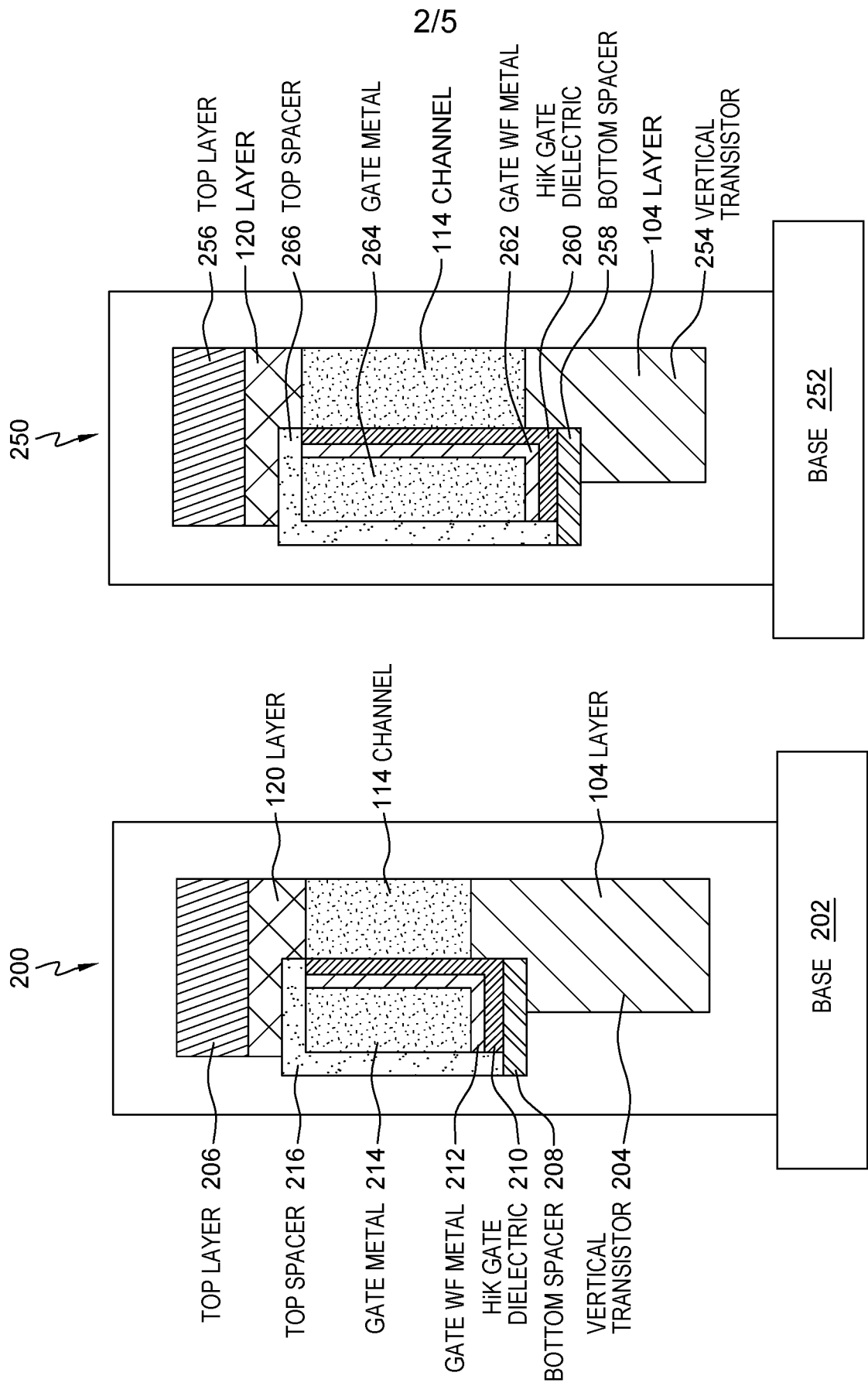


FIG. 2B

FIG. 2A

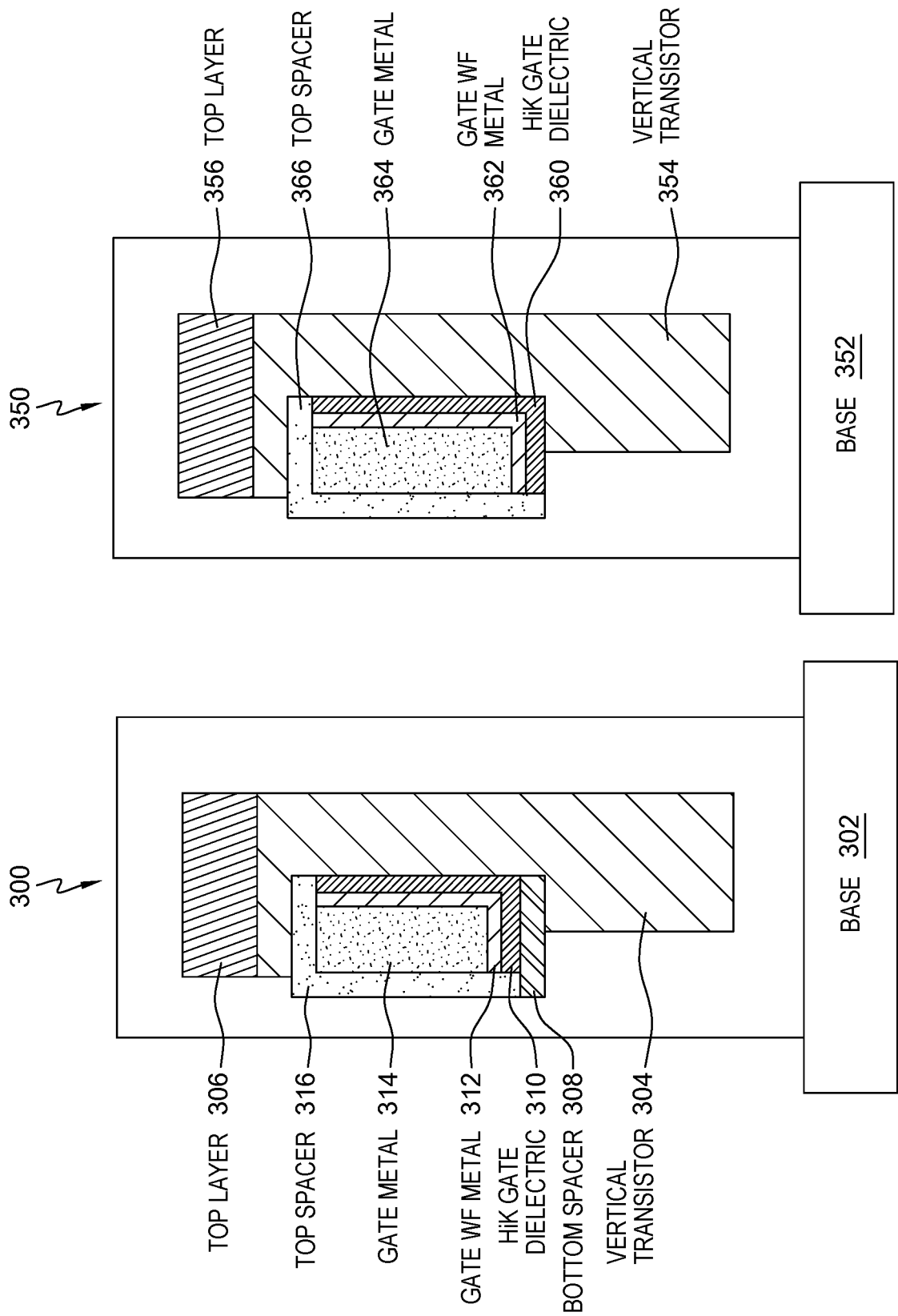


FIG. 3B

FIG. 3A

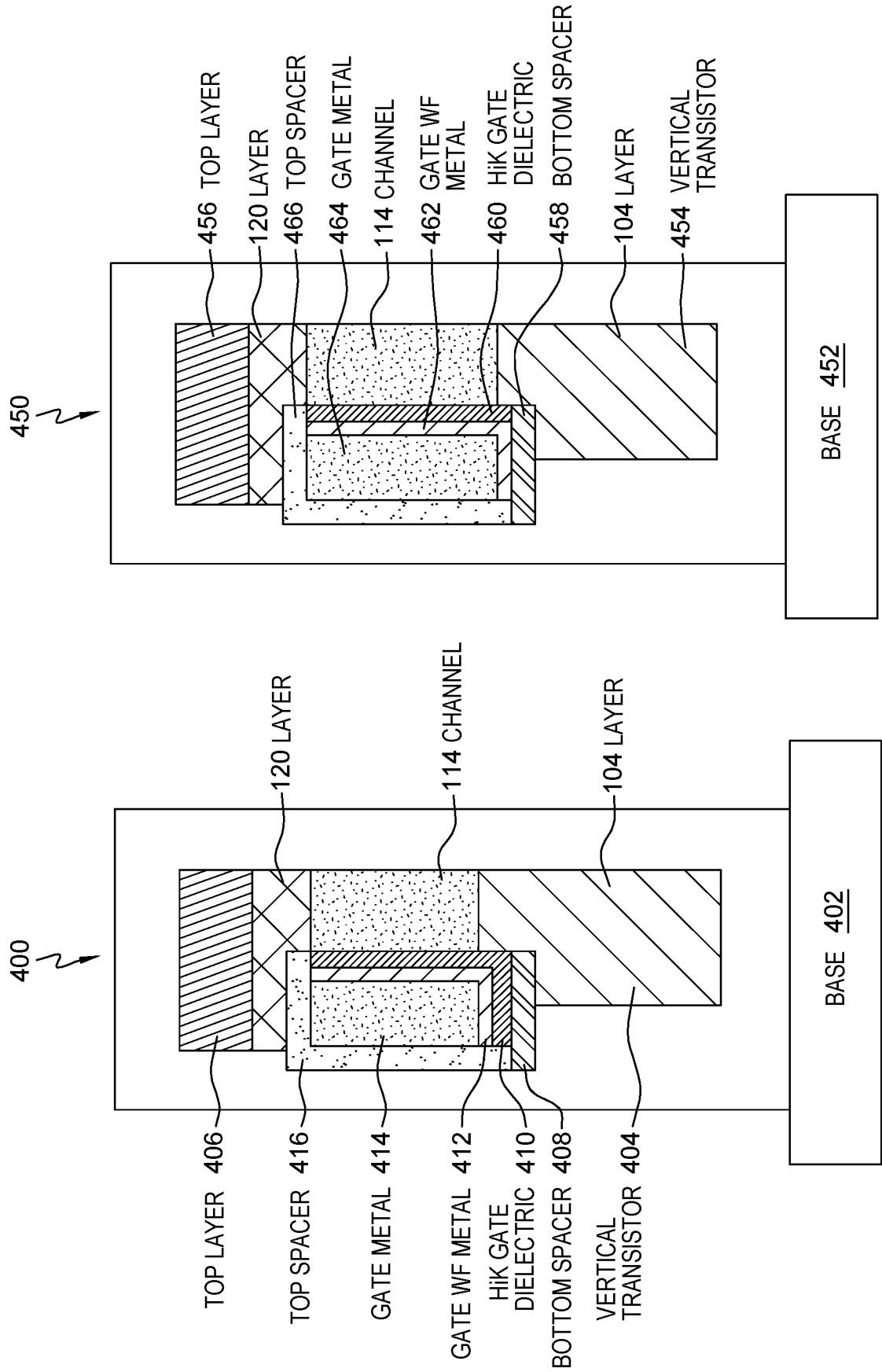


FIG. 4B

FIG. 4A

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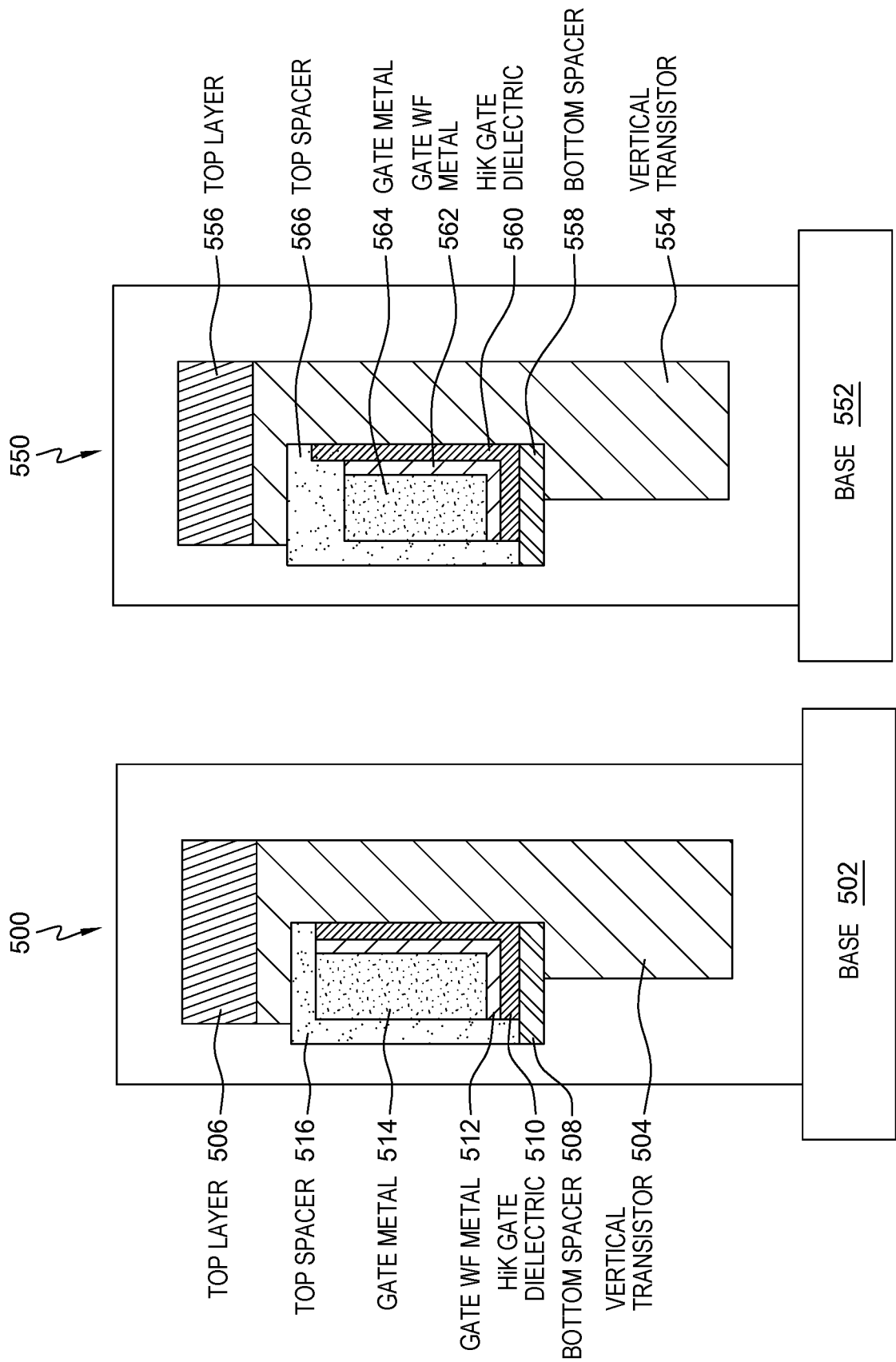


FIG. 5B

FIG. 5A

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2016/057484

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i; H01L 29/06(2006.01)i; H01L 21/335(2006.01)i; H01L 21/8232(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, EPODOC, WPI: vertical, FET, transistor, variable, different, modified, multi, dual, independent, gate, length, height, combination, co, planar, drain, source, etch, deposit, MIGFET

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6632712 B1 (CHARTERED SEMICONDUCTOR MFG. LTD.) 14 October 2003 (2003-10-14) the description, column 3, line 10- column 5, line 45, figures 1-10	7-8, 19-24
A	CN 101449367 A (FREESCALE SEMICONDUCTOR INC.) 03 June 2009 (2009-06-03) the whole document	1-24
A	US 2011042748 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 24 February 2011 (2011-02-24) the whole document	1-24
A	US 2015206970 A1 (TAIWAN SEMICONDUCTOR MFG. CO., LTD.) 23 July 2015 (2015-07-23) the whole document	1-24
A	US 2008121948 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 29 May 2008 (2008-05-29) the whole document	1-24

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

09 March 2017

Date of mailing of the international search report

29 March 2017

Name and mailing address of the ISA/CN

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P.R.CHINA**
**6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China**

Facsimile No. (86-10)62019451

Authorized officer

LIU,Ning

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/IB2016/057484

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