(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 August 2012 (23.08.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/109783 A1

(51) International Patent Classification:
H02M 3/28 (2006.01) *H02M 3/337* (2006.01)

(21) International Application Number:
PCT/CN2011/070969

(22) International Filing Date:
14 February 2011 (14.02.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERSIL AMERICAS INC.** [US/US]; 1001 Murphy Ranch Road, Milpitas, California 95035 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WANG, Wenguang** [CN/CN]; Room 01, 7th Floor, Building 5, Hangzhou, Zhejiang 310013 (CN). **YU, Long (Robin)** [CN/CN]; Room 02, 5th Floor, Building 5, Hangzhou, Zhejiang 310013 (CN). **ZHAN, Xiaodong (David)** [CN/US]; 7821 Case Dr, Plano, Texas 75025 (US).

(74) Agent: **SHANGHAI PATENT & TRADEMARK LAW OFFICE, LLC**; 435 Guiping Road, Shanghai 200233 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: ISOLATED BOOST DC/DC CONVERTER

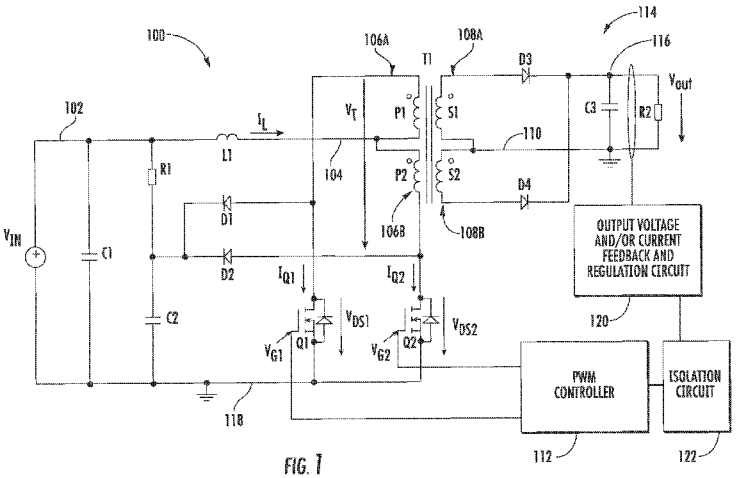


FIG. 1

(57) **Abstract**: A DC/DC converter (100) includes an inductor (L1) having a first end and a second end, and a transformer (T1) having a primary side and a secondary side. The first end is adapted to receive an input voltage (V_{IN}). The primary side has a first primary winding (106A) and a second primary winding (106B). The first primary winding (106A) and the second primary winding (106B) each has a first end coupled to the second end of the inductor (L1) and each has a respective second end. A first switch (Q1) is coupled to the second end of the first primary winding (106A), and a second switch (Q2) is coupled to the second end of the second primary winding (106B). An output circuit is coupled to the secondary side of the transformer (T1). The first and second switches are turned on and off during selected time periods such that energy is stored in the inductor (L1) and then passed through the transformer (T1) to the output circuit to provide a boosted output voltage (V_{OUT}).

WO 2012/109783 A1

ISOLATED BOOST DC/DC CONVERTER

DRAWINGS

[0001] Embodiments of the present invention can be more easily understood and further advantages and uses thereof more readily apparent, when considered in view of the description of the preferred embodiments and the following figures in which:

[0002] Figure 1 is a schematic diagram of a DC/DC converter according to one embodiment of the present invention.

[0003] Figs. 2A-F are timing diagrams for the operation of a DC/DC converter according to one embodiment of the present invention.

[0004] Fig. 3 is a block diagram of one embodiment of a system including a DC/DC converter according to one embodiment of the present invention.

[0005] In accordance with common practice, the various described features are not drawn to scale but are drawn to emphasize features relevant to the present invention. Reference characters denote like elements throughout figures and text.

DETAILED DESCRIPTION

[0006] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

[0007] Figure 1 is a schematic diagram of a DC/DC converter, indicated generally at 100, and constructed according to one embodiment of the present invention. Converter 100 is a boost converter in that the DC output voltage (V_{out}) is proportional to 1/(1-D) (D is the on-state duty cycle of both Q1 and Q2) and maybe smaller or greater than the DC input voltage (V_{IN})

depending on the transformer turns ratio. In addition, converter 100 also implements isolation by including a transformer T1 interposed between input voltage V_{IN} and output voltage V_{OUT}.

[0008] Converter 100 operates in current feed mode. Input voltage V_{IN} is applied at input node 102. Converter 100 also includes inductor L1. Inductor L1 has a first end coupled to node 102 and a second end coupled to node 104. In this manner, current from input voltage V_{IN} is provided to inductor L1 during operation of converter 100.

[0009] Transformer T1 has a primary side with primary windings 106A and 106B and a secondary side with secondary windings 108A and 108B. The primary windings 106A and 106B are connected to a center tap. The center tap of the primary windings 106A and 106B is coupled to node 104. Similarly, the center tap of secondary windings 108A and 108B is coupled to node 110.

[0010] The operation of converter 100 is controlled by pulse width modulation (PWM) controller 112. Controller 112 is coupled to first and second switches Q1 and Q2. Controller 112 receives an error signal from the output voltage and/or current feedback and regulation circuit 120 through the isolation barrier 122 to provide PWM control to Q1 and Q2 and keep the output voltage or current in regulation. In one embodiment, the switches Q1 and Q2 are implemented as field effect transistors (FETs). Switch Q1 is coupled between primary winding 106A and node 118. In one embodiment, node 118 is coupled to ground potential. Switch Q2 is coupled between primary winding 106B and node 118. Switches Q1 and Q2 are controlled by control signals V_{G1} and V_{G2}, respectively.

[0011] Converter 100 also includes output rectifier circuit 114 that provides the DC output voltage to a load represented by resistor R2. Output rectifier circuit 114 is coupled to secondary windings 108A and 108B of transformer T1. Output circuit 114 includes first and second diodes D3 and D4. Diode D3 is coupled between secondary winding 108A and output node 116. Diode D3 is coupled between secondary winding 108B and output node 116. Output circuit 114 further includes an output capacitor C3 coupled between output node 116 and node 110. It is noted that in one embodiment, node 110 is coupled to ground potential.

[0012] The operation of converter 100 is described with reference to timing diagrams in Figures 2A-2F. The operation is described in four phases or time periods. It is understood that during

operation, these four time periods are repeated, as necessary, for a particular implementation. Further, the four time periods are established by controlling the duty cycle and phase of the switches Q1 and Q2. In one embodiment, the duty cycle of each switch is set at a level greater than 50 percent. Further, the switches Q1 and Q2 are switched at the same frequency and 180 degrees out-of-phase. In this manner, inductor L1 is enabled to alternate between storing energy during one time period and passing energy through transformer T1 to output node 116 during a subsequent time period as explained in more detail below.

[0013] During the first time period, energy from the input DC voltage source, V_{IN}, is stored in the inductor L1. As shown in Figs. 2A and 2B, controller 112 provides control signals V_{G1} and V_{G2} to switches Q1 and Q2. During time period t_0 to t_1, both V_{G1} and V_{G2} are at a high voltage level that turns on both switches Q1 and Q2. As shown in Fig. 2C and 2D, this forces the voltage, V_{DS1} and V_{DS2}, to a low voltage level, e.g., 0 volts. Further, as seen in Fig. 2F, the voltage across primary windings 106A and 106B is also brought to a low voltage level, e.g., 0 volts, during this time period. With both switches Q1 and Q2 turned on at the same time, transformer T1 is effectively shorted out, e.g., from t_0 to t_1. With the transformer T1 shorted, the current in inductor L1 increases (Fig. 2E). Thus, the inductor receives the current from the input DC voltage, V_{IN}, and stores energy in inductor L1.

[0014] During the next time period, t_1 to t_2, energy is transferred by transformer T1 from inductor L1 and input source V_{IN} to the output circuit 114. To accomplish this, controller 112 turns off switch Q2 by reducing control signal V_{G2} to a low voltage level, e.g., 0 volts as shown in Fig. 2B. With switch Q2 off, a conduction path is formed such that current passes from inductor L1 (Fig. 2E) through primary winding 106A and switch Q1. This further causes a current in secondary winding 108B of transformer T1 based on the turns ratio of secondary winding 108B to primary winding 106A. The output capacitor C3 is charged through diode D4 to provide the desired output voltage V_{OUT} at node 116. In one embodiment, the output voltage is calculated according to the following equation:

(1) $$\frac{V_{out}}{V_{in}} = \frac{n}{1-D}$$

[0015] In equation (1), V_{out} is the output voltage at node 116, V_{IN} is the voltage applied to inductor L1, D is the on-state duty cycle of switches Q1 and Q2, i.e., the time interval between t_0

and t_1 divided by the time interval between t_0 and t_2, or the time interval between t_2 and t_3 divided by the time interval between t_2 and t_4, shown in Fig. 2 and *n* is the turns ratio, e.g., the ratio of the number of turns in the secondary side (108A or 108B) to the number of turns in the primary side (106A or 106B).

[0016] Between t_2 and t_3, energy from the input DC voltage source, V_{IN}, is again stored in inductor L1. During this time period, switch Q2 is turned back on (Fig. 2B) such that both switches Q1 and Q2 are in the on state and primary windings 106A and 106B of transformer T1 are shorted. As shown in Fig. 2F, V_T is at a low voltage, e.g., 0 Volts during this time period. Further, the voltage across switch Q2 returns to a low voltage, e.g., 0 Volts (Fig. 2D). With the transformer T1 shorted, the current in inductor L1 increases (Fig. 2E). Thus, the inductor receives the current from the input DC voltage, V_{IN}, and stores energy in inductor L1.

[0017] In the fourth time period, between t_3 and t_4, the converter releases the stored energy through primary winding 106B of transformer T1 to the output circuit 114. This is accomplished by turning off switch Q1. As shown in Fig. 2A, controller 112 reduces the voltage V_{G1} to a low level, e.g., 0 Volts. This creates a conduction path from inductor L1 to discharge current (Fig. 2E) through primary winding 106B and switch Q2. This further causes a current in secondary winding 108A based on the turns ratio between secondary winding 108A to primary winding 106B. The output capacitor C3 is charged through diode D3 to provide the desired output voltage V_{OUT} at node 116. As discussed above, the voltage, V_{OUT}, is calculated according to equation (1) above.

[0018] In subsequent time periods, controller 100 periodically repeats these four time periods to alternate between storing and releasing energy in and from inductor L1 through transformer T1 and output circuit 114.

[0019] It is noted that diodes D1 and D2, resistor R1 and capacitor C1 are used to absorb the energy in the inductor L1 and the T1 leakage inductance during shut down or other conditions when Q1 and Q2 are both off during the same time period.

[0020] Fig. 3 is a block diagram of one embodiment of a system, indicated generally at 300, and including a DC/DC converter 302 according to one embodiment of the present invention. Converter 302 comprises a boost DC/DC converter with an isolating transformer. In one

embodiment, the converter 302 is constructed as described above with respect to Figs. 1, and 2A-2F.

[0021] Converter 302 converts a DC voltage provided by power source 306 to a functional circuit 304. In one embodiment, functional circuit 304 comprises one or multiple strings of LEDs for commercial or residential lighting.. In other embodiments, functional circuit 304 comprises any appropriate electronic circuit, e.g., a microprocessor, memory, circuit board, or the like.

[0022] Converter 302 includes an inductor configured to store and release energy from the power source 306 for the functional circuit 304. Further, converter 302 includes an isolation transformer that forces the inductor to store energy during one phase of operation and to pass energy from the inductor and the power source through the transformer to the functional circuit 304 during a second phase of operation.

[0023] Embodiments of the methods described above can be implemented in a DC/DC converter for telecommunication, computing, automotive and consumer applications. A number of embodiments of the invention defined by the following claims have been described. Nevertheless, it will be understood that various modifications to the described embodiments may be made without departing from the scope of the claimed invention. Features and aspects of particular embodiments described herein can be combined with or replace features and aspects of other embodiments. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A DC/DC converter, comprising:

an inductor having first and second ends, the first end adapted to receive an input voltage;

a transformer having a primary side and a secondary side, the primary side having first and second primary windings, the first and second primary windings each having a first end coupled to the second end of the inductor and each having a respective second end;

a first switch coupled to the second end of the first primary winding;

a second switch coupled to the second end of the second primary winding;

an output circuit coupled to the secondary side of the transformer; and

wherein the first and second switches are turned on and off during selected time periods such that energy is stored in the inductor and then passed through the transformer to the output circuit to provide a boosted output voltage.

2. The DC/DC converter of claim 1, and further including a controller, coupled to the first and second switches, that generates control signals for the first and second switches.

3. The DC/DC converter of claim 2, wherein the controller generates control signals to run each of the first and second switches with a duty cycle greater than 50 percent.

4. The DC/DC converter of claim 2, wherein the control signals for the first and second switches have the same frequency and the same duty cycle and are 180 degrees out-of-phase.

5. The DC/DC converter of claim 1, wherein the first and second switches are both on for a period of time to store energy in the inductor.

6. The DC/DC converter of claim 1, wherein the output voltage is n/(1-D) times the input voltage wherein n is the turns ratio of the transformer, and D is duty cycle of the first and second switches.

7. The DC/DC converter of claim 1, wherein the secondary side of the transformer includes a center tap and the output circuit includes:

an output capacitor having first and second nodes, the first node coupled to the center tap of the secondary side of the transformer;

a first diode coupled between the second node of the capacitor and a first end of the secondary winding; and

a second diode coupled between the second node of the capacitor and a second end of the secondary winding.

8. A method for boosting an input DC voltage, the method comprising:

receiving the input DC voltage;

storing energy in an inductor from a current associated with the input DC voltage during a first time period;

passing the stored energy from the inductor through an isolation transformer during a second time period; and

outputting a DC voltage from the transformer at a higher voltage level than the input DC voltage.

9. The method of claim 8, further comprising:

storing energy in the inductor during a third time period;

passing the stored energy from the inductor through the transformer during a fourth time period; and

repeating the process of storing and passing energy through the transformer in subsequent, periodic first, second, third and fourth time periods.

10. The method of claim 8, wherein storing energy in the inductor comprises shorting a primary side of the transformer so that current is fed to the inductor.

11. The method of claim 8, wherein passing the stored energy during the second time period comprises passing current through a conduction path from the inductor to the transformer, the conduction path established by a first transistor in an on state.

12. The method of claim 9, wherein passing the stored energy during the fourth time period comprises passing current through a conduction path from the inductor to the transformer, the conduction path established by a second transistor in an on state.

13. The method of claim 10, wherein shorting the primary side comprises having both a first transistor, coupled to a first end of the primary side, and a second transistor, coupled to a second end of the primary side, on during the first time period.

14. The method of claim 13, wherein the first and second transistors are operated at greater than 50 percent duty cycle, and 180 degrees out of phase.

15. A method for boosting an input DC voltage, the method comprising:

receiving the input DC voltage at an inductor, the inductor coupled to an isolating transformer;

generating control signals for first and second transistors coupled to the isolating transformer;

when the control signals turn on both of the first and second transistors, storing energy in the inductor from the input DC voltage; and

when the control signals turn on only one of the first and second transistors, releasing energy from the inductor through the isolating transformer.

16. The method of claim 15, wherein generating control signals for the first and second transistors comprises generating control signals to drive the transistors at greater than 50 percent duty cycle, and 180 degrees out of phase.

17. The method of claim 15, wherein each of the first and second transistors turns off and back on during the time that the other transistor is on.

18. An electronic system comprising:

a functional circuit; and

an isolated boost DC/DC converter coupled to provide DC power to the functional circuit, the converter comprising:

an inductor, coupled to a power source, the inductor configured to store and release energy from the power source for the functional circuit; and

a transformer, coupled to the inductor, the transformer configured force the inductor to store energy during one phase of operation and to pass energy from the inductor through the transformer to the functional circuit during a second phase of operation.

19. The system of claim 18, wherein the functional circuit comprises an LED lighting circuit.

20. The system of claim 18, wherein the transformer includes a primary side and a secondary side and wherein a first transistor is coupled to a first end of the primary side and a second transistor is coupled to a second end of the transistor, the first and second transistors controlled to short the primary side of the transformer when the inductor stores energy.

21. The system of claim 20, wherein the converter includes a controller that controls the on state of each of the first and second transistors such that each has a duty cycle greater than 50 percent and the first and second transistors are out-of-phase with each other.

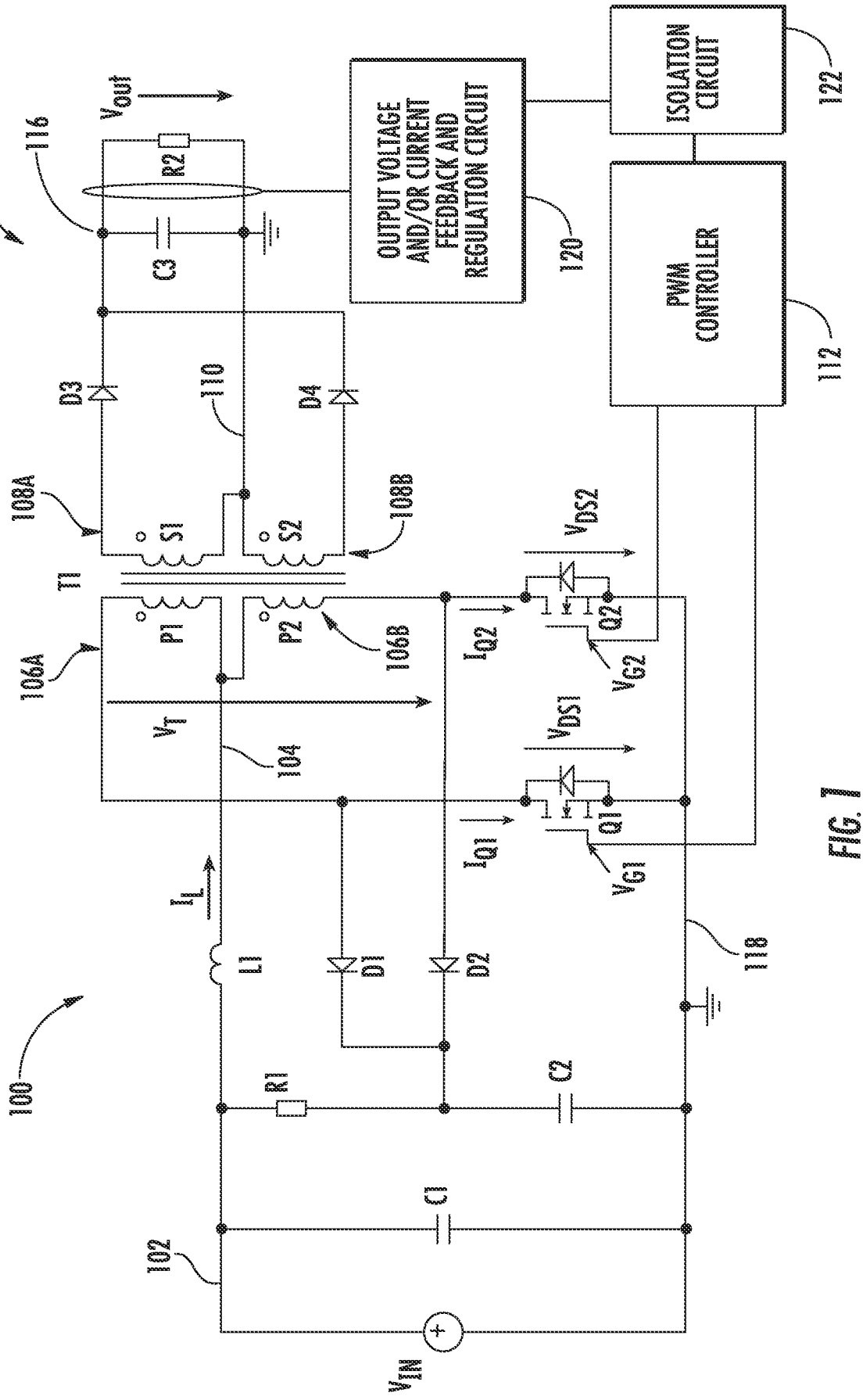

ISOLATION CIRCUIT
122
OUTPUT VOLTAGE AND/OR CURRENT FEEDBACK AND REGULATION CIRCUIT
120
PWM CONTROLLER
112
V_{out}
R2
C3
114
116
D3
D4
110
108A
108B
S1
S2
T1
P1
P2
106A
106B
V_T
104
V_{DS2}
I_{Q2}
Q2
V_{G2}
V_{DS1}
I_{Q1}
Q1
V_{G1}
I_L
L1
D1
D2
118
100
R1
C2
C1
102
V_{IN}

FIG. 1

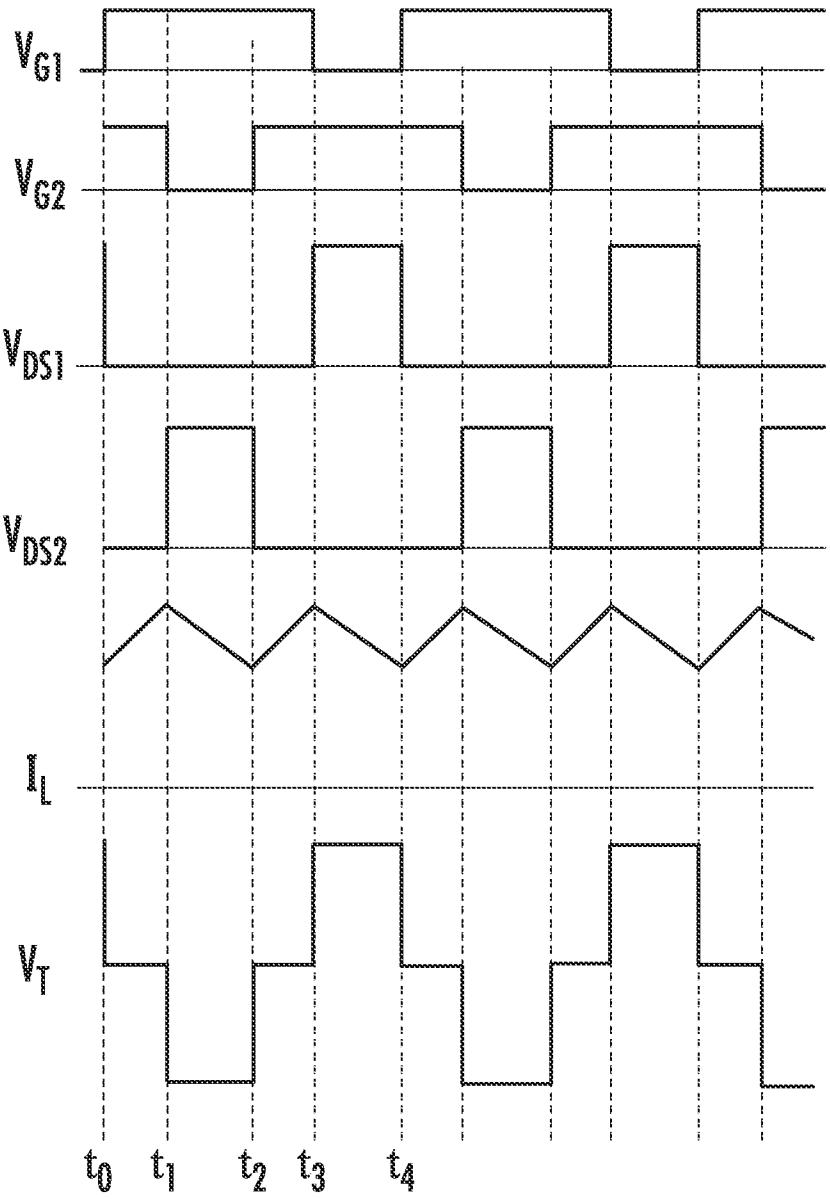


FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

FIG. 2E

FIG. 2F

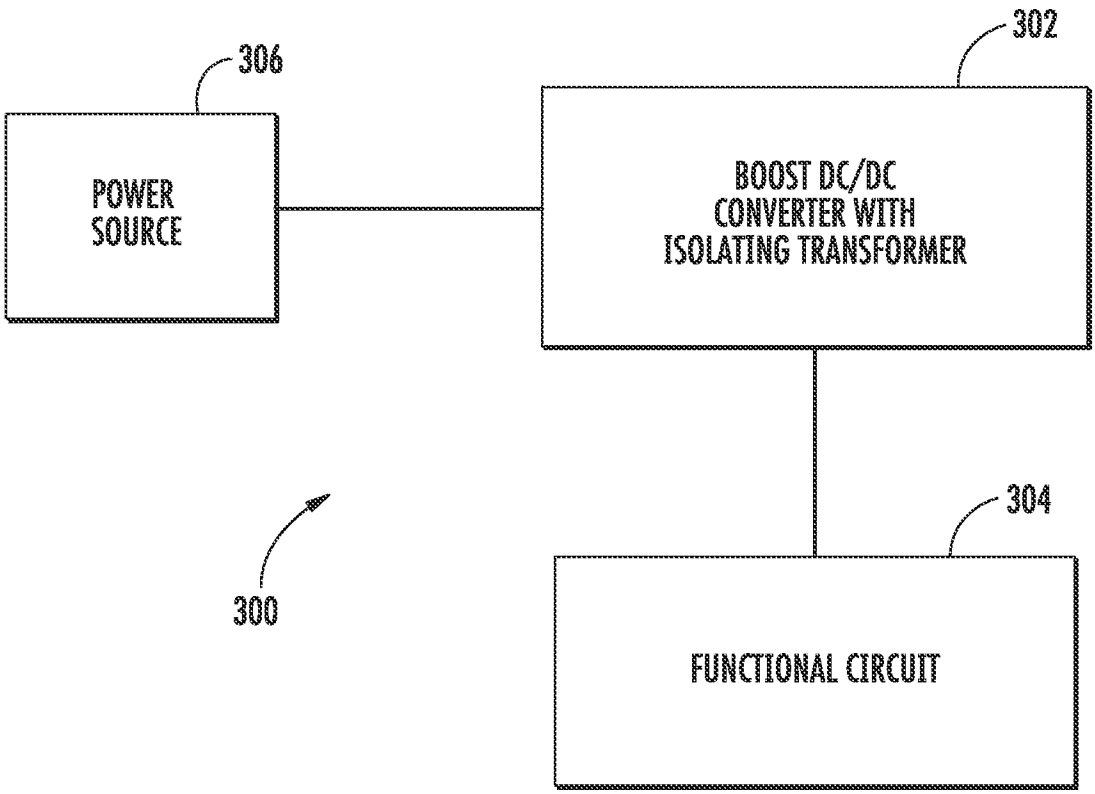

306
302
POWER SOURCE
BOOST DC/DC CONVERTER WITH ISOLATING TRANSFORMER
300
304
FUNCTIONAL CIRCUIT

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/070969

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI, CPRSABS, CNKI: TRANSFORMER, INDUCTOR, INDUCTIVE, WINDING, COIL, REACTOR, SWITCH, MOS, FET, TRANSISTOR, IGBT, BOOST, STEP UP, DOUBLER, TWO, SECOND, TAP

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5654881 A (LOCKHEED MARTIN CORP) 05 Aug. 1997 (05. 08. 1997) column 2, line 38 to column 6, line 64 of the description, Figs. 1, 3-5	1-21
X	JP 2007312464 A (KIKUSUI DENSHI KOGYO KK) 29 Nov. 2007 (29. 11. 2007) paragraphs 0003-0004 of the description, Figs. 1-3	1-21
X	JP 2004147436 A (SANKEN DENKI KK) 20 May 2004 (20. 05. 2004) paragraphs 0012-0025 of the description, Figs. 2-5	1-21
A	CN 101478253 A (UNIV HUANAN SCI & ENG) 08 Jul. 2009 (08. 07. 2009) the whole document	1-21

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 Oct. 2011 (24. 10. 2011)	**24 Nov. 2011 (24.11.2011)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer SONG, Xuemei Telephone No. (86-10)62411797

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/070969

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US 5654881 A	05. 08. 1997	NONE	
JP 2007312464 A	29. 11. 2007	JP 4391496 B2	24. 12. 2009
JP 2004147436 A	20. 05. 2004	NONE	
CN 101478253 A	08. 07. 2009	CN 101478253 B	08. 12. 2010

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/070969

Continuation of Box A in second sheet:

CLASSIFICATION OF SUBJECT MATTER

H02M 3/28 (2006.01) i

H02M 3/337 (2006.01) i