United States Patent

Falk

[15] **3,651,317**

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[54] DIGITAL FUNCTION GENERATOR

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[52] **U.S. Cl.** **235/197,** 235/150.53

[51] **Int. Cl.** **G06f 15/34**

[58] **Field of Search** 235/197, 150.53, 150.3, 164, 235/152; 328/140, 141, 142; 307/223, 271, 220, 225

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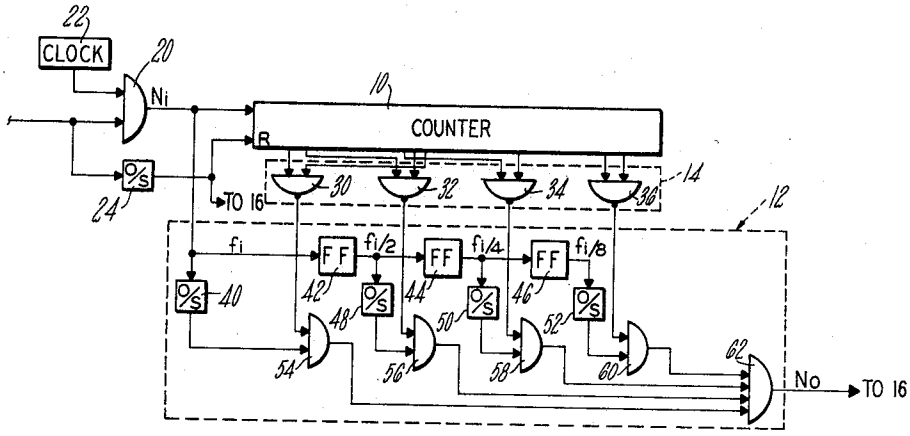
Primary Examiner—Joseph F. Ruggiero

Attorney—Fishman and Van Kirk

[57] **ABSTRACT**

A digital function generator which may be programmed to provide an output signal which is an arbitrary function of the applied input is disclosed. An input signal is applied simultaneously to a counter and binary divider. The input counter and divider are interconnected by logic circuitry which controls the division rate in accordance with the number in the counter whereby the output of the divider will be commensurate with the number of input pulses delivered to the function generator divided by the factors decoded from the incremental position of those input pulses during each sampling period.

7 Claims, 4 Drawing Figures



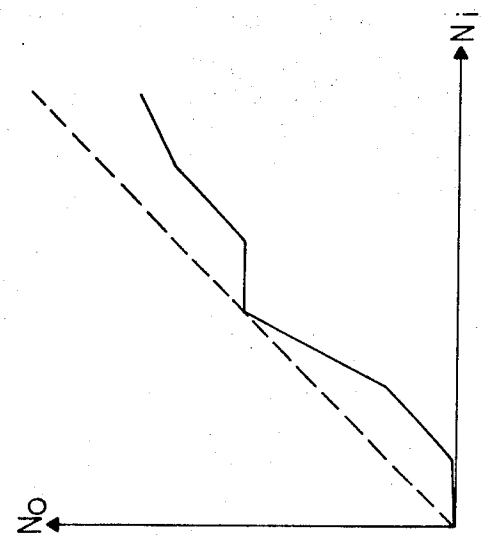


FIG. 2

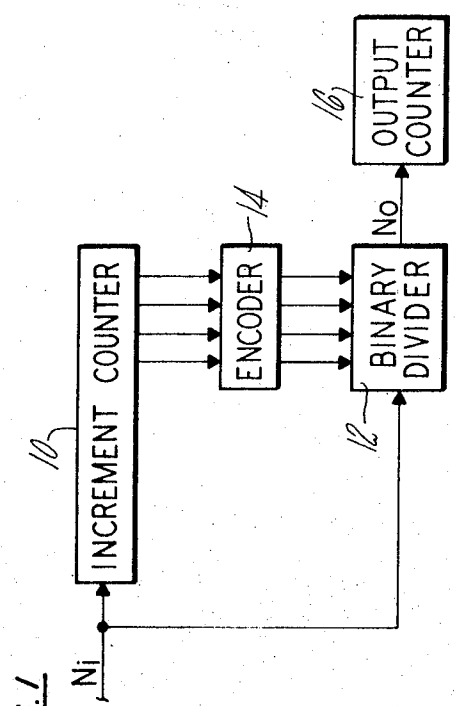


FIG. 1

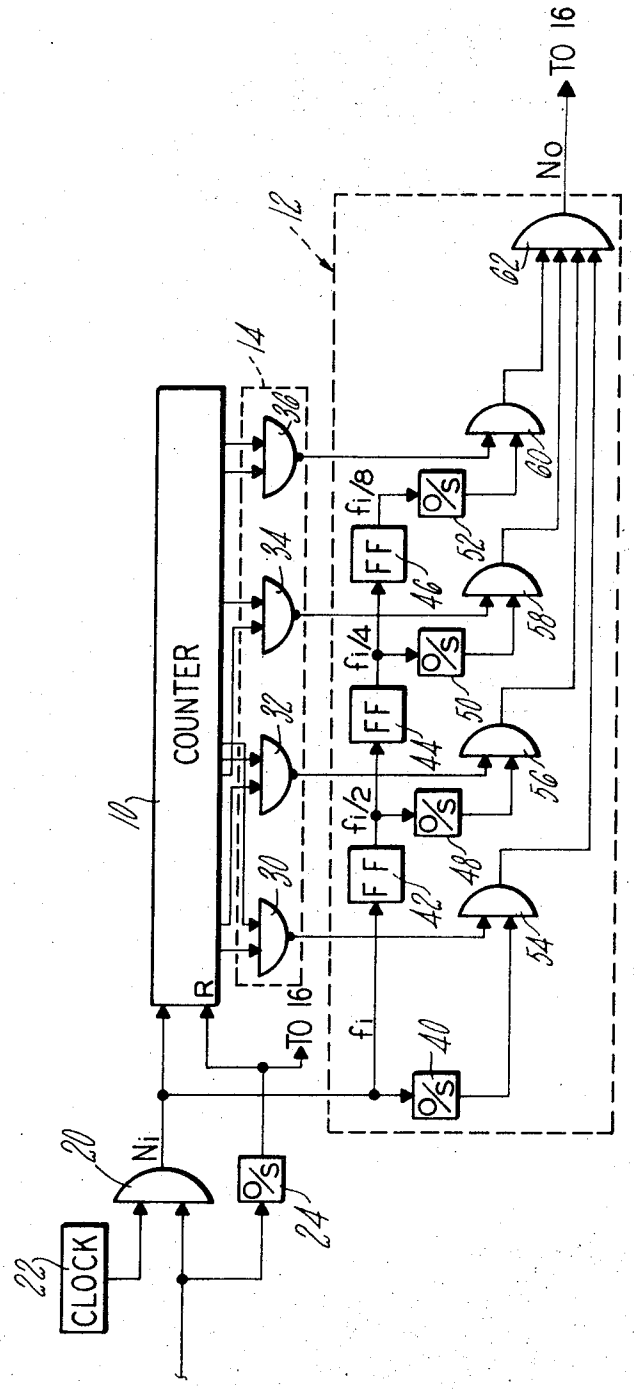


FIG. 3

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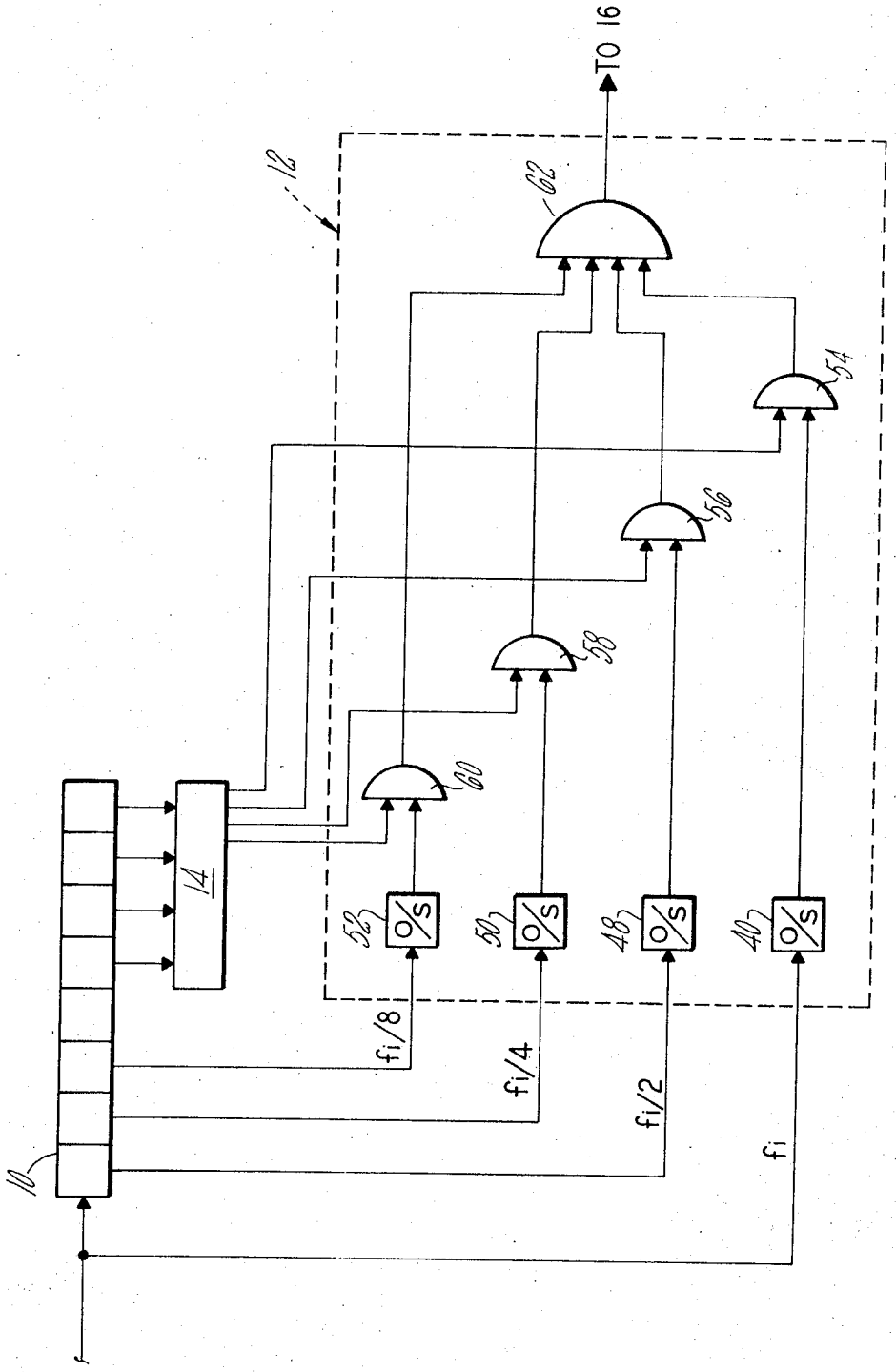

FIG. 4

DIGITAL FUNCTION GENERATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the electrical simulation of nonlinear functions. More specifically, the present invention is directed to arbitrary function generators and particularly to function generators which employ digital circuit techniques. Accordingly, the general objects of the present invention are to provide novel and improved methods and apparatus of such character.

2. Description of the Prior Art

Electrical function generators are well known in the art. When the output of the function generator varies linearly with the input signal, both digital and analog techniques have been employed in the prior art. However, in situations where it was necessary or desirable to generate a schedule or function, the prior art has universally resorted to the use of analog circuit techniques. The advantages of digital computation when compared to achieving the same result by analog techniques are numerous and well known in the art.

While not limited thereto in its utility, the present invention is particularly well suited for use in a digital fuel control system for combustion engines; particularly for gas turbine engines. As is well known, fuel controls for gas turbine engines must provide for the scheduling of fuel flow in response to input speed signals on a nonlinear basis under certain operating conditions. For example, it is well known that a fuel control for a gas turbine engine must accommodate an acceleration schedule whereby the rate of fuel delivery to the engine during periods of acceleration may be varied in a nonlinear fashion, in accordance with a predetermined schedule, from the fuel delivery rate which will be commanded under steady-state operation. The fuel flow rate will, of course, be varied as a linear function of speed error during steady-state operation; the acceleration schedule having effect only under the condition when the fuel flow commanded is at the maximum permissible for safe engine operation.

SUMMARY OF THE INVENTION

The present invention overcomes the above-discussed and other disadvantages of the prior art by providing a digital, arbitrary function generator. Accordingly, an object of the present invention is to provide an arbitrary function generator, typically with a single program, which provides an output signal in binary form which corresponds to a scheduled value of a number commensurate with an independent variable delivered to the function generator as a series of pulses.

In accordance with the present invention, a digital input signal in the form of a pulse packet and commensurate with the magnitude of a sensed independent variable is loaded serially into an input binary counter. The binary input counter keeps static account, during each input pulse packet, of the number of pulses which have passed through a binary divider. An encoder connected to the counter and having, as its input, the most significant bits of the counter, controls the rate at which the binary divider will divide the input number as represented by the pulse packet. The output pulses from the binary divider are delivered serially into an output counter which thus contains a number resulting from the division of the number of pulses in the input packet by a factor determined by the connection between the encoder and binary or input counter. That is, the number loaded into the output counter is commensurate with the number of pulses in each input pulse packet divided by the factors encoded from the incremental position of those pulses in the packet for every position in that packet.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be better understood and its numerous objects and advantages will become apparent to those skilled in the art by reference to the accompanying drawing wherein like reference numerals refer to like elements in the several figures and in which:

FIG. 1 is a functional block diagram of a first embodiment of the present invention;

FIG. 2 is a graphical representation of an output function which may be generated by the present invention;

FIG. 3 is a block diagram of a portion of the embodiment shown in the functional diagram of FIG. 1; and

FIG. 4 is a block diagram of a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to FIG. 1, an input signal N_I will be delivered simultaneously to an input increment counter **10** and a binary divider **12**. The input signal N_1 will be a pulse packet consisting of a group of pulses corresponding in number to the magnitude of an independent variable. Considering a fuel control application of the present invention, signal N_I will be a packet of pulses commensurate in number with a speed signal generated by means well known in the art. Counter **10** will be a binary counter with serial read-in and parallel readout. As will be described below in connection with the description of FIG. 3, counter **10** keeps static account, for each input pulse packet, of the number of pulses which have been passed through divider **12**.

Preselected stages of counter **10** are connected to a logic circuit or encoder **14**. As will also be described below in the discussion of FIGS. 3 and 4, encoder **14** comprises a plurality of NAND or other suitable logic gates. The particular numbers to which encoder **14** will be responsive will be predetermined and, again considering utilization of the present invention in a turbine engine fuel control, these numbers will be commensurate with predetermined speed magnitudes which require nonlinear adjustment of the maximum fuel delivery rate.

The output of encoder **14** will be a plurality of control signals which are applied to binary divider **12**. These control signals, in the manner to be described below, determine the factor by which the number of pulses comprising each input pulse packet is divided before being delivered to an output counter **16**. Accordingly, the number loaded into output counter **16** will vary non-linearly with the input signal in accordance with a schedule determined by the interconnection of encoder **14** and input counter **10**.

The number N_o loaded into counter **16** will be a nonlinear function of the input number N_1. A typical nonlinear function is depicted by the solid line in FIG. 2. The broken line in FIG. 2 represents the linear function which would result from the application of the input signal directly to output counter **16**. Counter **16** will have parallel readout and the number in counter **16** will typically be periodically sampled and employed for the desired control purposes. Again considering the digital fuel control application, the number in counter **16** would be read out to schedule the maximum permissible fuel flow at that engine operating point.

Referring now to FIG. 3, an input signal commensurate with the independent variable will be applied to a first input of AND-gate **20**. The input will typically be a pulse width modulated signal; the duration of the input pulses being related to the magnitude of the sensed parameter. A high-frequency pulse train generated by an oscillator or clock **22** is applied to the second input of gate **20**. Accordingly, gate **20** will pass a packet of pulses from clock **22** during the periods when an input signal pulse is applied thereto; the number of pulses in each packet being proportional to the instantaneous value of vehicle speed in the fuel control acceleration flow scheduling application.

The pulse width modulated input signals are also applied to a one shot or monostable multivibrator **24**. Multivibrator **24** is responsive to the leading edge of each input pulse and generates reset pulses which are applied to the reset terminals of counters **10** **16**. The response of multivibrator **24** is sufficiently fast so that none of the clock pulses passed by gate **20** will be lost.

The pulse packet appearing at the output of AND-gate **20** will be applied to counter **10** and to binary divider **12**. Counter **10**, as noted above, is a binary counter which will have the necessary capacity. A typical eleven bit counter which may be employed in the present invention comprises three Signetics Corporation type S8281 four-bit binary counters suitably interconnected.

As noted above, encoder **14** may comprise a plurality of NAND gates. In the embodiment being described, four gates **30, 32, 34** and **36** are employed. These NAND gates, which will typically be Signetics Corporation type S8417, are connected to preselected stages of counter **10**. As a result of the selection of which counter stages are connected to the inputs of gates **30, 32, 34** and **36**, each of these gates will sense when the counter has been filled to a preselected, different binary number. Gates **30, 32, 34** and **36** will, in the manner known in the art, each provide a control signal which will be delivered to binary divider **12** and employed in the manner to be described below.

As noted above, the pulse packet passed by gate **20** is delivered to binary divider **12** where each pulse in the packet triggers one shot multivibrator **40**. The packet of clock pulses delivered to divider **12** is also applied as the input to a division network comprising series connected bistable multivibrator circuits **42, 44** and **46**. The division of a binary input signal by means of series connected bistable circuits is a technique well known in the art. The input pulse train is applied to multivibrator **42** which produces an output signal for every second input pulse. The output signals from multivibrator **42** are applied as the the input to multivibrator **44** and also as the control signal to a one shot multivibrator **48**. In response to the applied input, bistable multivibrator **44** will provide an output signal commensurate with every fourth pulse in the packet applied to divider **12**. The output pulses from bistable multivibrator **44** are applied as the input to bistable multivibrator **46** and also as the control signal for a one shot multivibrator **50**. Bistable multivibrator **46** will provide an output pulse, commensurate with every eighth pulse in the input pulse packet, which controls a one shot multivibrator **52**. The use of one shot multivibrators **40, 48, 50** and **52** is in the interest of insuring that the output pulses resulting from the division of the input pulse train will be displaced in time from one another. The one shot multivibrators provided against overlapping in time of the pulses resulting from the switching of bistable multivibrators **42, 44** and **46**.

Binary divider **12** also comprises AND-gates **54, 56, 58** and **60**. Each of these AND gates has a first or enabling input connected to the respective one of the NAND gates comprising encoder **14**. The second input to each of the AND gates in divider **12** is connected to a respective one shot multivibrator. The pulses generated by one shot multivibrators **40, 48, 50** and **52** will be passed to a summing circuit **62**, which will comprise an OR gate, and thence to output counter **16** only when the respective AND-gates **54, 56, 58** and **60** are enabled by control signals from encoder **14**. Thus, through programming the gates comprising encoder **14** to be responsive to preselected numbers loaded into counter **10**, the pulses generated by the divider circuit comprising the combination of bistable and one shot multivibrators will be summed in a predetermined manner to provide an output binary signal commensurate with the desired output signal scheduling. This may result in the example curve depicted in FIG. **2** wherein the various changes in slope of the curve are commensurate with the enabling of an additional one or combination of AND gates **54, 56, 58** and **60**. Thus, considering jointly FIGS. **2** and **3**, only AND-gate **60** will initially be enabled and the input pulse packets will be divided by a factor of eight before being applied to output counter **16**. As counter **10** is filled, in the manner described above, the AND-gates **54, 56, 58** and **60** will be enabled and disabled whereby the curve of FIG. **2** will be produced. The steepest portion of the output schedule will, of course, be achieved when all four AND gates in divider **12** are enabled. Between the extremes of only gate **60** being enabled and all four gates being enabled are a substantial number of possibilities which will generate different output pulse rates during the sampling of each input pulse packet.

FIG. **4** depicts a second embodiment of the function generator of the present invention. The embodiment of FIG. **4** differs from the embodiment of FIGS. **1** and **3**, as described above, only with respect to the method of dividing pulses comprising the packet delivered to increment counter **10**. Thus, in the embodiment of FIG. **4**, the first three stages of counter **10** serve the dual functions of counter stages and portions of a series connected bistable circuit division network. This dual use of a binary counter is a technique well known in the art and permits the circuit simplification whereby bistable multivibrators **42, 44** and **46** of the FIG. **3** embodiment are not employed in the FIG. **4** embodiment. The embodiment of FIG. **4**, however, functions in the identical manner as the embodiment of FIG. **3**.

While a preferred embodiment has been shown and described, various modifications and substitutions may be made thereto without departing from the spirit and scope of the present invention. Accordingly, it is to be understood that the present invention has been described by way of illustration and not limitation.

What is claimed is:

1. A digital function generator comprising:

counter means for receiving and counting input pulses comprising pulse packets commensurate with a monitored variable, said counter means providing a plurality of output signals commensurate with the number of input pulses received;

frequency divider means responsive to the input pulses for generating a plurality of output signals at a plurality of frequencies below the input pulse frequency;

scheduling means connected to said counter means and responsive to selected of said counter means output signals for generating gating control signals commensurate therewith; and

gate means connected to said scheduling means and controlled thereby, said gate means also being connected to said frequency divider means whereby a signal at a frequency determined by the incremental position of the input pulses in said counter means will be passed to an output terminal.

2. The apparatus of claim **1** wherein said counter means comprises:

a binary counter having serial input and parallel output.

3. The apparatus of claim **3** wherein said scheduling means comprises: a plurality of gate circuits.

4. The apparatus of claim **3** further comprising:

means connected to receive the signals passed by said gate means for summing said signals at different frequencies.

5. The apparatus of claim **4** wherein said frequency divider means for generating a plurality of signals at a plurality of frequencies comprises:

binary divider means.

6. A method of generating, from electrical input pulses at a first frequency, an arbitrary digital function comprising the steps of:

counting the number of electrical input pulses received during a sampling period;

simultaneously dividing the input pulse frequency to provide a plurality of signals at differing frequencies; and

selecting the instantaneous output frequency, from at least one of those signals produced by dividing the input frequency, as a function of the incremental position of the last counted input pulse.

7. The process of claim **7** further comprising:

counting a number of electrical pulses commensurate with the output frequency selected.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,651,317 **Dated** March 21, 1972

Inventor(s) Ronald E. Falk

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 2, line 14, change "$_{1}$" to --$_{i}$--

Column 2, line 46, change "$_{1}$" to --$_{i}$--

Claim 3, line 1 (column 4, line 49), change "3" to --2--

Claim 5, line 1 (column 4, line 54), change "4" to --3--

Claim 7, line 1 (column 4, line 69), change "7" to --6--

Signed and sealed this 11th day of July 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents