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McMaster

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[54] **CIPHER LOCK**

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[52] **U.S. Cl.**..... **307/115,** 340/147 R, 317/134

[51] **Int. Cl.**..... **E05b 49/00**

[58] **Field of Search**. 317/134; 340/147 R, 147 MD; 70/277–283; 307/115

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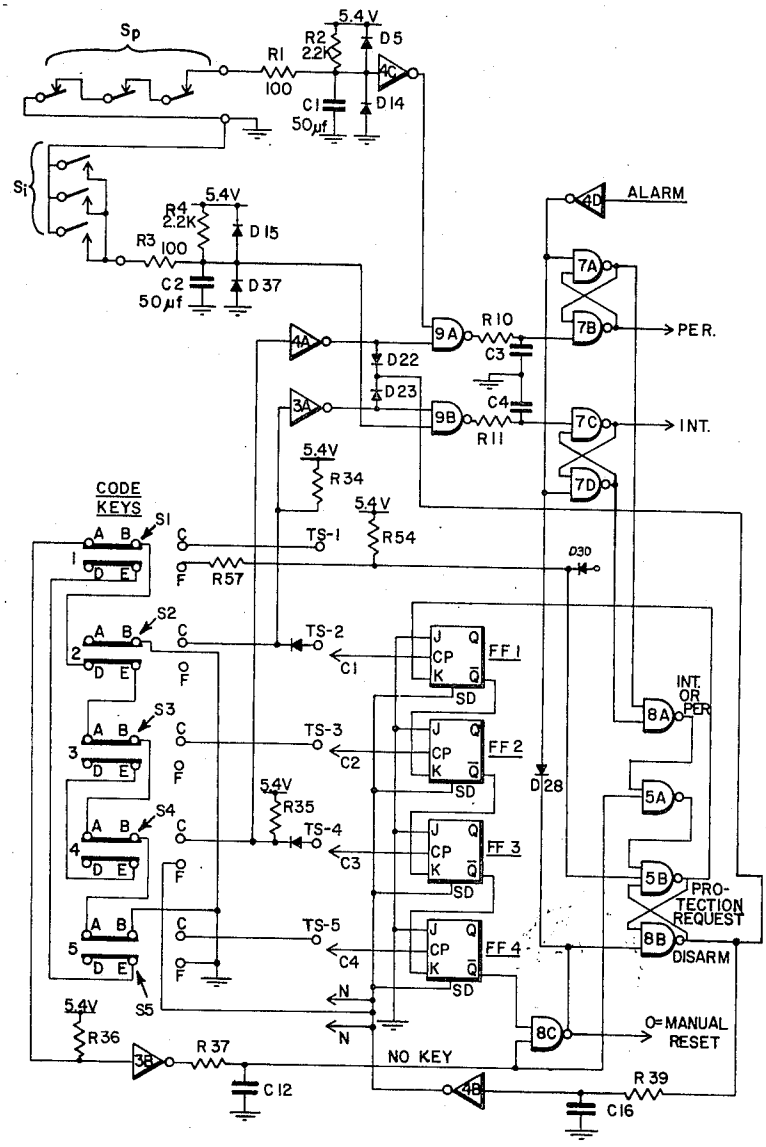
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[57] **ABSTRACT**

An electronic cipher lock in which the same switches which are used to enter the unlocking code can be used to serve additional switching functions.

4 Claims, 2 Drawing Figures



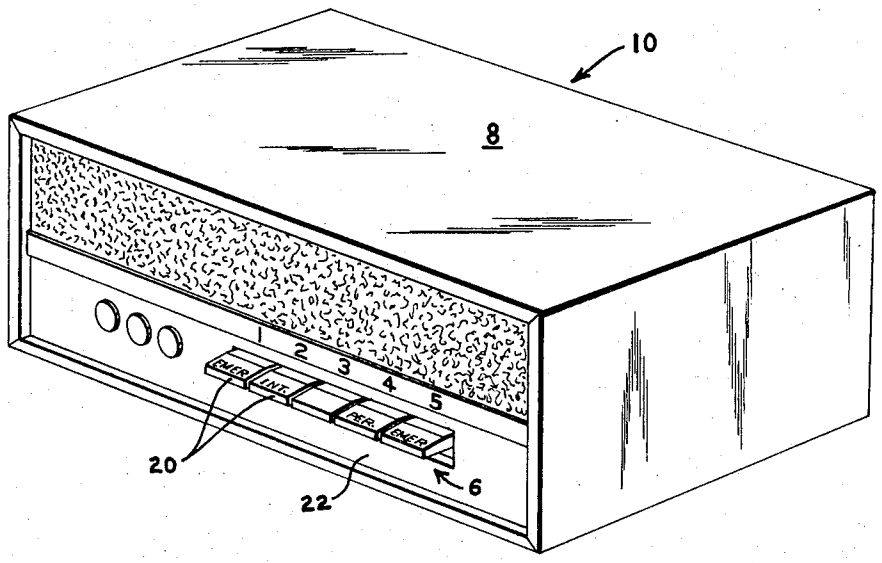


Fig. 1

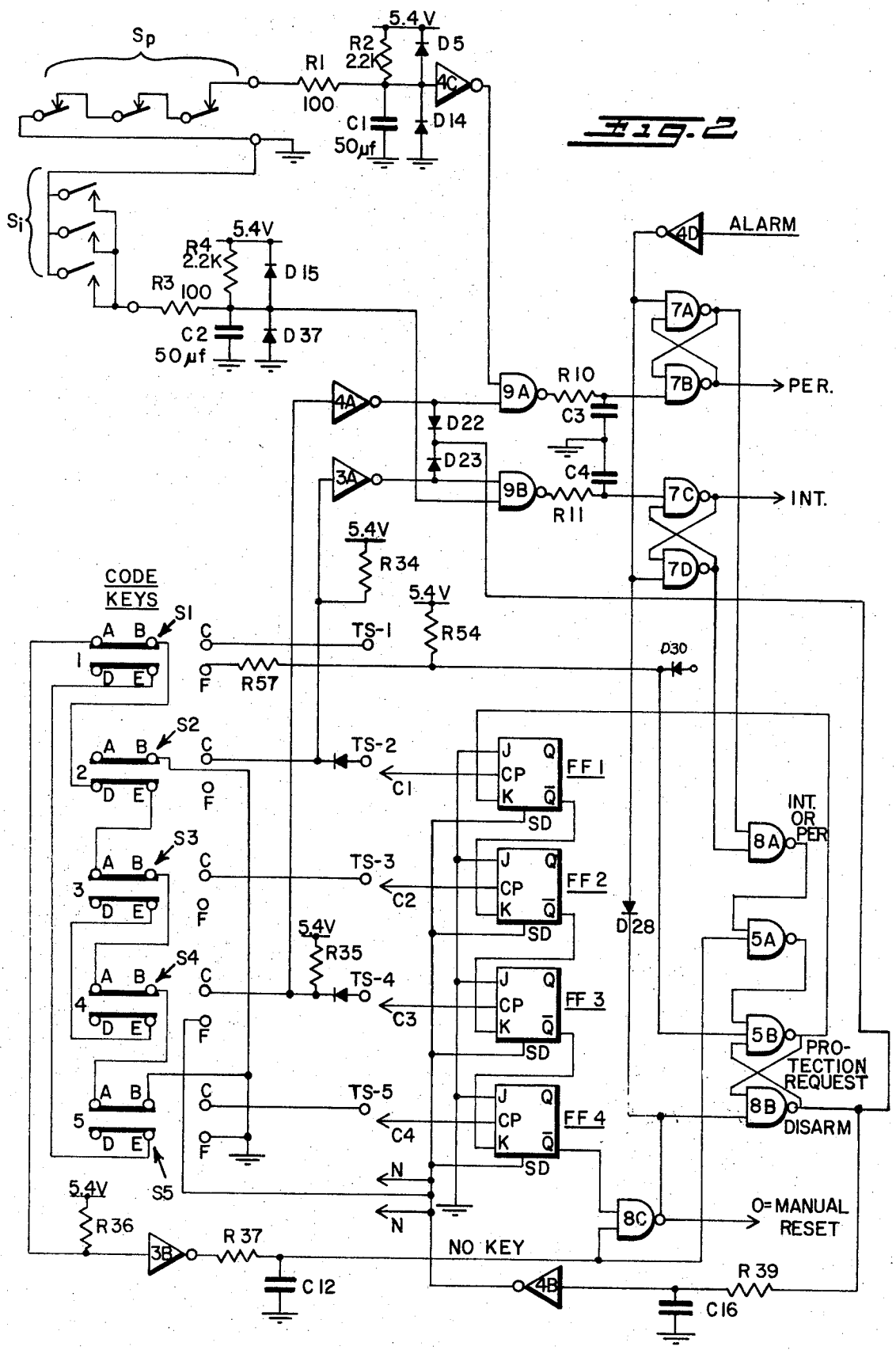

Sp
Si
R1
100
R2
2.2K
5.4V
D5
4C
C1
50μf
D14
R3
100
R4
2.2K
5.4V
D15
C2
50μf
D37
4D
ALARM
7A
7B
PER.
9A
R10
C3
4A
D22
D23
3A
9B
C4
R11
7C
INT.
7D
5.4V
R34
5.4V
R54
CODE
KEYS
S1
S2
S3
S4
S5
TS-1
TS-2
TS-3
TS-4
TS-5
R57
D30
FF 1
FF 2
FF 3
FF 4
C1
C2
C3
C4
5.4V
R35
D28
8A
INT.
OR
PER
5A
5B
PRO-
TECTION
REQUEST
8B
DISARM
N
N
8C
O=MANUAL
RESET
5.4V
R36
3B
R37
NO KEY
C12
4B
R39
C16

Fig. 2

CIPHER LOCK

BACKGROUND OF THE INVENTION

This invention relates to security devices and, more particularly, to a novel electronic cipher lock in which each of the individual code-entering keys thereof can also provide an additional switching function.

In the security industry, electronic cipher locks have been used primarily as a means for controlling the admittance of personnel into secured areas. These locks commonly comprise a plurality of finger-depressible keys, typically five in number, and logic circuitry for controlling the opening of a door or the like in response to the sequential depression of the individual keys according to a predetermined sequence which constitutes a code. Because of the relatively large numbers of permutations of the unlocking code afforded by a multikeyed cipher lock, the chance of unauthorized entry by a person who, by trial and error, discovers the unlocking code is relatively small. The cipher lock, of course, offers the advantage over conventional keyed locks of not requiring a key or the like for operation, as well as the advantage over conventional combination locks of not requiring a relatively lengthy period of time for dialing the proper combination.

In addition to being useful in the manner described above, the cipher lock has also found use in the security industry as a means for controlling the intentional disarming of a security system. For instance, a number of commercially available intruder detection devices incorporate a cipher lock as a means for enabling an authorized person to disarm the device prior to the sounding of an alarm. The cipher lock is commonly incorporated in the housing of the device, and the device usually comprises circuitry for delaying alarm activation for several seconds after intrusion is detected. Such delay affords an authorized person, upon entering an area under surveillance and being detected, ample opportunity to enter the appropriate code into the cipher lock and thereby disarm the device prior to the sounding of an alarm. Ideally, the code-entering keys of the cipher lock are readily accessible on the device housing, preferably on the front or face plate thereof. This arrangement facilitates the disarming of the device within the built-in delay period.

A major problem with positioning the cipher lock keys on the face plate of the housing of a detection component is that the keys often interfere and can be confused with other keys or switches on the same face plate which control the various functions of the device. For instance, the face plate of many intruder detection devices include a so-called "panic" button or switch which immediately sounds an alarm upon being activated. In addition, it is often desirable to arrange other switches or keys on the face plate for the purpose of controlling the operation of other detection components which, together with the cipher lock-incorporating device, make up a security system. Also, the separate provision for a multitude of control functions in addition to a cipher lock capability often conflicts with a desire to make the detection device as small and unobtrusive as possible.

SUMMARY OF THE INVENTION

An object of this invention, therefore, is to provide an improved electronic cipher lock in which the same

code-entering keys can also serve as switches for controlling various functions of a security system of which it forms a part. Due to the dual function capability of the cipher lock keys, control function keys or switches in addition to the cipher lock keys are obviated. Thus, there is less chance for confusion of the user.

The novel electronic cipher lock of the invention comprises a plurality of electrical switches and logic circuitry for generating an electrical signal in response to the activation of two or more of such switches according to a predetermined sequence which constitutes a code. Moreover, the lock comprises circuit means, operatively connected to at least one of the switches and responsive to the generation of such electrical signal, for rendering the logic circuitry insensitive to the first activation of any of the switches following the generation of such electrical signal, whereby any or all of the switches can be used to provide a control or switching function in addition to that of code entry.

Other objects of the invention and its various advantages will become apparent to those skilled in the art from the ensuing detailed description of a preferred embodiment, reference being made to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a perspective view of an intruder-detection device incorporating the novel cipher lock of the invention, and

FIG. **2** is an electrical schematic of the cipher lock circuitry according to a preferred embodiment of the invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The novel cipher lock of the invention is described hereinbelow with particular reference to its utility as an integral part of an intruder detection system. It is apparent, however, that this lock has substantial utility in other types of systems.

Referring now to FIG. **1**, the cipher lock **6** of the invention is shown incorporated in the housing **8** of a conventional intruder-detecting device **10.** The detection device may comprise for instance, means for transmitting acoustic or electromagnetic energy waves into a region in which unauthorized entry is to be detected, and means for sounding an alarm in response to the sensing of a predetermined change in the level of reflected energy returned to the device by objects in the region under serveillance. As shown, cipher lock **6** comprises a plurality of finger-depressible keys **20** which extend outwardly from the face plate **22** of the detection device housing. As will be explained subsequently, keys **20** are the movable members of double pole, double throw switches. When depressed, keys **20** can serve either (1) to enter one digit of a multidigit cipher lock code into a memory circuit, such code serving to disarm the device and all devices operatively coupled thereto, or (2) to control the manner in which the device, or other security devices which are connected thereto, function. In other words, each of the keys **20** can provide a dual function. When not being used to control the operation of a cipher lock, the keys can serve a control function, and vice versa.

For purposes of illustration, keys **20** are numbered **1** through **5.** Upon depressing the keys according to a coded sequence, (e.g., **1,3,4,2**) and thereby generating

an electrical signal which acts to disarm or turn off the security system, the same keys might then be used to rearm the system or, alternatively, be used to immediately activate an alarm in a panic situation. For instance, simultaneous depression of keys **1** and **5** could serve as a "panic button" to immediately sound an alarm. Depression of key **2** alone could serve to activate only those security devices in which the completion of a normally open circuit serves to activate an alarm relay. Conventional ultrasonic, microwave and electro-optical detection devices are devices of this variety, as are conventional floor mat sensors. These devices are commonly known as "interior" security devices, as distinguished from "perimeter" security devices. The latter include door switches, window tapes, etc., which are typically wired in series and comprise a normally closed circuit which is rendered open by the presence of an intruder. Depression of key **4** alone could serve to activate only the perimeter devices, and the simultaneous depression of keys **2** and **4** could be used to activate both interior and perimeter security devices. The ensuing description describes the logic circuitry for utilizing the cipher lock keys for the dual functions suggested above. It will be appreciated, however, that once the keys have been used to enter the cipher lock code, they may be subsequently used to serve virtually any switching function.

The cipher lock of the invention can be best understood by referring to the circuitry schematically illustrated in FIG. **2.** There, the cipher lock keys **1–5** of FIG. **1** are shown as being a part of the double pole, double throw switches **S1–S5,** respectively. Each switch comprises a spring biased key which, when in its rest position or inactivated, serves to connect the A contacts to the B contacts, as well as to connect the D contacts to the E contacts. When activated, or moved to the right as viewed in FIG. **2,** the individual keys act to disconnect the aforementioned connections, and connect the B contacts to the C contacts, and to connect the E contacts to the F contacts. Note, due to the spring bias on the keys, a connection between contacts B and C, and between contacts E and F is only maintained while the key is depressed by the user. Upon release, the switches return to the state illustrated in FIG. **2.** Switches **S1–S5** are so connected that the activation of any one of them serves to connect contact C of the activated switch to ground. In the ensuing description, circuitry for utilizing switches **S1–S5** for controlling the operation of the cipher lock will be discussed first, followed by a description of the circuitry which permits these switches to be used for controlling other functions.

The logic circuitry for providing an electrical output signal y which may be used to disarm all detection devices in response to the proper sequential activation of switches **S1–S5** comprises a chain of conventional JK flip-flops, **FF1-FF4.** All flip-flops except flip-flop **FF4** have the $\overline{Q}$ output connected with the K input terminal of the succeeding flip-flop in the chain. By this arrangement, none of the flip-flops can change state until all of those preceding it in the chain have done so. Note, the Q output is not required for the operation of the invention and, hence, it is not used. In order for an output (i.e., logical **1**) to appear at the $\overline{Q}$ output of any flip-flop, two conditions must be met: (1) the so-called clock pulse input, CP, must be grounded to produce a logical **0** input, and (2) the K input must be a logical **1.** Note, all J inputs of the flip-flops are grounded to provide a logical **0.** Each of the CP inputs are normally logical **1.** In order to change the CP input to logical **0,** the associated input leads **C1–C4** must be grounded. This can be achieved by connecting any one of the leads **C1–C4** to one of the terminals **TS-1** through **TS-5,** the latter being connected directly to the C contacts of the cipher lock switches, and activating or depressing the appropriate switch. As mentioned above, switch activation results in the grounding of contact C of the switches.

As indicated above, in order to produce a $\overline{Q}$ output signal y from the last flip-flop in the chain, this being the signal which produces the disarming of the detection system, there must be a $\overline{Q}$ output (i.e., a logical **1**) from all other flip-flops in the chain so that the K inputs will be logical **1**; also, there must be a logical **0** at the CP input.

Assuming that the cipher code is the sequence **1,2,3,4,** then lead **C1** of the first flip-flop **FF1** must be connected to terminal **TS-1,** lead **C2** of the second flip-flop **FF2** must be connected to terminal **TS-2,** etc. Assuming for the time being that the K input of the first flip-flop is a logical **1,** then the activation of switch **S1** will produce a logical **0** at the CP input of **FF1** which, in turn, will produce a $\overline{Q}$ output of logical **1.** The latter being fed to the K input of the second flip-flop satisfies one of the two conditions for producing a $\overline{Q}$ output therefrom, the other condition being satisfied when switch **S2** is activated thereby producing a logical **0** at the CP input of the second flip-flop. This sequence continues until all of the code digits have been correctly entered via the cipher lock switches. The unlocking cipher code, of course, can be changed to a different sequence of numbers by merely connecting leads **C1–C4** to different terminals **TS-1** through **TS-5.** For instance, a code of **2,4,3,1** requires that flip-flop leads **C1–C4** be connected to terminals **TS-2, TS-4, TS-3** and **TS-1,** respectively.

It should be noted that each of the flip-flops can be reset by applying a logical **0** or ground to the SD input. Such a signal would serve to make the $\overline{Q}$ output of the flip-flop a logical **0.** In order to make the cipher code more difficult to solve by trial and error, one or two of the switches **S1–S5** can be connected to leads N, both of which are connected to the reset or SD input of all flip-flops. Thus, whenever a switch connected to an N lead is activated, thereby grounding the N lead, all flip-flops will be reset and any accumulated correct entries will be cancelled.

In conventional cipher locks, the electrical output signal produced upon the correct entry of the cipher code is, in addition to serving a disarm function or some other function which the lock is intended to control, used to immediately reset the cipher lock circuitry so as to render it sensitive to the activation of the cipher lock switches. Such is not the case with the cipher lock of the invention. To the contrary, the output signal y of flip-flop **FF4** is used to render the cipher lock logic circuitry insensitive, at least to the first activation of any one switch or to the first simultaneous activation of any two or more switches immediately following the entry of the cipher lock code. Circuitry for rendering the flip-flops insensitive following the correct code entry is described below.

Output y which is produced from the $\overline{Q}$ output of flip-flop **FF4** after this code has been entered, serves as one

of the two inputs to a NAND gate 8C. Its other input is connected to a switch-activation-sensing circuit which provides a logical 1 at the output of inverter 3B when all switches are deactivated (as depicted in FIG. 2), and a logical 0 when one or more of the switches is activated. Such sensing circuitry comprises a series circuit through a pair of contacts on each switch to ground and the inverter 3B. While the switch which produces the last digit in the code is activated, or said otherwise, while the key which provides the last code digit is depressed, signal y becomes a logical 1 and, at the same time, the output of inverter 3B becomes a logical 0. Upon release or deactivation of the switch producing the last code digit, the output of inverter 3B becomes logical 1. Since the $\overline{Q}$ output of flip-flops FF4 remains unchanged, the output of NAND gate 8C becomes a logical 0. When the output of gate 8C is a logical 0, circuitry is activated for applying a logical 0 to both the K input of the first flip-flop FF1 and the SD or reset inputs of all flip-flops in the chain. Resetting all flip-flops makes all $\overline{Q}$ outputs logical 0. As a result, the chain of flip-flops becomes insensitive to the activation of any switch thereafter, thereby permitting any and all switches S1–S5 to be used for additional control functions. The manner in which switches S1–S5 are used to control other functions is described below.

Once reset has occurred following a correct code entry, code keys 2 and 4 may be used to arm the system for interior and/or perimeter protection modes. Depressing key 2 causes a logical 0 to appear at the input of an inverter 3A whose output is normally a logical 0. The resulting logical 1 at one of the inputs to gate 9B will produce a logical 0 at its output if its other input is at a logical 1; this can occur only if the switches, S_I, in all equipment connected in parallel to the interior loop terminals are all open indicating a fault-free situation. The logical 0 appearing at the output of NAND gate 9B causes a storage element comprised of cross-coupled NAND gates 7C and 7D to store the fact that an arming key was pushed and that the interior loop is free of faults. The logical 0 output of NAND gate 7D causes a logical 1 to appear at the output of gate 8A. This output is fed to one of the inputs of another NAND gate 5A, the output of which goes to a logical 0 after key 2 is released because its other input is a logical 1 when no keys are depressed. Note that depressing key 2 causes an arming signal to be stored in storage element 7C/7D if there is no fault present in the external interior loop circuitry. Upon release of key 2, arming information is transferred via gate 5A to a second storage element comprised of cross-coupled NAND gates 5B and 8B, the armed condition being a logical 1 at the output of gate 5B and a logical 0 at the output of gate 8B. This situation represents the satisfaction of three conditions: (a) an arming key has been depressed, (b) the external circuitry has no faults and (c) all keys have been released. The logical 1 stored at the output of gate 5B is connected to the K input of code flip-flop FF1, thereby enabling it to respond to a code input at its CP terminal and effectively converting the keyboard into a code key set.

A sequence similar to that which occurs when the interior loop is armed occurs when the perimeter loop is activated by key 4, the only difference being that a valid arming is accepted when exterior switches, S_P, are all closed rather than open. Note that gate 8A transfers an arming signal to storage element 5B/8B when perimeter and/or interior arming information is stored as a logical 0 at the output of gate 7A or 7D. Since it is the release of a key that transfers arming information through gate 5A, in order to obtain perimeter and interior arming simultaneously, both keys must be depressed before either one is released.

The logical 0 appearing at the output of gate 8B when the system is armed is connected to the junction of diodes D22 and D23 to make gates 9A and 9B unresponsive to key signals. After a successful code sequence is completed, the logical 1 at output y of FF4 resets storage element 5B/8B via gate 8C when the last code key is released. The logical 1 appearing at the output of gate 8B releases the inhibit on both arming channels at D22, D23 and, after passing through inverter 4B, resets all flip-flops in the code chain by applying a logical 0 to their SD inputs. The logical 0 at the output of gate 8C also resets both arming storage elements 7A/7B and 7C/7D via diode D28. Resistor R39 and capacitor C16 delay the reset signal from inverter 4B to permit the logical 1 at output y of FF4 to last long enough to effect the reset of storage element 5B/8B, thereby removing a potentially troublesome race condition.

Provision is made for the transmittal of an instant alarm when keys 1 and 5 are pressed simultaneously. When this occurs, terminal F on key switch 1 is connected to O volts. The logical 0 occurring as a result is transmitted directly to supplementary alarm circuits via diode D30. It also puts the system into an armed condition by forcing the output of storage element 5B to a logical 1, thereby enabling the code keys to permit turning off the system. Note that this occurs regardless of the perimeter or interior loop arming status.

It is seen that when armed, the system will respond to a code entry and ignore arming signals and when disarmed, the system will accept arming signals and ignore code inputs. Thus, a single set of key switches may be used to accomplish multiple functions.

Resistor R37 and capacitor C12 act to filter the output of inverter 3B so as to prevent multiple signals from occurring due to key switch contact bounce. Resistor-capacitor filters R1C1, R3C2, R10C3 and R11C4 remove electrical noise injected from external wiring which might cause false triggering of storage elements 7A–7D.

While the invention has been described with particular reference to a preferred embodiment, it is understood that various modifications can be effected without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. In an electronic cipher lock comprising a plurality of electrical switches and logic circuitry, operatively connected to such switches, for generating an electrical signal in response to the activation of two or more such switches according to a predetermined sequence which constitutes a code, the improvement comprising: circuit means, operatively connected to at least one of said electric switches and responsive to the generation of said electrical signal, for rendering said logic circuitry insensitive to the first activation of any said switches following the generation of said electrical signal, whereby any of said switches can serve a switching function in addition to that of code entry.

2. The invention of claim 1 wherein said circuit means comprises:

a. means for sensing the activation of any of said switches and for providing a voltage in response thereto; and

b. a logic gate having at least a pair of inputs, one of said inputs being connected to said sensing means for receiving said voltage, and the other of said inputs being connected to said logic circuitry for receiving said electrical signal, said logic gate being adapted to provide an output signal upon receipt of said voltage and said electrical signal at the inputs thereof for rendering said logic circuitry insensitive to the first activation of any said switches following the generation of said electrical signal.

3. An electronic cipher lock comprising:

a. at least two electrical switches, each having a switching member which is movable between first and second switching positions and means for biasing each of said members into said first position;

b. logic circuitry operatively connected to said switches for generating an electrical signal in response to the sequential movement of said switching members according to a predetermined order; said logic circuitry comprising a chain of at least two flip-flop circuits, each flip-flop circuit having at least two inputs and an output and being arranged such that one of said two inputs is operatively coupled to a unique one of said switches, and the other input in said chain is operatively connected to the output of flip-flop circuit which precedes it in said chain, each of said flip-flop circuits being capable of providing an output signal in response to the simultaneous occurrence of both an output signal from the flip-flop circuit preceding it in said chain and the movement of the switching member of the switch to which it is connected from said first switching position to said second switching position; and

c. circuit means, operatively coupling the output of the last flip-flop circuit in said chain with the other of said inputs of said first flip-flop circuit in said chain, for preventing said first flip-flop circuit from producing an output signal in response to the first movement of the switching member of the switch to which said first flip-flop circuit is connected from said first switching position to said second switching position, whereby any of said switches can be used to serve switching functions other than that required for producing said electrical signal.

4. The electronic cipher lock of claim **3** wherein said circuit means further comprises means for eliminating said preventing function after the switching member of at least one of said switches is moved from said first switching position to said second position and then back to said first switching position.

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