

June 4, 1946.

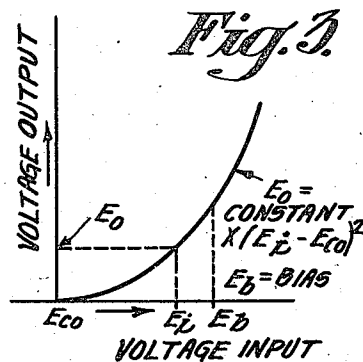
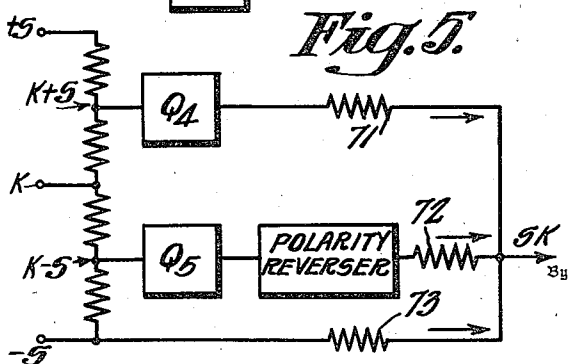
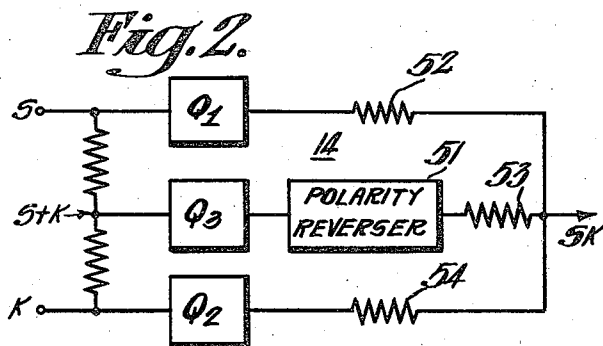
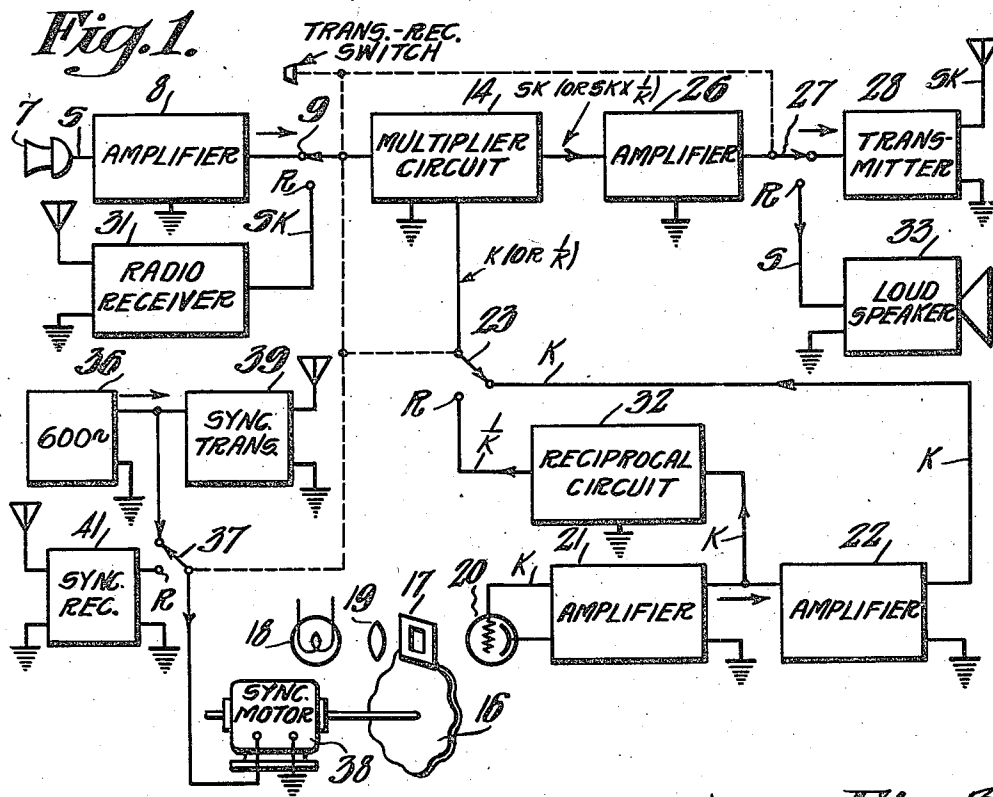
F. P. WIPFF

2,401,447

MULTIPLIER CIRCUIT

Filed April 23, 1943

2 Sheets-Sheet 1



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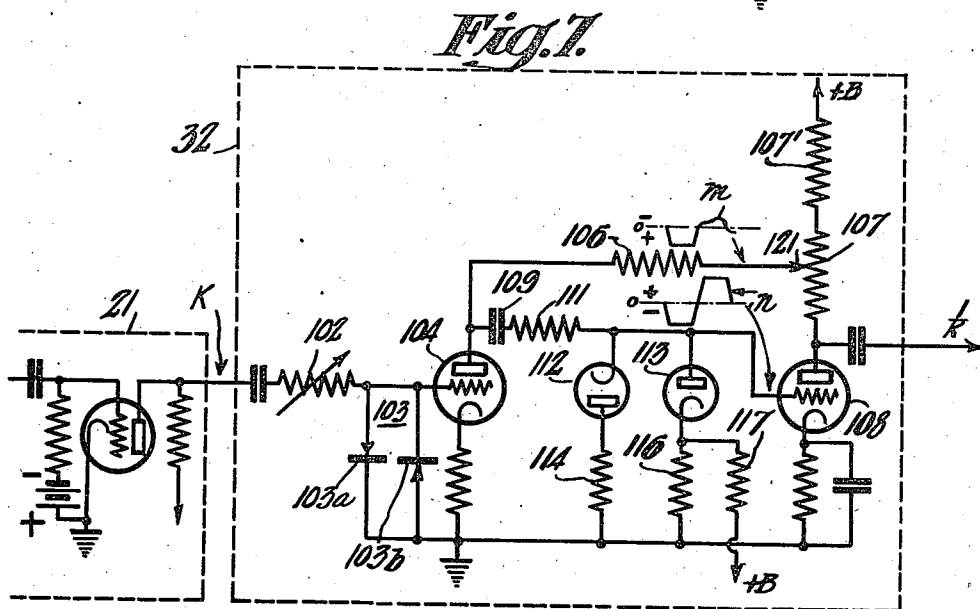
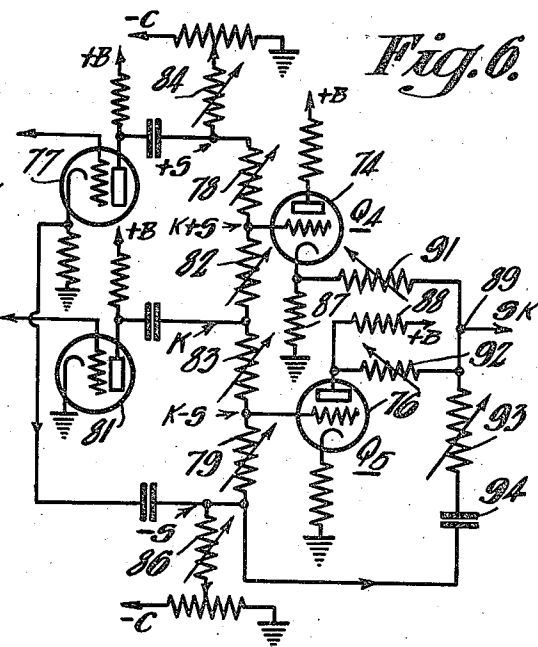
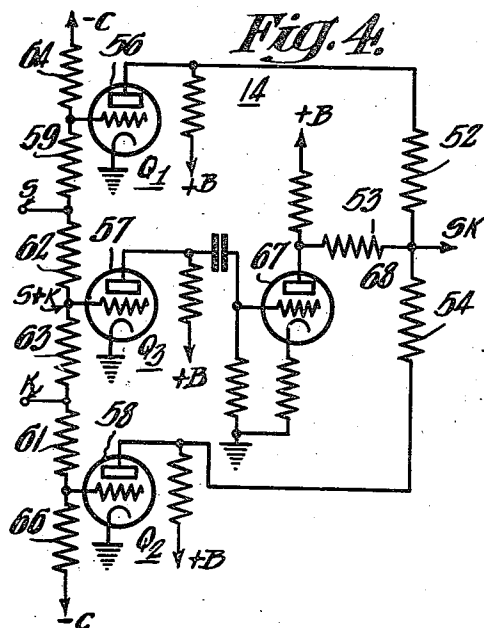
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MULTIPLIER CIRCUIT

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2 Sheets-Sheet 2



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UNITED STATES PATENT OFFICE

2,401,447

MULTIPLIER CIRCUIT

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Application April 23, 1943, Serial No. 484,303

11 Claims. (Cl. 179-1.5)

My invention relates to the multiplication of voltages and particularly to methods of and means for obtaining the product of two signals for use in a secret communication system.

In the copending application of Alda V. Bedford, Serial No. 456,578, filed August 29, 1942, and

entitled Secret communication system, there is described a communication system in which the speech or other communication signal S is multiplied by a coding signal K and in which the product SK is transmitted. At the receiver the incoming signal SK is multiplied by the reciprocal of the coding signal K to obtain the original signal S, that is $SK \times 1/K = S$. According to the above Bedford application the product SK is obtained by putting the positive cycles of either the signal S or the signal K on a carrier wave and then passing it through a modulator tube which has its bias varied by the positive cycles of the other signal. The same thing is done with the negative cycles of the signals after they have been reversed in polarity. The several product components are then added together with the correct polarity to obtain the product SK.

An object of the present invention is to provide an improved and simplified method of and means for multiplying a plurality of signal voltages by each other to obtain their product.

An additional object of the invention is to provide an improved circuit for obtaining the product of two electrical signals such as the above-mentioned signals S and K without having the signals S and K themselves appear in the output.

A further object of the invention is to provide an improved communication system for secret signalling.

In practicing the invention I utilize one of several known types of circuits that have the property of providing an instantaneous output voltage which is proportional to the square of the instantaneous input voltage for a reasonable voltage swing in a single polarity. Such circuits will be referred to as "squaring circuits" and will be designated "Q" where referred to in the description and drawings. In one embodiment of the invention the waves S and K to be multiplied are each separately squared in two squaring circuits Q₁ and Q₂. In a branch circuit the signals

S and K are added, then the sum S+K is squared in a third squaring circuit Q₃ and the squared signal is reversed in polarity. The three outputs of Q₁, Q₂ and Q₃ are then added to obtain the sum as shown in the following equations:

$$\begin{aligned} \text{Output of } Q_1 &= (S+A)^2 = S^2 + A^2 + 2SA \\ \text{Output of } Q_2 &= (K+A)^2 = K^2 + A^2 + 2KA \\ \text{Output of } Q_3 &= -(S+K+A)^2 = -S^2 - K^2 - A^2 - 2SK - 2KA - 2SA \end{aligned}$$

$$\text{Sum output} = A^2 - 2SK$$

The value "A" above is the D.-C. component or bias that is applied to the squaring circuits to cause the voltage swing always to be on the desired portion of the squaring circuit characteristic curve.

The invention will be better understood from the following description taken in connection with the accompanying drawings in which

Figure 1 is a block diagram of signalling apparatus embodying the invention,

Figure 2 is a block diagram of one multiplier circuit embodying the invention,

Figure 3 is a graph which is referred to in explaining the invention,

Figure 4 is a circuit diagram of the embodiment of the invention shown in Fig. 2,

Figures 5 and 6 are block and circuit diagrams, respectively, of another embodiment of the invention, and

Figure 7 is a circuit diagram of a reciprocal circuit that may be employed in the system of Fig. 1.

In the several figures, similar parts are indicated by similar reference characters.

Referring to Fig. 1, the invention is shown applied to radio apparatus that may be switched for operation either as a transmitter or as a receiver. The several switches are shown in the position for transmitter operation. This is the operation of the apparatus that will first be described. A microphone and a speech amplifier are shown at 7 and 8, respectively. The signals S is applied through a switch 9 to a multiplier unit 14 which preferably is designed in accordance with the present invention. The code signal K may be produced by means of a code disc 13, a mask 17, a light source 18, a condensing lens 19, and a photo-electric cell 20. The signal K is supplied through amplifiers 21 and 22 and through a switch to the multiplier unit 14. The resulting multiplier output signal SK is supplied through an amplifier 26 and through a switch 27 to a radio transmitter 28 or to a wire line, if preferred.

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The receiver for decoding the signal SK may be the same apparatus as in Fig. 1 with switches 9, 23 and 27 thrown to their contact positions R. The multiplier 14 is unchanged. The signal SK is supplied from a radio receiver 31 through the switch 9 to the multiplier 14. The coding signal K produced by the disc 16 is supplied through the amplifier 21 to a reciprocal circuit 32 which may be designed in accordance with the invention described and claimed in application Serial No. 484,304, filed on the same day as the present application in the name of Carl A. Meneley, and entitled Reciprocal circuits. The reciprocal circuit of this type is shown in Fig. 7. The reciprocal circuit 32 supplies the decoding signal $1/K$ through the switch 23 to the multiplier 14. The resulting output of multiplier 14 is the original communication signal S since $SK \times 1/K = S$. The signal S is amplified by the amplifier 26 and supplied through the switch 27 to headphones or to the loudspeaker 33.

The code disc 16 at the transmitter and the corresponding code disc at the receiver are held in synchronism and in the proper phase relation by suitable synchronizing means. For example, at the transmitter a 600-cycle per second current from a source 36 may be supplied through a switch 37 to a synchronous motor 38 which rotates the code disc 16. The 600-cycle current also modulates a radio transmitter 39 for the transmission of synchronizing signal to the receiver. At the receiver the switch 37 is in its contact position R whereby the received 600-cycle current is supplied from a radio receiver 41 to the synchronous motor 38. In some cases it may be preferable to transmit the synchronizing signal over a wire line.

One of my preferred designs for the multiplier circuit 14 is illustrated in Figs. 2 and 4. As previously stated, the invention makes use of devices having a square law characteristic when used in a suitable circuit. Most such devices have a characteristic of the type shown in Fig. 3, i. e., voltages more negative than E_{co} (cutoff) produce no output. Hence, they must be operated with a bias voltage E_b of such value that negative signal swings will remain on the characteristic. In Fig. 3, E_i and E_o are the corresponding abscissa and ordinate values, respectively, at any point on the square law curve. If a signal e_s is applied to the input of a "squaring circuit" Q_2 , the instantaneous input voltage will be equal to $E_b + e_s$. The instantaneous output voltage will be given by

$$e_o = C(E_b - E_{co} + e_s)^2 = C(A + e_s)^2$$

where

$A = E_b - E_{co}$ = the bias measured from cutoff.
 C = a constant.

If the signal voltage e_s consists of the sum of two voltage waves S and K as indicated in Fig. 2, the output voltage will be

$$\frac{e_o}{C} = (A + S + K)^2 = A^2 + S^2 + K^2 + 2AS + 2AK + 2SK$$

2SK is the desired term. The undesired terms are cancelled in the circuit of Fig. 2 by the use of two additional squaring devices Q_1 and Q_3 which square the waves $(A+S)$ and $(A+K)$, respectively. A polarity reverser 51 is inserted in the output of Q_3 so that cancellation, and not addition, will result. The various outputs which are supplied through resistors 52, 53 and 54 to a

common point are added with the proper polarity as indicated below:

$$\begin{aligned} \text{Output of } Q_3 &= -A^2 - S^2 - K^2 - 2AS - 2AK - 2SK \\ \text{Output of } Q_1 &= A^2 + S^2 + 2AS \\ \text{Output of } Q_2 &= A^2 + K^2 + 2AK \end{aligned}$$

$$\text{Sum output} = A^2 - 2SK$$

The term A^2 is direct current and is dropped in the first resistor-capacitor coupled stage following the multiplier.

Fig. 4 shows a circuit diagram corresponding to the block diagram of Fig. 2 in which vacuum tubes 56, 57 and 58 are utilized as the squaring circuits Q_1 , Q_3 and Q_2 , respectively. These tubes must have plate current vs. grid voltage characteristic that follows substantially a square law. Vacuum tubes of the types 6J5, 6SN7, 6C5, and other triodes have suitable characteristics. The plate resistors for such tubes should be kept small, not more than 1000 ohms.

The signals S and K are applied to the grids of tubes 56 and 58 through resistors 59 and 61, respectively. Both of the signals S and K are applied to the grid of tube 57 through resistors 62 and 63, respectively. A suitable negative bias is applied to the grids of the tubes 56, 57 and 58 through grid resistors 64 and 66. The resistors 59, 61, 62, 63, 64 and 66 all have the same comparatively high resistance, such as between 0.1 megohm and 1 megohm, so as not to load the comparatively low impedance driving source too much. However, the resistance is not made so high as to permit excessive phase shift due to grid-cathode capacity. Since the pairs of resistors 59-64, 62-63, and 61-66 act as voltage dividers for the applied signals, the voltages applied to the grids of tubes 56, 57 and 58 will be

$$\frac{S}{2}, \frac{S+K}{2} \text{ and } \frac{K}{2}$$

respectively.

The grid bias ($-C$) on tubes 56, 57 and 58 should be about to the middle of the straight portion of the grid voltage vs. mutual conductance curve. For a 6SN7 or 6J5 with 250 volts on the plate, this is about -14 volts.

A vacuum tube 67 serves to reverse the polarity of the output of tube 57 and should have approximately unity gain and very low distortion. The outputs of the tubes 56 and 58 and of the reversing tube 67 are added by supplying them to a common junction point 68 through the resistors 52, 53 and 54. These resistors may have a resistance of from 0.05 megohm to 0.1 megohm, for example. If everything is properly adjusted, only the desired product term $-2SK$ and the D.-C. component A^2 appear at the junction. In practice it is necessary to adjust the system carefully for minimum residual signal when either the signal S or the signal K is removed.

A somewhat simpler circuit requiring only two squaring devices Q_4 and Q_5 is shown in Fig. 5. To the unit Q_4 is applied the signal $K+S$; and to the other unit Q_5 is applied the signal $K-S$. After the output of the unit Q_5 has its polarity reversed, the two outputs are added through resistors 71 and 72 as shown below:

$$\begin{aligned} \text{Output of } Q_4 &= A^2 + K^2 + S^2 + 2AK + 2AS + 2SK \\ \text{Output of } Q_5 &= -A^2 - K^2 - S^2 - 2AK + 2AS + 2SK \end{aligned}$$

$$\text{Sum output} = 4AS + 4SK$$

In order to cancel the term $4AS$, an equal amount of signal $-4AS$ is added to the above sum output through a resistor 73.

The arrangement of Fig. 5 has the advantage

of providing a better ratio of signal SK to residual signal K, but has the disadvantage of having to feed signal S around the squaring devices. If the gain of the squaring devices changes, cancellation will be impaired.

Fig. 6 is a circuit diagram corresponding to the block diagram of Fig. 5 where a pair of vacuum tubes 74 and 76 are utilized as the squaring circuits Q_4 and Q_5 , respectively. The signal S may be taken off the anode and cathode circuits of an amplifier tube 77 and applied with opposite polarities to the grids of tubes 74 and 76 through resistors 78 and 79, respectively. The signal K may be taken off the anode circuit of an amplifier tube 81 and applied through resistors 82 and 83, respectively, to the grids of the tubes 74 and 76. Thus the signal $K+S$ is impressed upon the tube 74 while the signal $K-S$ is impressed upon the tube 76. A suitable negative bias is applied to the grids of the tubes 74 and 76 through grid leak resistors 84 and 86, respectively.

The outputs of tubes 74 and 76 are taken off their cathode resistor 87 and anode resistor 88, respectively, and applied to a common junction point 89 through resistors 91 and 92. The algebraic sum of the two outputs at the junction point 89 is $4AS+4SK$. The term $4AS$ is cancelled by applying a signal $-ZS$ through a blocking capacitor 93 and a resistor 94 to the junction point 89 and by making the constant Z equal to the constant $4A$. The signal $-ZS$ is given the desired value $-4AS$ by adjusting the resistor 93. Thus, the only term that will appear at the junction point 89 is the desired term $4SK$.

It should be noted that in the circuits of Figs. 4 and 6, the signals S and K will never appear in the output with the product signal SK if the circuits are properly balanced even though the signal K alone or the signal S alone is being applied to the multiplier. This is particularly important where the multiplier is being employed in a secret communication system.

Fig. 7 shows, by way of example, one circuit that may be employed to obtain the reciprocal wave $1/K$. This circuit is described and claimed in the above-mentioned Meneley application. The resistor 102 is of high enough resistance so that the driving source for the non-linear resistance unit 103 is of high impedance whereby there is only a slight variation in the current flow through unit 103. The unit 103 may consist of a pair of copper oxide rectifiers 103a and 103b connected to conduct current in opposite directions.

The voltage appearing across the non-linear unit 103 is the voltage m having a flattened wave form. This voltage is amplified by a cathode biased vacuum tube 104 and appears across an anode resistor 106 and a portion of the resistor 107-107' of a second amplifier tube 108.

The rectangular wave n is produced in this particular example by applying the output of the tube 104 through a blocking capacitor 109 and a high impedance resistor 111 to a pair of diodes 112 and 113 which are connected to conduct in opposite directions. Output resistors 114 and 116 of comparatively low resistance are connected in series with the diodes 112 and 113, respectively. A biasing voltage drop for opposing current flow through diode 113 is produced across the resistor 116 by connecting a source of voltage (not shown) thereacross, a resistor 117 being in series with the voltage source. The diodes 112 and 113 clip the applied wave m symmetrically about its A.-C. axis because a bias voltage which causes current

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flow through the diode 112 and resistor 114 is built up across the capacitor 109 by the positive cycle pulses flowing through the diode 113. Thus the diodes 112 and 113 become conducting on alternate cycles when the signal voltage exceeds the D.-C. voltage drop across the resistors 114 and 116, respectively. The resulting rectangular wave n is amplified and reversed in polarity by the tube 108. The wave n and the flattened wave m add in the portion of the anode resistor 107-107' that is common to the tubes 104 and 108 to produce the desired reciprocal wave $1/K$.

If the wave m is flattened correctly and if the waves m and n are added with the correct relative amplitudes, the resulting signal will be substantially a true reciprocal of the wave K. The waves m and n may be mixed with the correct relative amplitudes by adjusting a variable tap 121 on the anode resistor 107'. The correct shaping of the flattened wave m may be obtained by selecting a non-linear resistor unit 103 having a suitable voltage-resistance characteristic and by adjusting the value of the resistor 102.

Since the above-described reciprocal circuit is purely resistive whereby its operation is independent of frequency, if it is adjusted to produce the reciprocal of an applied wave having one wave form, it will then always produce the reciprocal of an applied wave regardless of its wave form.

I claim as my invention:

1. The method of obtaining the product of a plurality of voltages of varying amplitude which comprises the steps of adding said voltages, squaring the sum of said voltages whereby the desired product term is obtained and whereby undesired terms are obtained, and balancing out said undesired terms.

2. Apparatus for obtaining the product of a plurality of voltages of varying amplitude which comprises means for adding said voltages, means for squaring the sum of said voltages whereby the desired product term is obtained and whereby undesired terms are obtained, and means for balancing out said undesired terms.

3. Apparatus for obtaining the product of two voltages of varying amplitude which comprises means for adding said voltages, means for squaring the sum of said voltages whereby the desired product term is obtained and whereby undesired terms are obtained, and means including additional voltage squaring means for balancing out said undesired terms.

4. The method of obtaining the product of two electrical signals S and K of varying amplitude which comprises the steps of adding said signals together, squaring the sum $S+K$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, producing balancing out signals which are the same as said undesired terms, and adding the latter signals to said squared sum with a polarity opposite that of the squared sum whereby the undesired terms are cancelled.

5. A multiplier circuit for obtaining the product of two electrical signals S and K of varying amplitude which comprises means for squaring the sum $S+K$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, means for producing balancing out signals which are the same as said undesired terms, and means for adding the latter signals to said squared sum with a polarity opposite that of the squared sum whereby the undesired terms are cancelled.

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6. The method of obtaining the product of a plurality of voltages of varying amplitude which comprises the steps of squaring the sum of said voltages whereby the desired product term is obtained and whereby undesired terms are obtained, squaring said individual voltages and adding them to said squared sum with a polarity opposite to that of the squared sum whereby the undesired terms are cancelled.

7. The method of obtaining the product of two electrical signals S and K of varying amplitude which comprises the steps of squaring the sum $S+K$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, squaring said individual voltages S and K and adding them to said squared sum with a polarity opposite that of the squared sum whereby the undesired terms are cancelled.

8. A multiplier device for obtaining the product of two electrical signals S and K of varying amplitude which comprises means for squaring the sum $S+K$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, means for squaring said individual voltages S and K and means for adding them to said squared sum with a polarity opposite that of the squared sum whereby the undesired terms are cancelled.

9. The method of obtaining the product of a plurality of electrical voltages of varying amplitude which comprises the steps of squaring the

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sum of said voltages whereby the desired product term is obtained and whereby undesired terms are obtained, squaring the difference of said voltages, adding said squared sum and said squared difference after one of them has been reversed in polarity, and also adding with negative polarity the voltage that was subtracted to obtain said difference voltage.

10. The method of obtaining the product of two electrical signals S and K of varying amplitude which comprises the steps of squaring the sum $K+S$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, squaring the difference value $K-S$, adding said squared sum and said squared difference after one of them has been reversed in polarity to cancel certain of said undesired terms, and also adding the signal $-S$ to cancel the remaining undesired term.

11. A multiplier device for obtaining the product of two electrical signals S and K of varying amplitude which comprises means for squaring the sum $K+S$ whereby the desired product term SK is obtained and whereby undesired terms are obtained, means for squaring the difference value $K-S$, means for adding said squared sum and said squared difference after one of them has been reversed in polarity to cancel certain of said undesired terms, and means for also adding the signal $-S$ to cancel the remaining undesired term.

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