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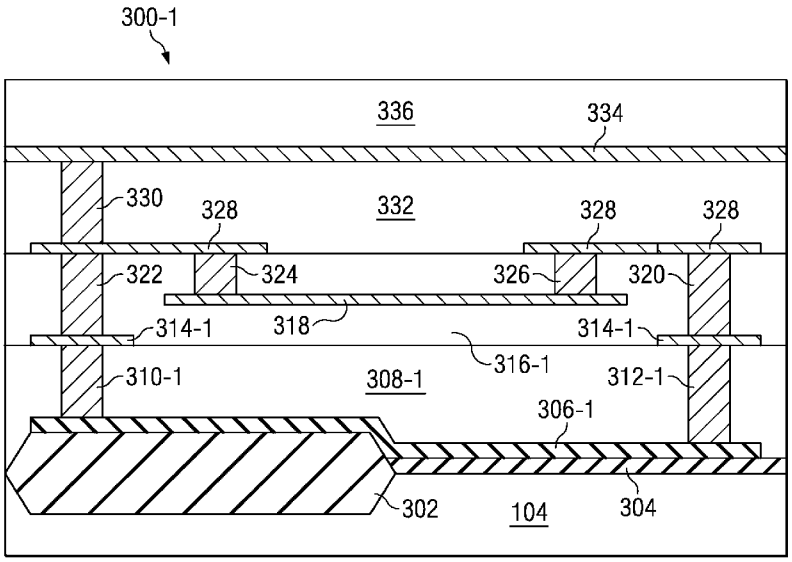

FIG. 10B

(57) Abstract: "On-chip" or monolithically integrated thermocouples are provided that employ different thicknesses of thermal insulators to create thermal differentials within an integrated circuit. Heat applied to a metallization layer (334) is transferred through other metallization layers (328, 314- 1) and vias (330, 322, 310-1) to a conductive layer (306-1) having portions overlying a thick dielectric layer (field oxide layer 302) and a more thermally conductive thin oxide layer (304), forming a "hot" junction between a via (310-1) and the conductive layer (306-1), and a "cold" junction between the conductive layer (306-1) and another via (312-1), to generate a voltage.

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SEMICONDUCTOR THERMOCOUPLE AND SENSOR

[0001] This relates generally to thermocouples and, more particularly, to monolithically integrated thermopiles.

BACKGROUND

[0002] Referring to FIG. 1 of the drawings, the reference numeral 100 generally designates a conventional monolithically integrated or "on-chip" thermocouple. Thermocouple 100 generally comprises a membrane 102 that includes two different thermally conductive materials 110 and 112 that extend from the silicon substrate 104 (which is typically referred to as a "rim") over a recess 108 formed in silicon substrate 104. As heat or infrared radiation is applied to the membrane 102, a temperature differential is created in the membrane 102 between the area over the recess 108 and the "rim" (where the substrate 104 operates as a heat sink). Many of the thermocouples 100 can then be arranged into a thermopile so as to be able to ascertain readable and reliable temperature measurements.

[0003] Thermocouple 100, however, has numerous drawbacks. First, the deep selective etching used to form recess 108 is a non-standard manufacturing step, which can dramatically increase the manufacturing costs. Second, the membrane 102 is very fragile, which generally requires special handling and packaging and which generally makes the membrane sensitive to pressure and vibration. Additionally, because of the fragility of the membrane 102, the size of the membrane is mechanically limited.

[0004] Turning to FIG. 2, another, alternative thermopile 200 can be seen. Thermopile 200 generally comprises a first set of materials 202-1, 202-2, 202-3, and 202-4 and a second set of materials 204-1, 204-2, 204-3, and 204-4 arranged in a "serpentine" on a silicon substrate 104. As air (or another fluid) traverses the thermopile, a temperature or thermal gradient is formed across the thermopile 200. While the arrangement of thermopile 200 is more mechanically

durable than a thermopile having an array of thermocouples 100, thermopile 200 has very low sensitivity and generally requires a large amount of area, making it prohibitively expensive.

[0005] Some other examples of conventional thermocouples and thermopiles are described in: U.S. Patent No. 3,393,328; U.S. Patent No. 5,059,543; U.S. Patent No. 5,343,064; U.S. Patent No. 6,531,899; U.S. Patent No. 6,565,254; U.S. Patent No. 6,793,389; U.S. Patent No. 6,987,223; U.S. Patent No. 7,042,690; U.S. Patent No. 7,282,712; U.S. Patent No. 7,406,185; U.S. Patent Pre-Grant Publ. No. 2009/0260669; Paul et al., "Thermoelectric Infrared Imaging Microsystem by Commercial CMOS Technology," Proc. Eur. Solid-State Device Conf., Bordeaux, France, Sept. 8–10, 1998, pp. 52–55; and Lahiji et al., "A Batch-Fabricated Silicon Thermopile Infrared Detector," IEEE Transactions on Electron Devices, Vol. 29, No. 1, Jan. 1982 pp. 14-22.

SUMMARY

[0006] An example embodiment of the invention, accordingly, provides an apparatus is provided. The apparatus comprises a substrate; a thin dielectric layer formed over a first portion of the substrate; a thick dielectric layer formed over a second portion of the substrate; a first conductive layer that extends over at least a portion of each of the thin dielectric layer and the thick dielectric layer, wherein the first conductive layer is made of a first material having a first Seebeck coefficient; a first portion of a second conductive layer that extends over at least a portion of the first conductive layer and the thin dielectric layer, wherein the second layer is made of a second material having a second Seebeck coefficient; a second portion of the second conductive layer that extends over at least a portion of the first conductive layer and the thick dielectric layer; a first conductive via that is formed between the first conductive layer and the first portion of second conductive layers; and a second conductive via that is formed between the first conductive layer and the second portion of the second conductive layer.

[0007] In accordance with an example embodiment of the invention, the first conductive layer is formed of polysilicon, and wherein the thin and thick dielectric layers are formed of silicon dioxide, and wherein the second conductive layer is a metallization layer formed of aluminum or copper, and wherein the first and second conductive vias are formed of tungsten or aluminum, and wherein the thin dielectric layer is between about 10nm and about 12nm.

[0008] In accordance with an example embodiment of the invention, the thick dielectric layer is a field oxide layer that is between 200nm and about 220nm.

[0009] In accordance with an example embodiment of the invention, the apparatus further comprises: a third conductive layer that extends over at least a portion of each of the first and second portions of the second conductive layer; a third conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the first conductive via; a fourth conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the second conductive via; an interconnect layer, wherein the interconnect layer has a higher thermal impedance than the third conductive layer; a fifth conductive via that is formed between the third conductive layer and interconnect layer; and a fourth conductive layer that is adapted to receive infrared radiation; a sixth conductive via that is formed between third conductive layer and the fourth conductive layer, wherein the sixth conductive via is generally coextensive with the second via.

[0010] In accordance with an example embodiment of the invention, the third and fourth conductive layers is each formed of aluminum or copper, and wherein the third, fourth, fifth, and sixth conductive vias are formed of aluminum or tungsten, and wherein the interconnect layer is formed of titanium nitride.

[0011] In accordance with an example embodiment of the invention, the thick dielectric layer is an isolation region that is between about 200nm and about 220nm.

[0012] In accordance with an example embodiment of the invention, the apparatus further comprises an absorption layer that extends over the second portion of the second conductive layer.

[0013] In accordance with an example embodiment of the invention, the apparatus further comprises a buried layer formed in the substrate below the first portion of the second conductive layer.

[0014] In accordance with an example embodiment of the invention, the absorption layer is formed of polyamide.

[0015] In accordance with an example embodiment of the invention, the first conductive layer is formed of polysilicon doped with a material of a first conduction type, and wherein the

thin and thick dielectric layers are formed of silicon dioxide, and wherein the second conductive layer is formed of polysilicon doped with a material of a second conduction type.

[0016] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a plurality of thermocouples that are coupled to one another in an array to form a thermopile, wherein each thermocouple includes: a thin dielectric layer; a thick dielectric layer; a first conductive layer that extends over at least a portion of each of the thin dielectric layer and the thick dielectric layer, wherein the first conductive layer is made of a first material having a first Seebeck coefficient; a first portion of a second conductive layer that extends over at least a portion of the first conductive layer and the thin dielectric layer, wherein the second layer is made of a second material having a second Seebeck coefficient; a second portion of the second conductive layer that extends over at least a portion of the first conductive layer and the thick dielectric layer; a first conductive via that is formed between the first conductive layer and the first portion of second conductive layers; and a second conductive via that is formed between the first conductive layer and the second portion of the second conductive layer.

[0017] In accordance with an example embodiment of the invention, each thermocouple further comprises: a third conductive layer that extends over at least a portion of each of the first and second portions of the second conductive layer; a third conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the first conductive via; a fourth conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the second conductive via; an interconnect layer, wherein the interconnect layer has a higher thermal impedance than the third conductive layer; a fifth conductive via that is formed between the third conductive layer and interconnect layer; a fourth conductive layer that is adapted to receive infrared radiation; a sixth conductive via that is formed between third conductive layer and the fourth conductive layer, wherein the sixth conductive via is generally coextensive with the second via; and a seventh conductive via that is formed between the second conductive layer and the third conductive layer, wherein the seventh conductive via is generally coextensive with the first conductive via so that the first portion of the second conductive layer is electrically connected to an adjacent thermocouple.

[0018] In accordance with an example embodiment of the invention, each thermocouple further comprises: an absorption layer that extends over the second portion of the second conductive layer; and a buried layer formed in the substrate below the first portion of the second conductive layer.

[0019] In accordance with an example embodiment of the invention, the apparatus further comprises: an amplifier that is coupled to the thermopile; an analog-to-digital converter (ADC) that is coupled to the amplifier; a digital linearization engine that is coupled to the ADC; and an interface that is coupled to the digital linearization engine.

[0020] In accordance with an example embodiment of the invention, the ADC is a sigma-delta ADC.

[0021] In accordance with an example embodiment of the invention, the interface is an SMBus compatible interface.

[0022] In accordance with an example embodiment of the invention, a method of manufacturing a thermocouple is provided. The method comprises forming a thick dielectric layer and a thin dielectric layer over a substrate; forming a first conductive layer that extends over at least a portion of each of the thick and thin dielectric layers, wherein the first conductive layer has a first Seebeck coefficient; forming an oxide layer over the first conductive layer; etching the oxide layer to form a first aperture that is generally coextensive with at least a portion of the first conductive layer and the thin dielectric layer and to form a second aperture that is generally coextensive with at least a portion of the first conductive layer and the thick dielectric layer; filling the first and second apertures to form first and second conductive vias; forming a second conductive layer over the oxide layer, wherein the second conductive layer has a second Seebeck coefficient; and etching the second conductive layer to form first and second portions of the second conductive layer that are substantially electrically isolated from one another.

[0023] In accordance with an example embodiment of the invention, the metallization layer further comprises a first metallization layer, and wherein the oxide layer further comprises a first oxide layer, and wherein the method further comprises: forming a second oxide layer over the first metallization layer; forming an interconnect layer over the second oxide layer; forming a third oxide layer over the interconnect layer; etching the second and third oxide layers to form: a third aperture that is generally coextensive with the first conductive via; a fourth aperture that is generally coextensive with the second conductive via; a fifth aperture that is generally

coextensive with at least a portion of the interconnect layer; and a sixth aperture that is generally coextensive with at least a portion of the interconnect layer; filling the third, fourth, fifth, and sixth apertures to form third, fourth, fifth, and sixth conductive vias; forming a second metallization layer over the third oxide layer; and etching the second metallization layer so that fourth and fifth conductive vias are electrically connected, that the third conductive via is electrically connected to a first adjacent thermocouple, and that the sixth conductive via is electrically connected to a second adjacent thermocouple.

[0024] In accordance with an example embodiment of the invention, the oxide layer further comprises a first oxide layer, and wherein the first and second portions of the metallization layer are electrically connected to first and second adjacent thermocouples, and wherein the method further comprises: forming a buried layer in the substrate underneath the first conductive via; forming a second oxide layer over the metallization layer; and forming an absorption layer over the second via.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Example embodiments are described with reference to accompanying drawings, wherein:

[0026] FIG. 1 is an example of a conventional thermocouple;

[0027] FIG. 2 is an example of a conventional thermopile;

[0028] FIG. 3A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0029] FIG. 3B is a elevation view of the process step along section line A-A;

[0030] FIG. 4A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0031] FIG. 4B is a elevation view of the process step along section line B-B;

[0032] FIG. 5A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0033] FIG. 5B is a elevation view of the process step along section line C-C;

[0034] FIG. 6A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0035] FIG. 6B is a elevation view of the process step along section line D-D;

[0036] FIG. 7A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0037] FIG. 7B is a elevation view of the process step along section line E-E;

[0038] FIG. 8A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0039] FIG. 8B is a elevation view of the process step along section line F-F;

[0040] FIG. 9A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0041] FIG. 9B is a elevation view of the process step along section line G-G;

[0042] FIG. 10A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0043] FIG. 10B is a elevation view of the process step along section line H-H;

[0044] FIG. 11A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0045] FIG. 11B is a elevation view of the process step along section line I-I;

[0046] FIG. 12A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0047] FIG. 12B is a elevation view of the process step along section line J-J;

[0048] FIG. 13A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0049] FIG. 13B is a elevation view of the process step along section line K-K;

[0050] FIG. 14A is a plan view of an example of a process step for forming a thermocouple in accordance with an example embodiment of the invention;

[0051] FIG. 14B is a elevation view of the process step along section line L-L;

[0052] FIG. 15 is an example of an integrate circuit (IC) that employs the thermocouples show in process steps of FIGS. 3A to 14B.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0053] In FIGS. 3A to 10B, the process for forming a thermocouple 300-1 (as shown in FIG. 10B) is illustrated. Initially, as can be seen in FIGS. 3A and 3B, a thin dielectric layer 304 and a thick dielectric layer or field oxide layer 302 are formed over the substrate 104. Typically, these layers 302 and 304 are formed of silicon dioxide and are grown on the substrate 104

through one or more conventional oxidation process steps. The thin oxide layer 304 can be between about 10nm and about 12nm thick, while the field oxide layer 302 can be between about 200nm and about 220nm thick. Additionally, substrate 104 can be formed of silicon, but substrate 104 may also be made of several other suitable materials.

[0054] Following the formation of the dielectric layers 302 and 304, a conductive layer 306-1 is formed over dielectric layers 302, as seen in FIGS. 4A and 4B. Typically, this conductive layer 306-1 is formed of polysilicon, which has a Seebeck coefficient of about 40μV/K and which is one of the thermally conductive materials used to form the thermocouple 300-1. In the formation of conductive layer 306-1, a layer of polysilicon is generally formed over layers 302 and 304, which is then patterned an etched to form the shape seen in the plan view of FIG. 4A. The conductive layer 306-1 can also be doped with either a P-type material (such as boron, indium, or aluminum) or N-type material (such as phosphorous, arsenic, and antimony).

[0055] Turning to FIGS. 5A and 5B, conductive contacts are formed with the conductive layer 306-1. To accomplish this, a dielectric layer (typically silicon dioxide) 308-1 is formed over the conductive layer 306-1 and is patterned and etched (forming apertures that are each generally or partially coextensive with the conductive layer 306-1 and one of the layers 304 or 302. These apertures are then filled with a conductive material (i.e., tungsten or aluminum) to form vias 310-1 and 312-1.

[0056] With vias 310-1 and 312-1 in place, a conductive layer or metallization layer 314-1 (as shown in FIGS. 6A and 6B) is formed over the dielectric layer 308-1. Typically, the metallization layer 314-1 is formed of a material having a similar or approximately the same Seebeck coefficient as the conductive material used for vias 310-1 and 312-1. For example, if tungsten or aluminum (which, respectively, have Seebeck coefficients of 7.5μV/K and 3.5μV/K), aluminum or copper (6.5μV/K) would have similar or approximately Seebeck coefficients. This metallization layer 314-1 (once in place) can be patterned and etched to form two separate portions or "pads" that are electrically isolated from one another. Additionally, each of these "pads" is in electrical contact with one of the vias 310-1 and 312-1. Alternatively, conductive layer 314-1 can also be formed of polysilicon doped with either a P-type material (such as boron, indium, or aluminum) or N-type material (such as phosphorous, arsenic, and antimony).

Typically, when conductive layer 314-1 is formed of doped polysilicon, conductive layer 306-1 has the opposite doping of conductive layer 314-1.

[0057] Tuning to FIGS. 7A and 7B, additional connective layers are formed. A dielectric layer (i.e., portion of dielectric layer 316-1) is first formed over the metallization layer 314-1 (and the dielectric layer 308-1), and an interconnect layer is formed (i.e., deposited and etched). Then, the remainder of the dielectric layer 316-1 is formed. As with the previous dielectric layer 308-1, apertures are formed and filled with a conductive material (i.e., aluminum or tungsten) to form vias 320, 322, 324, and 326. Typically, the interconnect layer 318 (which operates as a connective layer between adjacent thermocouples, such as thermocouple 300-1) is formed of a material that has good electrical conductivity, with a higher thermal impedance than the materials used for metallization layers 314-1 and 328. For example, interconnect layer 318 can be formed of titanium nitride. By using such a material, "hot" junctions of one thermocouple 300-1 can be thermally isolated from "cold" junctions in an adjacent thermocouple (i.e., thermocouple 300-1).

[0058] Following the formation of vias 320, 322, 324, and 326, a second metallization layer 328 (as shown in FIGS. 8A and 8B) is deposited, patterned, and etched. As with the first metallization layer 314-1, there are several portions or "pads" in metallization layer 328 that are generally electrically isolated from one another. In particular, metallization layer 328 electrically connects vias 322 and 324 together, electrically connects via 326 to one adjacent cell or thermocouple (i.e., thermocouple 300-1), and electrically connects via 320 to another adjacent cell or thermocouple (i.e., thermocouple 300-1). Additionally, as shown in FIG. 8B, vias 322 and 320 can be generally coextensive or can be generally aligned with vias 310-1 and 312-1, respectively.

[0059] Once the metallization layer 328 is formed, an additional via 330 and third metallization layer 334 are formed (which is shown in FIGS. 9A through 10B). As with the other vias 310-1, 312-1, 320, 322, 324, 326, via 330 is formed of a conductive material (i.e., tungsten or aluminum) that is deposited in an aperture in dielectric layer 332 (i.e., silicon dioxide). The third metallization layer 334 is then formed over the cell so as to conduct heat to the "hot junction." Additionally, an absorber 336 can be formed over the metallization layer 334; typically, this absorber 336 can be formed of polyamide or any other suitable infrared or heat absorber.

[0060] In operation, cell or thermocouple 300-1 is able to use the Peltier-Seebeck effect to generate a voltage. Heat or infrared radiation is applied to the metallization layer 334, which is transferred through metallization layers 328 and 314-1 and vias 330, 322, and 310-1 to conductive layer 306-1. Since the thick dielectric layer 302 (which is a field oxide layer) is a less thermally conductive than thin oxide layer 304 due to their relative thicknesses, a "hot" junction is formed at junction between via 310-1 and conductive layer 306-1, and a "cold" junction is formed at the junction between the conductive layer 306-1 and via 312-1. Thus, because of the dissimilar materials of the conductive layer 306-1 and metallization or conductive layers 314-1 and 328, a voltage is generated when infrared radiation or heat is applied to metallization or conductive layer 334.

[0061] As an alternative or additional feature, polymers and/or buried layers can be used for infrared absorption. Turning to FIGS. 11A to 13B, a structure that is similar to the structure of FIGS. 6A and 6B is formed. Some differences are: (1) that dielectric layer 302 is replaced with an isolation region 402 (i.e., shallow trench isolation or deep trench isolation) with oxide layer 406 extending over the isolation region 402; (2) that a buried layer 404 (which is generally comprised of an implanted or diffused dopant and is generally coextensive with or generally aligned with via 312-2) is provided in the substrate 104; and (3) that the "pads" or portions of metallization layer 314-2 are electrically connected to adjacent cells. Additionally, as shown in FIGS. 14A and 14B, an absorption layer 408 (which is generally formed of polyamide) is formed on the dielectric layer 316-2 so as to be generally coextensive with via 310-2. Typically, the buried layer is heavily doped with either a P-type material (such as boron, indium, or aluminum) or N-type material (such as phosphorous, arsenic, and antimony).

[0062] As a result of the configuration of cell or thermocouple 300-2 allows for absorption from both the top and bottom. Both the buried layer 404 and the absorption layer 408 operate to "trap" infrared radiation. Regardless of the direction of the radiation, heat is trapped on the "hot" junction (junction between via 310-2 and conductive layer 603-2) and is dissipated into the substrate 104 on the "cold" junction (junction between via 312-2 and conductive layer 306-2). Therefore, similar to thermocouple 300-1, thermocouple 300-2 generates a voltage when infrared radiation is received.

[0063] Turning to FIG. 15, an example of an application of thermocouples 300-1 and/or 300-2 can be seen. Generally, thermocouples 300-1 and/or 300-2 are formed as part of an

integrated circuit (IC). Cells or thermocouples 300-1 and/300-2 (which are each about 7.5μm^2) are arranged in an array to form thermopile 502. Typically, thermopile 502 includes tens of thousands of cells or thermocouples 300-1 and 300-2. The thermopile 502 is coupled to an amplifier 504, and an amplified signal is provided to analog-to-digital converter (ADC) 506. Typically, ADC 506 is a sigma-delta ADC that receives a local temperature LT from temperature sensor 508 and a reference voltage REF from reference voltage generator 510. The digital representation of the amplified signal is linearized by the digital linearization engine 512 and provided to interface 514 (which is generally SMBus compatible).

[0064] As a result of using cells or thermocouples 300-1 and/or 300-2, several advantages can be realized over conventional thermocouples. Thermocouples 300-1 and/or 300-2 are fully compatible with the standard semiconductor manufacturing processes. There are no extra processing steps, and the cost per wafer is equal to the base cost per wafer for the used process. There are no restrictions on the thermopile 502 size. The desired sensitivity and signal to noise ratio can be achieved by scaling up the thermopile 502. Thermocouples 300-1 and/or 300-2 have mechanical robustness that is generally equal to the robustness of the silicon chip itself. Thermocouples 300-1 and/or 300-2 are also not sensitive to pressure and/or vibrations or to chemical and/or ion contamination.

[0065] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a substrate;

a thin dielectric layer formed over a first portion of the substrate;

a thick dielectric layer formed over a second portion of the substrate;

a first conductive layer that extends over at least a portion of each of the thin dielectric layer and the thick dielectric layer, wherein the first conductive layer is made of a first material having a first Seebeck coefficient;

a first portion of a second conductive layer that extends over at least a portion of the first conductive layer and the thin dielectric layer, wherein the second layer is made of a second material having a second Seebeck coefficient;

a second portion of the second conductive layer that extends over at least a portion of the first conductive layer and the thick dielectric layer;

a first conductive via that is formed between the first conductive layer and the first portion of second conductive layers; and

a second conductive via that is formed between the first conductive layer and the second portion of the second conductive layer.

2. The apparatus of Claim 1, wherein the first conductive layer is formed of polysilicon, and wherein the thin and thick dielectric layers are formed of silicon dioxide, and wherein the second conductive layer is a metallization layer formed of aluminum or copper, and wherein the first and second conductive vias are formed of tungsten or aluminum, and wherein the thin dielectric layer is between about 10nm and about 12nm.

3. The apparatus of Claim 2, wherein the thick dielectric layer is a field oxide layer that is between about 200nm and about 220nm.

4. The apparatus of Claim 3, wherein the apparatus further comprises:

a third conductive layer that extends over at least a portion of each of the first and second portions of the second conductive layer;

a third conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the first conductive via;

a fourth conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the second conductive via;

an interconnect layer, wherein the interconnect layer has a higher thermal impedance than the third conductive layer;

a fifth conductive via that is formed between the third conductive layer and interconnect layer;

a fourth conductive layer that is adapted to receive infrared radiation; and

a sixth conductive via that is formed between third conductive layer and the fourth conductive layer, wherein the sixth conductive via is generally coextensive with the second via.

5. The apparatus of Claim 1, wherein the apparatus further comprises an absorption layer comprising polyamide that extends over the second portion of the second conductive layer.

6. An apparatus comprising a plurality of thermocouples that are coupled to one another in an array to form a thermopile, wherein each thermocouple includes:

a thin dielectric layer;

a thick dielectric layer;

a first conductive layer that extends over at least a portion of each of the thin dielectric layer and the thick dielectric layer, wherein the first conductive layer is made of a first material having a first Seebeck coefficient;

a first portion of a second conductive layer that extends over at least a portion of the first conductive layer and the thin dielectric layer, wherein the second layer is made of a second material having a second Seebeck coefficient;

a second portion of the second conductive layer that extends over at least a portion of the first conductive layer and the thick dielectric layer;

a first conductive via that is formed between the first conductive layer and the first portion of second conductive layers; and

a second conductive via that is formed between the first conductive layer and the second portion of the second conductive layer.

7. The apparatus of Claim 6, wherein the first conductive layer is formed of polysilicon, and wherein the second conductive layer is a metallization layer formed of aluminum or copper, and wherein the first and second conductive vias are formed of tungsten or aluminum, and wherein the thin dielectric layer is between about 10nm and about 12nm, and wherein the thin and thick dielectric layers are formed of silicon dioxide.

8. The apparatus of Claim 7, wherein each thermocouple further comprises:

a third conductive layer that extends over at least a portion of each of the first and second portions of the second conductive layer;

a third conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the first conductive via;

a fourth conductive via that is formed between the second and third conductive layer, wherein the third conductive via is generally coextensive with the second conductive via;

an interconnect layer, wherein the interconnect layer has a higher thermal impedance than the third conductive layer;

a fifth conductive via that is formed between the third conductive layer and interconnect layer;

a fourth conductive layer that is adapted to receive infrared radiation;

a sixth conductive via that is formed between third conductive layer and the fourth conductive layer, wherein the sixth conductive via is generally coextensive with the second via; and

a seventh conductive via that is formed between the second conductive layer and the third conductive layer, wherein the seventh conductive via is generally coextensive with the first conductive via so that the first portion of the second conductive layer is electrically connected to an adjacent thermocouple.

9. The apparatus of Claim 8, wherein the third and fourth conductive layers is each formed of aluminum or copper, and wherein the third, fourth, fifth, sixth, and seventh conductive vias are formed of aluminum or tungsten, and wherein the interconnect layer is formed of titanium nitride.

10. The apparatus of Claim 6, wherein the apparatus further comprises:

an amplifier that is coupled to the thermopile;

an analog-to-digital converter (ADC) that is coupled to the amplifier;

a digital linearization engine that is coupled to the ADC; and

an interface that is coupled to the digital linearization engine.

11. A method of manufacturing a thermocouple comprising:

forming a thick dielectric layer and a thin dielectric layer over a substrate;

forming a first conductive layer that extends over at least a portion of each of the thick and thin dielectric layers, wherein the first conductive layer has a first Seebeck coefficient;

forming an oxide layer over the first conductive layer;

etching the oxide layer to form a first aperture that is generally coextensive with at least a portion of the first conductive layer and the thin dielectric layer and to form a second aperture that is generally coextensive with at least a portion of the first conductive layer and the thick dielectric layer;

filling the first and second apertures to form first and second conductive vias;

forming a second conductive layer over the oxide layer, wherein the second conductive layer has a second Seebeck coefficient; and

etching the second conductive layer to form first and second portions of the second conductive layer that are substantially electrically isolated from one another.

12. The method of Claim 11, wherein the first conductive layer is formed of polysilicon, and wherein the thin and thick dielectric layers are formed of silicon dioxide, and wherein the second conductive layer is a metallization layer is formed of aluminum or copper, and wherein the first and second conductive vias are formed of tungsten or aluminum, and wherein the thin dielectric layer is between about 10nm and about 12nm.

13. The method of Claim 12, wherein the thick dielectric is a field oxide layer that is between about 200nm and about 220nm.

14. The method of Claim 11, wherein the metallization layer further comprises a first metallization layer, and wherein the oxide layer further comprises a first oxide layer, and wherein the method further comprises:

forming a second oxide layer over the first metallization layer;

forming an interconnect layer over the second oxide layer;

forming a third oxide layer over the interconnect layer;

etching the second and third oxide layers to form:

a third aperture that is generally coextensive with the first conductive via;

a fourth aperture that is generally coextensive with the second conductive via;

a fifth aperture that is generally coextensive with at least a portion of the interconnect layer; and

a sixth aperture that is generally coextensive with at least a portion of the interconnect layer;

filling the third, fourth, fifth, and sixth apertures to form third, fourth, fifth, and sixth conductive vias;

forming a second metallization layer over the third oxide layer; and

etching the second metallization layer so that fourth and fifth conductive vias are electrically connected, that the third conductive via is electrically connected to a first adjacent thermocouple, and that the sixth conductive via is electrically connected to a second adjacent thermocouple.

15. The method of Claim 14, wherein the second metallization layer is formed of aluminum or copper, and wherein the third, fourth, fifth, and sixth conductive vias are formed of aluminum or tungsten, and wherein the interconnect layer is formed of titanium nitride.

16. The method of Claim 11, wherein the thick dielectric layer is an isolation region that is between about 200nm and about 220nm; wherein the oxide layer further comprises a first

oxide layer, and wherein the first and second portions of the metallization layer are electrically connected to first and second adjacent thermocouples, and wherein the method further comprises:

forming a buried layer in the substrate underneath the first conductive via;

forming a second oxide layer over the metallization layer; and

forming an absorption layer over the second via.

17. The method of Claim 16, wherein the absorption layer is formed of polyamide.

18. The apparatus of Claim 17, wherein the first conductive layer is formed of polysilicon doped with a material of a first conduction type, and wherein the second conductive layer is formed of polysilicon doped with a material of a second conduction type.

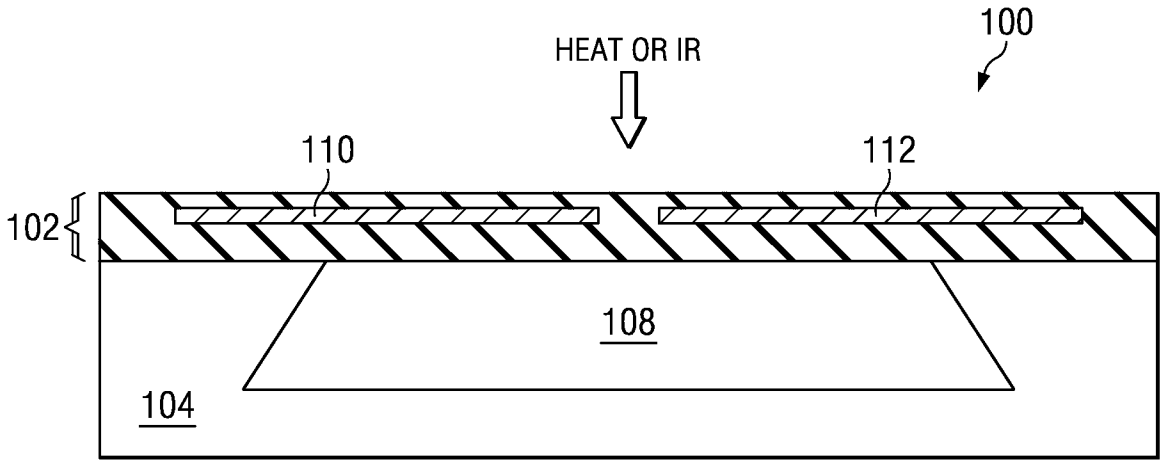

FIG. 1
(PRIOR ART)

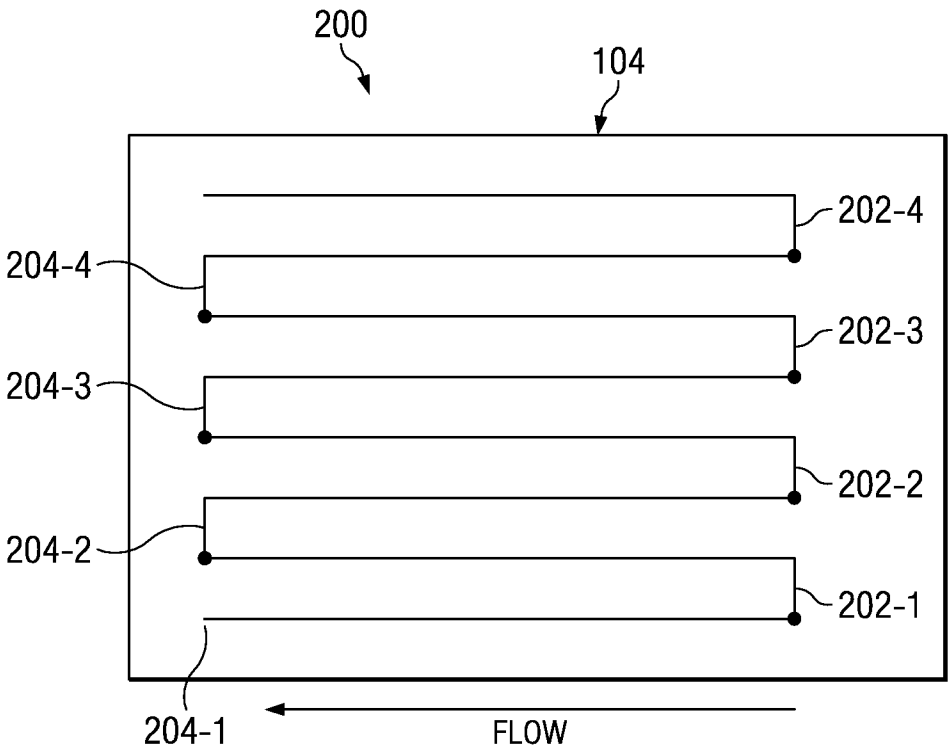

FIG. 2
(PRIOR ART)

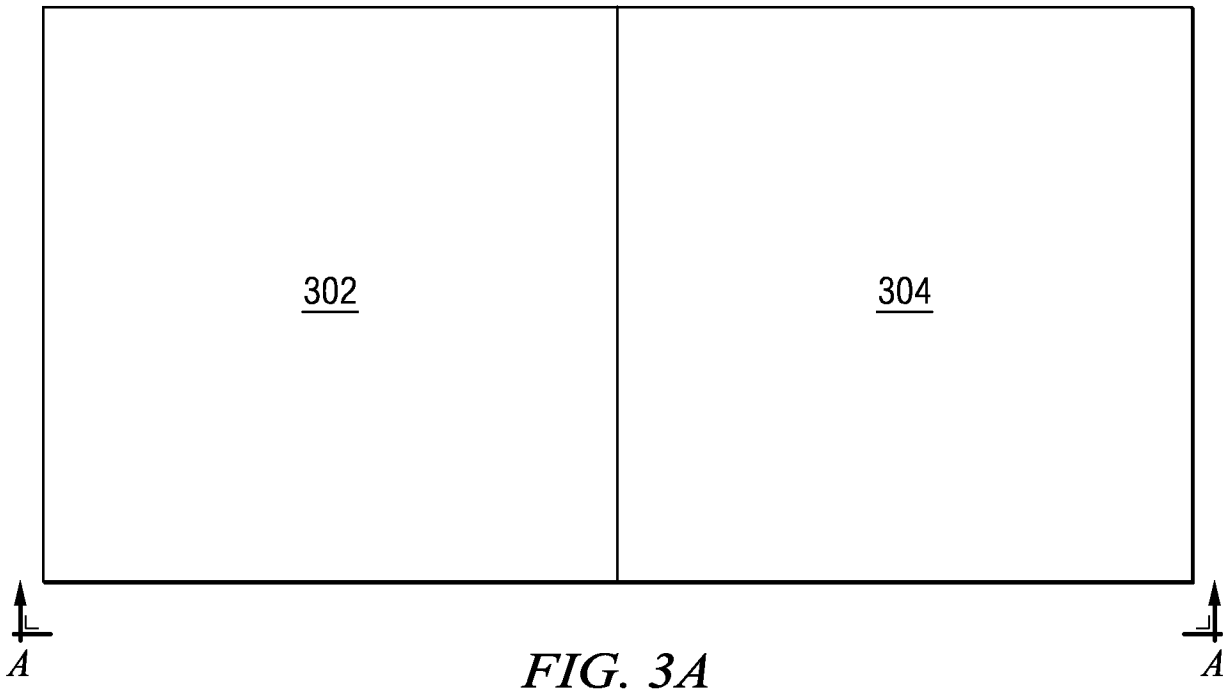

FIG. 3A

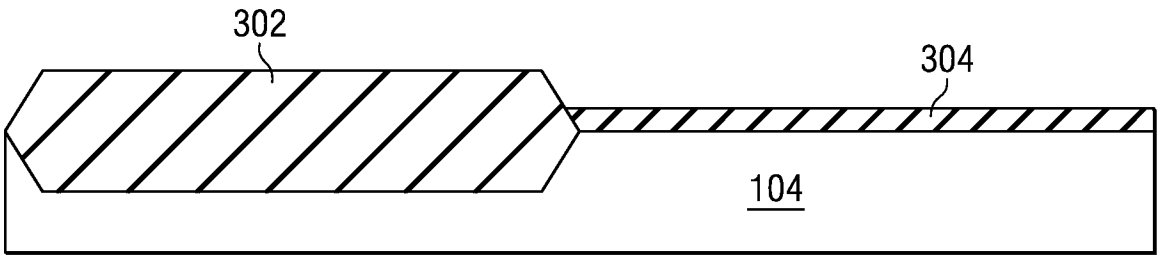

FIG. 3B

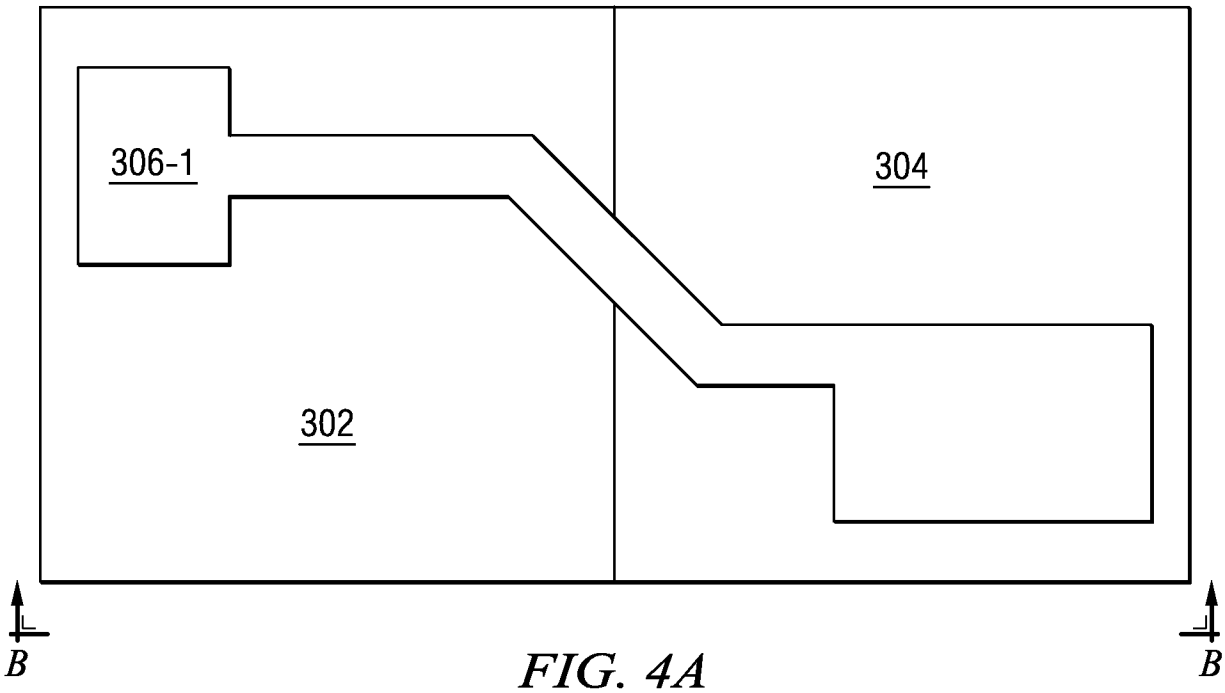

FIG. 4A

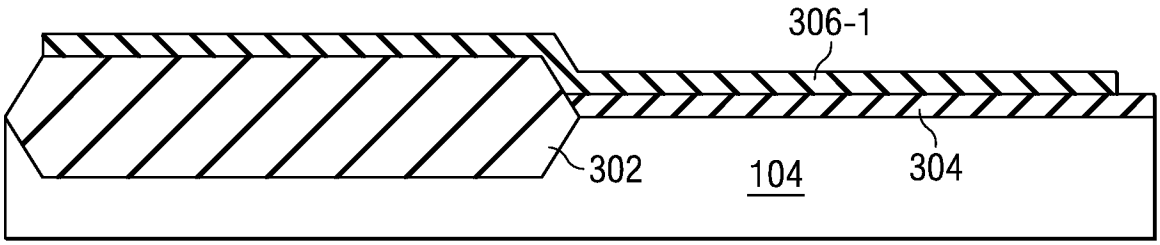

FIG. 4B

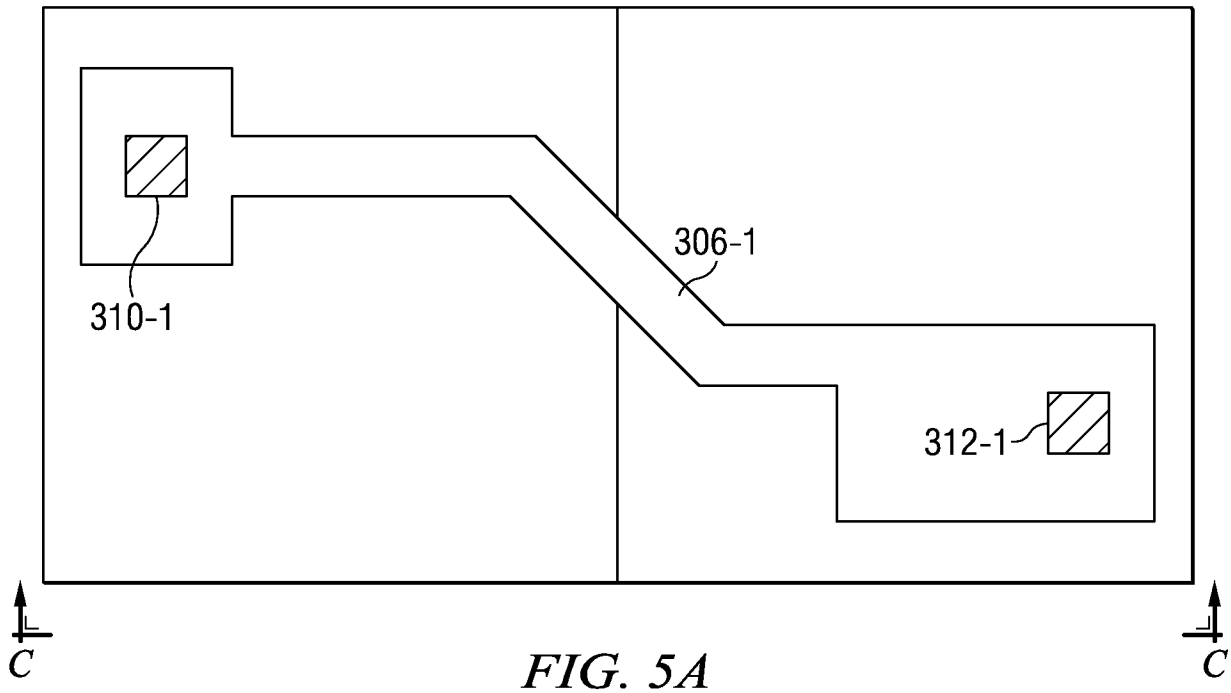

FIG. 5A

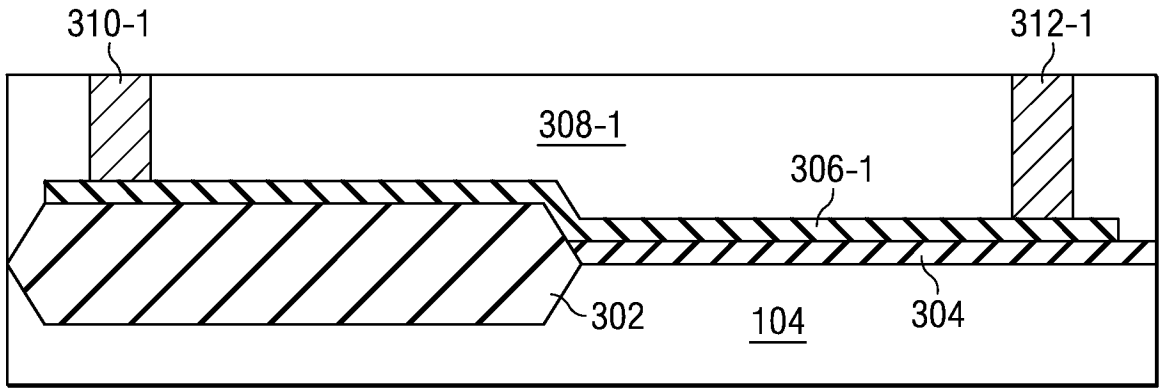

FIG. 5B

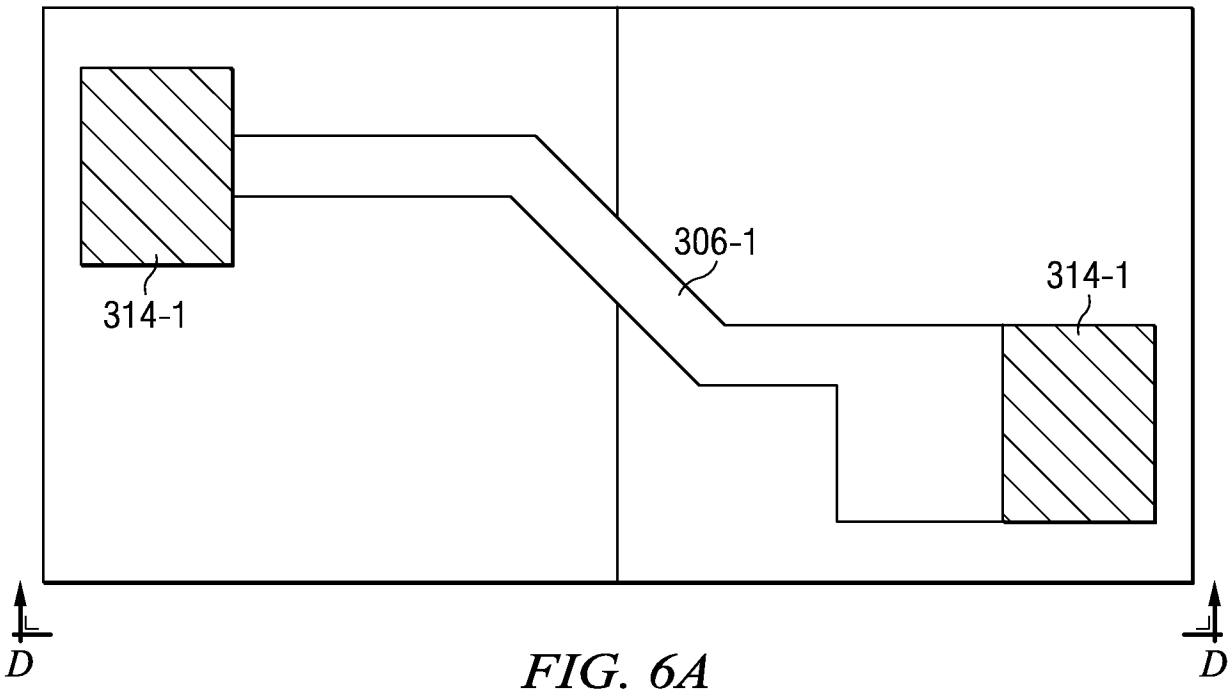

FIG. 6A

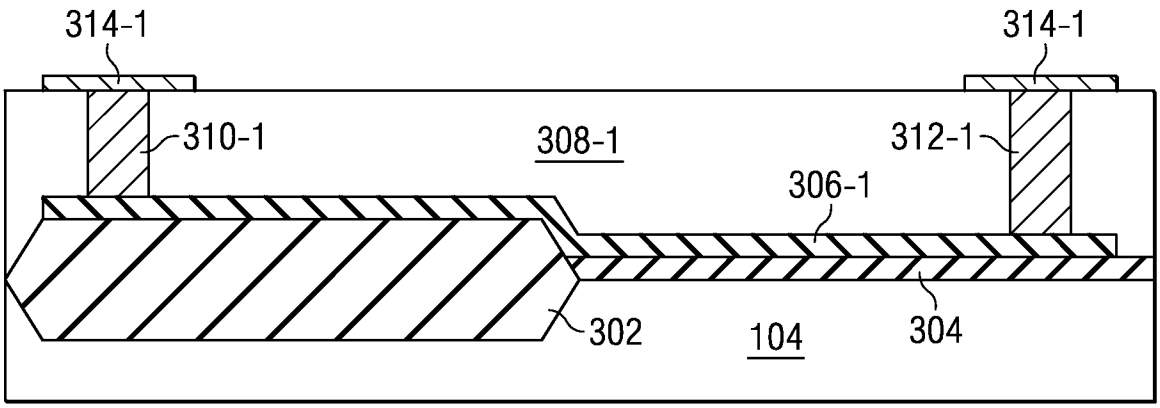

FIG. 6B

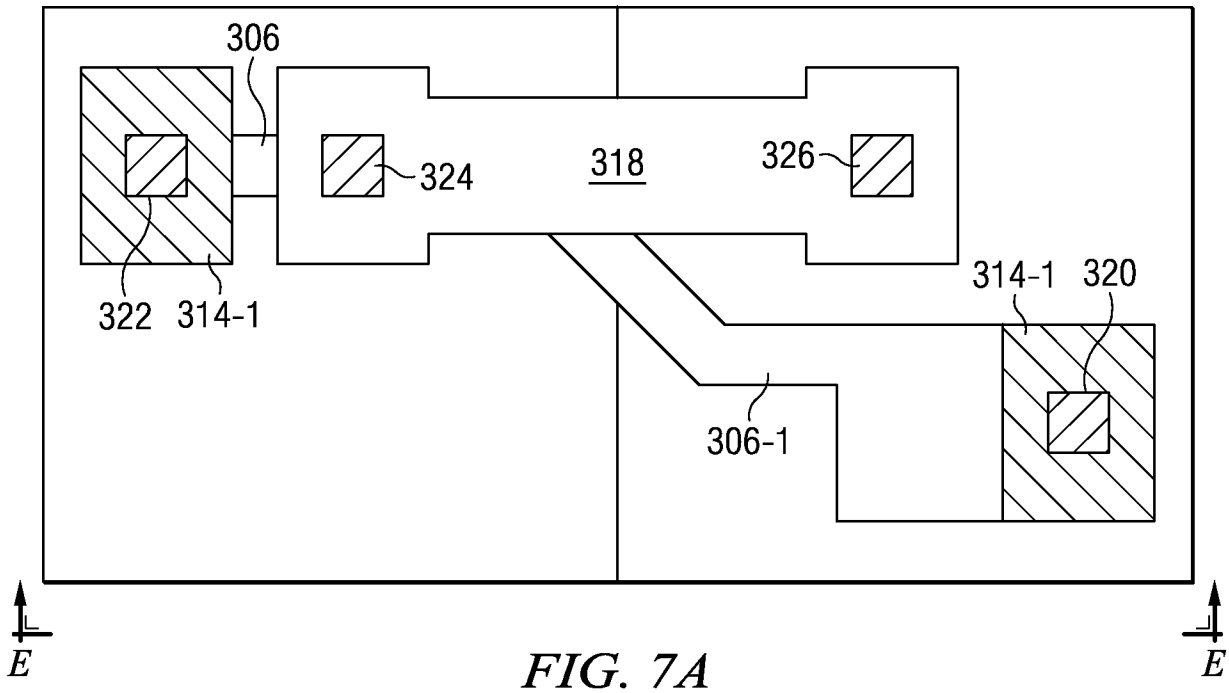
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FIG. 7A

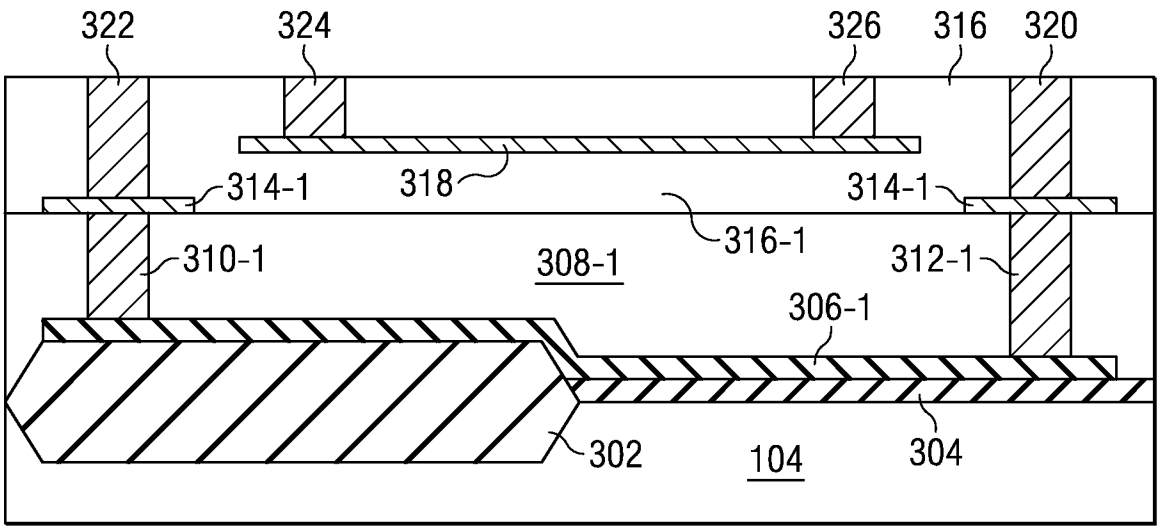
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FIG. 7B

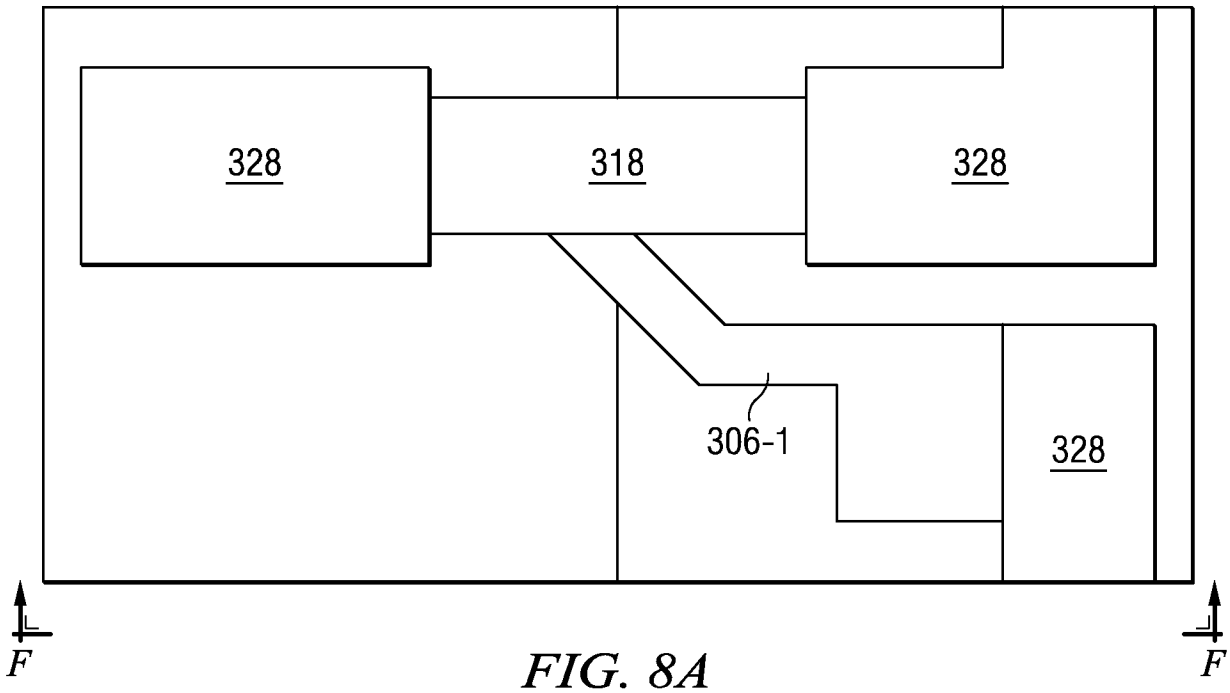
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FIG. 8A

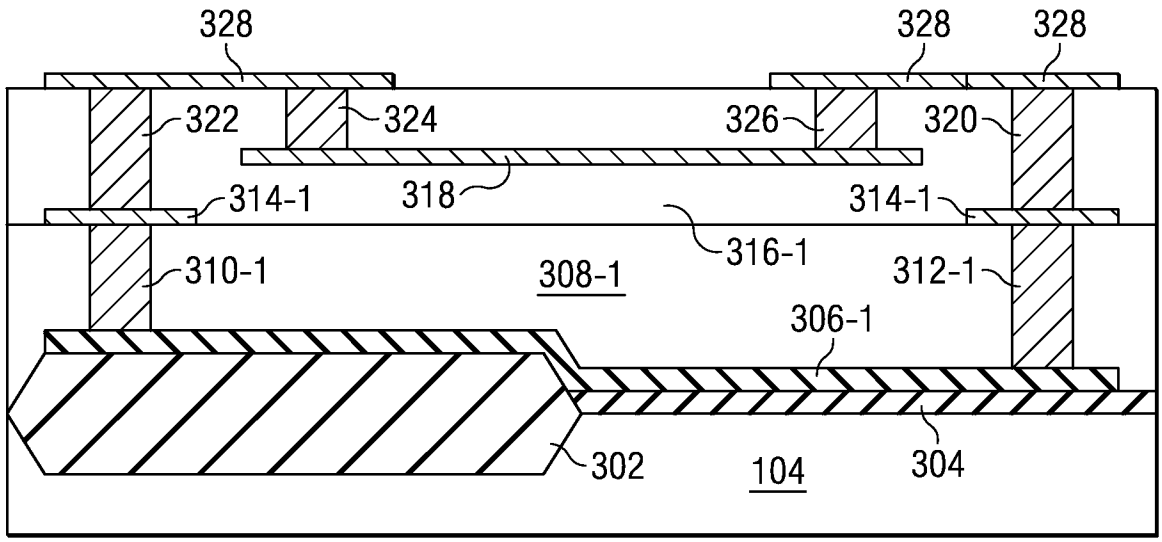
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FIG. 8B

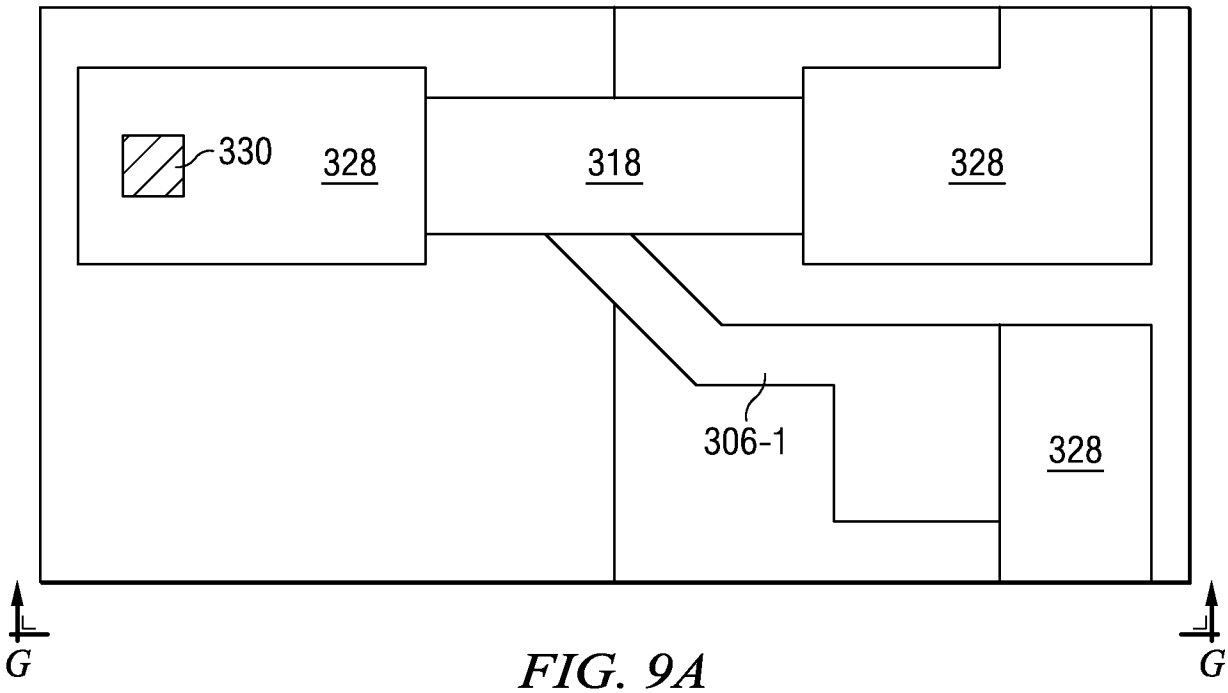
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FIG. 9A

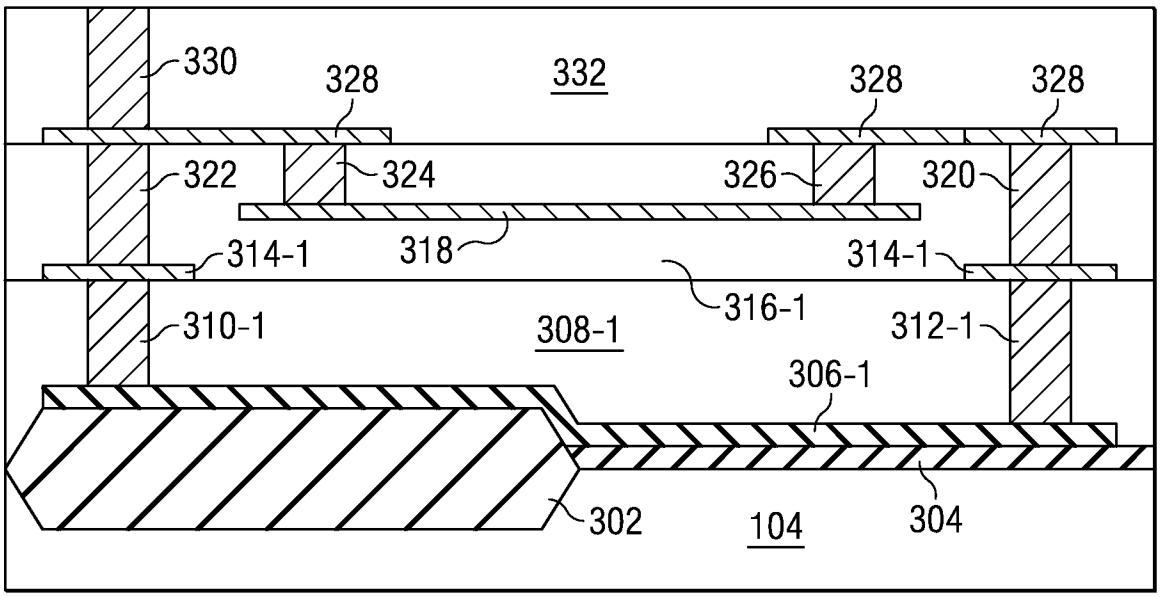
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FIG. 9B

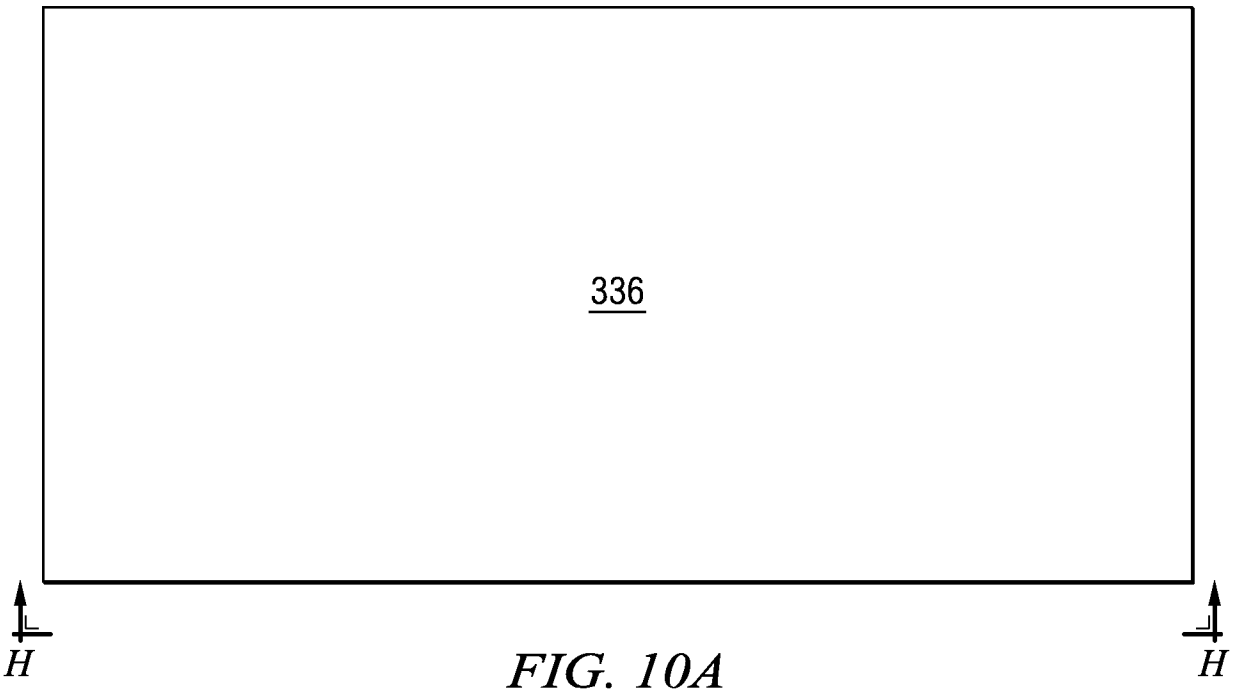


FIG. 10A

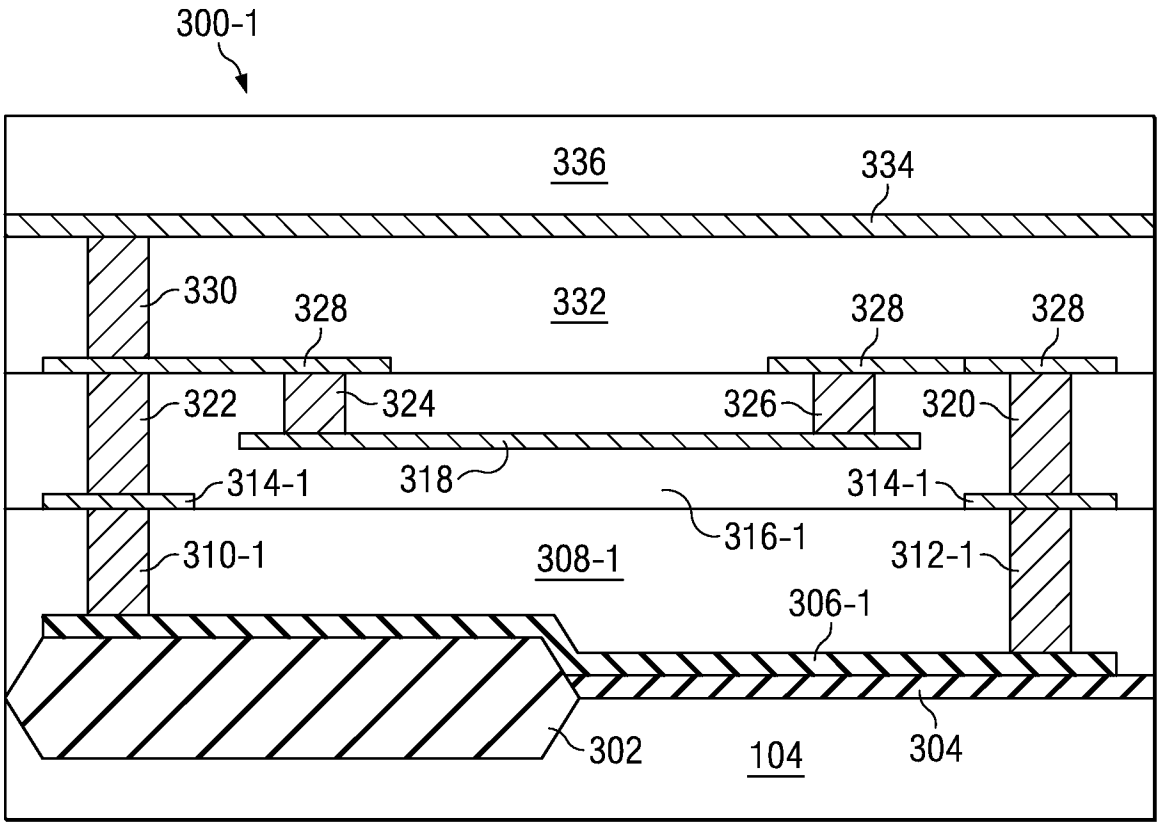


FIG. 10B

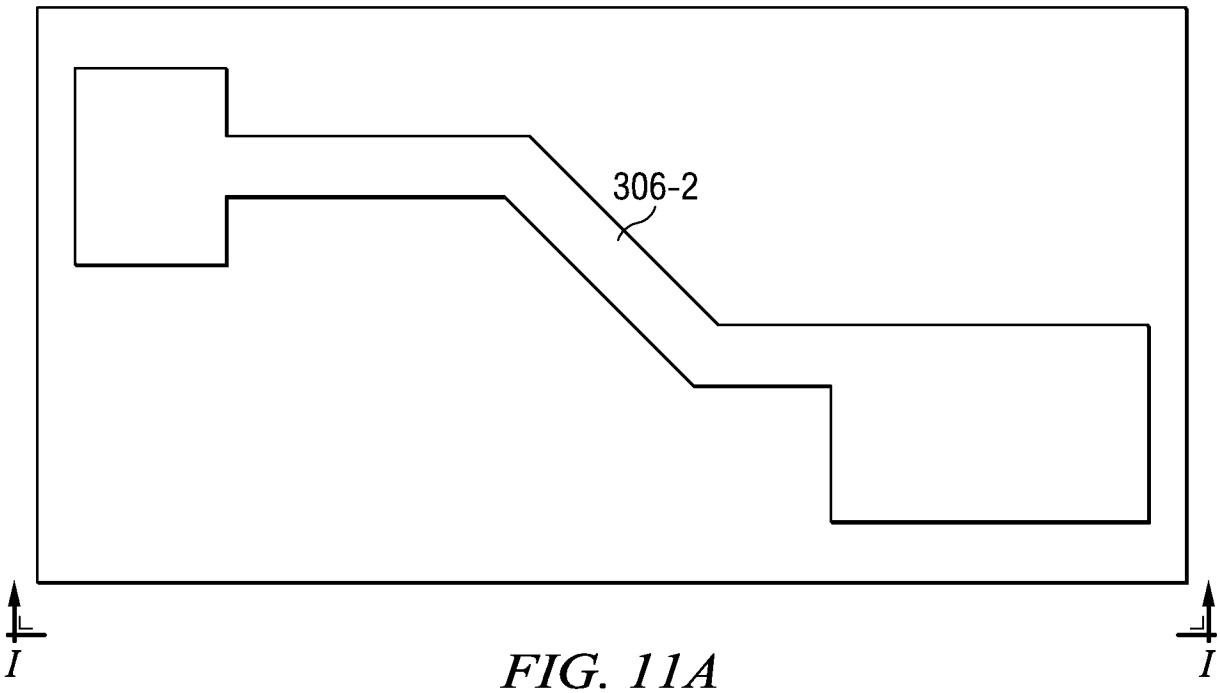


FIG. 11A

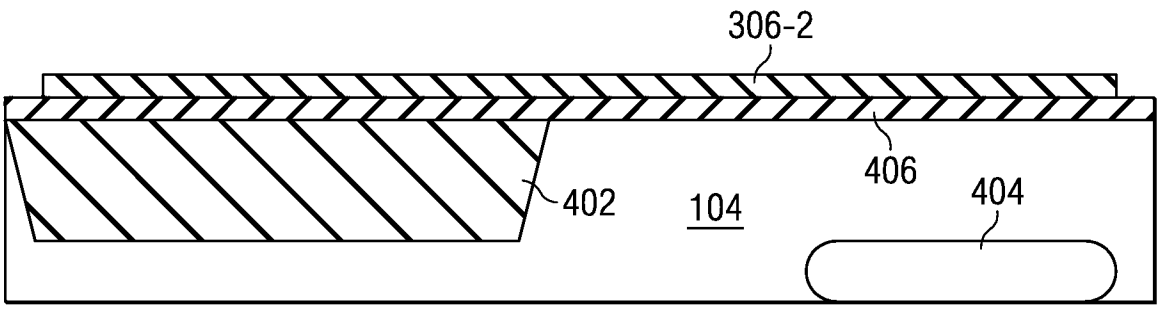


FIG. 11B

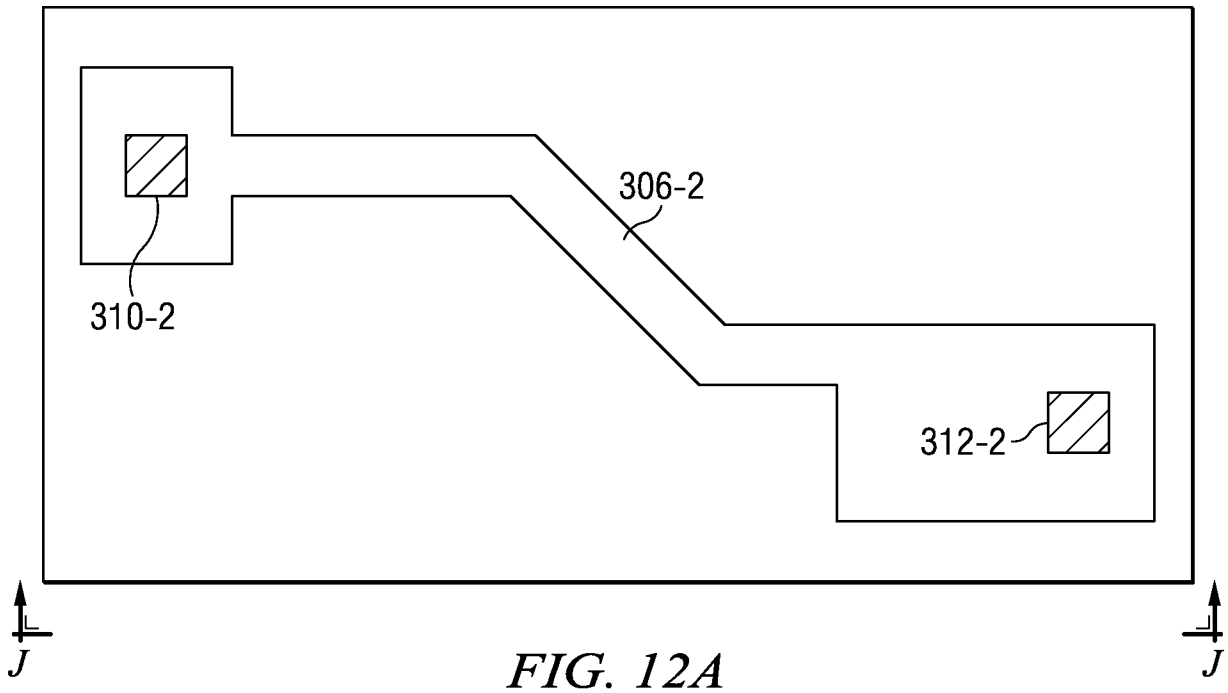


FIG. 12A

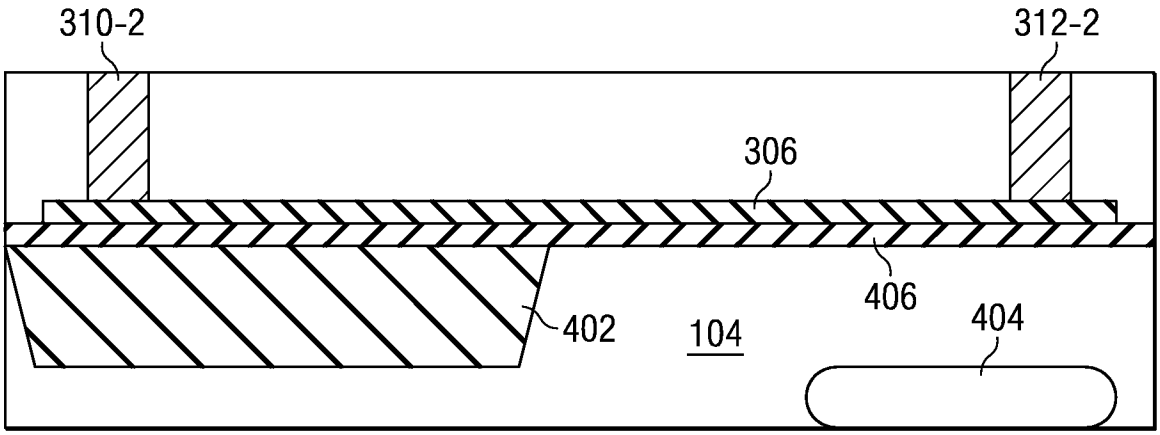


FIG. 12B

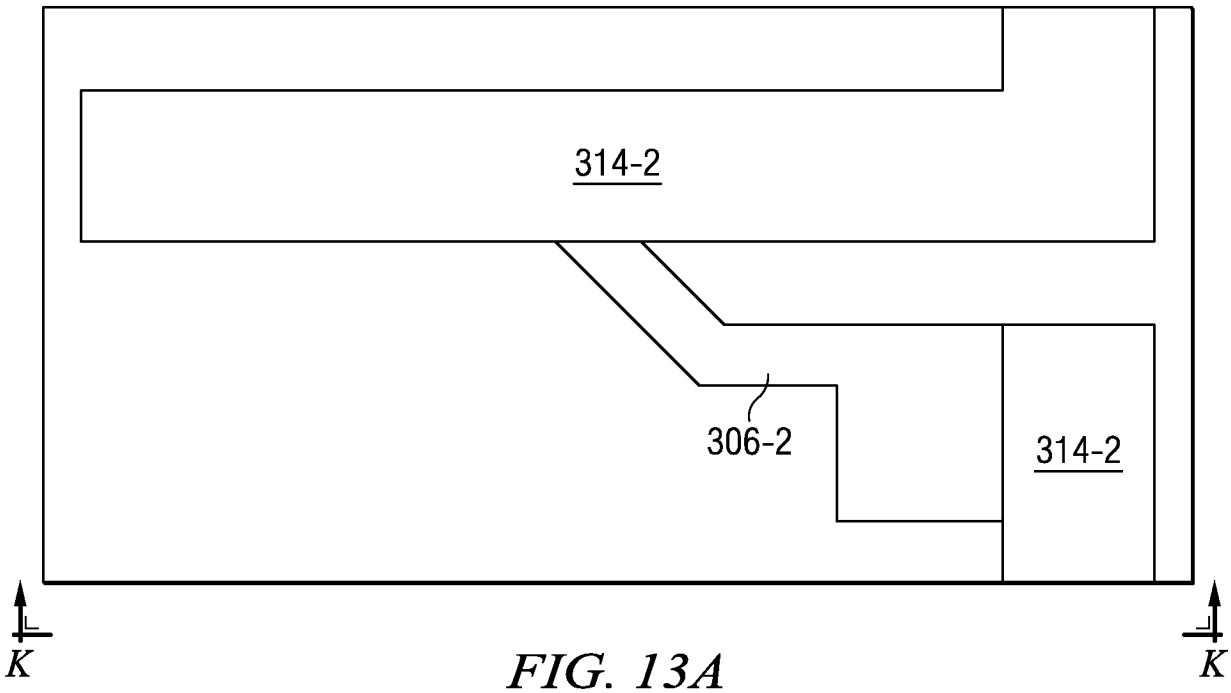


FIG. 13A

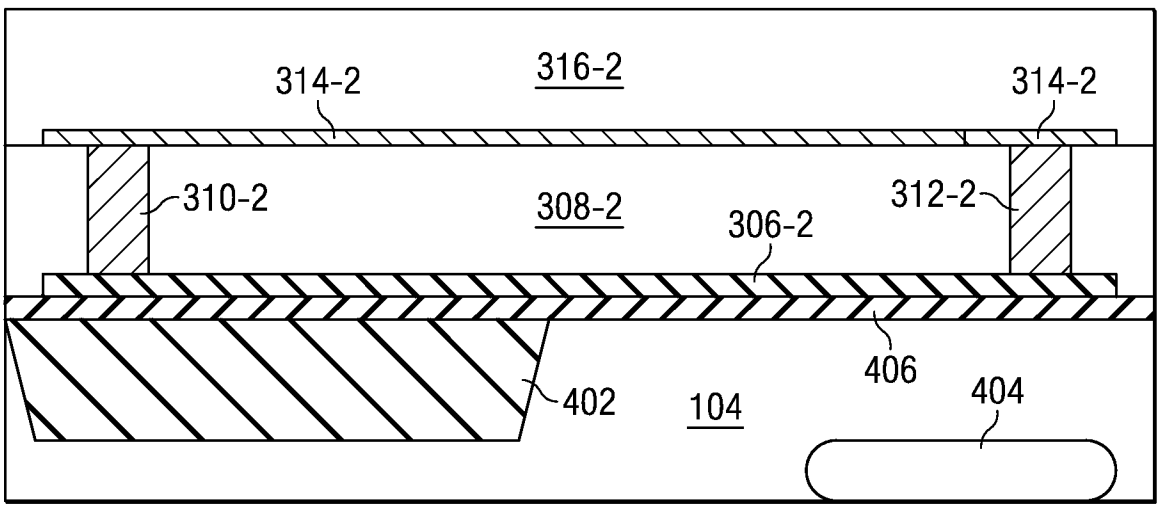


FIG. 13B

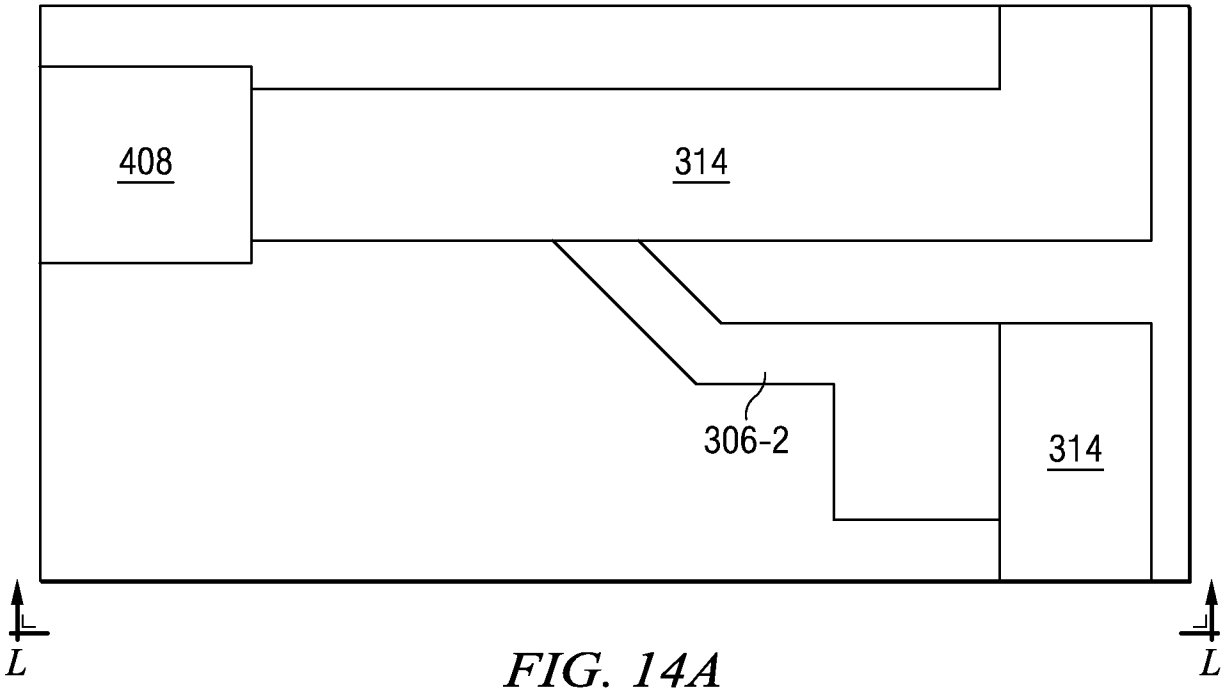


FIG. 14A

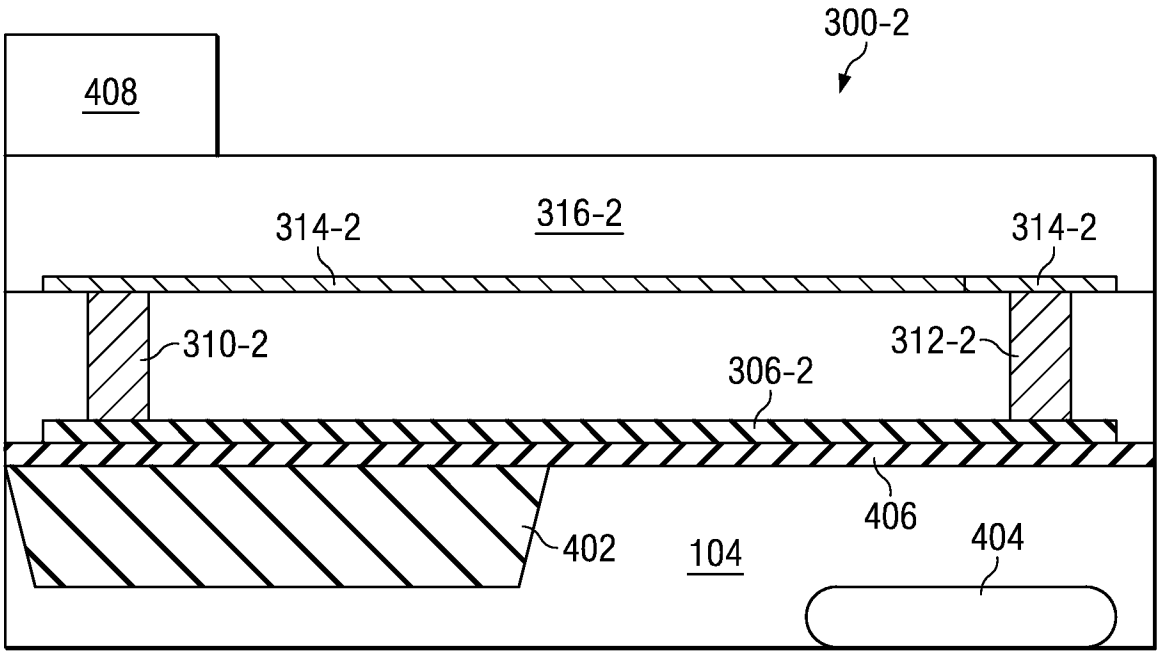
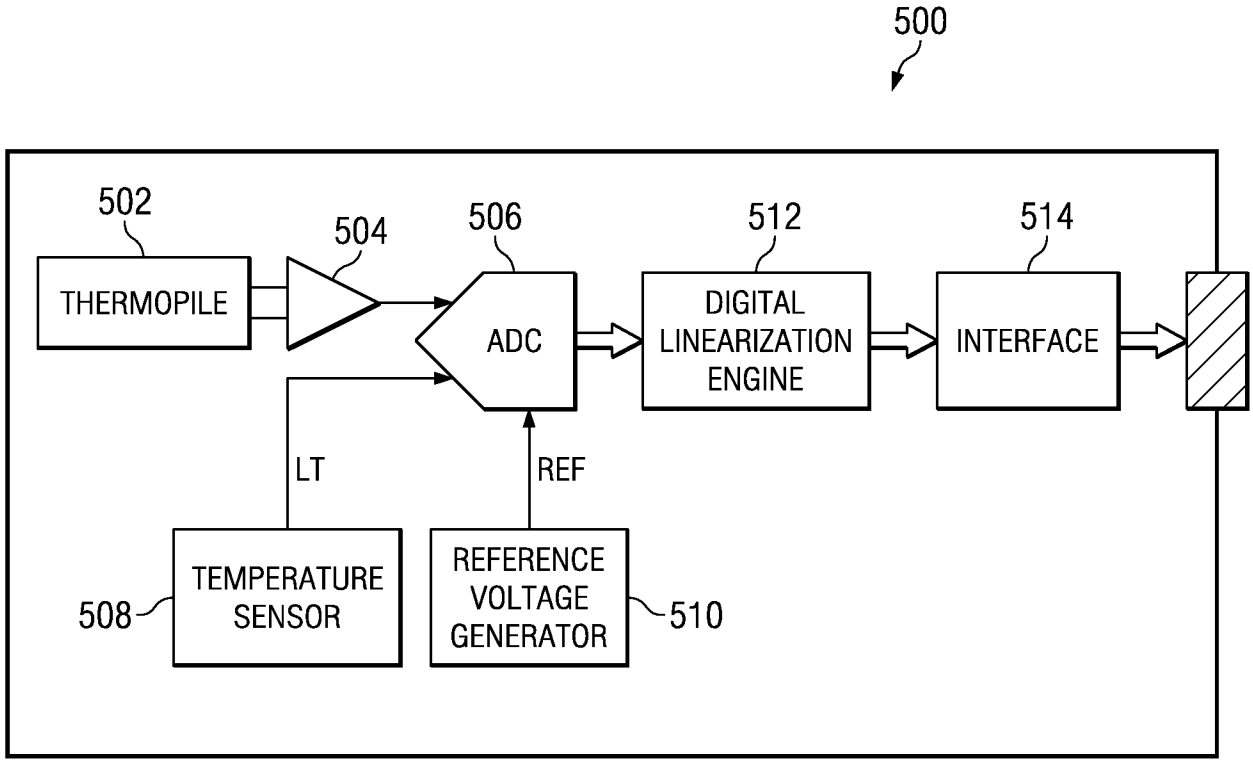


FIG. 14B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THERMOPILE
ADC
DIGITAL LINEARIZATION ENGINE
INTERFACE
LT
REF
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TEMPERATURE SENSOR
REFERENCE VOLTAGE GENERATOR
510

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/062055

A. CLASSIFICATION OF SUBJECT MATTER

H01L 35/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 35/32; H01L 35/02; H01L 35/00; H01L 35/34; H01L 27/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: thermocouple, seebeck, dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0095381 A1 (TE-HSI LEE) 03 May 2007 See abstract and paragraphs [0011]-[0024].	1-18
A	US 05909004 A (HEDENGREN et al.) 01 June 1999 See claim 1 and figure 2.	1-18
A	EP 1333503 A2 (DELPHI TECHNOLOGIES, INC.) 06 August 2003 See abstract and paragraphs [0011]-[0024].	1-18
A	US 05689087 A (MICHAEL D. JACK) 18 November 1997 See claim 1 and figure 1.	1-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 SEPTEMBER 2011 (22.09.2011)	**22 SEPTEMBER 2011 (22.09.2011)**

Name and mailing address of the ISA/KR

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Government Complex-Daejeon, 189 Cheongsa-ro,
Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Han Jae Gyun

Telephone No. 82-42-481-5716

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2010/062055

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US 2007-0095381 A1	03.05.2007	TW 264837 B	21.10.2006
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		US 06084174 A	04.07.2000
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		EP 1333503 B1	06.07.2011
US 05689087A A	18.11.1997	None	