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(54) Title: ELECTRONIC DEVICE HAVING A LEAD WITH SELECTIVELY MODIFIED ELECTRICAL PROPERTIES

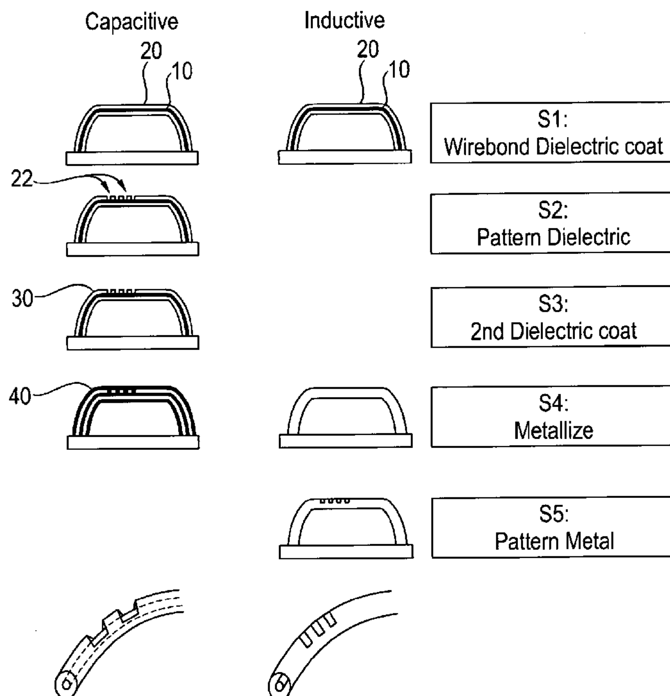

Fig. 1

(57) Abstract: The present invention relates to a die package comprising a die having a plurality of connection pads, a die substrate supporting a plurality of connection elements, a first lead having a first metal core (10) with a first core diameter, and a dielectric layer (20,30) surrounding the first metal core (S1), the dielectric layer (20,30) having a first dielectric thickness that varies along its length and/ or the dielectric layer having an outer metal layer (40, S4) at least partially surrounding the dielectric layer (20,30), for selectively modifying the electrical characteristics of the lead

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ELECTRONIC DEVICE HAVING A LEAD WITH SELECTIVELY MODIFIED ELECTRICAL PROPERTIES

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Field of the Invention

Leads for die packages are modified by selective application of dielectric or metal coatings, allowing better control of electrical properties, including changes to inductance and capacitance, and optimization for desired interconnect properties. In certain embodiments, signal phase matching is encouraged by layout changes
20 that match lead length or selectively vary other electrical properties.

Background

Electronic devices and components are operating at ever increasing speeds and over increasing frequency ranges. Popular semiconductor package types use wire bonds that can connect to a substrate or leadframe, which in turn can
25 connect to second level interconnects, vias, substrate or package traces, solder balls, or the like, for connection to a printed circuit board (PCB) of an electronic device.

However, in packages leads might not be optimized for particular electrical characteristics, including signal phase transmission properties, induction, or
30 capacitance.

Summary of the Invention

Bearing in mind the problems and deficiencies of the prior art, it is an object of the present invention to provide a die package with at least one lead connecting a connection pad of a die with a connection element of a die substrate that is optimized for particular electrical (in particular capacitive and/or inductive) characteristics.

The above and other objects, which will be apparent to those skilled in the art, are achieved in the present invention which is directed to a die package comprising a die having a plurality of connection pads, a die substrate supporting a plurality of connection elements, a first lead having a first metal core with a first core diameter, and a dielectric layer surrounding the first metal core, the dielectric layer having a first dielectric thickness that varies along its length.

Further, the present invention is directed to a die package comprising a die having a plurality of connection pads, a die substrate supporting a plurality of connection elements, a first lead having a first metal core with a first core diameter, a dielectric layer surrounding the first metal core, the dielectric layer having a first dielectric thickness, and an outer metal layer at least partially surrounding the dielectric layer.

The dielectric layer and/or the metal layer may be structured or patterned in given areas of the lead for selectively modifying the electrical characteristics of the lead. In particular, EM perturbations can be created allowing for modifications of the electrical response as a function of frequency in terms of attenuation and/or phase.

The dependent claims are directed to advantageous embodiments of the invention.

Brief Description of the Drawings

Fig 1 is an illustration of structures and methods for forming dielectric and metal coated leads optimized for various induction and capacitance requirements,

Figs. 2 and 3 respectively illustrate in plan and side view two leads having differing loop height but matched length to better match impedance and signal phase,

Fig. 4 illustrates method steps for manufacture of dielectric coated leads with
5 outer ground connected metallization,

Fig. 5 illustrates a subtractive method for manufacture of dielectric coated leads with outer ground connected metallization,

Fig. 6 illustrates a BGA package having dielectric coated leads with outer ground connected metallization, and

10 Fig. 7 illustrates a portion of leadframe package having dielectric coated leads with outer ground connected metallization.

Detailed Description

As seen in Fig. 1, leads suitable for a semiconductor die package can be formed from dielectric coated metal cores, with outer ground connected metallization. As
15 seen with respect to Fig. 1, an initially uniform dielectric or metal coating can be selectively modified to adjust electrical characteristics. These adjustments can result in changes primarily in capacitance (through dielectric removal) or inductance (through metal removal). In certain embodiments, a loop can be formed to have a substantially flat section to permit improved consistency in
20 selective patterning. These adjustments can occur with a single lead, groups of leads, or all leads in a package, as needed. In effect, a lead having a thickness that varies along its length is created, or alternatively or in addition, a lead having metal reduced or removed entirely along some portion of the lead length is formed to selectively modify electrical characteristics of the lead.

25 The process of electrical modification begins with attachment of a metal core 10 of a lead to die and substrate connection pads. The metal core is coated (S1) with a dielectric 20 that can be patterned (S2) by selective removal or ablation of the dielectric to a predetermined depth (while still leaving a thin dielectric layer surrounding the metal core) using laser ablation, photoresist based patterning of

photosensitive dielectrics, or mechanical, chemical, or thermal removal of dielectric material in defined areas 22 along the lead. If the dielectric layer 20 is removed completely to expose the metal core 10, a second, thinner dielectric layer 30 can be applied (S3). The dielectric layer is metallized (S4), with the metal 40 being connected to a ground. This metal 40 can in turn be patterned (S5) using laser ablation, mechanical, chemical, or thermal removal, with the resultant changes in electrical characteristics being primarily related to inductive characteristics.

As seen in Figs. 2 and 3, which respectively illustrate in plan and side view two leads 2, 4 having differing loop height but matched length to better match impedance and signal phase, other lead properties can be selectively adjusted to optimize or improve electrical characteristics. For die accepting or sending signals at Gigahertz frequencies, micron scale differences in lead length can result in significant mismatch in signal phase between different leads. The phase can be better matched by adjustments or capacitance or inductive characteristics such as discussed in connection with Fig. 1, or alternatively, by adjusting loop height so overall lead length is the same for signal lines that require phase matching. As will be appreciated, combinations of changes to lead length or electrical characteristics, including lead construction and patterning, can be used alone or in combination as necessary. In effect, phase matched first and second leads 2, 4 can be created so that loop height of the first lead 2 differs from lead length of the second lead 4, with loop height of the first lead 2 selected so lead length of the first lead 2 matches lead length of the second lead 4, despite a difference in straight line distance between respective connection pads 5 on the die 1 and connection elements 7 on the die substrate 6.

	3000 microns	3050 microns	Delta
GHz	Electrical length [degrees]	Electrical length [degrees]	Electrical length difference [degrees]
0.3	1.8	1.8	0.0
3	17.9	18.2	0.3

30	178.6	181.5	2.9
60	357.1	363.1	6.0

Table 1 illustrates the impact of a 50 micron difference in lead length on phase at different frequencies for a 50 ohm lead fabricated as described above. In some applications, a substantial fraction of 1 degree difference in phase can create performance detriments. The 30 and 60 GHz performance would thus be impacted per this example.

Dielectric and metal coated leads can be structured in their dielectric or metal layer(s) to create EM perturbations allowing for modifications of the electrical response, as a function of frequency, in terms of attenuation and/or phase to create well known electrical responses such as delay, coupling and filter characteristics. Multilayering of structured dielectric and metal layers is possible and can create elliptical responses well known to those skilled in the art. Once the dielectric 20 is deposited, the film can be patterned using a variety of methods; such methods being chosen based on attributes such as feature resolution, sidewall profile and depth, among others. Examples of these methods are laser, plasma and lithography.

In certain embodiments electrical characteristics can be adjusted by having dielectric coated leads used in semiconductor die packaging formed to have varying dielectric thickness. Thick, thin, and intermediate thicknesses are possible by varying dielectric coating times and manufacture steps. Both the core diameter and the dielectric thickness can be varied. In certain embodiments the composition of the deposited dielectric can be also varied, with for example distinct dielectric 20, 30 materials surrounding a metal core 10 and in turn be surrounded by a ground connectable metal coating 40. This allows, for example, a high performance dielectric 30 having superior vapor barrier, oxygen degradation resistance, or the like, to be thinly deposited over a thick layer of a low cost dielectric material 20. In still other embodiments multiple layers of

dielectric of varying thickness, can be separated by thin metal layers, with the outermost metal layer being connected to ground.

Generally, thin dielectric layers will provide low impedance good for power lines, thick dielectric layers are good for signal integrity, and outer metal layers are connected to same ground. Note that a combination of core diameters and dielectric thicknesses is possible and a series of such steps may be performed to achieve more than two impedances. In certain embodiments it may be desirable to have large cores on power lines to increase power handling capacity, reduce power line temperatures, and/or further reduce any inductance on power supply and ground lines that would exacerbate ground bounce or power sag. Dielectric layers of intermediate thickness are also useful, since many packages could benefit from having leads of three (3) or more different dielectric thicknesses. For example, a lead have an intermediate dielectric thickness could be used to connect a source and load of substantially different impedance to maximize power transfer. For example, a 10 ohm source can be coupled to a 40 ohm load with a 20 ohm lead. Also, since cost of dielectric can be high, critical signal pathways can be interconnected using thick dielectric, with less critical status, reset, or the like leads can be coated with a dielectric layer having a thickness greater than the power leads, but less than (intermediate) to the critical signal leads. Advantageously, this can reduce dielectric deposition material cost and time.

The precise thickness of the dielectric coating may be chosen, in combination with the wirebond diameter, to achieve a particular desired impedance value for each lead.

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\varepsilon_r}} \cdot \log\left(\frac{b}{a}\right) \quad (1)$$

The characteristic impedance of a coax line is given in Eq. (1), where L is the inductance per unit length, C is the capacitance per unit length, a is the diameter of the bond wire, b is the outside diameter of the dielectric and ε_r is relative permittivity of the coaxial dielectric.

As illustrated in Fig. 4, in one embodiment manufacture of dielectric coated leads with outer ground connected metallization can proceed using the following steps. Connection pads are cleaned (50) on the die and the substrate and a wirebonder is used to connect the die to the connection pads (51). Optionally, a second diameter wire can be attached (52) (e.g. a larger diameter wire suitable for power connections), or areas of the die can be masked (53) or otherwise protected to allow for selective deposition. One or more layers of dielectric of the same or different composition can be deposited (54), followed by selective laser or thermal ablation, or chemical removal of portions of the dielectric to allow access to ground connections covered in the dielectric deposition step (55). This step is optional, since in some embodiments, the need for a ground via can be eliminated. This is particularly true for die operating at higher frequencies, since a virtual RF ground may be established through capacitive coupling. Metallization (57) follows, covering the dielectric with a metal layer that forms the outermost metallized layer of the leads, and also connecting the leads to ground. The entire process can be repeated multiple times (58), useful for those embodiments using selective deposition techniques, and particularly for those embodiments supporting multiple die or complex and varied impedance leads. In the final step, for non-cavity packages, an overmold can be used to encapsulate leads (59). Alternative embodiments and additional or variant method steps are also described in US20120066894 and US Patent 6,770,822, the disclosures of which are fully incorporated by reference.

In certain embodiments, modifications and additions to the described process are possible. For example, providing conformal coatings of dielectric can be accomplished through a variety of methods using chemical (electrophoretic), mechanical (surface tension), catalytic (primer, electromagnetic [UV, IR], electron beam, other suitable techniques. Electrophoretic polymers are particularly advantageous because they can rely on self-limiting reactions that can deposit precise thicknesses readily by adjusting process parameters and or simple additive, concentration, chemical, thermal, or timing changes to an electrophoretic coating solution.

In other embodiments, dielectric precoated bondwires can be used to form leads. While commercially available coated wires typically are thinner in dielectric thickness than is necessary to create, for example, 50 ohm leads, the foregoing discussed dielectric deposition steps can be used to increase dielectric thickness 5 to set the desired impedance. Use of these precoated wires can simplify other process steps necessary to create coaxes, and can allow for thinner layers of needed vapor deposited dielectrics and faster processing times to create ground vias. Precoated bondwires can be used to prevent shorting for narrowly spaced or crossing leads. In certain embodiments the precoated bondwire can have a 10 dielectric made from a photosensitive material to allow for selective patterning techniques.

In other embodiments, the dielectric parylene can be used. Parylene is the trade name for a variety of chemical vapor deposited poly(p-xylylene)polymers used as moisture and dielectric barriers. Parylene can be formed in a growth limited 15 condensation reaction using a modified parylene deposition system where the die, substrate, and leads are aligned to a photoplate which allows EM radiation (IR, UV or other) to strike in a precise manner causing selective growth rate of dielectric. Advantageously, this can minimize or eliminate the need for processes to create contact vias, bulk removal of parylene, etc.

20 Parylene and other dielectrics are known to suffer from degradation due to oxygen scission in the presence of oxygen, water vapor and heat. Damage can be limited by metal layers that form excellent oxygen vapor barriers, with thin layers of 3-5 micron thickness capable of forming true hermetic interfaces. Alternatively, if metal has been selectively removed, or not deposited in certain 25 areas due to electrical, thermal, or manufacturing requirements, a wide range of polymer based vapor oxygen barriers can be used, with polyvinyl alcohol (PVA) being one widely used polymer. These polymers can be glob topped, screen printed, stenciled, gantry dispensed, sprayed onto parylene surface that will be exposed to the oxygen or H2O vapor environment. Advantageously, use of vapor 30 barrier polymers can be a part of a cost reduction strategy, since thicker layers of high cost parylene or other oxygen sensitive might otherwise be required.

As will be appreciated, all of the described method steps can benefit from various selective deposition techniques. Selective deposition can be by physical masking, directed polymer deposition, photoresist methods, or any other suitable method for ensuring differential deposition thickness on the metal core, dielectric layer, or other outermost layer at time of deposition. While selective deposition allows for additive methods to build leads, it also allows for subtractive techniques in which dielectric or metal is removed to form interconnects of differing impedances. For example, a package populated by one or more die can be wire-bonded as appropriate for interconnect of all package and device pads. As seen with respect to Fig. 5, which illustrate steps and structures for manufacture of a die package, the dielectric coating 200 can be deposited (Step A) to a thickness X-A over a wirebond metal conductor 202, where A is the thickness of the dielectric needed for the secondary interconnect impedance. The secondary impedance wirebond dielectrics can be removed (Step B) for example by an etch step, followed by a second coating 204 deposition (Step C) followed by metallization 206 of both interconnects (Step D). This subtractive process will create wirebonds of two distinct impedances.

In an embodiment illustrated with respect to Fig. 6, a ball grid array (BGA) package 210 that includes dielectric and metal coated leads 212, 214 having well defined and adjustable lead electrical characteristics is described.

A BGA is a surface-mount packaging widely used for integrated circuits, and can generally provide more interconnection pins than dual in-line, leadframe, or other flat package since the entire bottom surface of the BGA can be used for connection pads. In many types of BGA packages, a die 216 is attached to a substrate 218 having fillable vias 220 connected to connection pads. Wirebonds 212, 214 can be used to connect the top side die 216 to the pads/vias 220, consequently providing electrical connections from a top side of the substrate to the bottom. In a BGA package, balls of solder 222 are attached to the bottom of the package and held in place with a tacky flux until soldering to a printed circuit board or other substrate. As described herein, the wirebonds of conventional BGA packages can be replaced with improved leads having a dielectric layer and an outer ground connectable metal layer. The leads can have varying dielectric

thickness over an inner core and an outer metal layer, as well as being selectively optimized to have specific impedances, which can be selected to be different or well-matched based in part on dielectric layer thickness. As seen in the Fig. 6, both long 212 and short 214 leads are supported.

5 In more detail, assembly of an improved BGA package can require face up attachment of a die to a substrate supporting a connection pad formed adjacent and around a via in the substrate. This assembly is wirebonded as appropriate for each required interconnect, with a wirebond formed between a connection pad on the substrate and a connection pad on the die. Low frequency and power inputs
10 are connected to the low frequency signal leads, while high-frequency inputs and outputs are connected to the high frequency signal leads. In some embodiments, the low frequency and power inputs can have a thickness that differs from high frequency signal leads. The assembly is then subjected to the coating of any essentially conformal dielectric material. Because of its low cost, ease of vacuum
15 deposition, and superior performance characteristics, parylene can be used. A small part of the dielectric layer near the leadframe attachment point can be selectively removed by etch, thermal degradation, or laser ablation, in order to form electrical connection to a ground contact point or ground shield layer. Similarly, a small portion of the dielectric layer is removed near the die connection
20 pads to permit ground connections. Connection to ground in the structure follows from application of a metallized layer over the top of the dielectric layer, forming a ground shield. The thickness of the preferred metal layer should be chosen in consideration of skin depth and DC resistance issues, and should be composed primarily of an excellent electrical conductor such as silver, copper, or gold. For
25 most applications, a 1 micron coating thickness is adequate for functionality, but thicker coatings can help minimize cross-talk between leads. These coatings may be added in defined areas through a combination of lithography or other masking methods, and plating or other selective deposition methods. The package can be completed by placement of an overmold or lid over the die, followed by dicing
30 (singulation) and testing.

Alternatively, in an embodiment illustrated with respect to Fig. 7, low cost leadframe based die package 300 including wire bonds extending from the die to

a leadframe can be manufactured by forming a leadframe strip containing a two-dimensional array of individual package sites and outside frame portion. Leadframe fabrication is conventional, and can include formation of separate leads through etching, stamping, or electrodeposition. The leadframe strip can be placed in a mold including, but not limited to, an injection molding or transfer molding apparatus. An appropriate dielectric material, preferably plastic such as commercially available epoxy mold compound, is injected, pumped or otherwise transferred into the mold to achieve a leadframe/mold material composite structure. The properties of the mold material are important for their dielectric constant, loss tangent, and electrically dispersive properties as well as their temperature, moisture, and other mechanical performance attributes.

Each package site on the resulting composite leadframe strip is cleaned of mold release material and or mold-flash, and prepared for deposition of a metal finish over the exposed metal portions of the leadframe. This may be accomplished through plating techniques such as immersion or electroplating, and the metals would be chosen for corrosion suppression and ease of wirebonding. An example of such finishing is a thin layer of nickel (for protection) followed by a layer of gold (added protection and ability to wirebond). Each package site of the resultant molded leadframe strip can then be populated with the required die , which are attached to the base, with die attach material being chosen for mechanical and thermal properties for a particular packaging application. The resultant assembly is then wirebonded as appropriate for each required interconnect, with a wirebond formed between a lead on the leadframe and a connection pad on the die. Low frequency and power inputs are connected to the low frequency signal leads, while high-frequency inputs and outputs are connected to the high frequency signal leads. In some embodiments, the low frequency and power inputs can have a thickness that differs from high frequency signal leads

Like the foregoing described BGA package 210, the populated leadframe strip is then subjected to the coating of any essentially conformal dielectric material including parylene. In the case of parylene, it may be preferable to mask the bottom of the packages with tape, such as a vacuum-compatible polyimide with acrylic adhesive, or similar material to prevent deposition onto the area of the

leads that will eventually attached to the PCB. This will facilitate easier soldering at a subsequent step. A small part of the dielectric layer near the leadframe attachment point is selectively removed by etch, thermal degradation, or laser ablation, in order to form electrical connection to a ground contact point or ground
5 shield layer. Similarly, a small portion of the dielectric layer is removed near the die connection pads to permit ground connections. Connection to ground in the structure follows from application of a metallized layer over the top of the dielectric layer, forming a ground shield. The thickness of the preferred metal layer should be chosen in consideration of skin depth and DC resistance issues,
10 and should be composed primarily of an excellent electrical conductor such as silver, copper, or gold. For most applications, a 1 micron coating thickness is adequate for functionality, but thicker coatings can help minimize cross-talk between leads. These coatings may be added in defined areas through a combination of lithography or other masking methods, and plating or other
15 selective deposition methods. The package is completed by placement of an overmold or lid over the die, followed by dicing (singulation) and testing.

In particular, the present invention is directed to a die package comprising a die having a plurality of connection pads, a die substrate supporting a plurality of connection elements, a first lead having a first metal core with a first core
20 diameter, and a dielectric layer surrounding the first metal core having a first dielectric thickness that varies along it length.

Further, the present invention is directed to a die package comprising a die having a plurality of connection pads, a die substrate supporting a plurality of connection elements, a first lead having a first metal core with a first core
25 diameter, a dielectric layer surrounding the first metal core having a first dielectric thickness, and an outer metal layer at least partially surrounding the dielectric layer.

The die package may be at least part of a BGA package or a leadframe package.

Further, the present invention is directed to a die package comprising a die
30 having a plurality of connection pads, a die substrate supporting a plurality of connection elements, phase matched first and second leads, each lead having a

metal core with a core diameter, and a dielectric layer surrounding the metal core having a dielectric thickness, with loop height of the first lead differing from lead length of the second lead, with loop height of the first lead selected so lead length of the first lead matches lead length of the second lead, despite a difference in
5 straight line distance between respective connection pads on the die and connection elements on the die substrate.

Further, the present invention is directed to a device block comprising a die substrate supporting a plurality of connection elements, a first lead having a first metal core with a first core diameter, and a dielectric layer surrounding the first
10 metal core having either a first dielectric thickness that varies along its length, or an outer metal layer at least partially surrounding the dielectric layer, or both the above, creating perturbations of the electrical response.

In the above device block, the response perturbation may be an electrical delay, coupling and/or filter characteristics.

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Claims

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1. A die package comprising
a die (216) having a plurality of connection pads,
a die substrate (218) supporting a plurality of connection elements,
a first lead (212, 214) having a first metal core (10) with a first core diame-
10 ter, and a dielectric layer (20) surrounding the first metal core (10), the dielectric layer having a first dielectric thickness that varies along its length and/or the dielectric layer having an outer metal layer (40) at least partially surrounding the dielectric layer, for selectively modifying the electrical characteristics of the lead.

15 2. The die package of claim 1, wherein the dielectric layer (20) is patterned by selective removal or ablation of the dielectric to a predetermined depth in defined areas (22) along the lead.

3. The die package of claim 1 or 2, wherein a second, preferably thinner dielectric
20 layer (30) is applied to the dielectric layer (20).

4. The die package of any of the preceding claims, the dielectric layer being metallized with the metal (40) being connected to a ground.

25 5. The die package of claim 4, wherein the metal is patterned, preferably by using laser ablation, mechanical, chemical or thermal removal, for modifying the inductive characteristics of the lead.

6. The die package of any of the preceding claims, further comprising: phase
30 matched first and second leads (2, 4), each lead having a metal core with a core diameter, and a dielectric layer surrounding the metal core having a dielectric thickness, with loop height of the first lead (2) selected so that lead length of the first lead matches lead length of the second lead (4), despite a difference in straight line distance between respective connection pads (5) on the die (1) and
35 connection elements (7) on the die substrate (6).

7. The die package of claim 6, wherein the loop height of the first lead differs from the lead length of the second lead.

8. The die package of any of the preceding claims, wherein the dielectric layer
5 and/or the metal layer is structured to create EM perturbations allowing for modifications of the electrical response as a function of frequency, in terms of attenuation and/or phase.

9. The die package of any of the preceding claims, wherein said die substrate in-
10 cludes filled via to allow formation of a BGA package.

10. The die package of any claims 1 to 8, wherein said die substrate includes a leadframe to form a leadframe package.

15 11. A BGA package (210) including a die package of any of claims 1 to 9.

12. A leadframe package (300) including the die package of claim 10.

13. A device block comprising
20 a die substrate supporting a plurality of connection elements,
a first lead having a first metal core with a first core diameter, and a dielectric layer surrounding the first metal core having either
a first dielectric thickness that varies along its length, and/or
an outer metal layer at least partially surrounding the dielectric layer,
25 to create EM perturbations allowing for modifications of the electrical response.

14. The device block of claim 13, wherein the dielectric layer and/or the metal layer is structured for allowing modifications of the electrical response in terms of at-
30 tenuation and/or phase to create electrical responses with given delay, coupling and/or filter characteristics.

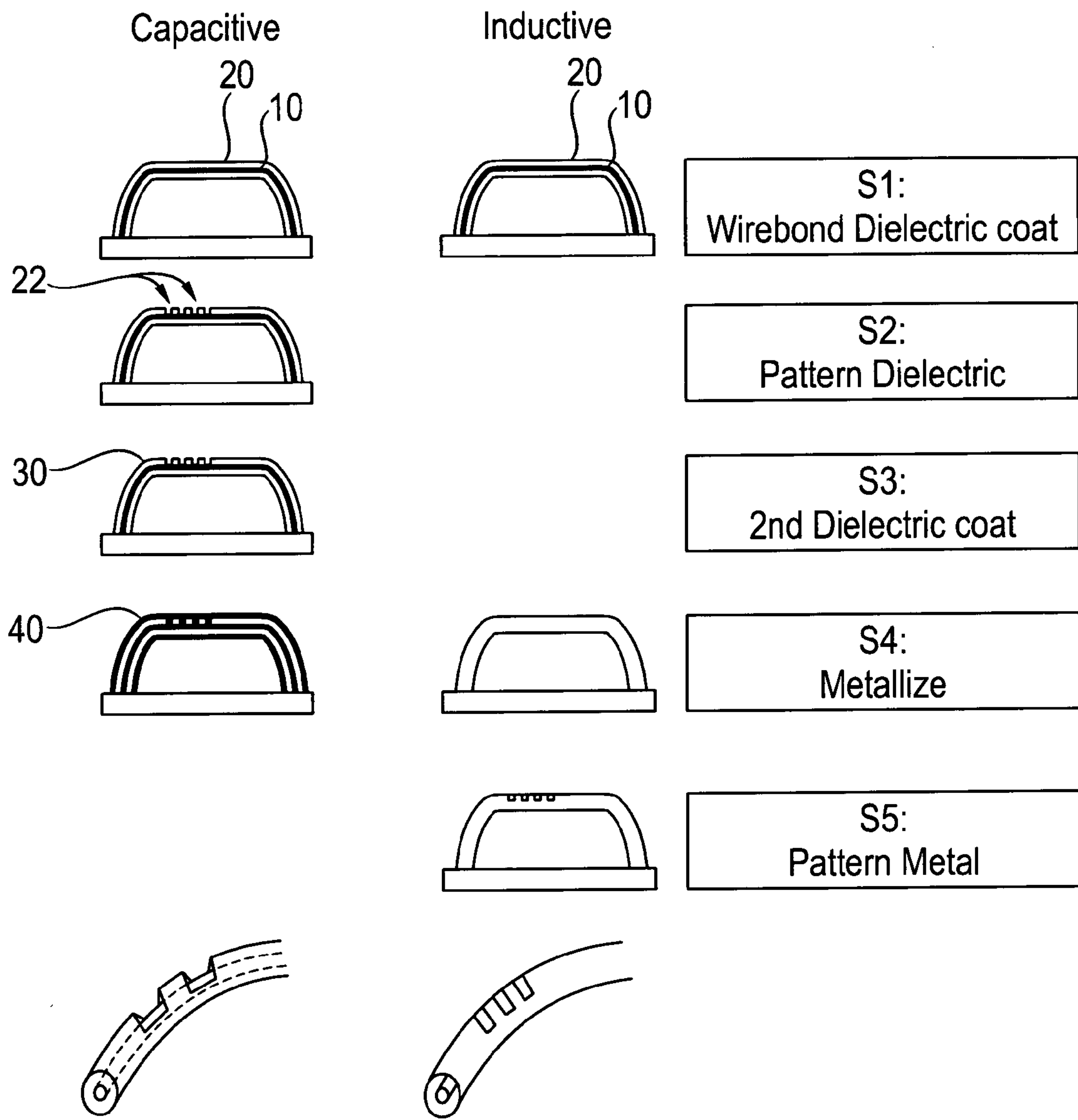

Fig. 1

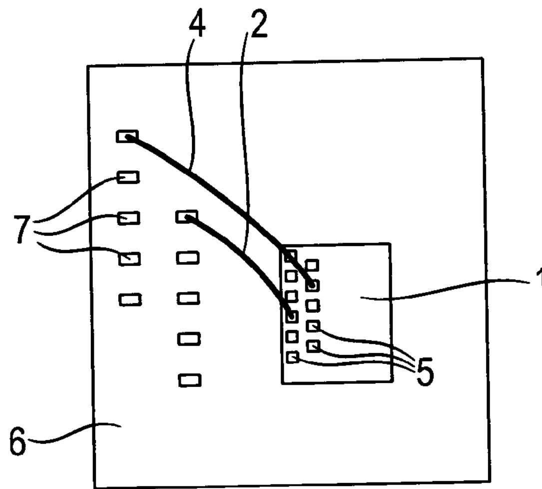

Fig. 2

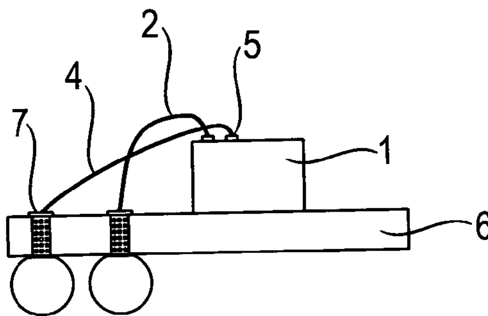

Fig. 3

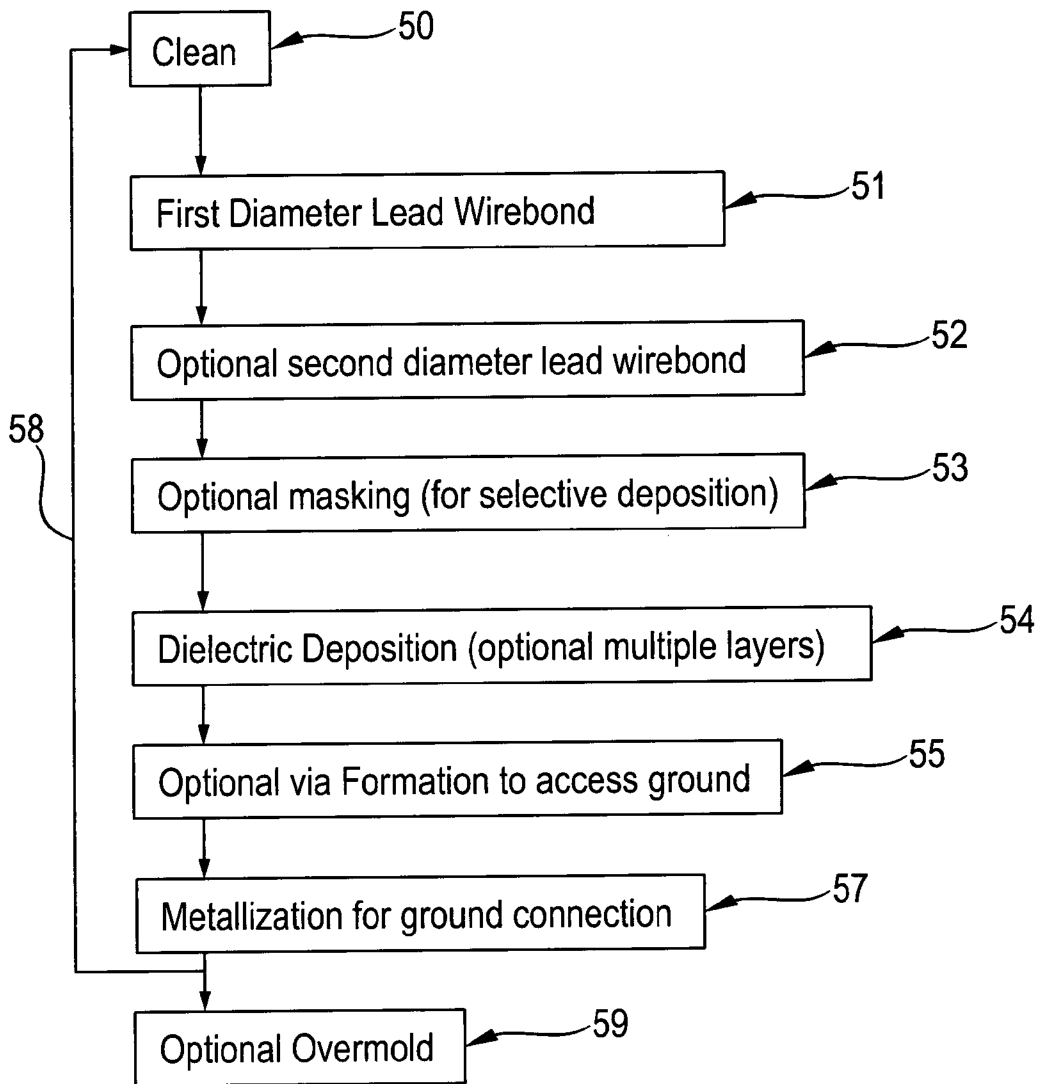

Fig. 4

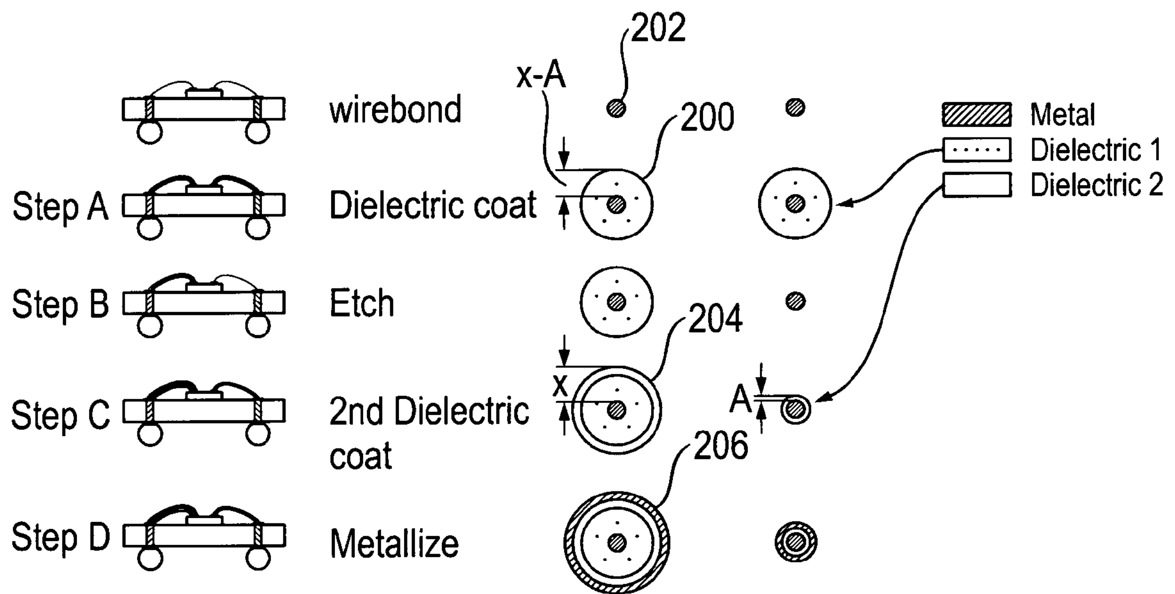

Fig. 5

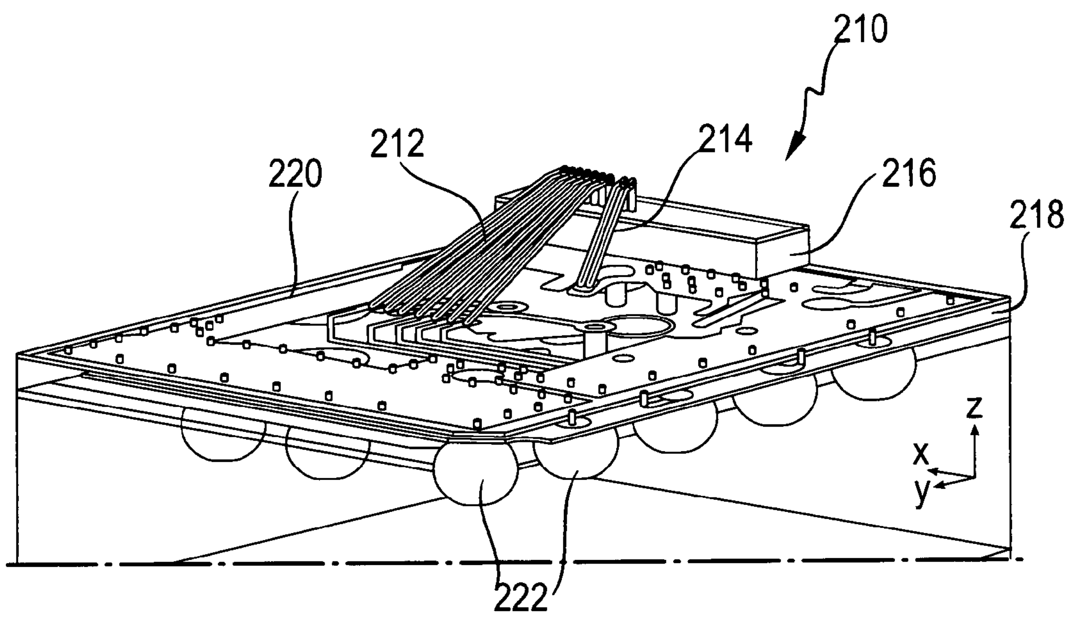

Fig. 6

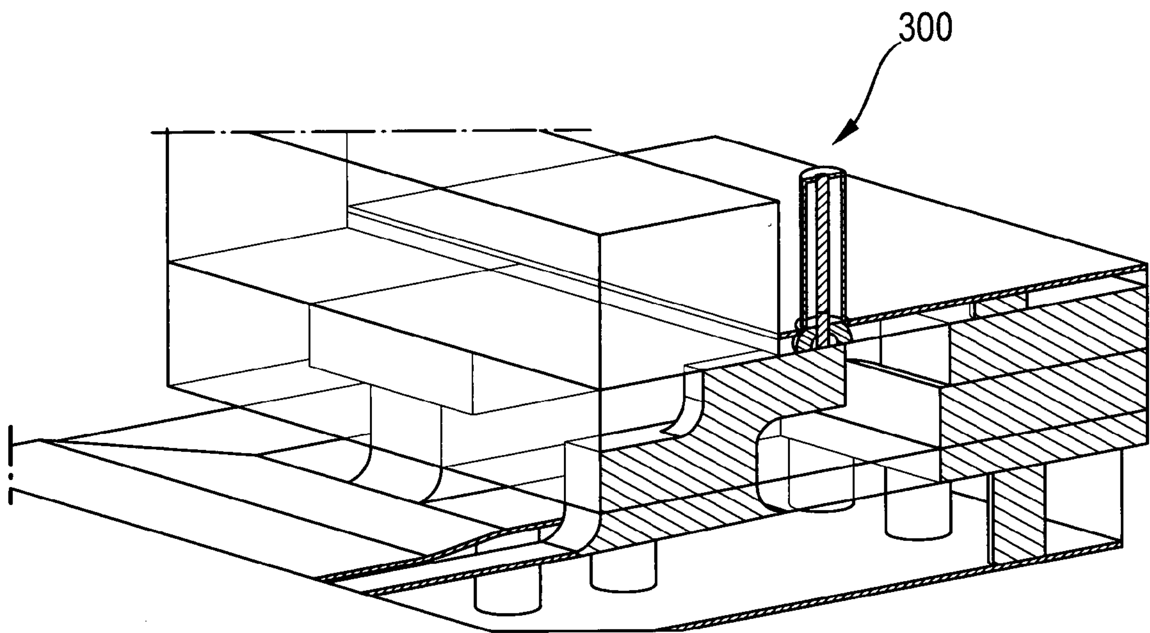

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/001824

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/49 H01L23/50 H01L23/66
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/159320 A1 (SANJUAN ERIC A [US] ET AL) 25 June 2009 (2009-06-25) cited in the application paragraphs [0001], [0026], [0047] - [0053]; figures 6,14,16 -----	1,4,10, 12,13
X	US 2008/296780 A1 (YOO CHEOL-JOON [KR]) 4 December 2008 (2008-12-04) paragraphs [0006], [0037] - [0043], [0053], [0054], [0061], [0062]; claims 16-20; figures 1,7,11,12,24 -----	1,2,8,9, 11,13,14
X	US 7 202 109 B1 (ZAKHARIAN DAVID [US] ET AL) 10 April 2007 (2007-04-10) column 3, line 48 - column 4, line 67; figures 4,5 -----	1,2,8, 12-14
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 September 2014	01/10/2014

Name and mailing address of the ISA/	Authorized officer
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2004/089929 A1 (CHIU CHI-TSUNG [TW] ET AL) 13 May 2004 (2004-05-13) paragraphs [0004], [0016], [0023] - [0033], [0036]; figures 2,4	1,4,13
X	US 2010/025864 A1 (BAILEY MARK J [US] ET AL) 4 February 2010 (2010-02-04) paragraphs [0003] - [0006], [0014] - [0021], [0025]; claims 1-7; figures 1-3,5	1,4,13
X	US 8 377 749 B1 (PATTERSON JOSEPH MARTIN [US]) 19 February 2013 (2013-02-19) column 1, line 5 - line 10; figures 2a,3,4,5 column 2, line 45 - column 5, line 60	1,4,13

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