United States Patent [19]
Walker

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[45] **June 10, 1975**

[54] **MESSAGE ANNOUNCEMENT APPARATUS AND METHOD**

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[73] Assignee: **The Audichron Company,** Atlanta, Ga.

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[52] **U.S. Cl.**..... **360/12;** 179/100.1 R; 179/100.1 C; 360/72

[51] **Int. Cl.**..................... **G11b 15/02;** G11b 23/18

[58] **Field of Search**............ 360/12, 72, 71, 78, 74, 360/62, 61; 179/100.1 PS, 100.1 TC, 100.1 C, 1 SW; 340/147

[56] **References Cited**

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3,647,991	3/1972	Gaon et al.	360/12
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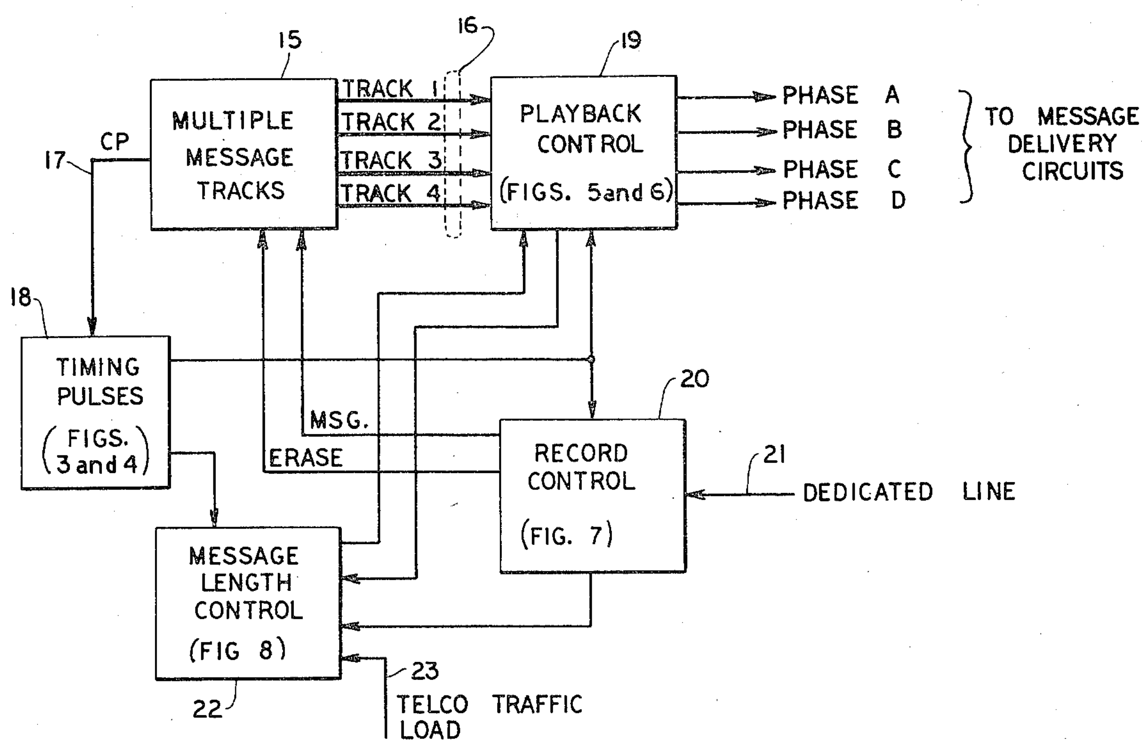
Primary Examiner—Alfred H. Eddleman

[57] **ABSTRACT**

Apparatus and method providing repetitive delivery of recorded messages composed of several separate message segments which are serially delivered. A composite message is provided by serial delivery of individual message segments which have an extent of overlap in message segment delivery time, so that an end portion of a message segment and a beginning portion of the next sequential message segment are concurrently recorded on a message recording medium. A message delivery circuit switches from delivery of the one message segment to delivery of the next sequential message segment during the period of concurrent message overlap, so that possible noise occurring at the beginning or end of the message segments is excluded from the delivered composite message. Part or all of a new composite message can be supplied from a remote location for recording and subsequent playback delivery by the present apparatus, and the apparatus can provide delivery of a predetermined shortened message component in response to certain signal conditions. Multiple announcement delivery phases are provided from a single set of message announcement segments, and each message phase can be selectively shortened in response to a single message length apparatus.

20 Claims, 10 Drawing Figures



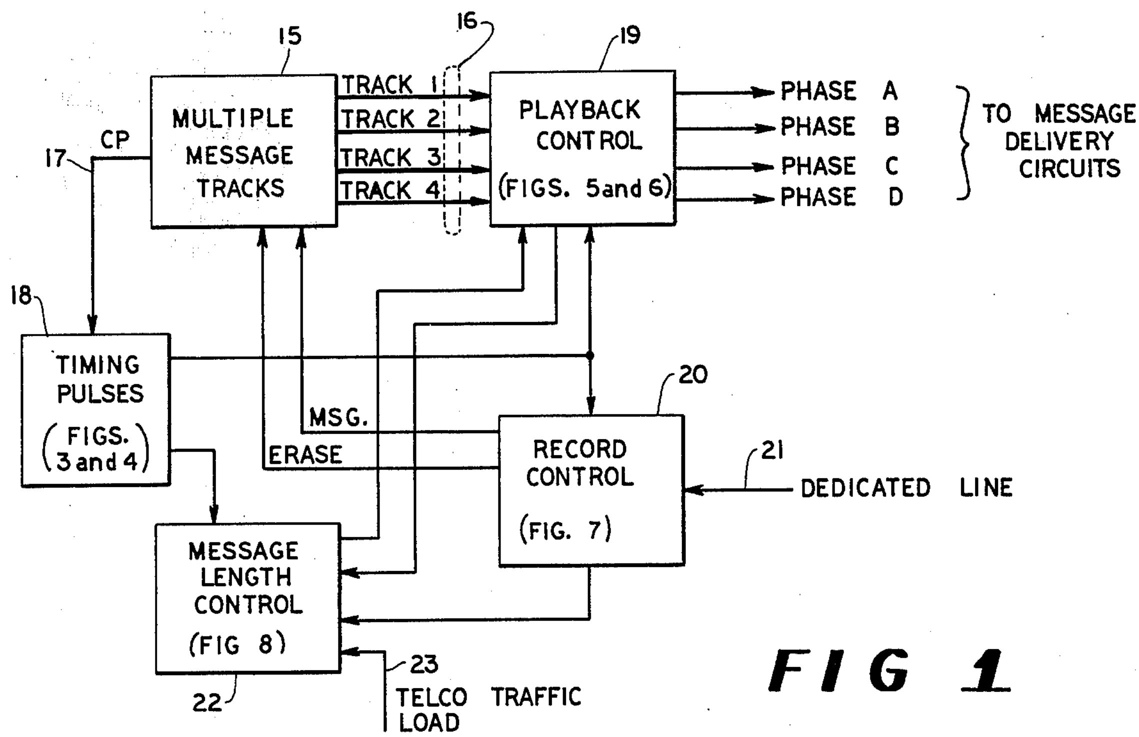

15
16
19
MULTIPLE MESSAGE TRACKS
TRACK 1
TRACK 2
TRACK 3
TRACK 4
PLAYBACK CONTROL (FIGS. 5and 6)
PHASE A
PHASE B
PHASE C
PHASE D
TO MESSAGE DELIVERY CIRCUITS
17
CP
18
TIMING PULSES (FIGS. 3and 4)
MSG.
ERASE
20
RECORD CONTROL (FIG. 7)
21
DEDICATED LINE
MESSAGE LENGTH CONTROL (FIG 8)
22
23
TELCO TRAFFIC LOAD

FIG 1

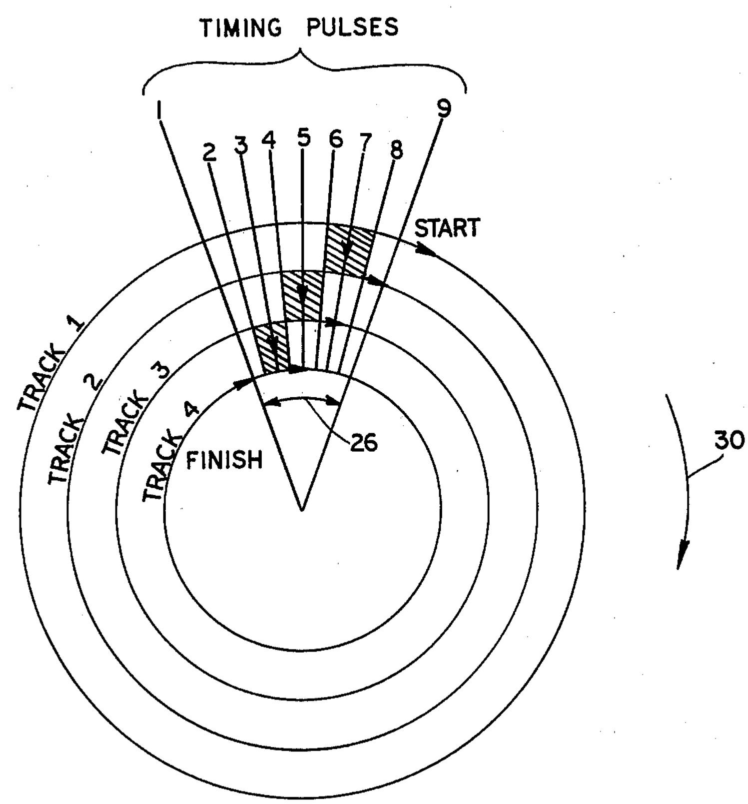

TIMING PULSES
1
2
3
4
5
6
7
8
9
START
TRACK 1
TRACK 2
TRACK 3
TRACK 4
FINISH
26
30

FIG 2

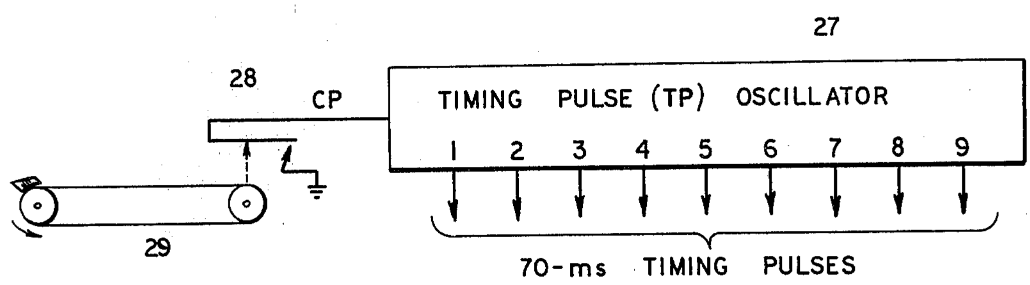

27
28
CP
TIMING PULSE (TP) OSCILLATOR
1 2 3 4 5 6 7 8 9
29
70-ms TIMING PULSES

FIG 3

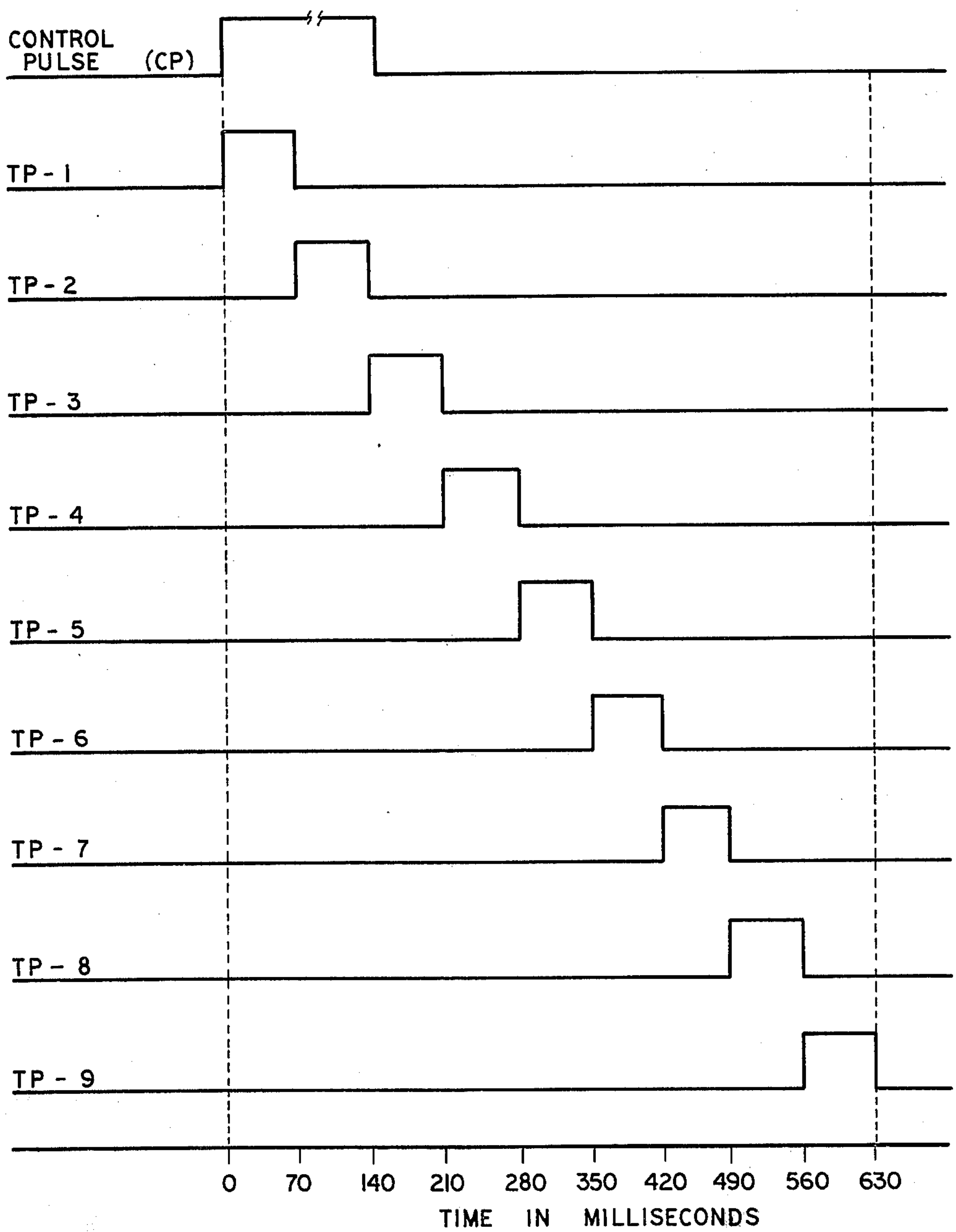

CONTROL PULSE (CP)
TP - 1
TP - 2
TP - 3
TP - 4
TP - 5
TP - 6
TP - 7
TP - 8
TP - 9
0 70 140 210 280 350 420 490 560 630
TIME IN MILLISECONDS

FIG 4

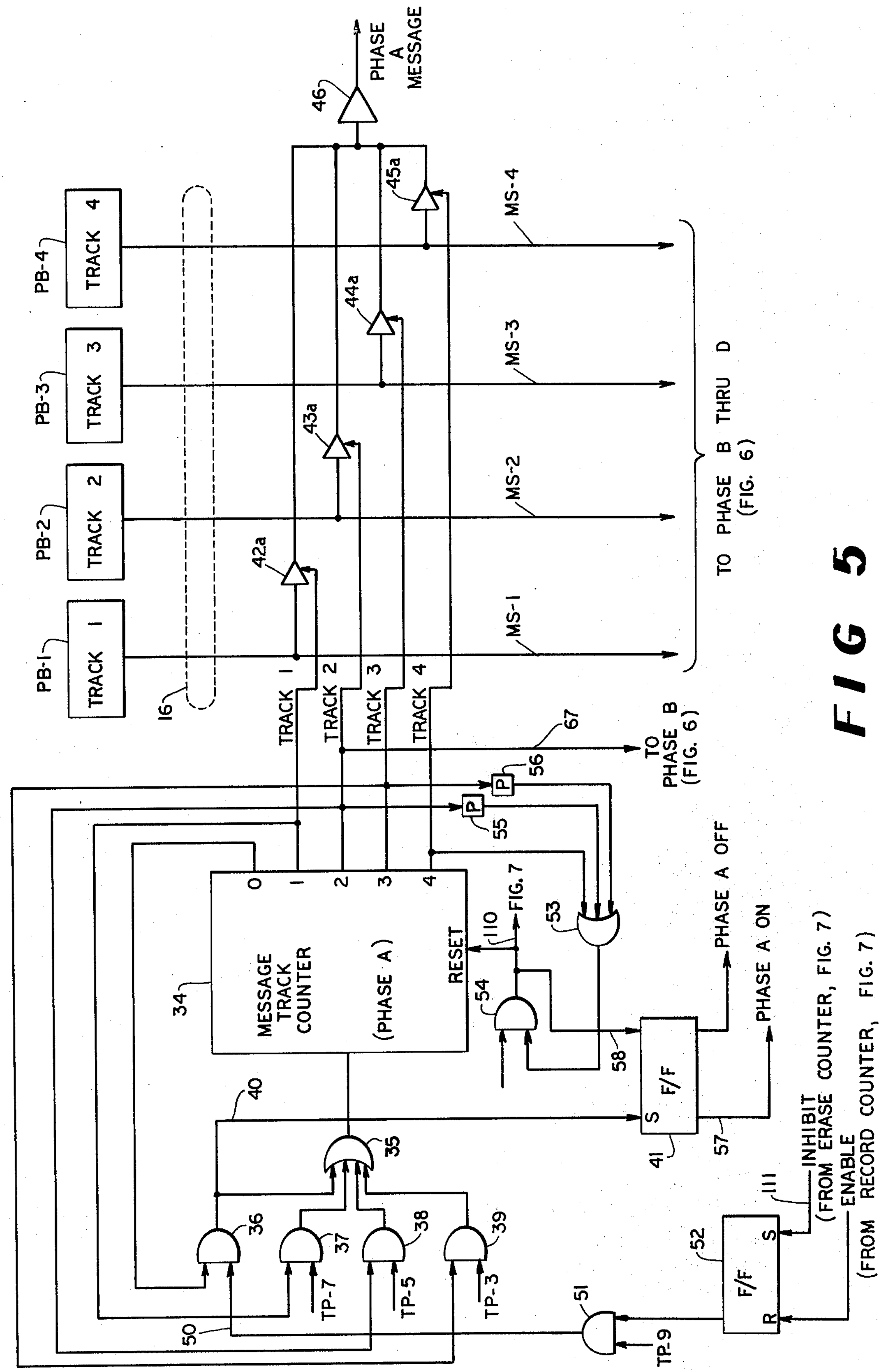

PB-1
TRACK 1
PB-2
TRACK 2
PB-3
TRACK 3
PB-4
TRACK 4
16
42a
43a
44a
45a
46
PHASE A MESSAGE
MS-1
MS-2
MS-3
MS-4
TO PHASE B THRU D (FIG. 6)
TRACK 1
TRACK 2
TRACK 3
TRACK 4
67
TO PHASE B (FIG. 6)
P
55
P
56
53
110
FIG. 7
RESET
34
MESSAGE TRACK COUNTER
(PHASE A)
0
1
2
3
4
54
58
F/F
S
41
57
PHASE A OFF
PHASE A ON
40
35
36
37
38
39
TP-7
TP-5
TP-3
50
51
TP-9
52
F/F
S
R
111
INHIBIT (FROM ERASE COUNTER, FIG. 7)
ENABLE (FROM RECORD COUNTER, FIG. 7)

FIG 5

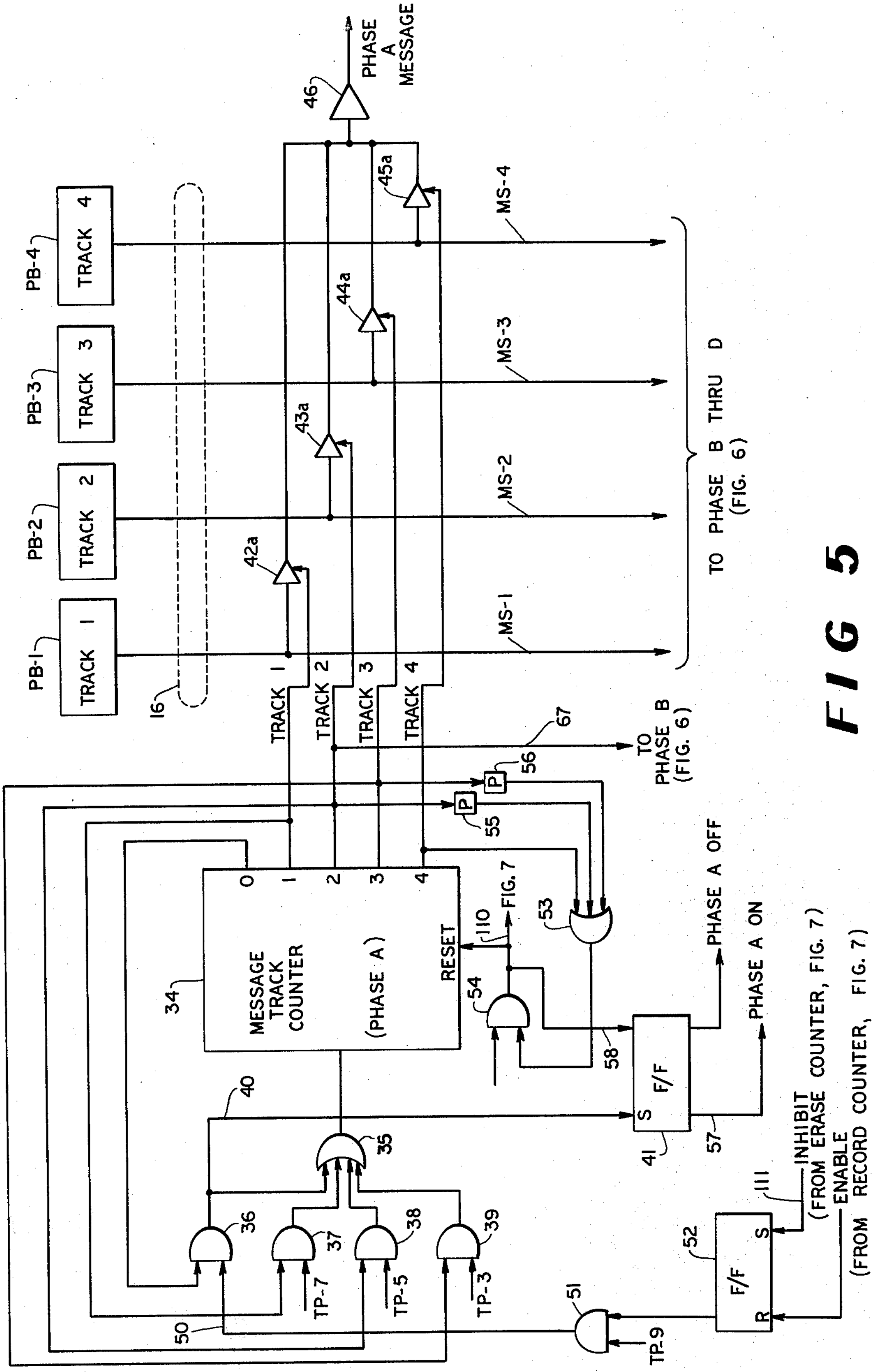

TRACK 1
TRACK 2
TRACK 3
TRACK 4
PB-1
PB-2
PB-3
PB-4
16
42a
43a
44a
45a
46
PHASE A MESSAGE
MS-1
MS-2
MS-3
MS-4
TO PHASE B THRU D (FIG. 6)
MESSAGE TRACK COUNTER (PHASE A)
34
0
1
2
3
4
RESET
110
FIG. 7
TO PHASE B (FIG. 6)
67
55
56
P
53
54
58
F/F
S
41
57
PHASE A OFF
PHASE A ON
40
35
36
37
38
39
TP-7
TP-5
TP-3
50
51
TP-9
52
R
111
INHIBIT (FROM ERASE COUNTER, FIG. 7)
ENABLE (FROM RECORD COUNTER, FIG. 7)

FIG 5

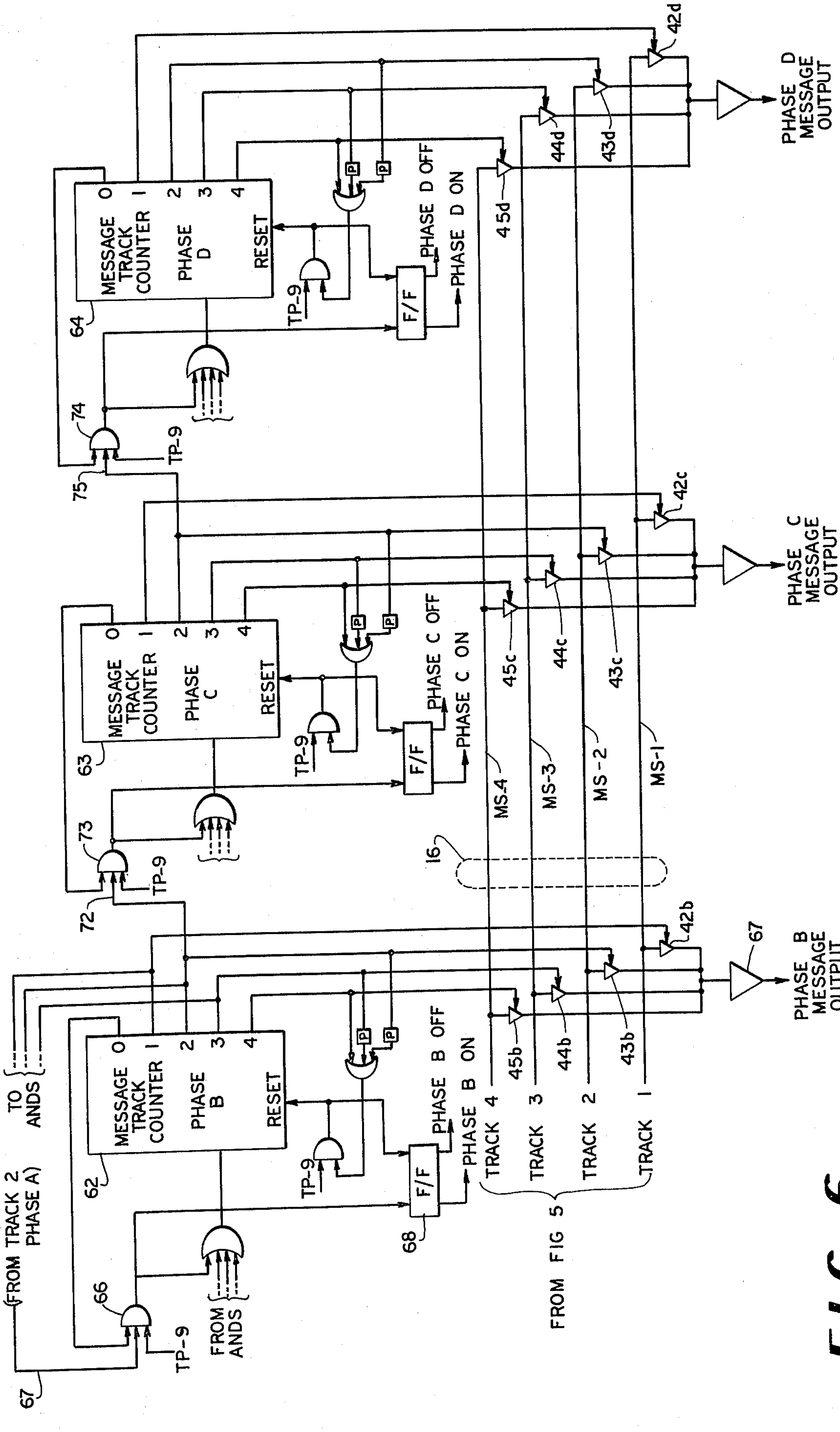

MESSAGE TRACK COUNTER PHASE B
MESSAGE TRACK COUNTER PHASE C
MESSAGE TRACK COUNTER PHASE D
RESET
0 1 2 3 4
F/F
PHASE B OFF
PHASE B ON
PHASE C OFF
PHASE C ON
PHASE D OFF
PHASE D ON
TP-9
P
FROM ANDS
TO ANDS
(FROM TRACK 2 PHASE A)
FROM FIG 5
TRACK 4
TRACK 3
TRACK 2
TRACK 1
MS-4
MS-3
MS-2
MS-1
PHASE B MESSAGE OUTPUT
PHASE C MESSAGE OUTPUT
PHASE D MESSAGE OUTPUT
16
42b
43b
44b
45b
42c
43c
44c
45c
42d
43d
44d
45d
62
63
64
66
67
68
72
73
74
75

FIG 6

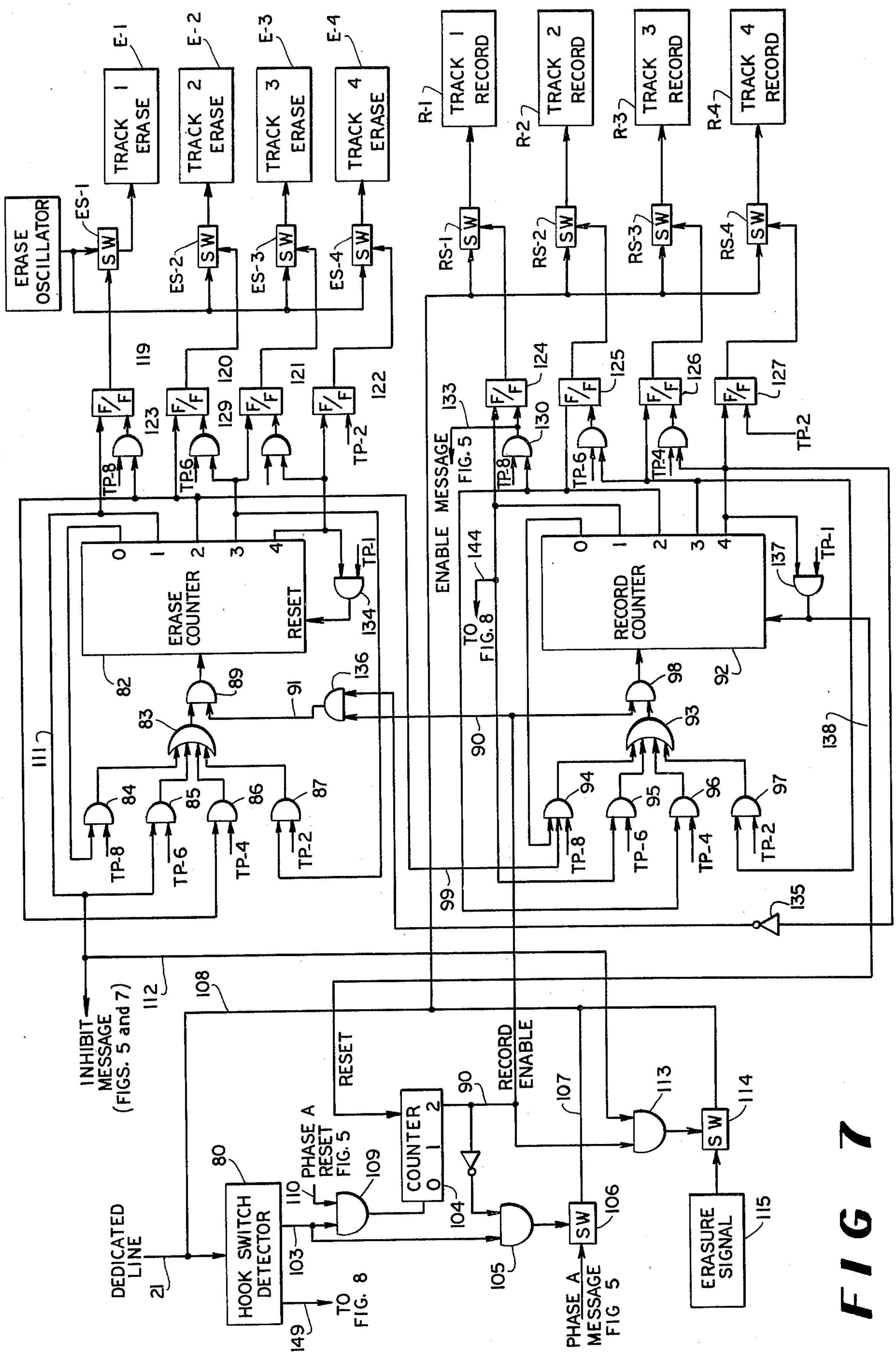

ERASE OSCILLATOR
ES-1
SW
ES-2
ES-3
ES-4
TRACK 1 ERASE
TRACK 2 ERASE
TRACK 3 ERASE
TRACK 4 ERASE
E-1
E-2
E-3
E-4
TRACK 1 RECORD
TRACK 2 RECORD
TRACK 3 RECORD
TRACK 4 RECORD
R-1
R-2
R-3
R-4
RS-1
RS-2
RS-3
RS-4
F/F
119
120
121
122
123
129
124
125
126
127
130
133
ENABLE MESSAGE FIG. 5
TP-8
TP-6
TP-4
TP-2
TP-1
ERASE COUNTER
RESET
0 1 2 3 4
82
83
84
85
86
87
89
91
134
136
111
RECORD COUNTER
92
93
94
95
96
97
98
90
99
137
138
135
144
TO FIG. 8
INHIBIT MESSAGE (FIGS. 5 and 7)
112
108
DEDICATED LINE
21
HOOK SWITCH DETECTOR
80
103
149
110
PHASE A RESET FIG. 5
109
COUNTER
RESET
104
105
106
107
PHASE A MESSAGE FIG 5
RECORD ENABLE
113
114
ERASURE SIGNAL
115

FIG 7

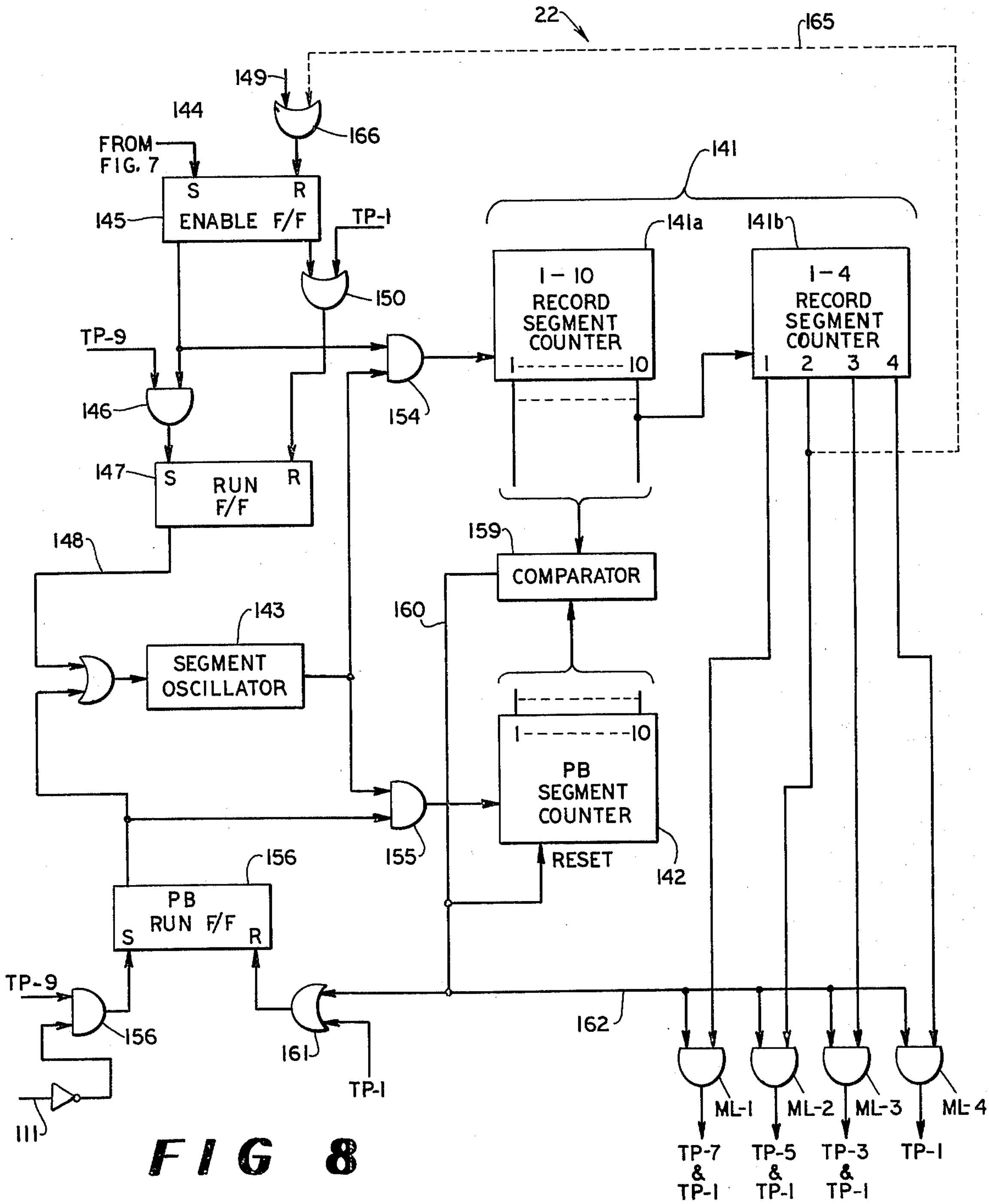

22
165
149
144
166
FROM FIG. 7
S R
145 ENABLE F/F
TP-1
141
141a
141b
150
1 – 10 RECORD SEGMENT COUNTER
1 – 4 RECORD SEGMENT COUNTER
1 2 3 4
TP-9
154
146
147 S RUN F/F R
148
159
COMPARATOR
143
160
SEGMENT OSCILLATOR
1 10
PB SEGMENT COUNTER
155
RESET
142
156
PB RUN F/F
S R
TP-9
156
161
162
TP-1
111
ML-1 ML-2 ML-3 ML-4
TP-7 & TP-1
TP-5 & TP-1
TP-3 & TP-1
TP-1

FIG 8

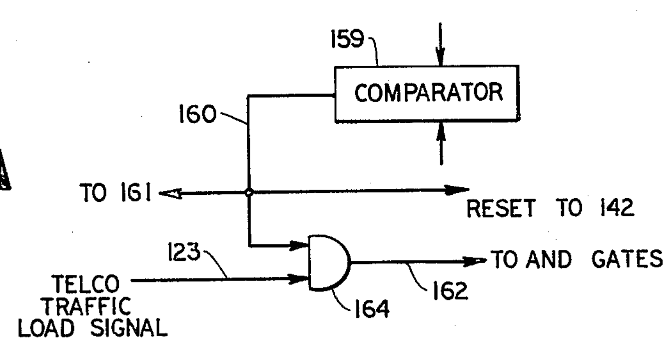

159
COMPARATOR
160
TO 161
RESET TO 142
123
TO AND GATES
TELCO TRAFFIC LOAD SIGNAL
162
164

FIG 8A

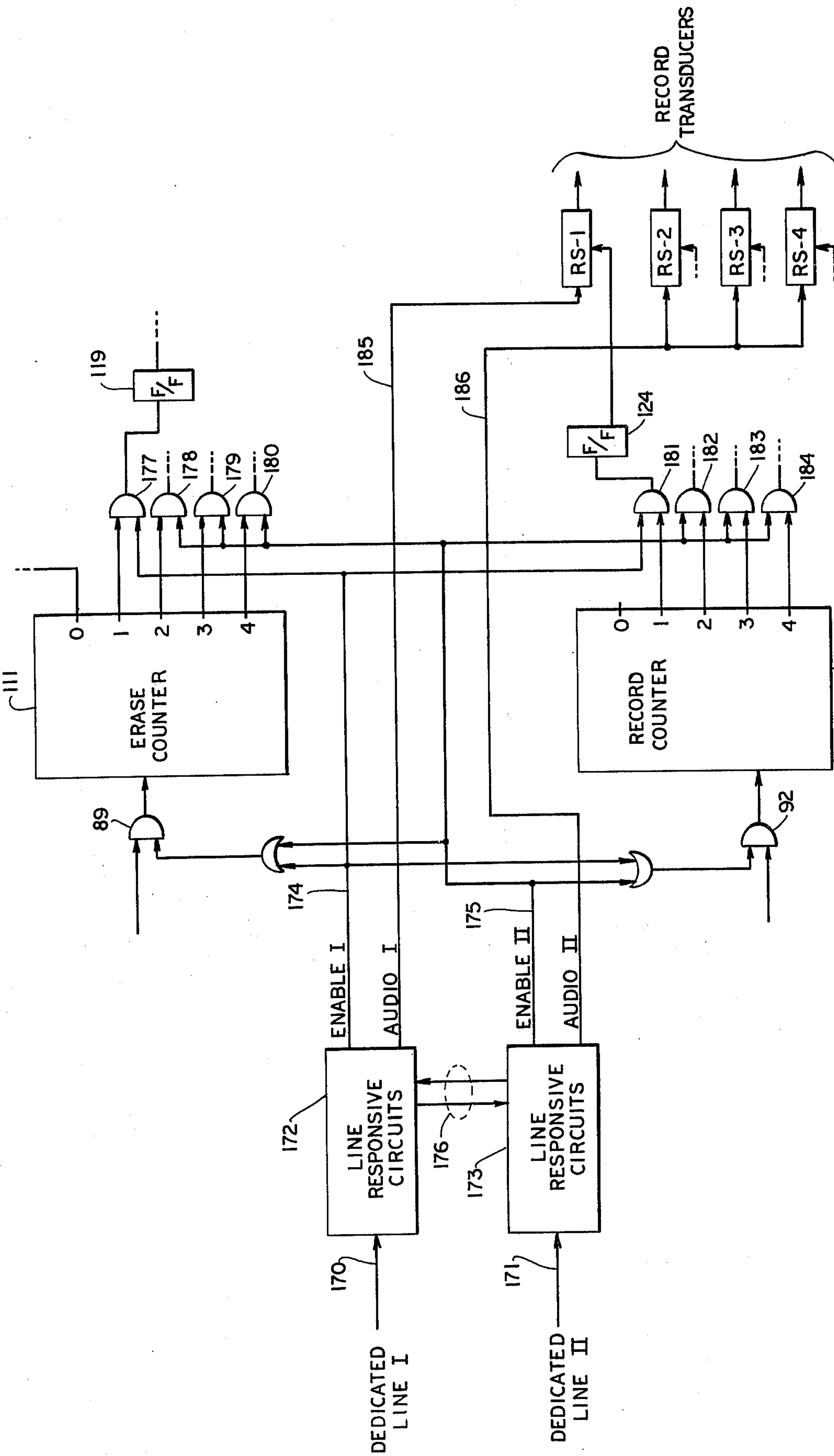

RECORD TRANSDUCERS
RS-1
RS-2
RS-3
RS-4
119
F/F
185
186
124
F/F
177
178
179
180
181
182
183
184
0
1
2
3
4
ERASE COUNTER
111
0
1
2
3
4
RECORD COUNTER
92
89
92
174
175
ENABLE I
AUDIO I
ENABLE II
AUDIO II
LINE RESPONSIVE CIRCUITS
172
LINE RESPONSIVE CIRCUITS
173
176
170
171
DEDICATED LINE I
DEDICATED LINE II

FIG 9

MESSAGE ANNOUNCEMENT APPARATUS AND METHOD

This invention relates in general to a system for delivering message announcements, and more particularly relates to apparatus and method for providing repetitive delivery of recorded messages of a general nature.

Various types of message announcement systems, machines, and methods are known in the prior art. Message announcement apparatus, as the term is used herein, refers generally to apparatus which repetitively delivers one or more messages which have previously been recorded on a recording medium associated with the apparatus. Various types of apparatus for delivering recorded message announcements are frequently used in conjunction with telephone subscriber circuits, so that anyone dialing a certain telephone number is connected by the telephone central office switching equipment to a subscriber trunk to receive the recorded announcement.

Those skilled in the art will recognize that such message announcement apparatus may be used in association with a number of telephone trunk circuits, and that more than one calling party may be concurrently connected to receive a particular delivered message from the message announcement apparatus.

The message delivery apparatus of the prior art has generally been designed either for the delivery of specialized types of messages (e.g., time-of-day, or weather), or for the delivery of general-purpose messages. It should be understood that a general-purpose message announcement apparatus is readily usable to deliver a recorded message pertaining to weather conditions, for example, and that special-purpose weather announcement apparatus refers to apparatus of the kind which may have preprogrammed announcement segments corresponding to predetermined types of weather forecast conditions. While the general-purpose message announcement apparatus of the prior art is satisfactory for some applications, the cost and/or alternative operating limitations of the equipment has tended to limit the acceptance and general utility of such equipment. The general-purpose message announcing systems of the prior art have generally involved a compromise between cost and features such as maximum message length and various accessory features, with extended message length being available only on equipment which has been too expensive for many potential users.

It has been proposed in the art to provide a message announcement by serially delivering several message segments, so that the message segments could be received as a composite message consisting of the segments. Because of the precise timing required to switch from the end of a message segment to the beginning of the next segment, each message segment was required to contain a complete sentence or other message portion; a unitary message longer than the length of a single message segment could not be delivered with acceptable clarity and absence of noise during transfer between message segments.

Accordingly, it is an object of the present invention to provide an improved message announcement system.

It is another object of the present invention to provide an apparatus and method for providing a composite message by the serial delivery of concurrent message segments.

It is another object of the present invention to provide apparatus and method for substantially noisefree serial delivery of composite message segments which may include noise at the ends of the message segments.

Still another object of the present invention is to provide message announcement apparatus and method for recording and subsequently delivering messages of variable length.

Other objects and attendant advantages of the present invention will become apparent from the following description of a preferred embodiment thereof, including the drawings wherein:

FIG. 1 is a block diagram showing the operative interrelation of components of a message announcement system according to the disclosed embodiment of the present invention;

FIG. 2 shows a schematic representation of the individual message segments and corresponding timing pulses associated with the disclosed embodiment;

FIG. 3 shows a schematic diagram of apparatus for generating the timing pulses utilized in the disclosed embodiment;

FIG. 4 shows the timing relationship between the several timing pulses provided by the disclosed embodiment of the invention;

FIG. 5 is a schematic diagram showing the message playback apparatus for delivering a single message announcement phase, according to the disclosed embodiment;

FIG. 6 is a schematic diagram of apparatus for providing additional message announcement phases according to the disclosed embodiment;

FIG. 7 is a schematic diagram of the erase and record control apparatus according to the disclosed embodiment;

FIG. 8 is a schematic diagram of the message length control portion of the disclosed embodiment;

FIG. 8A is a schematic diagram of an alternative embodiment of message length control apparatus; and

FIG. 9 is a schematic diagram of apparatus for recording selected portions of a composite message from different message sources, according to an alternative embodiment of the present message system.

Stated in general terms, the system of the present invention provides a multiple number of individual message segments that are available for recording a composite message of maximum length approximately equal to the summation of the individual message segment lengths. Each message segment may be provided on a separate message track of a common recording medium, so that playback of the several individual message segments occurs concurrently. A composite message is provided by serially delivering each of the message segments in predetermined sequence, and a number of separate identical messages or message phases that are mutually offset in time can be delivered with appropriate switching. A terminal portion of each message segment is recorded synchronously with an initial portion of the next message segment, so that serial switching between adjacent message tracks can occur at any point during the concurrent portions of the serial message segments. Timing means are provided which divide the message segments into a predetermined number of time intervals, and a memory means remembers the time interval corresponding with the end of a recorded message or predetermined message portion. Subsequent message playback can terminate at a count corresponding to the previously determined timing count stored in the memory means.

The foregoing and other aspects of the present invention are more readily understood with reference to the following description of the disclosed embodiment. The disclosed embodiment operationally comprises a number of separate subsystems as shown in FIG. 1. Individual message segments of some predetermined maximum duration are recorded and played back on multiple track message apparatus **15**, which can be any apparatus operable to provide repetitive playback of plural message segments in a predetermined time sequence. The message apparatus **15** in the disclosed embodiment is capable of recording and playing back a maximum of four separate message segments, with each individual message segment being identified hereinafter as "track **1**", "track **2**", and so on, and being provided on separate message segment track lines collectively denoted at **16** on FIG. **1**. The message apparatus **15** also operates to provide a periodic control signal at a predetermined point in each repetitive message delivery cycle; this periodic control signal, known hereafter as a control pulse "CP", is supplied along the line **17** to the timing pulse apparatus **18**.

A specific example of apparatus which may be utilized as the message apparatus **15** is found in U.S. Pat. No. 3,787,637, entitled "Announcing System." The announcing system of that patent has an endless belt recording medium and provides separate parallel message tracks on which can be recorded the separate message segments; the messages on each track of the recording belt are recorded, played, and erased with appropriate transducing heads associated with each track. A switch senses the passage of an indicium formed in the message belt, from which is established the control pulse CP corresponding to each revolution or message delivery cycle of the message belt. It will be understood by those skilled in the art that the present invention is not confined to a message apparatus as disclosed in the aforementioned U.S. Pat. No. 3,787,637, and that other announcing apparatus utilizing recording media such as drums, discs, or tapes may alternatively be provided. It is preferable, however, that the message apparatus **15** contain each of the separate message segments on a unitary recording medium, or that the apparatus alternatively provide for accurate synchronism between each and every message segment, for reasons which will become apparent hereinafter.

Each of the message segment track lines is supplied to the playback control apparatus **19**, which sequentially operates in a manner described below to select the message segments delivered on the individual message track and to provide separate identical composite messages which are identified as "phase A," "phase B," and so on. The composite messages are available for delivery to suitable message delivery circuits, which are typically interconnected with telephone central office switching equipment; details of such delivery circuits are known to those skilled in the art and need not be described herein.

The message segments on some or all of the individual message tracks of the message apparatus **15** can be erased and provided with newly recorded messages from the record control apparatus **20**, which may be connected to receive an incoming message dictated on a dedicated telephone line **21**. The record control apparatus provides both erase signals and new message signals to the message apparatus **15**.

The message length control apparatus **22**, which is interconnected with both the playback control apparatus **19** and the record control apparatus **20**, provides a memory function which remembers the maximum duration of the composite message recorded on the message apparatus **15**, and monitors the duration of each message playback cycle to terminate the playback cycle when the recorded message has been delivered. The message length control also can operate to terminate delivery of a shortened message at a predetermined intermediate point, in response to a traffic load signal condition on the line **23**.

Message Announcement Delivery

FIG. **2** is a schematic diagram showing the relative message delivery times of the four message segment tracks used in the disclosed illustrative embodiment. It will be realized by those skilled in the art that the use of four message tracks in the disclosed embodiment is only a matter of choice, and that the apparatus and method of the present invention is readily adaptable to a number of message segments either greater or less than four. The message segment tracks are depicted in FIG. **2** as concentric circles bearing the respective legends track **1**, track **2**, and so on. Each of the message segment tracks depicted in FIG. **2** may correspond with a particular track on a recording medium, such as the magnetic recording belt described in the aforementioned U.S. Pat. No. 3,787,637, and it will be understood that the total length of each of the four message segment tracks is preferably identical. Each of the message segment tracks has a maximum duration of 14 seconds, in a specific embodiment of the present invention.

A composite message announcement is provided by switching between the message segments at certain times during a switching period indicated at **26** on FIG. **2**. The switching period **26** is divided into nine timing pulses serially designated as TP-**1**, TP-**2**, . . . TP-**9**. The relative extent of the switching period **26** is graphically exaggerated in FIG. **2** for illustrative purposes; each timing pulse can have a duration in the order of 70 milliseconds, with the overall nine-pulse switching period **26** having a total duration of 630 milliseconds compared to the 14-second total length of each message segment track. The timing pulses are generated once for each repetitive delivery cycle of the message segments contained on the several tracks, and it is important that the switching period defined by the timing pulses consistently commence at the same predetermined time relative to the message segments recorded on the tracks. The timing pulses can be provided by a circuit as shown in FIG. **3**, where a timing pulse oscillator **27** operates in response to a control pulse (CP) trigger to provide consecutive 70-millisecond timing pulses on the nine separate outputs of the oscillator. The control pulse CP may be provided to the timing pulse oscillator **27** by a switch **28** which provides a control pulse once for each revolution of a message belt **29** (or other recording medium). It will be understood that the switch **28** is actuated by an indicium at a certain predetermined point in each cycle of the message belt **29**, and that the oscillator **27** operates in response to actuation of the switch to deliver the nine consecutive timing pulses.

The duration and relative occurrence of the several timing pulses are graphically depicted in FIG. 4. It will be seen that the duration of the control pulse need not be less than the duration of a timing pulse, since the timing pulse oscillator **27** of the disclosed embodiment commences operating in response to the leading edge of the control pulse provided in response to operation of the switch **28.** After the final timing pulse TP-9 is provided, the oscillator **27** awaits the next control pulse to commence another sequence of timing pulses.

The playback control portion of the disclosed embodiment is first described with respect to a typical delivery sequence of a composite message announcement. It is assumed in the following description of playback control that the composite message is divided into four message segments, and that each message segment has been recorded on a corresponding one of the four message segment tracks. The initial segment of the message is recorded on track **1**, commencing at a track location corresponding to timing pulse TP-**8** and progressing in the direction indicated by the arrow **30** in FIG. **2**. The message segment on track **1** thus starts at TP-**9** on an initial revolution of the recording medium, and terminates at TP-**8** at the next revolution of the message belt. The next segment of the composite message is contained on track **2**, commencing at TP-**6.** For the two-pulse interval extending between TP-**6** and TP-**8**, an identical message portion is recorded on track **1** and track **2**; that is, the terminal portion of the message on track **1**, extending from TP-**6** to TP-**8**, is identical in content and timing with the initial portion of the message segment on track **2**, commencing at TP-**6**

The message segment on track **2** has a possible duration extending to TP-**6** of the next or third revolution of the message belt. The message segment on track **3** commences at TP-**4**, however, with the identical message portion being on track **2** and track **3** for the two-pulse interval commencing at TP-4 and ending at TP-**6.** In a similar manner, the recorded message segment on track **3** extends from TP-4 to TP-4 of the next revolution, and the message segment on track **4** commences at TP-**2** with an overlap of two timing pulses between the start of the track **4** message segment and the termination of the track **3** message segment.

It is thus seen that there is an interval of message segment overlap between each of the consecutive message segments recorded on the message belt or other recording medium. Each of the message segments is repetitively delivered by rotation of the message belt relative to a separate transducer head associated with a corresponding message track. Since the identical message portion is contained on track **1** and track **2** for the interval between TP-**6** and TP-**8**, it will be seen that the message announcement circuit can be switched from track **1** to track **2** at any time during the interval of concurrent delivery, without requiring switching between message segments at a precisely predetermined time. Since the message segments recorded on the several tracks not infrequently include unwanted noise at the beginning and end of each recorded message segment, arising from such transient recording conditions as signal switching, raising and lowering of recording heads, and the like, it will be seen that switching between consecutive message segments preferably occurs, during the identical message, at a time when the following message segment (on track **2**, for example) has already commenced but before the ending message segment (on track **1**, for example) terminates. It is thus seen that delivery of a composite message announcement is accomplished by serial sequential playback of the message segments which are individually delivered in substantial parallelism.

An embodiment of playback control apparatus for compiling one phase of a composite message consisting of the several message segments is shown in FIG. **5.** It is assumed for the illustrative embodiment that there is a separate message playback transducer corresponding to each of the four message segment tracks; these separate transducers are designated on FIG. **5** as PB-**1**, PB-**2**, PB-**3**, and PB-**4**. Each of the four playback transducers repetitively delivers a message segment signal, corresponding to the message segment recorded on the corresponding message track, to a separate message segment track line MS-**1**, MS-**2**, MS-**3**, and MS-**4**. The message segment track lines extend to the multiple announcement phase apparatus shown in FIG. **6** and described in further detail hereinbelow. The playback apparatus depicted in FIG. **5** delivers a composite message known as the phase A message.

The playback control apparatus for phase A includes a message track counter **34** in the form of a shift register having at least one output position in excess of the total number of message segment tracks. The message track counter **34** receives shift signals from the OR gate **35**, which provides a shift signal in response to an input from any one of the AND gates **36, 37, 38,** and **39.** The output from AND gate **36** is also supplied along the line **40** to the set input of a flip-flop **41**, for a purpose described hereinafter.

The output line **1** of the message track counter **34** is connected to gate the message segment amplifier **42A** which receives a message input from the message segment line MS-**1**. The output lines **2, 3,** and **4** of the message track counter **34** are correspondingly connected to gate the message segment amplifiers **43A, 44A,** and **45A**, respectively connected to receive the message segments delivered on tracks **2, 3,** and **4.** Each of the message segment amplifiers **42A-45A** is turned on by the respective outputs of the counter **34** to connect the corresponding message segment line to the emplifier **46**, the output of which provides the phase A composite message for any suitable message delivery circuit.

The AND gate **36** is connected to receive the signal on the "zero" output line of the message track counter **34**, and is also connected through the line **50** to receive an input whenever the timing pulse TP-**9** is present, assuming that the AND gate **51** is also receiving an appropriate input from the inhibit flip-flop **52.** The AND gate **37** is connected to output line **1** of the counter **34**, and TP-7. The AND gate **38** is connected to the output line **2** of the counter **34**, and TP-**5.** Finally, the AND gate **38** is connected to output line **3** of the counter **34**, and TP-3.

A typical playback sequence for a complete composite message is now described, with the assumption that the message track counter **34** has been previously reset to provide a signal at the zero output line and that a control pulse condition is applied by the switch **28** to the timing pulse generator **27** to initiate delivery of a train of timing pulses. Only the AND gate **36**, of the AND gate **36-39**, is receiving an input signal from the message track counter **34** at this time, and so the counter first receives a shift pulse at TP-**9.** The message track counter **34** shifts to provide a signal on output line 1, gating on the message segment amplifier 42A and allowing the start on the track 1 message segment to be delivered to the message amplifier 46. None of the other message segment amplifiers 43A-45A is gated on at this time, and so the message segments on the other three tracks are not supplied to the phase A message amplifier 46 at this time.

When the message track counter 34 shifted to its line 1 output, the signal on message track counter line zero was removed from the AND gate 36 and the line 1 signal was supplied to the AND gate 37. Delivery of the first message segment continues as the message belt 29 moves past the playback heads until the switch 28 again triggers the timing pulse generator 27 to provide another train of timing pulses. The message track counter is shifted to output line 2 in response to TP-7 applied to AND gate 37, the only one of the four AND gates 36–39 presently receiving an enabling output signal from the message track counter. When the counter 34 switches from output line 1 to output line 2, the message segment amplifier 42A is gated off and the message segment amplifier 43A is concurrently gated on. Referring again to FIG. 2, it will be seen that the transfer from delivery of the track 1 message segment to delivery of the track 2 message segment occurred at TP-7, or midway in the period of identical-message overlap of track 1 and track 2. It will be seen, accordingly, that the aforementioned message changeover occurred after any start-up noise associated with the beginning message on track 2, but before the occurrence of any noise associated with the termination of the recorded message on track 1.

Shifting of the message track counter 34 to the output line 2 causes the AND gate 38 to receive an enabling input, and it will be understood that the message track counter is next shifted in response to TP-5 of the next train of timing pulses. Shifting of the message track counter to the output line 3, occuring at TP-5, causes message segment transfer from track 2 to track 3 at the midpoint of the concurrent-message portion of such tracks. The signal on the output line 3 of the message track counter 34 is applied as an enabling input to the AND gate 39, so that TP-3 of the next-occurring train of timing pulses causes the message track counter 34 to shift to output line 4 at the midpoint of the concurrent-message overlap of tracks 3 and 4.

The output line 4 signal from the message track counter 34 is also supplied as an input to the OR gate 53, thereby enabling the reset AND gate 54. The OR gate 53 is also connected to receive signals from the track output lines 2 and 3 of the message track counter 34, through momentary pulse circuits 55 and 56; at no time presently considered, however, has the OR gate 53 operated to provide a logic input to the reset AND gate 54 concurrent with occurrence of a timing pulse TP-1. The pulse circuits 55 and 56 are any suitable circuits which provide a momentary pulse in response to a steady-state input, and it will be understood that a conventional RC circuit can be so utilized.

Delivery of the fourth and final message segment continues until occurrence of the first timing pulse TP-1 of the next train of timing pulses, whereupon TP-1 applied to the reset AND gate 54 along with the output from the OR gate 53 applied a reset pulse to reset the message track counter 34 to output zero. The message segment amplifier 45A is gated off at this time, the AND gate 36 is again supplied with an enabling signal from the output line zero of the message track counter 34, and the counter 34 is again ready to be shifted to output line 1 in response to TP-7 of the same timing pulse train which initiated reset of the counter 34. The flip-slop 41 is set by an output on the line 40, at the same time that the message track counter 34 is shifted to track 1 and the phase A message delivery commences. This set output of the flip-flop 41 remains on the output line 57 from the flip-flop during delivery of the entire phase A composite message, and the set signal from the flip-flop may be used to initiate switching of announcement-receiving circuits or for any other appropriate purpose. The flip-flop 41 is reset by the counter reset signal supplied along the line 58, concurrent with reset of the message track counter to the zero output line, thus signaling that the delivery of the complete phase A composite message is ended.

It is seen from the foregoing that the delivery of a complete composite message occurs over four complete revolutions of the message belt 29, so that a composite message having a miximum length of four times the length of the message segments is available. In the case of 14-second message segments, accordingly, it is possible to provide an uninterrupted unitary composite message of up to approximately 56 seconds, without interruption or pauses in message delivery at the several transfers between message segments.

Since each individual message track is utilized only once during delivery of a complete composite message, additional composite message phases may be provided utilizing the same message apparatus 15 and timing pulse apparatus 18 used for the phase A message. The apparatus for providing three additional phases of composite messages is shown on FIG. 6, and includes separate message track counters 62, 63, and 64 corresponding with each of the additional phases B, C, and D. Each of the message track counters 62, 63, and 64 can be provided by a five-position shift register in the manner of the message track counter 34 for phase A, with output lines 1 through 4 gating message segment amplifiers for corresponding message tracks and with a zero output line supplied to enable an AND gate which is also responsive to timing pulse TP-9.

The phase B message track counter 62 receives shift inputs through the OR gate 65, which receives inputs from four AND gates corresponding (except as noted below) in function and in inputs to the AND gates 36-39 associated with phase A. Only the AND gate 66 which receives timing pulse TP-9 is shown in FIG. 6, however, since that AND gate also receives an enabling input along the line 67, supplied from output line 2 of the phase A message track counter 34.

A typical playback sequence for phase B is now considered, with the phase B message track counter 62 assumed to be reset to provide an output signal on the zero output line. It is also assumed at this time that the phase A message track counter 34 is also reset to provide an output signal at its zero output line, so that the next-occurring timing pulse TP-9 shifts the phase A message track counter 34 to the output line 1. The phase B message counter 62 cannot shift at this time, however, since the absence of an enabling logic signal on line 67 to the AND gate 66 prevented TP-9 from shifting the phase B counter 62. After the track 1 message segment is delivered in phase A, the phase A message track counter 34 is shifted to output line 2 in response to timing pulse TP-7. The signal on output line

2 of counter **34** is immediately applied along line **67** to enable the AND gate **66,** so that the following timing pulse TP-9 causes the phase B message track counter **62** to shift to its output line **1.** The message segment amplifier 42B is gated on at this time, allowing the track **1** message segment signal on the message segment line **MS-1** to be supplied to the phase B message amplifier **67.** The phase B message counter **62** is stepped through the three remaining track outputs, in a manner identical to the operation of the phase A message track counter **34** described above, and the phase B message track counter is reset to zero at the end of the track **4** message segment in the manner described above with respect to phase A. The flip-flop **68** is set and reset at the beginning and the end, respectively, of the phase B composite message for use in message announcement switching circuitry as required.

It will now be understood that the phase B composite message lags behind the phase A message by one repetitive message delivery cycle of the message belt **29,** since the phase B message track counter **62** is enabled to shift to its output line **1** only after the phase A message track counter **34** has shifted to its output line **2.** The phase C message track counter **63** similarly lags one cycle behind the composite message pf phase B, inasmuch as an enabling signal supplied on line **72** from output line **2** of the phase B message track counter is required to enable the AND gate **73** to shift the phase C message track counter **63** to its track **1** output, at timing pulse **TP-9.**

The phase D message track counter **64** likewise lags one cycle behind the phase C composite message, inasmuch as the AND gate **74** must receive an enabling signal on line **75** from output line **2** of thhe phase C message track counter **63** before the phase D message track counter can shift to its output line **1** in response to a timing pulse **TP-9.**

It is apparent from the foregoing description that the disclosed embodiment of apparatus as depicted in FIGS. **5** and **6** delivers a composite message for each repetitive operating cycle of the message apparatus **15.** The provision of multiple announcement phases allows persons awaiting delivery of a complete message totaling, for example, 56 seconds duration, to wait for maximum of 14 seconds before being connected to receive a complete composite message. The four-phase system in the disclosed embodiment thus provides an average waiting time of 7 seconds for connection to the commencement of a complete composite message, so that listeners need not be subjected to prolonged waiting times or to annoying "barge-in" connection with an ongoing message.

Change of Recorded Message

Although the composite message available for delivery from the message belt **29** can be changed from time to time by substituting a new message belt in the message apparatus **15,** many users of the present message announcement equipment prefer the convenience of the direct message changing capability provided by the present apparatus and shown with regard to FIG. **7** of the disclosed embodiment. A private message line is preferably made available for delivering the new message to the apparatus, and the private line may preferably be the aforementioned dedicated telephone line **21** which is connected to the present apparatus so that hookswitch signaling is available. The dedicated line **21** is connected to hook-switch detector apparatus **80** which provides output signal conditions as described below in response to the on-hook or off-hook status of the dedicated line.

Since the entire existing message recorded on each of the message segment tracks must be initially erased before a new message can be recorded, each message track on the message belt **29** is provided with a separate erase head **E-1, E-2, E-3,** and **E-4.** Each of the erase heads is selectively connectable to a suitable erase signal provided by the erase oscillator **81,** upon closure of the corresponding erase switches **ES-1, ES-2, ES-3,** and **ES-4.** Each message segment track is also associated with a separate record transducer **R-1, R-2, R-3,** and **R-4.** Those skilled in the art of magnetic recording will realize that the functions of playback and record are frequently combined in a single transducer head, and so the aforementioned record transducers can in fact be provided by the playback transducers **PB-1. . .PB-4** depicted in FIG. **5.** It will be understood that suitable switching will, in such case, be required to isolate the incoming message signals during the record operation, from the message segment lines normally connected with the transducers during playback operation.

Control of message erasure is provided by the erase counter **82,** which may be provided by a five-position shift register similar to the aforementioned message track counters. The shift input of the erase counter **82** is provided from the OR gate **83,** which receives output signals from each of the two-input AND gates **84, 85,** 86, and **87.** The four AND gates **84–87** are respectively connected to receive an input from each of output lines **1–4** of the erase counter **82,** in the manner described above with respect to the message track counters. The AND gate **84** also receives timing pulse **TP-8,** while the gates **85, 86,** and **87** are respectively connected to receive timing pulses **TP-6, TP-4,** and **TP-2.** Although the erase operation is described in detail below, it will be apparent that the erase counter **82** sequentially shifts through its five output lines in response to occurrence of the appropriate timing pulse inputs to an AND gate **84-87** which is also receiving the proper enabling input from the erase counter. Each output signal from the OR gate **83** is supplied through the AND gate **89** to shift the erase counter **82,** provided that the AND gate **89** is concurrently receiving an enabling signal on the line **91** as described below.

Recording of new message segments on the several tracks is accomplished at the control of the record counter **92,** which may also be a five-position shift register. The record counter **92** is shifted in response to signals applied through the OR gate **93** from one of the four AND gates **94, 95, 96,** and **97,** provided that the shift signal from the OR gate **93** is not inhibited by the absence of a record enable signal supplied by the line **90** to the AND gate **98.** Each of the AND gates **94–97** is respectively connected to receive signals on the output lines **1–4** of the record counter **92,** and each of such AND gates is also respectively connected to receive timing pulses **TP-8, TP-6, TP-4,** and **TP-2.** The AND gate **94** is a 3-input gate, the third input of which is connected by the line **99** to output line **2** of the erase counter **82.** It will thus be seen that operation of the record counter **92** is inhibited until the erase counter **82** is shifted to provide an output on output line **2.**

The remainder of the erase-record structure depicted in FIG. **7** is described in connection with the description of a typical sequence of events involved in placing a new message on the apparatus. As long as the dedicated line **21** remains on-hook, the absence of an output signal on the line **103** from the hook-switch detector **80** prevents the cycle counter **104** from receiving shift pulses, so that the record enable line **90** remains in a logic state to inhibit the AND gates **136** and connected to the shift input of the erase counter **82**, and the AND gate **89**, **98**, connected to the record counter **92**. The erase switches ES-1 through ES-4, as well as the record switches RS-1 through RS-4 connected to the record transducers, are all gated off at this time, as will be understood below, and the erase-record apparatus is thus inhibited from functioning. Message playback continues at this time, in the manner described above.

Assume now that the dedicated line **21** becomes off-hook, indicating that a person desires to dictate a new message on the dedicated line for substitution with the present message recorded on the message apparatus **15**. In response to off-hook status, the hook switch detector **80** places a logic signal on the line **103** which combines in the AND gate **105** with the inverted absence of a record enable signal on the line **90** to gate on the playback-review switch **106**. The playback-review switch is connected to receive the phase A composite message (provided by the apparatus shown in FIG. 5) and supplies this message along lines **107** and **108** to the dedicated line **21**. The person listening on the dedicated line thus receives barge-in connection to listen to the phase A composite message. At the end of the phase A composite message, the AND gate **109** is enabled by the phase A reset signal supplied on the line **110**, thus providing a shift signal which shifts the 3-position cycle counter **104** from the "zero" position to the "one" position. The phase A composite message is then repeated in its entirety, in normal playback operation, so that the person listening on the dedicated line next hears a complete phase A message. At the end of the complete phase A message, the AND gate **109** is again enabled and the cycle counter **104** is shifted to its "two" position to provide a record enable signal on the line **90**. The inverted record enable signal immediately gates the switch **106** off, so that the dedicated line **21** no longer receives the phase A message. The record control apparatus is now ready to commencce the erase-record operation.

It will be recalled that the phase A reset signal was provided in response to timing pulse TP-1; timing pulse TP-8 of the same train of timing pulses causes the AND gate **84** to provide a shift pulse shifting the erase counter **82** from the zero output line to output line **1**. Output line 1 of erase counter **82** is applied on line **111** to set the inhibit flip-flop **52** (FIG. 5), thereby removing an input from the AND gate **51** and inhibiting the operation of the phase A message track counter **34**. Since the phase B message is inhibited from starting until after track 1 of the phase A message is completed, it is seen that the inhibit signal on the line **111** effectively inhibits all message delivery phases. The inhibit signal on line **111** is also applied along line **112** to the AND gate **113**, causing the switch **114** to be gated on and connecting the dedicated line **21** with an erase signal tone **115**, thus advising the person listening on the dedicated line that message segment track **1** is being erased. The listening person is advised by the commencement of the erase signal tone that he has 14 seconds (the length of a message segment, in the disclosed embodiment) before he should commence dictating a new message.

When the erase counter **82** shifted to output line **1** at **TP-8**, the track **1** erase flip-flop **119** was set to provide a signal gating the erase switch **ES-1** to the closed position, allowing the erase transducer **E-1** to receive an erase signal from the oscillator **81**. The erasure of message track **1** thus commences at time **TP-8.**

The next train of timing pulses, produced after one complete cycle of the message belt **29**, causes the erase counter **82** to shift at **TP-6** to output line **2**, thereby setting the erase flip-flop **120** and gating closed the erase switch **ES-2** to commence erasing track **2**. Output **2** of the erase counter **82** is also connected to the AND gate **123** to enable the erase flip-flop **119** to be reset at **TP-8**, so that erasure of track **1** terminates two timing pulses after erasure of track **2** commences. It will be understood that overlapping erasure of contiguous message tracks is necessary to erase the overlapping message portions previously recorded thereon.

The inhibit signal was removed from the line **111** when the erase counter **82** shifted from output line **1** to output line **2**, with the result that the switch **142** is gated open and the erase signal tone is removed from the dedicated line **21**. The inhibit flip-flop **52** has not received a reset signal at this time, however, and so the message delivery phases remain inhibited from operation.

It will be recalled that the erase counter **82** shifted to position 2 at time **TP-6**, thereby placing an enable signal along the line **92** to the flip-flop **94** associated with the record counter **92**. At time **TP-8**, occurring two timing pulses later, the AND gate **94** provides a signal shifting the record counter **92** to the line one output position whereupon the record flip-flop **124** becomes set and gates the record switch **RS-1** closed. The track **1** record transducer **R-1** is now interconnected with the dedicated line **21** by means of the line **108** and the line **128**, so that any message dictated on the line **21** is now recorded on the first track of the message belt **29**.

At the conclusion of the message belt cycle during which track 2 is being erased and track 1 is being recorded, the erase counter **82** is shifted at time **TP-4** to output line **3**, setting the erase flip-flop **121** to gate erase signals through the erase switch **ES-3** to commence erasing track **3**, and also enabling the AND gate **129** to allow the track 2 erase flip-flop **120** to be reset in response to **TP-6**. Erasure of track 3 is thus commenced, and erasure of track 2 is terminated after another erase overlap of two timing pulses. The record counter **92** is shifted to output line 2 by the same **TP-6** that shifted the erase counter **82** to position **3**. The record flip-flop **125** is immediately set to gate the record switch **RS-2** closed so that the transducer **R-2** is receiving the message dictated on the dedicated line **21**. The track **1** record switch **RS-1** is opened two timing pulses later, when **TP-8** is applied through the AND gate **130** to reset the record flip-flop **124**. It will thus be understood that the dictated message is simultaneously recorded on track 1 and track 2 for the period of two timing pulses, commencing at TP-6 and ending at **TP-8**, providing the necessary portion of message segment overlap described above with regard to playback operation.

It will now be understood that the erase counter **82** and record counter **92** will be shifted in response to timing pulses generated at the end of subsequent cycles of the message belt **29**, so that each of the remaining message tracks is erased and is subsequently connected for recording the new message dictated on the dedicated line **21**. When the reset signal is supplied to the record flip-flop **124**, such signal is also supplied along the line **133** to reset the inhibit flip-flop **52** (FIG. **5**). The phase A message track counter **34** is now enabled to commence delivery of the newly-recorded track **1** message segment, thereby minimizing the total time that the massage announcement delivery function of the present apparatus is inoperative during new-message recording.

The erase operation is completed in response to timing pulse TP-**1** supplied to the AND gate **134** at the end of the message cycle after the erase counter **82** was shifted to output line **4**. The following timing pulse TP-**2** resets the erase flip-flop **122**, and concurrently shifts the record counter **92** to output line **4** so that recording of track **4** is enabled by the record flip-flop **127** and the record switch RS-**4**. The output line **4** signal from the record counter **92** is also supplied through an inverter **135** to inhibit the AND gate **136** associated with the shift input of the erase counter **82**, so that the erase counter is not shifted by the subsequently-occurring timing pulse TP-**8**. The last segment of the new message is now being recorded on message track **4**.

At the end of the next cycle of the message belt, the record counter **92** is reset in response to TP-**1** applied to the AND gate **137**, and the reset signal is also supplied along the line **138** to reset the cycle counter **104**. The entire erase-record cycle is now complete, and the person listening on the dedicated line **21** can remain on the line to receive playback of the newly-dictated composite message delivered on phase A. It will also be understood that, by remaining on the dedicated line **21** until the cycle counter **104** again shifts to position **2**, the previously-dictated composite message may be replaced by yet another message, should the dictator be dissatisfied with his previously dictated message.

Message Length Control

Although the above-described erase and recording apparatus makes available the entire length of the composite message to receive a new recorded message, the apparatus according to the present invention can also be used to record a message of duration which is less than the sum of the available message segments. Message length control is accomplished with the present invention by dividing the duration of each repetitive message segment into a number of time segments, providing a memory capability for counting and remembering the maximum time segment count when message recording is terminated, and then counting the segments during subsequent playback operations to determine when the playback time segment count equals the previously remembered record segment count. When the two segment counts are equal, the delivered message is completed and the message playback can be immediately reset to commence delivery of another composite message.

Message length control is provided in the disclosed embodiment with the apparatus shown in FIG. **8**, and including a record segment counter **141** and a playback segment counter **142**. The time of each complete operating cycle of the message belt **29**, excluding the switching period **26** occupied by the train of timing pulses, is divided into ten time segments of equal duration, in the disclosed embodiment, although a greater or lesser number of time segments may alternatively be chosen. Since the message belt **29** in the disclosed embodiment contains four message tracks, the record segment counter **141** must be capable of remembering the time segment count at which the recorded message terminates, as well as the particular message track. The record segment counter **141** thus includes a ten-segment counter **141*a*** and a four-segment counter **141*b***, with the shift input to the four-segment counter **141*b*** being connected to the ten-count output of the segment counter **141*a***.

Further details of the message length control apparatus shown in FIG. **8** are described along with the operating description which follows. The record segment counter **141** counts pulses selectively supplied by the record oscillator **143**, and the record oscillator of the disclosed embodiment operates at a rate providing ten output pulses during each message track cycle (excluding the 640-millisecond switching period **26**). Assuming that the record segment counter **141** is set to the zero-count state and a message recording operation is commencing, shifting of the record counter **92** to output line **1** (to initiate recording on track **1**) also provides an enable signal along the line **144** to set the enable flip-flop **145**, thereby applying an output signal to the AND gates **146** and **154**. The subsequently occurring timing pulse TP-**9** is also applied to the AND gate **146**, causing the run flip-flop **147** to become set. The set output of the run flip-flop is applied on the line **148** to turn on the record oscillator **143**, so that the ten-segment counter **141*a*** commences receiving and counting oscillator pulses immediately after termination of the timing pulse train which initiated recording of track **1**.

The ten-segment counter **141a** continues to count during recording of the new message on track **1**. Assuming that the new message is longer than the maximum length of track **1**, the ten-segment counter reaches the ten-count and shifts the four-segment counter **141*b*** to its two-count state, before the first timing pulse TP-**1** of the next pulse train occurs. TP-**1** resets the run flip-flop **147** to disable the record oscillator **143** during the ensuing timing pulse train, although it will be understood that message recording continues as described above. As soon as the final timing pulse TP-**9** of the pulse train is supplied to the AND gate **146**, however, the record oscillator **143** is again turned on and the ten-segment record counter **141*a*** again commences counting up to ten.

Assuming that the newly-recorded message is finished at time segment **4** occurring during the recording of the second track, the person dictating the new message will normally hang up the dedicated line **21**; the hook-switch detector **80** senses the on-hook condition and applies a hook switch interrupt signal on the line **149** to reset the enable flip-flop **145**, so that the run flip-flop **147** is reset through the OR gate **149**. The record segment counter **141** thereafter remains at the previously-attained count, with the ten-segment counter **141*a*** being at count four and with the four-segment counter **141*b*** being at count two.

When the subsequent delivery of the newly recorded message announcement commences at timing pulse TP-**9**, the playback run flip-flop **156** is set (in the inverted absence of an inhibit signal applied to the AND gate **156** on the line **111**) and the segment oscillator

143 commences delivering segment pulses through the AND gate 155 to the ten-count playback segment counter 142. A comparator circuit 159 receives the count signals from both of the ten-count counters 141*a* and 142, and provides a signal condition on the line 160 when the count on the playback segment counter 142 equals the previously remembered count on the record segment counter 141*a*. The count comparison signal on the line 160 is supplied through the OR gate 161 to reset the playback run flip-flop 156, and is also applied along the line 162 to each of the message-length AND gates ML-1, ML-2, ML-3, and ML-4. The message-length AND gates are also individually connected to receive the respective four output lines of the four-count segment counter 141b. The output of the message length gate ML-1 is supplied to the inputs TP-1 and TP-7 of the message track counters 34, 62, 63, and 64 associated with each of the four composite message phases. The message-length gate ML-2 similarly provides an output to the TP-5 and TP-1 inputs of the message track counters; the ML-3 gate supplies an input signal to each of the TP-3 and TP-1 input gates for the message track counters; and the message-length gate ML-4 supplies an input to the TP-1 gates of such message counters.

The occurrence of a count comparison signal on the line 160, coincident with the signal supplied to the message-length gate ML-2 from the two-count output of the segment counter 141b, applies a TP-5 pulse to the AND gate 38 and a TP-1 pulse to the AND gate 54 associated with the phase A playback apparatus depicted in FIG. 5. Since track 1 of the phase A composite message is currently being delivered, however, the phase A message track counter 34 is currently at output line 1 and the AND gate 38 is not receiving an enabling input necessary to shift the phase A message track counter in response to the TP-5 pulse from the message-length gate ML-2. Nothing happens at this time, accordingly, and delivery of the track 1 message segment continues.

At the end of track 1 message segment delivery, the phase A message track counter 34 is shifted to output line 2 as described above, so that the abbreviated message segment recorded on track 2 is now being delivered. The playback run flip-flop 156 is again set in response to TP-9, and the playback segment counter 142 (previously reset in response to the count comparison signal on the line 160) again commences counting in response to the segment oscillator 143. The count comparator 159 again provides a count comparison signal output on the line 160 when the playback and record counts are equal, and the message-length gate ML-2 again provides a TP-5 pulse and a TP-1 pulse to the phase A message track counter 34 (as well as to the three additional message track counters). Since the phase A message track counter 34 is currently at output line 2, indicating that the shortened track 2 message is being delivered, the AND gate 38 provides a shift pulse to the counter 34 and the counter 34 immediately shifts to output line 3. Output line 3 is supplied to the pulse circuit 56, which provides a momentary pulse through the OR gate 53 to the AND gate 54. It will be remembered that the AND gate 54 is already receiving a TP-1 signal from the message length gate ML-2, and so the phase A message track counter 34 is reset to the zero state. The phase A message track counter will shift to the track 1 state in response to the next-occurring timing pulse TP-9 from the timing pulse apparatus 18, whereupon delivery of a new phase A message commences.

It will be seen that the message length control apparatus shown in FIG. 8 provides a message length control signal to each of the four message phase counters, during each repetitive message delivery cycle of the message belt 29. The message length signal contains information of the time segment count and also of the track count in which the recorded message terminates, and only the one playback phase which is on the proper message track will be reset in response to the message length track control signal. Thus, a single message length apparatus as shown in FIG. 8 provides the message length control function for each of the four composite message phases in the disclosed apparatus.

A variation of the message length apparatus which permits a composite message to be divided into two predetermined parts is shown in FIG. 8A. It is desired in certain applications, such as with message announcement apparatus used in conjunction with telephone central office facilities, to deliver a composite message which normally has a first duration and which can be shortened when the telephone trunk circuits associated with the message announcement apparatus are all in use, or have reached a predetermined utilization factor. Referring to the erase-record apparatus shown in FIG. 7, assume that the person dictating a new message over the dedicated line 21 has finished dictating a first portion of a composite message. This first message portion might consist, for example, of a summary weather report. After he finishes the first message portion, the dictator momentarily depresses and then releases the hook switch on his telephone set. The two output lines 103 and 149 of the hook-switch detector 80 reacts differently to the momentary on-hook condition; the line 149 is immediately provided with an on-hook signal condition in immediate response to the hook-switch closure on the dedicated line 21, while the detector 80 provides the line 103 with a slow-release condition which ignores momentary hook-switch closure of less than a predetermined minimum duration.

The momentary hook-switch closure at the end of the first message portion, accordingly, provides a signal along the line 149 to reset the enable flip-flop 145, stopping the record segment counter 141 at a time segment and message track count corresponding to the time at the end of the first message portion. The line 103 from the hook-switch detector 80 does not receive an on-hook signal condition, in response to the momentary hook-switch operation, and so the erase-record operation continues.

A second message portion (for example, a detailed weather report) can be dictated on the remaining portion of the composite message length, and the recording operation is terminated in the conventional manner by hanging up the dedicated line 21.

FIG. 8A shows those portions of the message length apparatus of FIG. 8 that are modified to allow message length shortening only in response to a traffic load signal on a line 23 supplied from the telephone central office equipment. The apparatus necessary to generate traffic load utilization signals in response to a predetermined utilization of maximum available trunk capacity is known to those skilled in the art. The count comparison line 160 and the traffic load signal line 23 are both connected to the AND gate 164, so that the count comparison signal on the line 160 can be supplied to the line **162** only in the concurrent presence of an enabling traffic load signal on the line **23.** During each message playback cycle, a count comparison signal appears on the line **160** when the count of the playback segment counter **142** arrives at the previously determined count on the segment counter **141***a*, corresponding with the termination of the first message portion. The count comparison signal on the line **160** is prevented from appearing on the line **162,** in the absence of a traffic load signal condition on the line **23,** so that the message length gates ML-1,. . . ML-4 cannot provide the signals necessary to terminate message delivery in response to the count comparison signal. As soon as an appropriate traffic load signal condition is present on the line **23,** however, each message announcement provided by the apparatus will be terminated at the end of the previously selected first message portion. The traffic load-responsive shortening of message length reduces the holding time for each telephone trunk circuit, thereby reducing the overall trunk circuit load of the announcement apparatus and enabling a greater number of calling parties to receive the shortened message.

It is desired in some applications to limit the maximum possible shortened duration of a first message portion, so that the purpose of the traffic load-responsive message shortening system cannot be defeated by someone who dictates his entire message without a momentary hook-switch interruption. This maximum shortened duration function is illustrated in the present embodiment by the interconnection, shown in FIG. **8** at line **165,** between the OR gate **166** of the reset input for the enable flip-flop **145,** and a selected one of the output lines of the four-segment counter **141**b. If the line **165** is connected to the second output of the counter **141**b, for example, it will be seen that the signal condition appearing on this second output line upon termination of recording message track **2** is applied on the line **165** to reset the enable flip-flop **145,** thereupon terminating further operation of the segment oscillator **143** and the record segment counter **141.** The remainder of the new message is recorded on the remaining two message tracks. Subsequent playback of the new message occurs in the normal manner unless a traffic load signal is received on the line **23,** whereupon the count comparison signal occurring on the line **160** is gated onto the line **162;** this count comparison signal is gated through the message length gate ML-2 to terminate the message announcement at the end of message track **2** (28 seconds in the disclosed embodiment). It will be apparent that the line **165** could alternatively be connected to another one of the outputs from the four-segment counter **141**b, so as to define a different maximum length of the short message.

Multiple Recording Sources

The control logic of the present message announcement apparatus is readily adaptable to alternative erase-record control apparatus depicted in FIG. **9,** which is used in association with two separate dedicated lines to provide the capability of enabling a first message track (or group of tracks) to receive new messages only from a first dedicated line, while another message track (or group of tracks) can receive a new message from only a separate dedicated line. The embodiment shown in FIG. **9** may be useful, for example, where a first message track or tracks are intended to receive a commercial message and where the remaining message tracks are intended to receive a utility message such as a weather report or the like. The first tracks could thus be connected to receive incoming messages from a first dedicated line available to the sponsor of the message announcement service, while the remaining message trunks could be connected to receive incoming messages from a dedicated line available to the weather bureau.

Turning to FIG. **9,** the erase counter **111** and record counter **92** shown therein are identical with the corresponding elements shown in FIG. **7.** Moreover, counter shifting gates, erase logic, record logic, and other elements shown in FIG. **7** are understood to be similarly required for the necessary operation of the apparatus shown in FIG. **9,** but are omitted from FIG. **9** for clarity of illustration. The apparatus shown in FIG. **9** is essentially that apparatus which is required for erasing and recording of message track **1** in response to the first dedicated line **170,** and for erasing and recording on message tracks **2–4** in response to the second dedicated line **171.** Each of the dedicated lines **170** and **171** is connected to separate line responsive circuits **172** and **173,** which may be similar to the dedicated line circuitry shown in FIG. **7** and which provide enable logic conditions along the respective enable lines **174, 175** when the respective dedicated line is off-hook. The AND gates **89** and **98** associated with the shift inputs of the erase counter **111** and the record counter **92** are connected through OR gates to the two enable lines **174** and **175,** so that both the erase counter and the record counter are enabled when either of the dedicated lines is off-hook. It will be understood that it may be desirable to provide appropriate crossover control circuitry, schematically indicated at **176,** so that an off-hook condition of one dedicated line is effective to render the other dedicated line inoperative.

The interconnections between each of the erase counter output lines **1–4,** and the set inputs of the corresponding erase flip-flops, is interrupted by the respective AND gates **177, 178, 179** and **180.** The AND gate **177** is connected to the enable line **174** of the first dedicated line, while each of the AND gates **178-180** are connected to the enable line **175** associated with the second dedicated line.

The record counter output lines **1–4** are similarly interconnected with the corresponding flip-flops by the AND gates **181–184.** The AND gate **181** is connected to the enable line **174,** while the AND gates **182–184** are connected to the enable line **175.** The audio circuit of the first dedicated line **170** is connected by the line **185** to the record switch RS-**1** for the first message track, while the record switches associated with the remaining message tracks are connected by the line **186** to receive audio signals from the second dedicated line.

Considering the operation of the apparatus depicted in FIG. **9,** the erase counter **111** and the record counter **92** are enabled and operated in response to either of the two dedicated lines becoming off-hook. Assuming that the first dedicated line **170** is off-hook, however, only the AND gate **177** assciated with the erase circuit for message track **1** is completed, and so only that first message track will actually be erased during the entire erase-record cycle. Similarly, only the AND gate **181** associated with the record circuit for message track **1** is enabled in response to an enable signal condition on the line **174,** and so only that first message track can receive a new message dictated on the first dedicated line. It will also be seen that an off-hook condition of the second dedicated line **171** enables the remaining message tracks **2–4** to be erased and subsequently to receive a new message for recording thereon.

It will also be understood by those skilled in the art that the foregoing relates only to preferred disclosed embodiments of the present invention, and that numerous alterations and modifications may be made therein without departing from the spirit and the scope of the invention as defined in the following claims.

What is claimed is:

1. Method of recording and delivering a message in plural segments, comprising the steps of:

recording a first message segment of certain duration and having a final portion;

recording a second message segment having an initial portion which is identical both in content and in time of occurrence with said final portion of said first message segment;

delivering a composite message comprising serially reproduced first and second message segments with synchronized concurrent reproduction of said final portion of the first message segment and said initial portion of the second message segment; and

transferring message segment delivery to said second message segment at a time during said synchronized concurrent reproduction.

2. Method as in claim **1**, wherein said message segment delivery transfer occurs before termination of said final portion and after commencement of said initial portion.

3. Method as in claim **1**, wherein said composite message delivery comprises delivery of a first composite message; and

delivering a second composite message which comprises serially reproduced first and second message segments with synchronized concurrent reproduction of said final and initial portions of said message segments, and with transfer of message segment delivery to said second message segment occurring during synchronized concurrent reproduction; and

commencing delivery of said second composite message after completing delivery of the first message segment of said first composite message.

4. Method of determining the duration of a message, comprising the steps of:

recording a message on a recording medium;

determining the time required to record said message;

subsequently commencing delivery of said recorded message;

determining the time elapsed since commencement of said message delivery; and

terminating said message delivery when said elapsed time is at least equal to said time required to record said message.

5. Method as in claim **4**, wherein said time required to record the message is determined by counting the number of equal time segments required to record said message;

said determination of elapsed time is determined by counting equal playback time segments occurring since commencement of said message delivery;

comparing the counted playback time segments with the previously determined number of segments required to record said message; and

terminating said message delivery when said playback time count segment becomes as great as said record time segment count.

6. Method as in claim **4**, further comprising:

generating repetitive signals corresponding to segments of time required for recording and playback of said message;

determining the number of said repetitive signals occurring during recording of said message;

counting the repetitive signals occurring during said message delivery; and

terminating said message delivery when the number of repetitive signals during message delivery attains a predetermined relation to said determined number of repetitive signals.

7. Method as in claim **4**, wherein said recorded message comprises a first message portion and a second message portion;

said recording time is the time required to record only said first message portion;

said elapsed time is the time from commencement of message delivery to the end of delivery of said first recorded message portion; and

terminating said message in response to said elapsed time equaling said recording time only if a certain signal condition exists.

8. Apparatus for providing a recorded message announcement, comprising:

first means operative to provide a first message segment;

second means operative to provide a second message segment having an initial portion which is coincident with a final portion of said first message segment;

control signal means responsive to operation of said first and second means to provide a control signal condition during said coincident portions of said first and second message segments; and

message delivery means selectively operative to deliver either of said first and second message segments to a message delivery circuit and operative in response to said control signal condition to terminate first message segment delivery and to commence delivery of said second message segment.

9. Apparatus as in claim **8**, wherein said first and second message means are operative to provide mutually synchronized respective message segments.

10. Apparatus as in claim **8**, wherein said control signal means is operative to provide said control signal condition at a time after said initial portion of said second message segment commences and before said final protion of said first message segment terminates.

11. Apparatus as in claim **8**, wherein said message delivery means is a first message delivery means and said message delivery circuit is a first message delivery circuit, and further comprising second message delivery means connected to receive said first and second message segments and selectively operative to deliver either of said message segments to a second message delivery circuit;

said control signal means is operative to provide a second control signal condition corresponding to termination of said first message segment; and

said second message delivery means is operative in response to said second control signal condition to commence delivery of said first message segment and is operative in response to said first control signal condition to terminate delivery of said first message segment and commence delivery of said second message segment.

12. Apparatus for delivering a recorded message of selectively variable duration, comprising:

message means operative to receive a recorded message not to exceed a predetermined maximum duration;

first circuit means operative to provide a plurality of timing signals during recording of the recorded message on said message means;

memory means operative to receive a signal condition from said first circuit means representing a timing signal count corresponding to a shortened time period less than said maximum duration;

second circuit means operative to provide a plurality of playback timing signals during playback of said message recorded on said message means;

comparison means responsive to said playback timing signals and also to said signal condition of said memory means, said comparison means operative to provide a control signal condition in response to said playback timing signals indicating a time period equal to said shortened time period; and

message delivery means operatively associated with said message means to control playback delivery of a message recorded thereon, said message delivery means being responsive to said control signal condition to terminate delivery of said shortened recorded message.

13. Apparatus as in claim 12, wherein said message delivery means operates to terminate said message delivery only in response to said control signal condition and the concurrent presence of another control signal condition.

14. Apparatus as in claim 12, wherein:

said timing signals provided by said first circuit means are repetitive signals representing time segments of said maximum message duration;

said memory means is connected to receive said time segment signals during said recording and is operative to provide a record length signal condition;

said second circuit means is operative to receive said repetitive time segment signals during said message delivery and to provide a delivery length signal condition corresponding to the number of time segment signals occurring since the message delivery commenced; and

said comparison means is operative to compare the time segment counts represented by said record length signal condition and said delivery length signal condition, and is operative to provide said control signal condition when the time segment count represented by said delivery length signal condition is equal to the time segment count represented by said record length signal condition.

15. Apparatus as in claim 12, wherein:

said message means has a plurality of message segment tracks for recording and repetitively delivering segments of a message;

said message delivery means is operative in response to said repetitive operation of said message means to supply said message segments to a message delivery circuit in a predetermined sequence making up a composite delivered message;

said memory means is operative to provide said record length signal condition identifying the particular message segment track on which said recorded message terminates; and

said message delivery means is responsive to said control signal condition from said comparison means and also to said record length signal condition to terminate delivery of said shortened recorded message only in response to a signal condition indicating that the message segment on said particular message segment track is being supplied to said message delivery circuit.

16. Apparatus as in claim 15, wherein:

said message delivery means is a first message delivery means and said message delivery is a first message delivery circuit; and further comprising

at least one other message delivery means operatively associated with said message means to supply said composite message to a second message delivery circuit by a predetermined message segment delivery sequence which is offset in time relative to said delivery sequence of said first message delivery means; and

each of said message delivery means is responsive to said control signal condition from said comparison means and also to said record length signal condition to terminate delivery of the shortened recorded message to a particular message delivery circuit only in response to a signal condition indicating that the message segment on said particular message segment track is being delivered to said particular message delivery circuit.

17. Apparatus for delivering a recorded message, comprising:

message means operative periodically to provide a composite message made up of plural sequential message segments, with the end portion of at least one said message segment being coincident in time and identical in content with the beginning portion of the next sequential message segment;

first message transducing means responsive to said message means periodically to provide a first message segment signal;

second message transducing means responsive to said message means to periodically provide a second message segment signal;

control means responsive to periodic operation of said message means to provide a playback control signal condition occurring at a time during said coincident time; and

message delivery switching means connected to receive said first and second message segment signals and operative in response to said control signal condition to switch from delivery of said first message segment signal to delivery of said second message segment signal.

18. Apparatus as in claim 17, further comprising:

message recording means operative to record a composite message on said message means, said recorded composite message including first and second message segments;

record control means responsive to operation of said message means to provide a record control signal condition during said coincident time and prior to the time of occurrence of said playback control signal condition;

said message recording means being operative in response to said record control signal condition to commence recording concurrently on both said first and second message segments for a period of time extending beyond said time of occurrence of said playback control signal condition.

19. Apparatus as in claim **17,** further comprising:

control signal means operative to provide a sequence of timing pulses in response to each periodic message segment of said message means, with one of said timing pulses corresponding to the termination of said first message segment and with an earlier occurring other said timing pulse corresponding to the initiation of said next message segment, and with at least one delivery timing pulse occurring between said one and said other timing pulses; and

said control means being operative to provide said control signal condition in response to said delivery timing pulse.

20. Apparatus as in claim **19,** further comprising:

message erase control means connected to receive a message erase signal and operative in response to a message substitution signal and a timing pulse corresponding to the initiation of said one message segment to apply said message erase signal to said one message segment;

said message erase control means thereafter being operative in response to occurrence of said other timing pulse to apply said message erase signal to said next message segment and to terminate said message erase signal on said one message segment in response to said one timing pulse;

message record control means connected to receive a new message signal and operative in response to said message substitution signal and termination of said message erase signal on said one message segment to apply said new message signal to said one message segment;

said message record control means being thereafter responsive to occurrence of said other timing pulse to apply said new message signal to said next message segment and to terminate said new message signal to said one message segment in response to said one timing pulse.

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