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NOTICE OF ENTITLEMENT

We RAYCHEM LIMITED

of Rolls House, 7 Rolls Buildings, Fetter Lane, LONDON EC4 1NH, ENGLAND

being the Applicant and Nominated Person, in respect of Application No. 45075/93, entitled SWITCHING ARRANGEMENT FOR A COMMUNICATIONS CHANNEL state the following:

Dennis Malcolm Pryor and Michael Challis are the actual inventors of the invention the subject of the Application.

The inventors made the invention for and on behalf of the applicant and nominated person in the course of their duties as employees of the applicant.

RAYCHEM LIMITED is the applicant of the application listed in the declaration under Article 8 of the PCT.

Convention priority is claimed from the following basic application(s) referred to in the declaration under Article 8 of the PCT:

Basic Applicant	Application Number	Application Date	Country	Country Code
RAYCHEM LIMITED	9213980	1 July 1992	Great Britain	GB
RAYCHEM LIMITED	9221348	12 October 1992	Great Britain	GB

The basic applications referred to in the declaration under Article 8 of the PCT were the first applications made in a Convention country in respect of the invention the subject of the Application.

DATED this 3rd day of April 1997

RAYCHEM LIMITED
By their Patent Attorney

GRIFFITH HACK

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(56) Prior Art Documents
US 4807277
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(57) Claim

1. A switching arrangement that can be connected in a communications channel that comprises a pair of lines between sets of terminal equipment, which comprises :

(i) a d.c. voltage window detector circuit that is connected between the lines and is responsive to the voltage between the lines; and

(ii) one or more switching circuits connected in or between the lines that can be actuated by the window detector circuit when, and only when, the voltage between the lines is within a predetermined band, the lower limit of the band being greater than a maximum communications signal voltage,

so that the or each switching circuit can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

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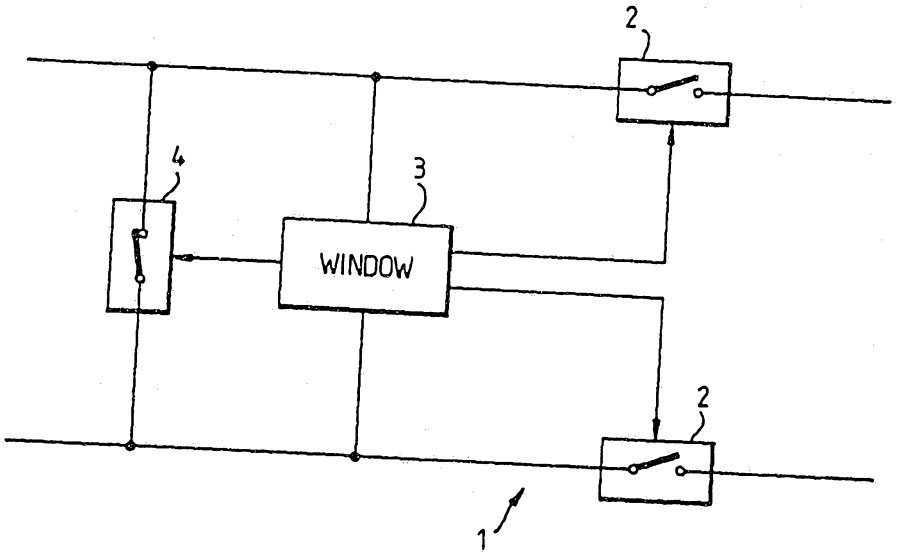


(57) Abstract

A switching arrangement that can be connected in a communications channel that comprises a pair of lines, between sets of terminal equipment, which comprises: (i) a d.c. voltage window detector circuit (3) that is connected between the lines and is responsive to the voltage between the lines; and (ii) one or more switching circuits (2, 4) connected in or between the lines that can be actuated by the window detector circuit (3) when, and only when, the voltage between the lines is within a predetermined band; so that the or each switching circuit (2, 4) can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

Switching Arrangement for a Communications Channel

This invention relates to communications circuits, and especially to maintenance termination units for use in telephone circuits.

In recent years, and especially in view of deregulation of many telephone systems, privately owned communication equipment has increasingly been installed in the premises of subscribers to the system, with the result that it is often necessary to determine whether any fault is located in the telephone line, or in the subscriber's premises, i.e. in the subscriber's equipment or cabling, in order to determine whose responsibility it is to repair the fault. It is highly advantageous economically if this determination can be performed remotely by sending an appropriate signal from the local exchange along the line, thereby obviating the necessity to send any telephone company personnel to the subscriber's premises.

In order to test the telephone line for any faults it is necessary firstly to install a so-called "maintenance termination unit" or MTU in the line at the subscriber's premises which can disconnect the subscriber equipment from the line (often called sectionalizing the line)

and connect the a and b or tip and ring lines on receipt of the appropriate signals from the exchange. During the line testing procedure determinations will typically be made of the line to line resistance and of the first and second line to ground resistance. Also the line continuity can be determined by detecting the presence of the MTU electronically.

Various forms of MTU are described in the prior art, and may employ solid state (silicon) switches or electrical relays. The present invention is concerned with solid state switching devices in view of their greater reliability and lower cost as compared with arrangements that incorporate relays. A number of such devices are described, for example, in US Patent No 4,710,949 to Om Ahuja. This device comprises a pair of voltage sensitive switches, one located in each of the tip and ring lines, and a distinctive termination connecting the tip and ring lines on the subscriber side of the voltage-sensitive switches. The voltage-sensitive switches may each have a threshold voltage of about 16 volts so that they are closed in normal operation by the 48 volt battery voltage but will open when this is replaced by a test voltage below about 32 volts in order to test the line-to-ground and tip-to-ring impedances. The distinctive termination may, for example, comprise a back-to-back diode and Zener diode which will exhibit an asymmetric resistance when large voltages (higher than the operating voltages) of different polarity are applied.

Although this form of MTU will perform adequately to sectionalise a fault in a line, it suffers from the problem that it requires the provision of ringing bypass capacitors in the signal path in parallel with the voltage-sensitive switches. These capacitors are necessary because the amplitude of the ringing signal (about 80V RMS) which is superimposed on the 48V d.c. battery voltage, is sufficiently large for the polarity of the resultant signal to change during the ringing signal cycles and to cause unacceptably large crossover distortion due to opening of the voltage-sensitive switches at the crossover points of the ringing signal. Because the ringing frequency is relatively low, about

20Hz, a large capacitance is required for the ringing bypass capacitors, typically in the order of 10μF. Because the capacitors are connected in the signal line they need to have a high voltage rating in order to withstand normal electrical transients etc, which increases their cost and physical size. In addition they can provide a low impedance path for transients.

According to the present invention, there is provided a switching arrangement that can be connected in a communications channel that comprises a pair of lines between sets of terminal equipment, for example between a subscriber and an exchange, which comprises :

(i) a d.c. voltage window detector circuit (referred to herein as a window detector circuit or simply as a window circuit) that is connected between the lines and is responsive to the voltage between the lines; and

(ii) one or more switching circuits connected in or between the lines that can be actuated by the window detector circuit when, and only when, the voltage between the lines is within a predetermined band, the lower limit of the band being greater than a maximum communications signal voltage,

so that the or each switching circuit can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

Normally the window detector circuit will allow current to flow through it only when the line voltage is within a predetermined band (which will be above normal signalling voltages), i.e. the current that flows through the window circuit is significantly greater when the line voltage is within the band than when it is outside the band, although at very high applied line voltages the leakage current through the windown circuit may approach or even exceed the within-band current

flow. Thus, according to a preferred aspect the invention provides a switching arrangement that can be connected in a communications channel that comprises a pair of lines between sets of terminal equipment, for example between a subscriber and an exchange, which comprises :

(i) a d.c. voltage window detector circuit that is connected between the lines and which will allow a current to flow through it when, and only when, the voltage between the lines is within a predetermined band; and

(ii) one or more switching circuits connected in or between the lines that can be actuated by the current flow in the window detector circuit

so that the or each switching circuit can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

The arrangement according to at least preferred embodiments of the present invention has the advantage that it can be actuated by a signal of amplitude between that of the normal communications signals and the ringing signal without the ringing signal triggering the switch or switches and without the need to employ ringing bypass capacitors in the lines. The distortion of the ringing signal is reduced by use of overcurrent switching circuits as the series switches. The circuits employed in the arrangement according to the invention can switch on to their conductive state with applied voltages as low as one p-n junction drop (0.6V) which, combined with the voltage drop across any diode bridges present will cause a crossover distortion of less than about 2 volts in the ringing signal, in contrast with one of about 32 volts caused by the voltage sensitive switches in the absence of ringing bypass capacitors.

As switching circuits the arrangement may employ a series switching circuit connected in each of the lines of the channel and/or one or more shunt switching circuits connected between the lines, or, in the case of systems having an earth, between the lines and earth.

Since the test voltage that is applied to the arrangement in order to open the series switching circuits and close the shunt switching circuit will normally be significantly less than the peak voltage applied during ringing, the switching circuits would attempt to switch during that period in the ringing cycle that the applied voltage is within the predetermined band. Such switching can be prevented by including a low pass filter in the arrangement with a sufficiently low cut-off frequency. The required cut-off frequency will depend on the width of the voltage band within which current will flow in the window circuit; the narrower the band is, the higher the cut-off frequency may be, since the applied voltage will spend less time within the predetermined band during each cycle. For example, a voltage band of 20V will correspond to a cut-off frequency of approximately 300Hz.

The window detector circuit that determines the applied voltage at which the switches will open and close may include a Zener diode that sets the lower limit of the applied voltage that will cause current to flow. The upper limit of the applied voltage may conveniently be set by means of an overcurrent switching circuit that will open when the current passing through the circuit, and hence the voltage applied across it, exceeds a predetermined value. When the applied voltage is within this band the window circuit will send a signal of some sort to the switching circuits.

It will normally be desirable for the shunt switching circuit to be capable of being switched independently of the series switching circuits. For example, the shunt switching circuit will need to be closed during a loop-back test to determine the line continuity (in which case it does not strictly matter whether the series switching circuits are open or closed), while the shunt switching circuit and the

series switching circuits will all need to be open in order to determine the line insulation resistance (tip to ring resistance etc.). Independent actuation of the switches may be achieved for example by altering the polarity of the applied d.c. signal in order to actuate different switches. In this case the signal inputs for the shunt and series switching circuits may be connected to different lines in the window circuit, in each of which current is constrained to flow only when the d.c. actuating signal has the correct polarity.

There is no constraint on where the upper and lower limits of the predetermined voltage band of the window circuit may be other than that its lower limit should be higher than the maximum signal voltage, and it is possible for different arrangements to have different voltage windows. Preferably, however, the voltage band should not be set at such a high voltage that it requires any different level of skill on the part of anyone required to maintain the telephone equipment, and most preferably the voltage band is below the peak value of the ringing voltage so that the required voltage is no more dangerous than the normal ringing voltage.

In addition to the ability of the arrangement to be operated in order to locate a fault in the channel, it is possible according to a preferred aspect of the invention, for the circuits to be capable of protecting the system from overcurrents and overvoltages by opening and closing respectively. This can be achieved by employing the switches described below.

The series switching circuit in each of the lines is a solid state switch, normally formed in silicon, and preferably comprises a switching transistor whose input voltage is controlled by an overcurrent control element which switches on when the switching circuit is subjected to an overcurrent, thereby turning the switching transistor off. Such a circuit on its own will only switch in response to an overcurrent in its associated line. However, the circuit includes a test control element that also controls the input voltage of the

switching transistor. The test control element turns on when current flows in the window circuit, thereby turning the switching transistor off. Thus, in this way the series switching circuits can be actuated either remotely or by an overcurrent in the line. The control elements may be formed from any of a number of devices, and the choice of control element will depend to some extent on the type of switching transistor employed. The overcurrent control element may, for example comprise a transistor whose base or gate is held in a potential divider that spans the switching transistor so that the base-emitter or gate-source voltage increases as the current in the line increases. Alternatively the control element may comprise a comparator that compares a fraction of the voltage across the switching transistor with a reference voltage and opens the switch if the fraction is greater than the reference voltage, as described in our copending international application No. PCT/GB91/02215. If a normally-on FET such as a JFET or a depletion mode MOSFET is employed as the switching transistor, a negative voltage generator e.g. a charge pump, or an optocoupler may be employed as the control element, as described in our copending British application No 9114717.3. The disclosures of these specifications are incorporated herein by reference.

Each series switching circuit is preferably capable of remaining open for a period of time after termination of the actuating d.c signal in order to be able to perform one or more tests on the line without the need to maintain the d.c. signal or while the polarity of the signal is reversed. For example, the circuit may remain open for up to 1 minute, but more usually for up to 20 to 40 seconds, and usually for at least 5 seconds. In the circuit described above, this may be achieved by including a capacitor between the base and emitter terminals or gate and source terminals of the test control element. The capacitor is charged up during actuation of the switching circuits by the d.c signal, and holds the test control element on and hence the switching transistor off, for a period of time after actuation by the d.c signal.

The series switching circuits may employ bipolar transistors and/or field effect transistors. Where bipoplar transistors are used they are preferably used in a darlington configuration as the switching transistor in order to reduce the base current required when the transistor is switched on. The base current must be supplied via a resistor connected between the base and collector of the switching transistor. When the circuit switches to its blocking or open state the switching transistor base current is diverted through the control transistor (which is now on) and becomes a leakage current. However, since the voltage drop across the resistor is much higher when the arrangement is in its blocking state, the leakage current is larger than the switching transistor base current. If a darlington pair or triplet is employed the effective d.c. current gain will be increased considerably so that a much higher resistance can be used.

Where field effect transistors are employed, MOSFETS are preferred, for example enhancement mode MOSFETS although depletion mode MOSFETs may be employed, particularly where linearity is important. Examples of depletion mode MOSFET switches are described in our copending British patent application No 9114717.3, mentioned above. The resistors employed in the switching circuit may be provided by MOSFETS, for example with their gates and drains connected as in NMOS logic. Alternatively, the control transistor and the resistor which together form the voltage divider for the base and gate of the switching transistor may be provided by a complementary n-channel and p-channel pair of FETS connected in the manner of CMOS logic.

It is preferred for the series switching circuits to include no resistive components in series with the switching transistor. Such an arrangement reduces the voltage drop or insertion loss along the line of circuit, and in addition, reduces the area of silicon that need be employed in an integrated circuit design of the arrangement.

The shunt switching circuit will normally comprise a triac connected between the tip and ring lines. The gate of the triac will be connected to one of the lines via a pair of back-to-back Zener diodes so that an overvoltage greater than the Zener breakdown voltage will cause a current pulse to be applied to the triac gate and cause the triac to operate. In addition the gate of the triac may be connected to the window circuit so the current flowing in the window circuit will also operate the triac. As with the series switching circuits, a low pass filter is provided in the shunt switching circuit in order to prevent nuisance tripping of the shunt switching circuit by the ringing signal. The shunt switching circuit may connect the two lines together directly or via a further component. For example the lines may be connected together via a distinctive termination, e.g. a diode and a Zener diode back-to-back so that the resistance of the termination is non linear and polarity dependent.

The window circuit may be connected to the switching circuits by any of a number of means. For example, in one form of device, they may be connected by means by of an optoelectronic coupler. In other forms of device they may be d.c. coupled to the window circuit for example taking their actuating voltage from the voltage drop across a resistor in the window circuit.

Preferably all components of the arrangement take their power from the current in the lines or from the voltage drop between them so that no separate power supply rails are needed.

It is quite possible to produce a number of arrangements each having a different d.c. actuation voltage window so that they can be connected at various points along a long channel in order to divide the channel into sections for locating a fault.

Three forms of arrangement according to the present invention will now be described by way of example with reference to the accompanying drawings in which :

Figure 1 is a block diagram indicating the main components of the arrangement according to the invention;

Figure 2 is a circuit diagram of one form of an arrangement shown in figure 1;

Figure 3 is a graph showing the line voltage and the window circuit output voltage of the arrangement shown in figure 2 during a ringing signal; and

Figure 4 is a circuit diagram of a second form of arrangement;

Figure 5 is a circuit diagram of a third form of arrangement; and

Figure 6 is a graph showing the I-V curves of the window circuits of the arrangements shown in figures 2 and 5.

Referring to the accompanying drawings, a maintenance termination unit 1 for a telephone line comprises a pair of series switching circuits 2 and 2' located in each of the lines of a communication channel, each series switching circuit being controlled by means of a window circuit 3. The window circuit 3 also controls an overvoltage shunt switching circuit 4 that shunts any overvoltage across the load. In an alternative circuit it is possible for an earth connection to be provided, in which case the overvoltage circuit may be employed to shunt the overvoltage to earth.

In order to perform a maintenance test on the line, which may be a routine test or may be due to a subscriber complaint, a positive d.c. voltage of 80 to 100V is first applied between the tip and ring lines, whereupon the shunt switching circuit 4 closes and connects the lines

together. This enables a loop back test to be performed in which the overall line resistance can be measured. As soon as the applied voltage is removed the shunt switching circuit will open. Application of a negative voltage of between 80 and 100V between the lines will cause the series switching circuits 2 to open, thereby isolating the subscriber from the line. The series switching circuits will remain open for a period of about 20s after the voltage is removed allowing the line to line and line to ground resistances to be evaluated.

The electrical circuit forming the MTU is shown in figure 2.

Each series switching circuit 2 and 2' comprises three transistors T_1, T_2 and T_3 in complementary darlington configuration that are series connected in the associated line within a diode bridge BR_1 and form a switching transistor. The base terminal of the darlington triplet is held in a potential divider formed by resistor R_1 and overcurrent control transistor T_4, the potential divider spanning the darlington triplet, and the base terminal of the control transistor T_4 is itself held in a potential divider formed by resistors R_2 and R_3 and which also spans the darlington triplet switching transistor. This circuit will protect the system from an overcurrent in the tip or ring line as follows: As the voltage on the line increases from zero all the transistors will be off until the voltage across the circuit exceeds the voltage dropped across the diode bridge plus a single pn junction drop for the switching transistor. The switching transistor will then turn on to allow current to flow while control transistor T_4 remains off. If the current in the line increases, the base voltage of control transistor T_4 will increase due to the voltage drop across R_3 until transistor T_4 turns on when an overcurrent is experienced. This will cause the base-emitter terminals of the switching transistor to be shorted and the switching transistor to turn off, thereby blocking current flow in the line. In this state the leakage current will be determined by the value of R_1, R_2 and R_3 which will typically be in the range of 50kΩ to 1MΩ. A 100nF capacitor C_1, is connected in parallel with resistor R_3 in order to inhibit switching on of transistor T_1. This will prevent tripping of

the switching circuit by transient surge currents due to inductance and capacitance on the line when the system is first switched on. In addition, a Zener diode Z_1 is connected across transistor T_1 in order to protect the switching circuit 2 from voltages exceeding the transistors' operating voltages, for example, large inductive spikes.

In addition to the overcurrent control transistor T_4, an enhancement mode test control FET T_5 is connected between the base and emitter terminals of the switching transistor. The gate terminal of FET T_5 is connected to the window circuit so that the switching circuit can be switched on and off remotely.

The shunt switching circuit 4 comprises a triac TR_1 that is connected between the tip and ring lines and whose gate terminal is connected to the tip line via a pair of back-to-back Zener diodes Z_5 and Z_6 and gate current limiting resistor R_{17}. When an overvoltage is experienced that exceeds the breakdown voltage of Zener diodes Z_5 and Z_6 a current pulse will be transmitted to the gate of the triac causing the tip and ring lines to be shorted. An enhancement mode FET T_{14} is also connected between the gate of triac TR_1 and the tip line in order to allow remote switching of the shunt switching circuit 4. A diode D_5 is included to provide reverse breakdown protection for FET T_{14}.

The window circuit comprises a voltage level detector Zener diode Z_4 and a current level detection circuit 6 that are connected in series within a diode bridge BR_2 which is itself connected between the tip and ring lines. The Zener diode Z_4 will allow current to flow through the window circuit only when the voltage across it is 75V, corresponding to a voltage between the tip and ring lines of 80V, while the current level detection circuit 6 will stop current flow through the window circuit at currents associated with a tip to ring voltage in excess of 100V. The current level detection circuit 6 works on essentially the same principle as the series switching circuits 2 and 2'. A complementary darlington pair of transistors T_7 and T_8 form the switching transistor whose base terminal is held in a potential divider

formed by 1MΩ resistor R_{11} and control transistor T_9 whose base terminal is itself held in a voltage divider formed by a pair of 1MΩ resistors R_{12} and R_{13}. When the voltage across transistor T_7 exceeds a pn junction drop, current will flow until the voltage across R_{13} is sufficient to turn transistor T_9 on, whereupon the base emitter terminal of transistor T_8 is shorted and the darlington pair switches off.

Three opto-isolators OPTO1-3 are connected with their inputs in series with the voltage level detector Zener diode Z_4 and the current level detection circuit 6 and their outputs connected to the series and shunt switching circuits. Isolators OPTO1 and OPTO2 which are connected to the series switching circuits are in series with each other and in parallel with opto-isolator OPTO3 which is connected to the shunt switching circuit 4. The input of opto isolator OPTO3 is connected with opposite polarity to that of isolators OPTO1 and OPTO2 so that the series and the shunt switching circuits will be actuated with applied voltages of different polarity. Diodes D_3 and D_4 are included to prevent reverse breakdown of the LEDs in the opto isolators caused by an application of a large reverse voltage.

When a d.c. signal of between 80 and 100V with the correct polarity is applied to the tip and ring lines, a current of about 10mA will flow through the LED inputs of the opto isolators OPTO1 and OPTO2. The output of each opto isolator is passed through a low pass RC filter formed from resistor R_5 and capacitor C_3 which prevents spurious triggering of the switching circuits, and charges capacitor C_2 which is connected between the gate and source of test control FET T_5. Diode D_1 allows current to flow from OPTO1 into the capacitor but not the other way round, so that the discharge of capacitor C_1 is controlled by resistor R_4 also connected between the gate and source of FET T5.

Thus once capacitor C_2 has charged sufficiently to exceed the gate voltage of the test control FET T_5 the series switching circuit will open to disconnect the subscriber, and will remain open after removal

of the actuating d.c. signal until capacitor C_2 has discharged through resistor R_4.

If the polarity of the applied d.c. signal is reversed, a 10mA current will flow through the LED of opto isolator OPTO3. The output voltage is passed through a low pass RC filter formed by resistors R_{14}, R_{15}, R_{16}, C_7 and C_8 and then to the gate of FET T_{14}, which will turn the FET on and trigger the triac effectively shorting the two lines together and allowing loop-back testing of the system.

The arrangement may even be employed where the fault is a short circuit in the subscriber's equipment. In such a case any voltage applied at the exchange will be dropped along the line so that it will not be possible to apply the required actuating voltage to the window circuit. If, however, the applied voltage is reduced to below about 3.6V, the voltage drop occurring across the switching transistor of each series switch will be insufficient to maintain the switch closed and the fault can thus be sectionalised.

Spurious triggering of the shunt and series switching circuits due to the ringing signal on the lines is prevented as shown in figure 3. Figure 3a shows the voltage appearing on the tip and ring lines when a ringing signal is transmitted. The signal comprise a sinusoidal ringing signal of 20Hz frequency and 80V RMS amplitude (226V p-p) superimposed on a battery voltage of - 48V. Although the instantaneous voltage on the line exceeds the testing voltage for a considerable period of time, the only time current is generated in the window circuit 3 is when the voltage on the lines is between 80 and 100V on the rising edge of the ringing signal. Figure 3b shows the input to the opto isolators (line 1). This consists of a train of pulses of about 1.7ms width and occurring once per ringing cycle. The output from the (open ended) opto isolators is shown as line 2 in Figure 3c (in which the scale has been expanded) together with the input to the opto isolators (line 1). This output starts to rise when the LED current has risen to about 5mA. Pulses can easily be filtered out by means of the

RC filters formed by C_3 and R_5 in the series switching circuits and by C_7, C_8, R_{14}, R_{15} and R_{16} in the shunt switching circuit. Usually the filters will have a cut-off point of at least 50Hz, but normally not more than 500Hz.

Figure 4 shows an alternative form of arrangement in which the window circuit is directly coupled to the series switching circuits. The series switching circuits 2 and 2' are largely the same as those shown in Figure 2, as is the combination the current level detection circuit 6 and Zener diode Z_4 for determining the voltage window that will actuate the switches.

Series switching circuit 2 includes a p-channel enhancement mode FET41, while switching circuit 2' includes an n-channel enhancement mode FET42 as test control elements.

The window circuit includes a pair of resistors 44 and 47 from which points the gate voltages of FETs 1 and 2 are derived. Capacitors 9 and 10 are connected in parallel with resistors 44 and 47 in order to filter out any short spurious signals and also so that they will charge up on receipt of the correct test voltage and hold FETs 41 and 42 open for a period of time after termination of the d.c actuating signal. Steering diodes are provided to prevent reverse system voltages affecting the two FETs 41 and 42.

When a test voltage signal is received, current will flow through the window circuit 3 and a voltage drop will develop across resistors 44 and 47, taking the gate of FET 41 more negative than its source, and the gate of FET 42 more positive than its source, thereby opening the switching circuits 2 and 2'.

A similar additional window circuit of opposite polarity may be provided in order to control a shunt switching circuit.

A preferred electrical circuit for forming the MTU is shown in Figure 5. The circuit comprises a pair of series switching circuits 2 and 2' that are controlled by a window circuit 3, as in the circuits described above, and a separate shunt switching circuit 4.

The series switching circuits 2 and 2' are largely the same as those shown in figures 2 and 4. Switching circuit 2 comprises three transistors T_{51}, T_{52} and T_{53} in complementary darlington configuration that form a series switching transistor and are controlled by an overcurrent control transistor T_{54} and a test control transistor T_{55}. The main difference is that a further transistor T_{56} is included between the test control transistor T_{55} and the series switching transistor in switching circuit 2 in order to prevent the gate-source junction of the test control transistor T_{55} being reverse biased by more that its breakdown voltage when the switch is opened.

The window detector circuit comprises an NPN bipoplar transistor T_{57} and a PNP transistor T_{58} connected in a push-pull configuration between the lines. Base current for the transistors is provided through 38V Zener diodes Z_{51} and Z_{52} so that current will flow through the window circuit only when the voltage across the lines is at least 75V. In addition, a further transistor T_{59} that is connected between the bases of the push-pull transistors T_{57} and T_{58} receives its base current from the anode of Zener diode Z_{51} via a further 10V Zener diode Z_{53}. Transistor T_{59} will switch the current in the window circuit off when the voltage across the lines is increased by a further 15V to -90V. Diodes D_{51} and D_{52} are included to prevent any current flowing in the reverse direction.

The current flowing through the window circuit develops a voltage across resistor R_{51} and this signal is passed to the test control transistor T_{55} via a low pass filter formed from capacitor C_{51}, resistor R_{52} and diode D_{53} in parallel with R_{52}. When the unit is subjected to a ringing signal a train of unipolar pulses of short duration is developed across resistor R_{51}. In contrast with the arrangements

described in figures 2 and 4, however, pulses are generated on the falling slope of the ringing signal in addition to the rising slope. The purpose of diode D53 is to enable capacitor C51 to discharge faster than it is charged when the low pass filter is subjected to this train of pulses and so limit the voltage developed across capacitor C51 to 0.7V. A timing capacitor C52 and resistor R53 are connected across the source gate junction of the test control transistor T55 and separated from the low pass filter by diode D54 which allows the timing capacitor to charge but limits the discharge path to resistor R53. An equivalent filter and timing circuit is provided to take the signal developed across resistor R'51 of the window circuit to test control transistor T'55 of the switching circuit 2'.

The shunt switching circuit comprises a triac U1 that is connected between the a and b lines whose gate is connected to the a line via back-to-back Zener diodes D55 and D56 and current limiting resistor R54 in order to provide overvoltage protection against transients etc. that exceed the Zener voltages. The test switching circuit comprises a PNP transistor T60 that can be turned on when the applied voltage exceeds the Zener voltage of Zener diode Z54 (75V). A further PNP transistor T61 will short the base-emitter junction of transistor T60 and so turn it off when the applied voltage exceeds the combined Zener voltages of Zener diode Z54 and a further 15V Zener diode Z55 connected to the base of transistor T61. Thus an applied voltage of +75V to +90V will cause current to flow through transistor T60 and a voltage to be developed across resistor R55. This signal is filtered by a low pass filter formed from capacitor C53, resistor R56 and diode D55 in order to prevent false triggering of the shunt switch. The voltage appears at the base of transistor T62 which turns transistors T62 and T63 on and fires the triac U1. Capacitor C54 is included in the circuit to prevent leakage current briefly turning on transistor T63, which would cause the triac to turn on, when the exchange battery voltage is initially connected to the circuit.

The triac used in the circuit should have a maximum gate and hold current of 5mA. This affects the maximum value of line resistance that can be measured as higher values will prevent the triac from latching on. If the window voltage is 75V to 90V, and the activation voltage is 90V, then this 90V may drop by 15V, due to resistance in the line, for the triac switch to still operate. This equates to a maximum line resistance that can be measured of 15V/5mA = 3KΩ

Subscriber disconnection may be performed by applying a voltage of between -75V and -90V to the line to open the two series switches 2 and 2'. The switches will remain open for a period that is determined by the values of the timing capacitor C52 and resistor R53 in order to enable the various line tests to be performed. Reversing the polarity of the voltage to +75V to +90V will trigger the shunt switching circuit and enable a loop back test to be performed. The loop resistance is measured by reducing the test voltage to 50V, without breaking the loop, and measuring the current flowing in the circuit. As soon as current flow through the triac is removed, caused by removable of the test voltage, the shunt switch of the MTU will reset to normal operation.

The circuit has the advantage that the initial slope of the I-V curve of the window circuit is much steeper as shown in figure 6 (curve A) as compared with that of the unit shown in figure 2 (curve B), thereby giving a precise voltage at which the series switches open. As can be seen, with curve B the particular point at which the window circuit current has risen to a value to open the switches is not clear. The increased slope of curve A at the turn-on voltage (75V) is due to amplification of the current of Zener diodes Z51 and Z52 by transistors T57 and T58. In addition the current variation within the voltage window of -75V to -90V is reduced with the result that variations in the charge held by the timing capacitors C52 and C'52 and consequently the periods for which the series switches are held open are also reduced.

In some circumstances, a window voltage range higher than that given above, for example a window between 110 V and 130 V (regarded as a "window voltage" of 120 V, ie about the mid-point) might be useful. This would allow testing to be carried out at, say, 100 V (ie about 10-20 V less than the window voltage depending on the width of the window), and as a result any line noise (perhaps about 1 V) would give rise to a reduced percentage error. It may be noted that prior art to Om Ahuja involves measurements at 10V where line noise could give rise to an unacceptably large percentage error. It was previously thought impossible to measure high impedances at low voltages due to the problem of noise.

Current leakage in the off-state below the lower of the window voltages (namely below 110 V in the preferred range above) might be, say, 1-3 micro amps, whereas in the off-state above that range, ie above 130 V it might be about 100 micro amps, increasing with voltage. For this reason a higher window voltage might be desirable, since a higher test voltage can be used whilst still suffering the smaller leakage current. A window voltage of about 120 V might therefore be preferred to that of about 85 V (range 75-90 V) indicated earlier in the specification, for a test voltage of about 100V.

Claims

1. A switching arrangement that can be connected in a communications channel that comprises a pair of lines between sets of terminal equipment, which comprises :

(i) a d.c. voltage window detector circuit that is connected between the lines and is responsive to the voltage between the lines; and

(ii) one or more switching circuits connected in or between the lines that can be actuated by the window detector circuit when, and only when, the voltage between the lines is within a predetermined band, the lower limit of the band being greater than a maximum communications signal voltage,

so that the or each switching circuit can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

2. A switching arrangement that can be connected in a communications channel that comprises a pair of lines, between sets of terminal equipment, which comprises :

(i) a d.c voltage window detector circuit that is connected between the lines and which will allow a current to flow through it when, and only when, the voltage between the lines is within a predetermined band; and

(ii) one or more switching circuits connected in or between the lines that can be actuated by the current flow in the window detector circuit;

so that the or each switching circuit can be remotely actuated by means of a d.c. signal on the line, the arrangement including a low

pass filter associated with the or each switching circuit having a cut off frequency that is sufficiently low to prevent the switching circuit(s) being actuated by a ringing signal on the channel.

3. An arrangement as claimed in claim 1 or claim 2, the window detector circuit includes a Zener diode that sets the lower limit of the voltage band within which current will flow.

4. An arrangement as claimed in any one of claims 1 to 3, which includes a series switching circuit connected in each of the lines.

5. An arrangement as claimed in claim 4, wherein the series switching elements will open when subjected to an overcurrent on the lines.

6. An arrangement as claimed in claim 5, wherein the series switching circuit in each of the lines comprises a switching transistor whose base or gate voltage is controlled by an overcurrent control element, the overcurrent control element switching on when the switching circuit is subjected to an overcurrent, thereby switching the switching transistor off.

7. An arrangement as claimed in claim 6, wherein each series switching circuit includes a test control element that also controls the base or gate voltage of the switching element, the test control element turning on when current flows in the window circuit, thereby turning the switching transistor off.

8. An arrangement as claimed in any one of claims 5 to 7, wherein each series switching circuit is capable of remaining open for a period of time after termination of the actuating d.c. signal.

9. An arrangement as claimed in claim 8, wherein each series switching circuit includes a capacitor connected to an input terminal of the test control transistor, the capacitor being charged during

actuation of the switching circuits by the d.c signal and holding the switching circuit open for a period of time after termination of the actuating d.c. signal.

10. An arrangement as claimed in any one of claims 1 to 9, which includes a shunt switching circuit connected between the lines or between each line and earth.

11. An arrangement as claimed in claim 10, wherein the shunt switching circuit will close when subjected to an overvoltage.

12. An arrangement as claimed in claim 10 or claim 11, wherein the or each shunt switching circuit comprises a triac.

13. An arrangement as claimed in claim 12, wherein the triac has a gate that is connected to the window detector circuit, so that current flowing in the window detector circuit will trigger the triac.

14. An arrangement as claimed in any one of claims 1 to 13, wherein the window detector circuit is connected to the or each switching circuit via an optoelectronic coupler.

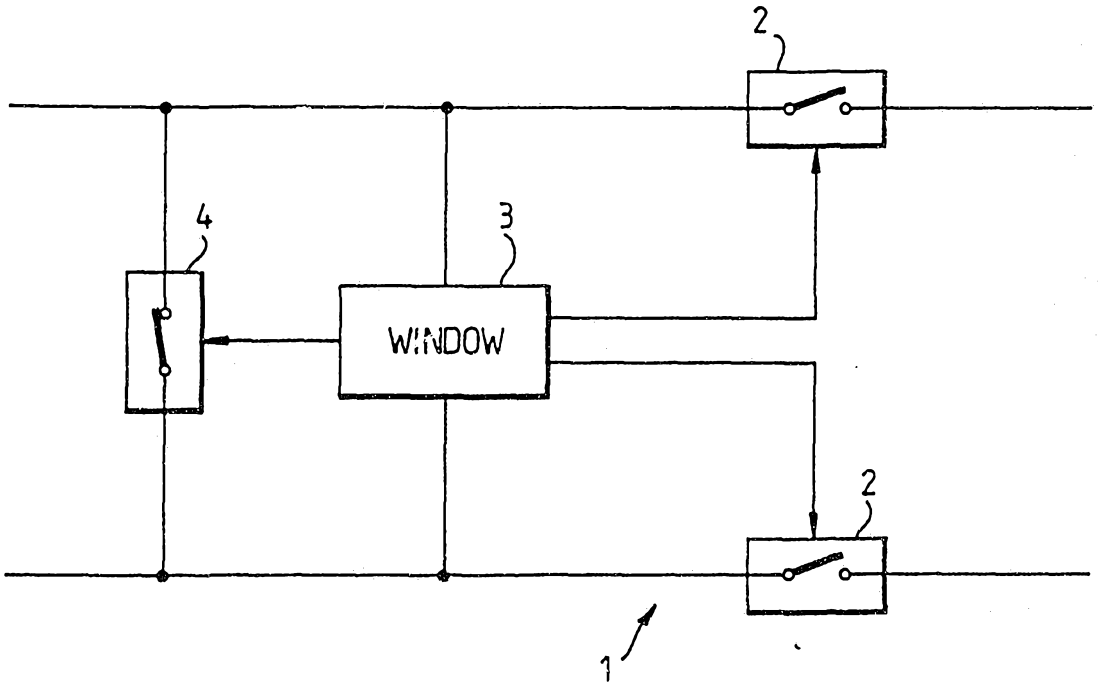
15. A switching arrangement, substantially as herein described with reference to the accompanying drawings.

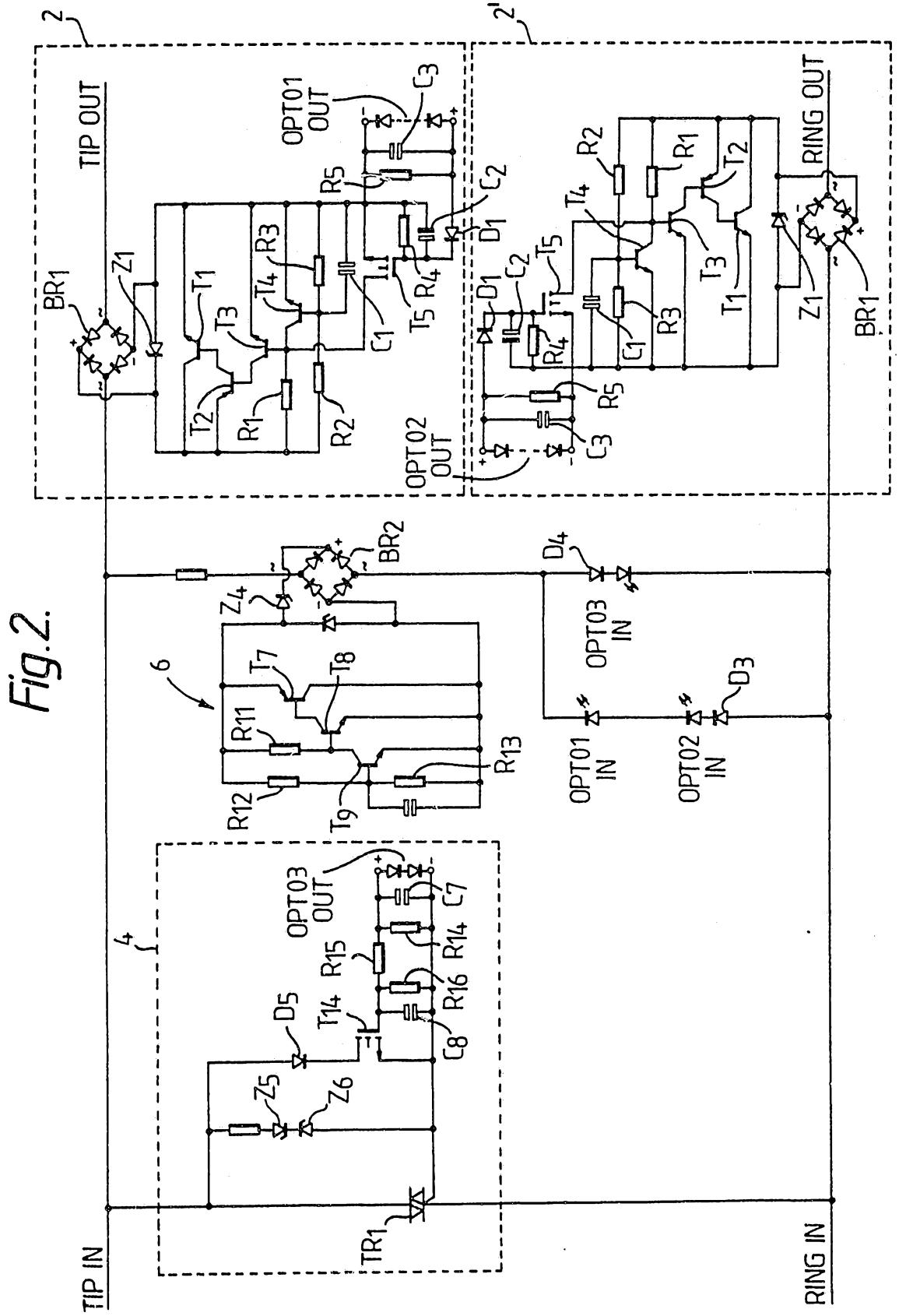
Dated this 3rd day of April 1997

RAYCHEM LIMITED
By their Patent Attorney
GRIFFITH HACK

45075/93

Fig. 1.

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T3
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T7
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R12
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R14
R15
R16
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C2
C3
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Fig.2.

Fig.3a

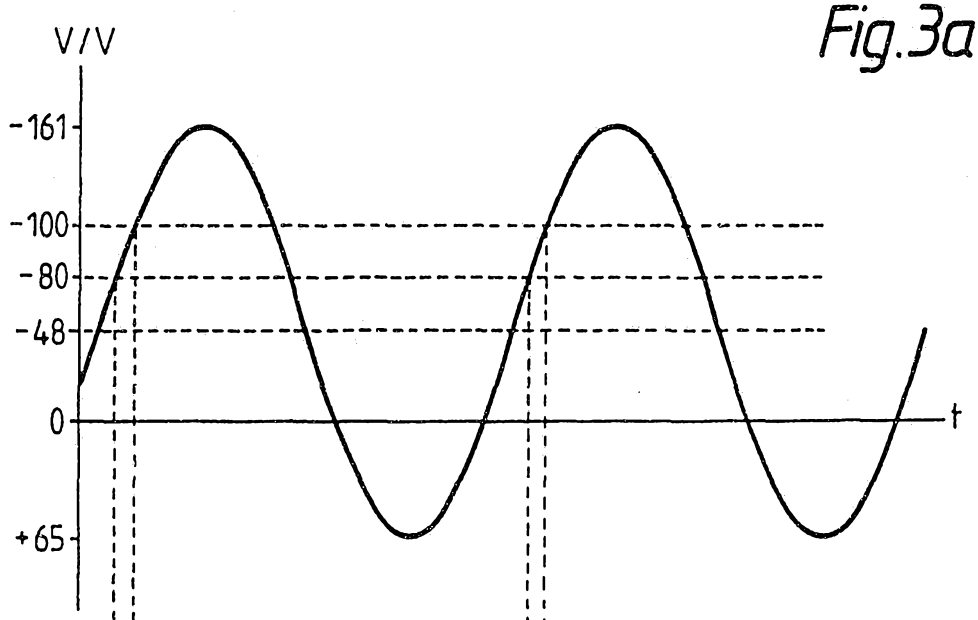


Fig.3b

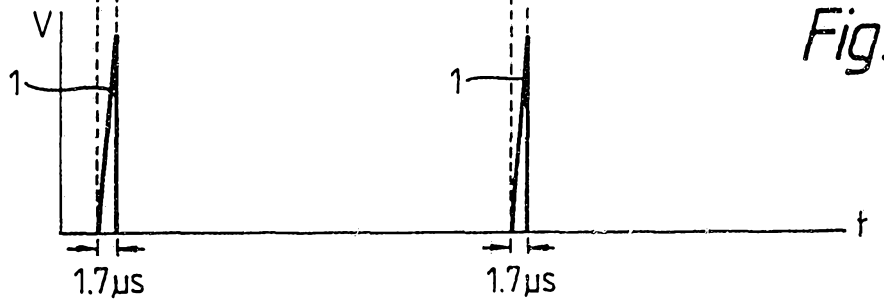


Fig.3c

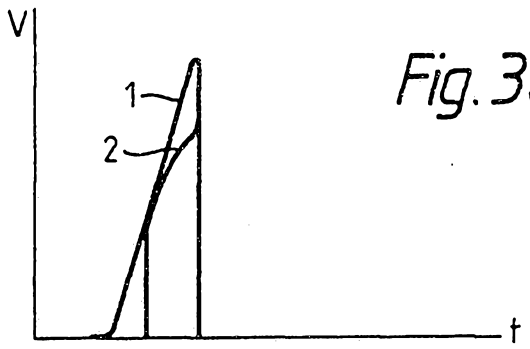


Fig. 4.

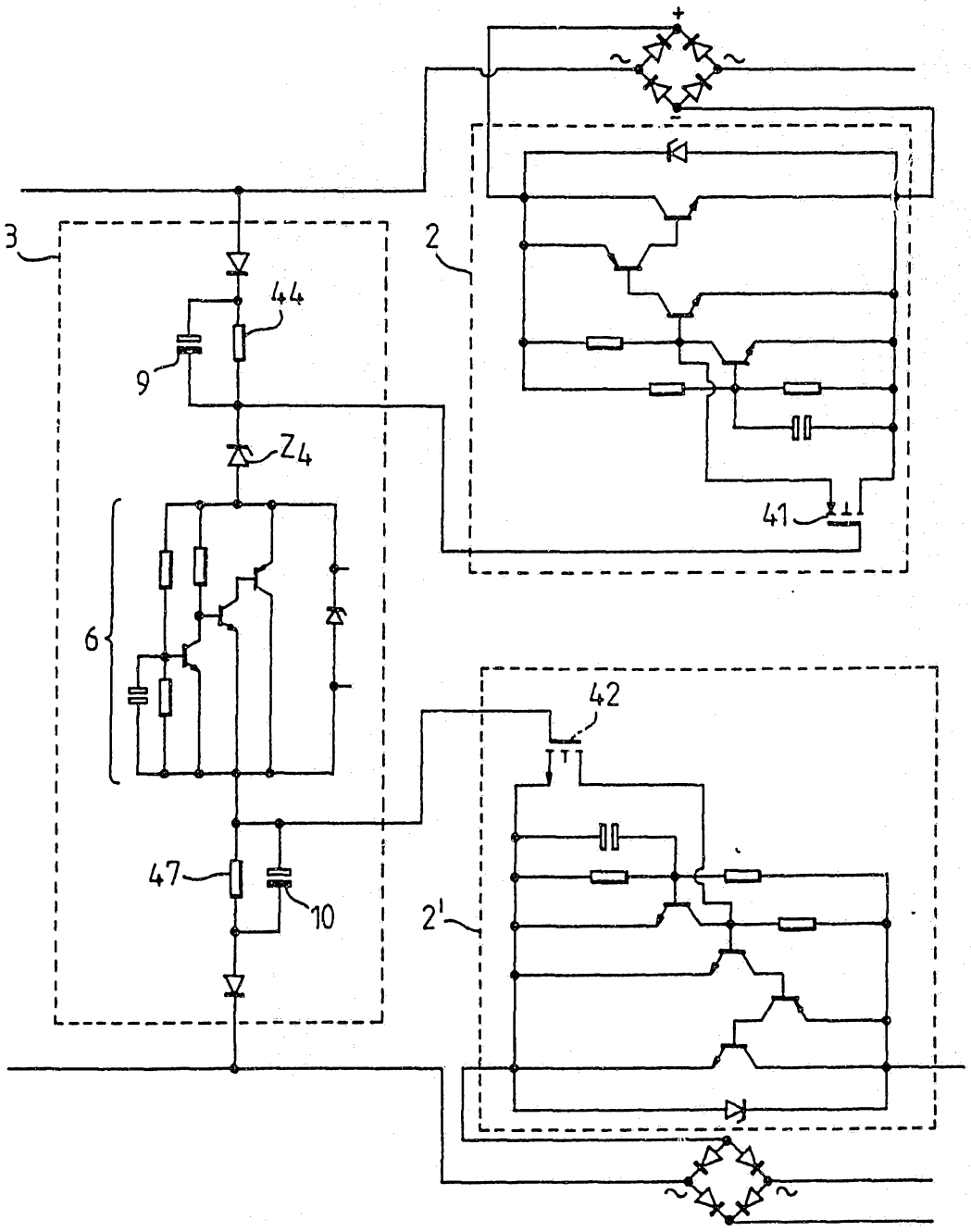


Fig.5.

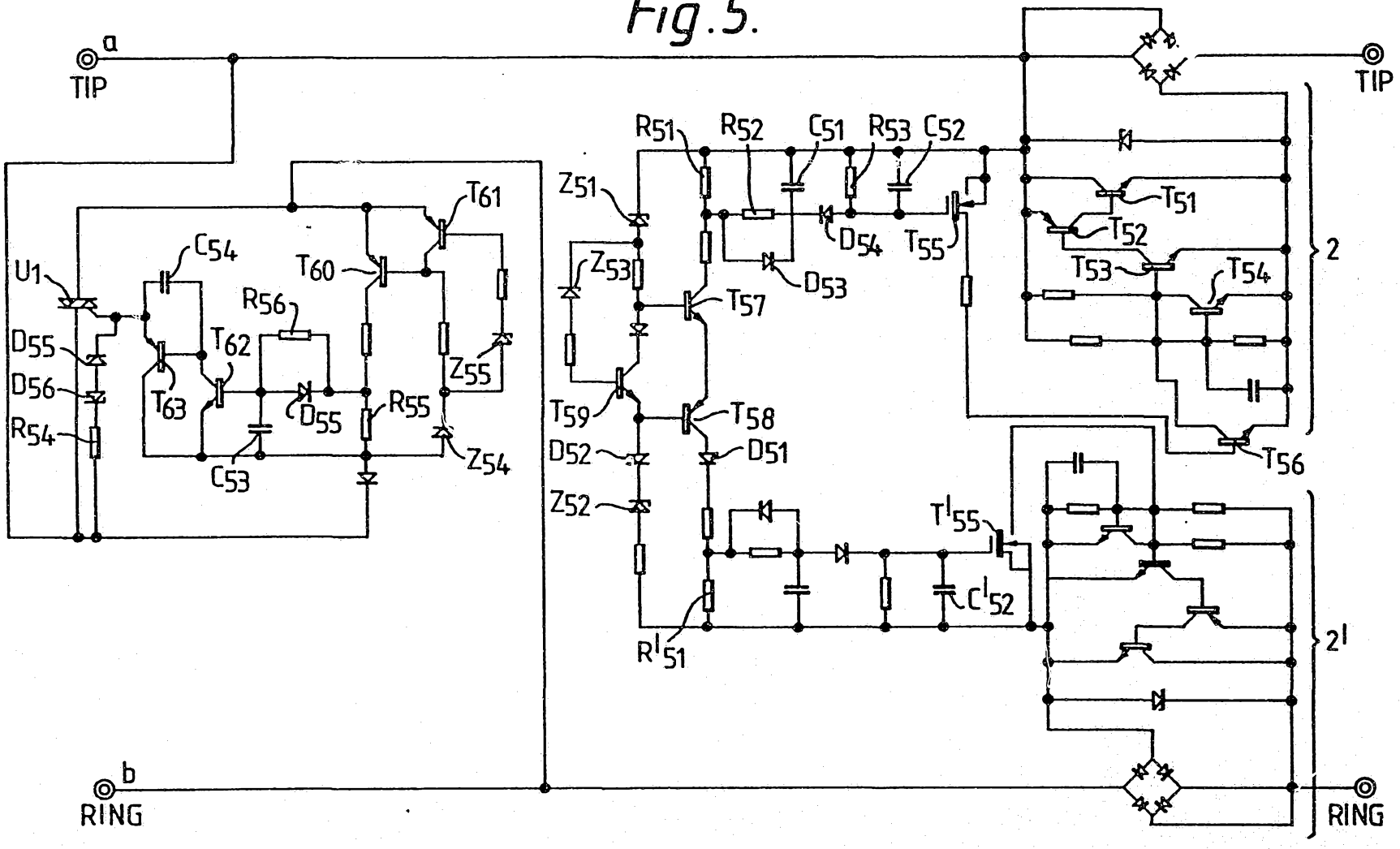


Fig.6A.

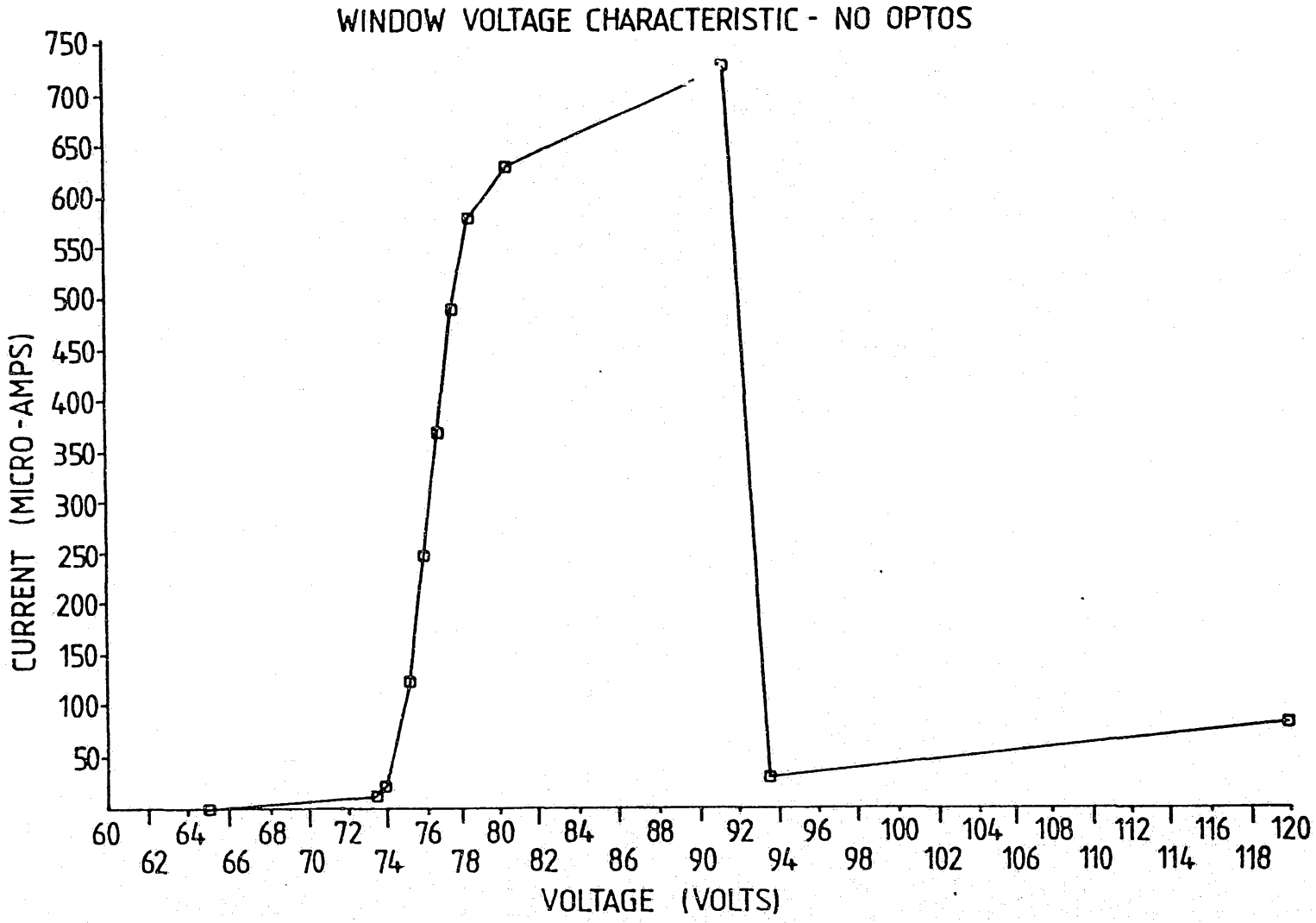
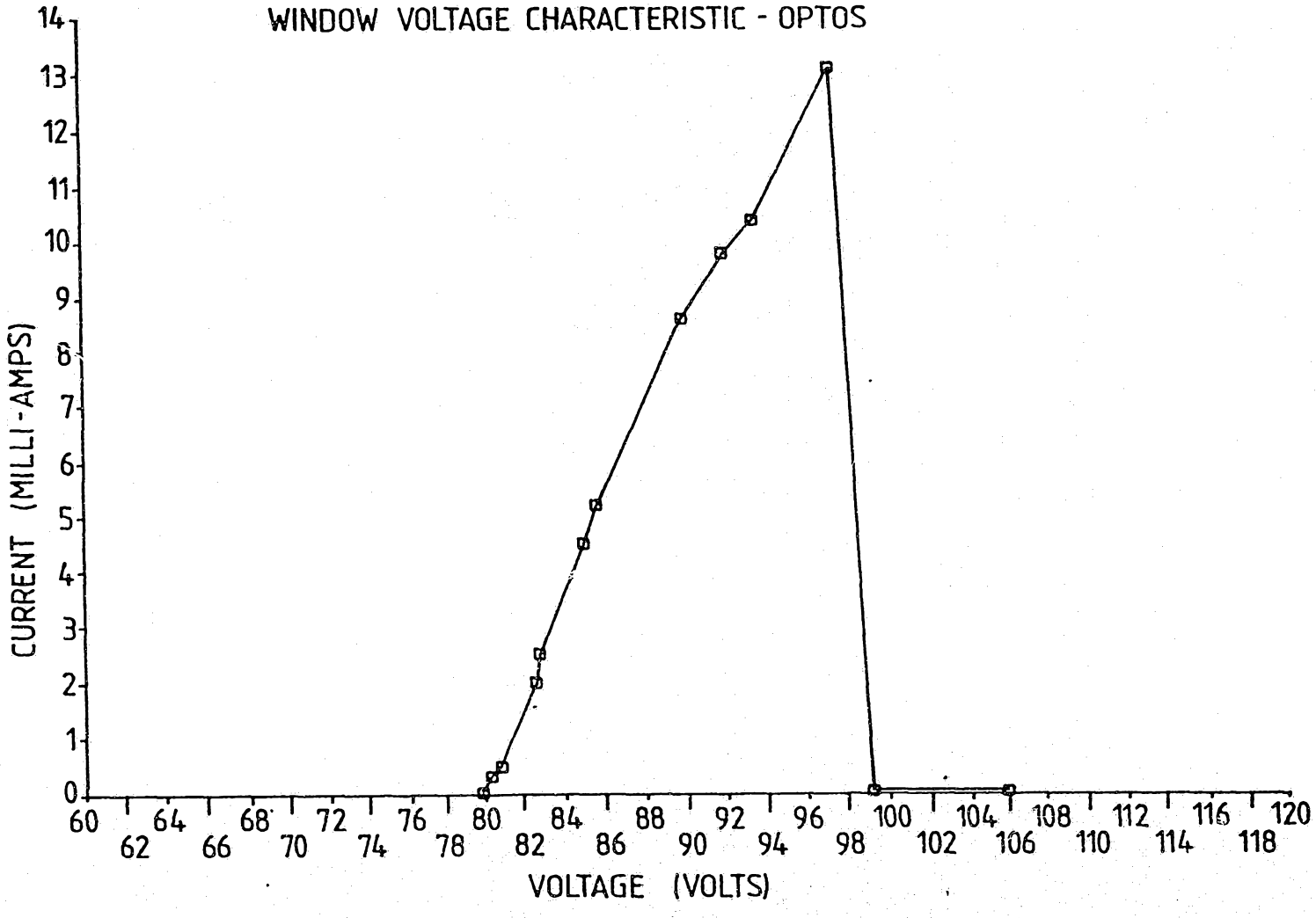


Fig.6B.



INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/01376

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04M3/30; H04M3/18; H02H3/10

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H04M ; H02H

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
E	GB,A,2 263 211 (GPT LIMITED) 14 July 1993 see page 6, line 29 - page 7, line 5 see abstract	1-4
X	US,A,4 489 221 (WALKER ET AL) 18 December 1984 see column 2, line 44 - line 58	1-4
X	US,A,3 725 613 (ALLEN ET AL) 3 April 1973 see column 3, line 1 - line 30	1-5,8-11
X	DE,A,3 513 598 (NEUMANN) 16 October 1986	1-2,4
X	US,A,4 807 277 (PERRY) 21 February 1989 see column 4, line 13 - line 55	1-4

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"P" document published prior to the international filing date but later than the priority date claimed

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21 SEPTEMBER 1993	29.09.93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VANDEVENNE M.J.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9301376
SA 75985

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2263211	14-07-93	None	
US-A-4489221	18-12-84	None	
US-A-3725613	03-04-73	None	
DE-A-3513598	16-10-86	None	
US-A-4807277	21-02-89	None	