(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SUCH A SEMICONDUCTOR DEVICE
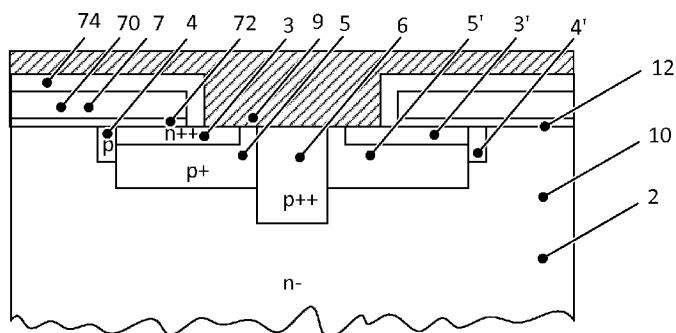
FIG. 13

(57) Abstract: A method of manufacturing a semiconductor device is provided with: (a) providing a wide bandgap substrate product (10), (b) forming source regions (3, 3') by applying a first mask (34) with a first and second mask layer (35, 36) and applying an n dopant (31), forming a well layer (5) by removing such part of the first mask (34), which is arranged between the two source regions (3, 3'), and applying a p dopant (51), forming two channel regions (4, 4') by forming a third mask (46) by performing an etching step, by which the first mask layer (35) is farther removed at the openings than the second mask layer (36), and then removing the second mask layer (36), wherein the remaining first mask layer (35') forms a third mask (46),) and applying a p dopant (41), wherein a well layer depth (50) is at least as large as a channel layer depth (40), (c) after step (b) for forming a plug (6) applying a fourth mask, which covers the source regions (3, 3') and the channel layers (4, 4') and applying a p fourth dopant to a greater depth than the well layer depth (50) and with a higher doping concentration than the well layers (5, 5').

Semiconductor device and method for manufacturing such a semiconductor device

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Description

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Technical Field

The invention relates to the field of power electronics and more particularly to a
method for manufacturing a semiconductor device and to such a semiconductor
20   device.

Background Art

In FIG 14 a prior art MOSFET 100 is shown as known from US 7 074643 B2.
The prior art MOSFET 100 is made of an n+ silicon carbide (SiC) substrate 80 and
comprises between a first main side 20 and a second main side 22 an n- doped
25   drift layer 2. On the first main side 20, two n++ doped source regions 3, 3' are
arranged, each which is separated from the drift layer 2 in lateral direction (i.e. in a
direction parallel to the first main side 20) by a p doped channel layer 4, 4' and on
a side opposite to the first main side 20 by a p+ well layer 5, 5', which is higher
doped than the channel layer 4, 4'. In between such two source regions 3, 3'
30   surrounded by a channel layer 4, 4' and a well layer 5, 5', a p++ doped contact
layer 65 is arranged, which laterally extends to the source regions. Due to its high
doping concentration the p++ doped contact layer provides a good ohmic contact
to a first main electrode 9 (source electrode). The contact layer 65 is a shallow
layer spatially (i.e. in depth direction, which direction is vertical to the first main
35   side 20) extending to a contact layer depth 67, which is less deep than the well
layers 5, 5', but electrically and mechanically contacting the well layers 5, 5' in

order to connect the well layers 5, 5' to the source electrode 9. The contact layer 65 overlaps with the source regions 3, 3' the channel layers 4, 4', so that the contact layer 65 is the only p doped layer in contact with the first main electrode 9.

JP 2010 267762 A describes a MOSFET which comprises on the first main side a highly p doped plug and a lower doped well layer below an n source layer and a channel layer, which surround the source regions. First the well layer is formed, followed by the channel layer with a new, wide mask. Afterwards the p plug is formed with another mask and then the n source layers are formed with a fourth mask. As four different masks are used, this method is susceptible to mask misalignments. Furthermore, angled implantation is used for forming the layers, which makes the implantation more difficult. As the n source layers and the p plug have a comparable doping concentration, there is a danger in the transition area between the two layers of compensated charges, i.e. there may be no dominating charge so that there is an undesired neutralized zone.

Disclosure of Invention

It is an object of the invention to provide a method for manufacturing a power semiconductor device having improved electrical properties comprising the following manufacturing steps:

(a)   providing a wide bandgap substrate having a lowly doped layer of a first conductivity type forming a drift layer in the semiconductor device, the substrate having a first side and a second side opposite to the first side, wherein the lowly doped layer is arranged on the first side,

(a)   then forming on the first side two source regions of the first conductivity type having higher doping concentration than the drift layer up to a source region depth,

at least one channel layer of a second conductivity type, which is different from the first conductivity type, having a channel layer depth and surrounding the two source regions in a lateral direction, which direction is parallel to the first side, thereby separating the two source regions from the drift layer in the lateral direction, and

at least one well layer of the second conductivity type having a well layer depth, which is at least as large as the channel layer depth, and having a higher doping concentration than the at least one channel layer, wherein the at least one well layer separates the two source regions from the drift

layer on a side of the at least one well layer opposite to the first side, wherein applying a first mask on the first side having openings, which first mask comprises a first mask layer and a second mask layer on top of the first mask layer, wherein the first mask layer has a higher etching

5   selectivity than the second mask layer,

then applying a second dopant of the first conductivity type for forming the two source regions up to the source region depth,

then removing such part of the first mask, which is arranged between the two source regions, thereby forming a second mask,

10   then applying a third dopant of the second conductivity type for forming the at least one well layer up to the well layer depth,

performing an etching step on the first side, by which etching the first mask layer is farther removed at the openings than the second mask layer,

removing the second mask layer, wherein the remaining first mask layer

15   forming a third mask,

then applying a first dopant of the second conductivity type for forming two channel layers up to the channel layer depth.

   (b)

   (c) after step (b) forming a plug of the second conductivity type having a plug

20   depth, which is at least as great as the well layer depth, and having a higher doping concentration than the at least one well layer, wherein the plug is arranged between the two source regions,

   (d) after step (c) forming two gate electrodes on the first side, each of which is separated from any doped layer by an insulating layer,

25   (e) after step (c) forming a first main electrode as an ohmic contact on the first side, which at least contacts the two source regions and the plug.

The masks for forming the well and the channel layers are self-aligned to the mask for forming the n source regions, which makes the manufacturing method reliable and of high quality due to the mask for forming the plug covering the n

30 source regions completely, there is no overcompensation of the charges of the n source regions and the plug, which means that there is no neutral zone in the device, which allows better operation of the device. The channel and well layers have a much lower doping concentration than the source regions, so that an overcompensation of these layers does not lead to a neutralized zone, but allows

35 to provide an easy manufacturing method.

A MOS (metal-oxide-semiconductor) cell is formed by the layers/regions beforehand. The deep highly doped plug improves the contact to the well layer. Its depth is as least as great as the depth of the well layer to protect the channel layers of the MOS cell from peaks of the electric field, which are highest

5   underneath the center of the MOS cell, i.e. below the location of the plug. This avoids undesired parasitic actions (parasitic transistor in case of a MOSFET and parasitic thyristor in case of an IGBT) as well as it diminishes short-channel effects (see FIG 19). In this FIG 19, it is shown that for a 300 nm wide channel (being the extension of the channel layer between the source region and the drift layer) the

10   leakage current abruptly rises for forward blocking voltages smaller than the avalanche breakdown voltage, resulting in a premature breakdown of the device. For an inventive MOSFET with the same channel width, breakdown can be shifted to higher forward blocking voltages.

In addition the strength of the electric field in the gate-insulator gets reduced by

15   the plug, wherein the effect is more pronounced for deeper plugs. The FIGs 15 to 18 show the electric fields through different planes of the MOS-cell of the device. In FIGs 15 to 18, the plug depth is given relative to the depth of the p well layer. "Prior Art" means that the plug is less deep than the p-well layer. "D1" means that the plug and the p-well layer have the same depth. "D2" shall mean that the plug

20   depth is 1.5 times the well layer depth and "D3" means that the plug depth is two times larger than the well layer depth.

FIG 15 shows the electric field from the first to the second main side between two MOS cells (cut along line A - - A in FIG 2). FIG 16 is a detail from FIG 15 at the interface between the first insulating layer 72 of the gate electrode 7 and the

25   drift layer 2 (dotted area of FIG 15). From this figure it is obvious, that the electric field is reduced in the wide bandgap material as well as in the insulating layer of the gate electrode (e.g. gate oxide). FIG 17 shows the electric field in a plane parallel to the first main side (cut along line B - - B in FIG 2); showing the electric field in a non-depleted region 47 of the channel layer and in a depleted region 48

30   of the channel layer. FIG 18 shows the electric field along line C - - C in FIG 2, which plane lies parallel to line A - - A and goes through the channel layer. For all planes, a tremendous reduction of the electric field is obvious, this effect even being larger, because of the plug in the prior art devices having a plug depth, which is smaller as compared to the well layer depth.

Due to the high doping concentration of the plug a good ohmic contact is established to the first main electrode.

Further preferred embodiments of the inventive subject matter are disclosed in the dependent claims.

5   ## Brief Description of Drawings

The subject matter of the invention will be explained in more detail in the following text with reference to the attached drawings, in which:

FIG 1 shows an inventive IGBT;

FIG 2 shows an inventive MOSFET;

10   FIGs 3 and 5 to 13 show steps for an inventive method for manufacturing a wide bandgap semiconductor device (IGBT/MOSFET);

FIG 4 shows an alternative manufacturing step (a);

FIG 14 shows a prior art silicon-carbide MOSFET;

FIG 14 to 18 show electric fields along different cuts through the MOS-cell

15   architecture shown exemplary in FIG 2; and

FIG 19 shows the diminishing of short-channel effects which cause premature breakdown.

The reference symbols used in the figures and their meaning are summarized in the list of reference symbols. Generally, alike or alike-functioning parts are given

20   the same reference symbols. The described embodiments are meant as examples and shall not confine the invention.

Modes for Carrying out the Invention

FIG 1 shows an inventive insulated gate bipolar transistor (IGBT) 1. The IGBT 1 is a wide bandgap device, e.g. a silicon carbide device, comprising a lowly (n-)

25   doped drift layer 2 between a first main side 20 and a second main side 22 of the device opposite to the first main side 20. Wide band gap materials shall be materials having a bandgap of at least 2 eV like silicon carbide, gallium nitride or diamond not excluding other wide bandgap materials. Depending on the voltage class, the doping concentration and thickness of the drift layer 2 are chosen.

30   Exemplarily, the drift layer 2 has a doping concentration between $1 * 10^{12}$ and $1 *$

10^{17} cm^{-3} and a thickness between 1 to 500 µm. The thicknesses shall be measured in depth direction, i.e. in a direction vertical to the first main side 20.

For an inventive IGBT, a p+ doped collector layer 8 is arranged on the second main side 22 and has exemplarily a doping concentration between 1 * 10^{18} and 1 * 10^{20} cm^{-3}. The collector layer 8 contacts a second main electrode 90, which is a collector electrode for an IGBT. Between the drift layer 2 and the collector layer 8, an n doped buffer layer 25 may be arranged, which has a higher doping concentration than the drift layer 2 (shown in FIG 1 by a dashed line). The buffer layer may have an exemplary doping concentration between 1 * 10^{17} and 1 * 10^{19} cm^{-3} and a thickness up to 3 µm.

For an inventive MOSFET as shown in FIG 2, on the second main side 22, an n+ doped drain layer 80 is arranged, which has exemplarily a doping concentration between 1 * 10^{18} and 1 * 10^{20} cm^{-3}. The drain layer 80 contacts a second main electrode 90, which is a drain electrode for a MOSFET.

In the following, the design on the first main side 20 is further explained for the example of an IGBT (FIG 1), but is also applicable to a MOSFET (FIG 2).

On the first main side 20 two n++ doped source regions 3, 3' having a source region depth 30 are arranged, which have a higher doping concentration than the drift layer 2. All depths shall be measured from the first main side 20, i.e. the depths shall be the maximum distance in depth direction, to which a layer/region extends. Exemplarily, the source region depth 30 measures up to 0.5 µm. The doping concentration may vary between 1 * 10^{18} and 1 * 10^{21} cm^{-3} or between 1 * 10^{19} and 1 * 10^{21} cm^{-3}. Exemplarily, the source regions 3, 3' belonging to one MOS cell have a lateral distance from each other of up to 7 µm.

On both outer lateral sides of the source regions 3, 3' (on the outer lateral sides of the n++ source regions not facing each other, i.e. which do not form a common opening in between, and which lie below a gate electrode 7) p doped channel layers 4, 4' are arranged. Thus, the p channel layers 4, 4' surround the n source regions 3, 3' on the outer lateral sides, i.e. on a side of the n source regions 3, 3' parallel to the first main side 20 and below the gate electrodes 7. Exemplarily, the channel layers 4, 4' have a channel layer depth 40, which is deeper than the source region depth 30. Each source region 3, 3' is separated from the drift layer 2 in lateral direction by a channel layer 4, 4' in a direction parallel to the first main side 20. The channel layer 4, 4' may have a doping concentration between 1 * 10^{16} and 1 * 10^{18} cm^{-3}.

P+ doped well layers 5, 5' which have a higher doping concentration than the channel layers 4, 4', separate the two source regions 3, 3' from the drift layer 2 on a side of the well layer opposite to the first main side 20.

5   Exemplarily, the doping concentration of the well layers 5, 5' may be at least 10 times higher than the doping concentration of the channel layers 4, 4' or the doping concentration of the well layers 5, 5' may be between 10 times and 100 times higher than the doping concentration of the channel layers 4, 4'. The well layers 5, 5' may have a doping concentration between $1 * 10^{17}$ and $1 * 10^{21}$ cm^{-3} or $1 * 10^{18}$ and $1 * 10^{20}$ cm^{-3}.

10   The well layers 5, 5' have a well layer depth 50, which is at least as large as the channel layer depth 40. Thus, the well layers 5, 5' may extend to the same depth as the channel layers 4, 4' or they may be deeper than the channel layers 4, 4'. The depth of the well layers 5, 5' and/or the channel layers 4, 4' may exemplarily be up to 3 µm.

15   In the channel layers 4, 4', a MOS channel may be formed from the source regions 3, 3' to drift layer 2. The channel extends in the substrate product 10 from the source region 3, 3' close to the surface to the drift layer 2. Thus, the doping concentration of the channel layers 4, 4', which has to be lower than the doping concentration of the well layers 5, 5', is the doping concentration from the first

20   main side 20 at maximum up to the depth of the source regions 3, 3', i.e. up to a depth, in which the channel is formable.

The channel layers 4, 4' and well layers 5, 5' may be designed as common layers (combined layer 4, 5 and combined layer 4', 5')) having a retrograde profile, such that the common layers have a low doping concentration at the first main

25   side and in the region beneath, i.e. close to the first main side, and lateral to the source regions 3, 3' (in which region the channel is formable), and the doping concentration then rises to a higher value underneath the source regions 3, 3'. For the formation of the channel it is of inferior importance that the common layer has a higher doping concentration lateral to the source region, but in greater depth

30   than the source regions 3, 3' (due to the common layer having a retrograde profile), because in such a great depth no channel is formed. The higher doping concentration of the common layer lateral to the source region, but in greater depth than the source regions 3, 3' improves the shielding of the high electric field (inside the device during blocking conditions) from the channel layer.

Between the two source regions 3, 3', a p++ doped plug 6 is arranged, which has a higher doping concentration than the well layers 5, 5'. In an exemplary embodiment, the doping concentration of the plug 6 is at least 10 times higher than the doping concentration of the well layer 5, 5'. In another exemplary

5   embodiment, the doping concentration of the plug 6 is between 10 times and 100 times higher than the doping concentration of the well layer 5, 5'. The plug 6 may have a doping concentration between $2 * 10^{17}$ and $2 * 10^{21}$ cm^{-3} or between $1 * 10^{19}$ and $2 * 10^{21}$ cm^{-3}.

The plug 6 has a plug depth 60, which is as least as deep as the well layer

10   depth 50, exemplarily greater than the well layer depth 50. The plug 6 does not overlap with the n source regions 3, 3', i.e. the doping concentration of the n source regions 3,3 ' is constant in planes parallel to the first main side 20 and the doping concentration of the p plug is constant in planes parallel to the first main side 20. The doping concentration of the n source regions 3, 3' and of the plug 6 is

15   not compensated at the interface between the two layers 3, 6 or 3', 6.

Between the plug 6 and the two source regions 3, 3', the well layer 5, 5' may extend to the first main side 20 and contact the first main electrode 9. Thus, the well layers 5, 5' may separate the plug 6 from the source regions 3, 3'. By such an arrangement, it is ensured that the source regions 3, 3' do not overlap with the

20   plug 6. As the intrinsic doping level of a wide bandgap semiconductor material is negligible as compared to a low-band gap semiconductor material (e.g. Silicon) and as the doping concentrations of the plug 6 and source regions 3, 3' are within the same order of magnitude, by an overlap of the n and p doped layers a region could be formed, in which no dopant is electronically active, i.e. such a region

25   would be insulating. Such an effect is avoided by the inventive structure.

The source regions 3, 3' are separated from the drift layer 2 by the plug 6, the well layers 5, 5' and the channel layers 4, 4'.

The plug 6, the well layers 5, 5' (if they extends to the first main side 20), the source regions 3, 3', the channel layers 4, 4' and the drift layer 2 form a planar

30   plane on the first main side 20. Thus, these layers form a common surface on the first main side 20, which is planar.

On the first main side 20, gate electrodes 7 are arranged, each of which comprises a first insulating layer 72, a second insulating layer 74 and a gate layer 70, which is separated from any doped layer by the first insulating layer 72. The

35   source regions 3, 3', the channel layers 4, 4 ' and the drift layer 2 extend to the

gate electrode 7, i.e. to the first insulating layer 72. The gate electrodes 7 are
formed as a planar gate electrodes (as shown in FIG 1 and 2), wherein the gate
electrodes 7 are arranged on top of the source regions 3, 3', the channel layers 4,
4' and the drift layer 2 such that a MOS channel may be generated in the channel
5   layer 4, 4' below the gate electrode 7 between the source regions 3, 3' and the
drift layer 2 by inversion of the channel layer p by the application of a gate-voltage
larger than the threshold-voltage of the MOS interface.

    In case of the first insulating layer 72 being an oxide layer and the gate layer 70
being a metal, the inversion-channel is called a MOS channel (metal-
10   oxide/insulator-semiconductor), whereas otherwise (insulating layers 72, 74 being
made of any insulating materials; e.g. dielectrics such as high-k materials or
Silicate glasses such as PSG or BPSG not excluding other insulators) the channel
may also be called MIS channel (metal-insulator-semiconductor). As a material for
the gate layer 70 any appropriate electrically conductive material like a metal or
15   doped polycrystalline silicon may be used. The term MOS device/MOSFET shall
also cover such MIS devices/ MISFETs and applies also for IGBTs which are
MOS/MIS-controlled.

    A first main electrode 9 is formed as an ohmic contact on the first main side 20,
which contacts the two source regions 3, 3' and the plug 6, and if the well layer 5,
20   5' extends to the surface on the first main side 20, also the well layer 5, 5' contacts
the first main electrode 9. For an IGBT 1 as shown in FIG 1 the first main electrode
9 functions as an emitter electrode, for a MOSFET as shown in FIG 2, the first
main electrode 9 functions as a source electrode. The first main electrode 9 may
be formed by first forming a metallic layer in the opening between two gate
25   electrodes 7 to form an ohmic contact to the plug 6, the well layer 5, 5' and the
source regions 3, 3'. On top of the metallic layer forming the ohmic contact,
another metallic layer is then generated, which contacts the first metallic layer.
Additionally the second metallic layer also covers the area on top of the gate
electrode 7, i.e. it covers the second insulating layer 74 and is thereby insulated
30   from the gate layer 70.

    The structure disclosed beforehand forms a MOS cell to control an IGBT and/or
MOSFET. The MOS cell is formed between one first main electrode contact
opening and the second electrode 90, i.e. the MOS comprises the plug 6, the well
layers 4, 4' on both sides of the plug 6, the source regions 3, 3', the channel layers
35   4, 4', the drift layer 2 and the collector layer 8 or the drain layer 80.

The cells, i.e. the regions in the cell may be designed to form of regular patterns like stripes, hexagonal, triangular or square design. In a power semiconductor device, one or more of such MOS cells may be arranged. Such MOS cells may be interconnected to each other.

5   The devices may be designed as vertical devices as shown in the FIGs 1 and 2, but it is also possible to have them designed as lateral devices, in which source and drain (MOSFET) or emitter and collector (IGBT) are arranged on the same side of the device. For an inventive IGBT, the inventive deep plug 6 is applicable for all different kinds of IGBTs such as reverse conducting IGBTs having

10   alternatingly p+ collector regions and n+ short regions arranged on the second main side 22, exemplarily also as a Bi-mode Insulated Gate Transistor (BIGT) additionally having a large pilot p+ collector region in the central part of the device on the second main side 22 surrounded by alternating smaller p+ and n+ short regions. The pilot and short regions may be connected. Such BIGTs are disclosed

15   in US 8 212 283 B2, which document shall be incorporated by reference for the design of a BIGT.

The inventive IGBT may be designed as a non punch-through IGBT or as a punch-through/soft-punch-through IGBT having a buffer layer 25 arranged between the n- doped drift layer 2 and the p+ doped collector layer 8. In case of

20   the non-punch through design the E-field is triangular in shape up to avalanche breakdown. In the other cases the E-field penetrates through the interface between drift layer 2 and buffer layer 25 where it gets stopped due to the high doping concentration of the buffer layer.

Super-Junction designs are possible for all kind of inventive devices. An

25   exemplary technological approach for superjunctions is based on either trench-etching followed by epitaxial-refill or sequential epitaxial growth followed by multiple implantation, not excluding other techniques.

For manufacturing an inventive wide bandgap semiconductor device, the following manufacturing steps are performed. In a step (a) a wide bandgap

30   substrate product 10 having a lowly doped layer of a first conductivity type forming a drift layer 2 in the semiconductor device is provided. The substrate product 10 has a first side 12 and a second side 14 opposite to the first side 12, wherein the lowly doped layer is arranged on the first side 12. On the second side 14, the substrate product 10 comprises in the case of a vertical IGBT a p+ doped

substrate, which or part of which forms the collector layer 8 in the finalized IGBT device. The layer 8 may be thinned down at the end of the manufacturing process.

In a step (b) on the first side 12 two n doped source regions 3, 3' having higher doping concentration than the drift layer 2 are formed up to a source region depth 30. At least one p doped channel layer 4, 4' having a channel layer depth 40 is formed. Each source region 3, 3' is separated from the drift layer 2 by a channel layer 4, 4' in a direction perpendicular to the first side 12. The channel layer depth 40 is larger than the source region depth 30. At least one p+ doped well layer 5, 5' having a well layer depth 50, which is at least as large as the channel layer depth 40, and having a higher doping concentration than the at least one channel layer 4, 4' is formed. The well layer 5, 5' separates the two source regions 3 from the drift layer 2 on a side of the well layer opposite to the first side 12.

In a step (c) and after step (b) a p++ doped plug 6 is formed having a plug depth 60, which is larger than the well layer depth 50. The plug is arranged between the two source regions 3, 3'. The doping concentration of the plug 6 is larger than that of the well layer 5. The doping concentration of the plug may be at least 10 times higher than the doping concentration of the well layer 5. In another exemplary embodiment, the plug 6 may be formed with a doping concentration, which is between 10 times and 100 times higher than the doping concentration of the well layer 5. The plug 6 may be formed with a doping concentration between $2 * 10^{17}$ and $2 * 10^{21}$ cm^{-3} or between $1 * 10^{19}$ and $2 * 10^{21}$ cm^{-3}. The plug may have a width of at maximum 5 μm or at maximum 3 μm.

In a step (d) after step (c) gate electrodes 7 are formed on the first side 12. Each gate electrode 7 comprises an electrically conductive gate layer 70, which is separated from any doped layer by an insulating layer in form of a thin first insulating layer 72. Exemplarily, a second insulating layer 74, which is thicker than the first insulating layer 72, is formed on top of the gate layer 70.

In a step (e) after step (c) a first main electrode 9 is formed as an ohmic contact on the first side 12, which at least contacts the two source regions 3, 3' and the plug 6.

In the FIGs 3 and 6 to 13 a method for manufacturing a wide bandgap non punch-through power IGBT is shown. In FIG 3 the substrate product of step (a) is shown. The substrate product 10 comprises a lowly doped layer forming the drift layer 2 in the device. On the second side 14, the substrate product 10 comprises a higher p+ doped layer forming the collector layer 8. Exemplarily the substrate

product 10 is made by providing a p+ doped substrate, which forms a collector layer 8 in the finalized IGBT, on which a lowly (n-) doped layer as a drift layer 2 is formed, exemplarily by epitaxial growth. The p+ doped layer may be thinned down at the end of the manufacturing process to form the collector layer 8.

5   Alternatively, as shown in FIG 4, for a punch-through IGBT, in which a buffer layer 25 is arranged between the drift layer 2 and the collector layer 8, a p+ doped substrate may be provided. On the p+ doped substrate, first an n doped buffer layer 25 and then an n- doped drift layer 2 is formed, exemplarily by epitaxial growth. Again, the p+ doped layer may be thinned down at the end of the

10   manufacturing process to form the collector layer 8.

By such an epitaxial growth, exemplarily a layer of constant doping concentration is formed, but of course also a variation of doping concentration is possible, e.g. a decreasing doping concentration in direction from the first side 12 to the second side 14. The values for the doping concentration given above shall

15   be understood as the mean doping concentration in case of constant doping concentration (not excluding variation of doping concentration due to imperfection of the manufacturing method) or as a maximum doping concentration in case of varying doping concentration. The same shall apply for implanted profiles which are defined by multiple cascades with different energies and doses and may form

20   any kind of graded profile by the superposition of several Gaussian profiles, for each cascade one Gaussian profile.

For forming an inventive MOSFET, a substrate product 10 may be provided (FIG 5) which is made by providing an n+ doped substrate, which or part of which forms the drain layer 80 in the finalized MOSFET device. On the n+ doped

25   substrate, a drift layer 2 may be formed, e.g. by epitaxial growth. The n+ doped layer may be thinned down at the end of the manufacturing process to form the drain layer 80.

After having provided a lowly doped substrate product 10 (FIG 3, 4 or 5) in step (a), a first mask layer 35 and on top of it a second mask layer 36 is applied on the

30   first side 12. The first mask layer 35 has a higher etching selectivity than the second mask layer 36, what shall mean that in the following etching process the material of the first mask layer 35 is more sensitive to the etching process than the material of the second mask layer 36. Openings are formed through the first and second mask layer 35, 36 down to the substrate product 10 (i.e. to the drift layer

35   2), thereby forming a first mask 34 on the first side 12 (FIG 6). A second dopant 31

(n dopant) is applied for forming the two source regions 3, 3' up to the source region depth 30. These source regions 3, 3' are shallower, but higher doped than the channel layers 4, 4', so that the channel layers 4, 4 'separate the source regions 3, 3' from the drift layer 2. The second dopant 31 is applied with a dose of

5   exemplarily between $1 * 10^{13}$ and $1 * 10^{16}$ cm^{-2} and/or an energy between 1 keV and 500 keV up to a source region depth 30 of exemplarily at maximum 0.5 μm. The implantation/deposition may be performed at a temperature higher than room temperature, exemplarily at a temperature up to 700 °C.

        The total mask stack shall have such a thickness that a dopant is hindered from

10   penetration into the substrate product 10 in such areas, which are covered by the mask. The dopants shall penetrate into the substrate product 10 at the positions of the mask openings.

        Then such part of the first mask 34 is removed, which is arranged between the two source regions 3, 3', thereby forming a second mask 54, which is self-aligned

15   to the first mask 34 (FIG 7). A third dopant 51 (p dopant) is applied (implanted/deposited) for the formation of the well layer 5 up to the well layer depth 50.

        The third dopant 51, e.g. aluminum or boron, is applied with a dose between $1 *$ 10^{11} and $1 * 10^{16}$ cm^{-2} and/or an energy between 1 keV and 1 MeV up to a well

20   layer depth 50 of exemplarily at maximum 2 μm. The well layer 5 is formed to have a doping concentration, which is at least 10 times higher than the doping concentration of the at least one channel layer 4, 4' or, exemplarily to have a doping concentration which is between 10 times and 100 times higher than the doping concentration of the at least one channel layer 4, 4'. The doping

25   concentration of the well layer 5 may be between $1 * 10^{18}$ and $1 * 10^{20}$ cm^{-3} or between $1 * 10^{17}$ and $1 * 10^{21}$ cm^{-3}.

        The well layer 5 may also be formed with a retrograde profile, which means that a maximum doping concentration of the well layer 5 is arranged close to the p/n junction to the drift layer 2, whereas the local doping concentration decreases

30   towards the first main side 20. The doping concentrations of the layers/regions shall be understood as the maximum doping concentrations of the layers/regions if not stated otherwise.

        Again, the implantation/deposition may be performed at a temperature higher than room temperature, exemplarily at a temperature up to 700 °C.

Now an etching step is performed on the first side 12, by which etching the first mask layer 35 is farther removed at the openings than the second mask layer 36 due to the higher etching selectivity of the first mask layer 35 so that the openings are enlarged in a self-aligned manner. The second mask layer 36 may now be

5 removed, thereby forming a third mask 46 from the remaining first mask layer 35'. Then a first dopant 41 (p dopant) is applied for forming the channel layers 4, 4' up to the channel layer depth 40 (FIG 8).

The first dopant 41 (p dopant) is applied, e.g. by implantation or deposition for forming the channel layers 4, 4'. In an exemplary embodiment, aluminum or boron

10 is applied as first dopant 41. This process may be performed at an elevated temperature, exemplarily at a temperature up to 700 °C. All dopants 31, 41, 51, 61 are applied at any appropriate angle to the first main side 20. They may be applied perpendicular to the first main side 20, but if desired any other incident angle may be used.

15 For the implantation (deposition) a dose between $1 * 10^{11}$ and $1 * 10^{16}$ cm^{-2} and/or an energy between 1 keV and 1 MeV may be applied. Thus, channel layers 4, 4' may be formed having a doping concentration between $1 * 10^{16}$ and $1 * 10^{18}$ cm^{-3}. The first dopant 41 may be applied into a channel layer depth 40 of at maximum 2 μm.

20 The well layer depth 50 is at least as large as the channel layer depth 40. It shall be ensured that the well layer does not deplete during blocking conditions, thereby preventing a short between the first and second main electrode.

The source regions 3, 3' are overcompensated layers, which means that in these layers also a dopant of the other conductivity type is present, e.g. in the

25 source regions 3, 3' also the first dopant 41 for the channel layer 4, 4' and the third dopant 51 for the well layer 5, 5' are applied, but as the second n dopant 31 dominates, this layer is n-type (higher n-doping concentration).

As shown in FIG 9, the third mask 46 is then removed after having formed the source regions 3, 3', channel layers 4, 4' and well layer 5. A new continuous mask

30 material layer which can be made from oxide is applied and etched to have an opening above the region between the two source regions 3, 3', thereby forming a fourth mask 62 (FIG 10). A fourth dopant 61 (p dopant, e.g. Al or B) may be applied, e.g. with a dose between $1 * 10^{11}$ and $1 * 10^{16}$ cm^{-2} and/or an energy between 1 keV and 1 MeV up to a plug depth 60, which is at least as great as or

35 greater than the well layer depth 50. Exemplarily, the plug depth 60 is 1.05 to 1.5

times (i.e. 5 to 50 %) or up to two or even up to four times larger than the well

layer depth 50 (FIG 10). An activation anneal step at a high temperature, e.g.

between 1500 °C to 1900 °C may follow. Afterwards, a sacrificial oxidation step

may be performed. Due to the introduction of the plug 6, the well layer 5 is split

5   into two well layers 5, 5'.

Now the fourth mask 62 is removed (FIG 11) and gate electrodes 7 are formed

(FIG 12) by applying first insulating layer 72s, which cover the drift layer 2 at those

parts extending to the surface at the first side 12, the channel layers 4, 4 ' and the

outer parts of the source regions 3, 3'. The outer parts shall means those parts of

10   the two source regions 3, 3' not facing each other. An electrically conductive gate

layer 70 is applied and on top of it, a second insulating layer 74 is applied which

electrically insulates the gate layer 70 from the first main electrode 9. In the

opening on top of the source regions 3, 3' not covered by the gate electrode 7 with

the plug 6 and the well layer 5, 5' in between, a first main electrode 9 as ohmic

15   contact in form of an emitter electrode for an IGBT 1 or a source electrode for a

MOSFET 1' (metal-oxide semiconductor field-effect transistor) is formed.

Exemplarily, the first main electrode 9 is formedby first applying a metallic layer in

the opening to contact the p++ plug 6, the well layers 5, 5' and the source regions

3, 3' and then another metallic layer additionally covering the second insulating

20   layer 74 on top of the gate layer 70 is applied (FIG 13).

On the second side 14, a second main electrode 90 as ohmic contact in form of

a collector electrode for an IGBT 1 or a drain electrode for a MOSFET 1' is formed.

In the process, shown in the FIGs 6 to 13, p channel layers 4, 4' and source

regions 3, 3' are formedin one MOS cell as separate regions, wherein the well

25   layer 5 are first formedas one common layer (FIG 8) and by the introduction of the

p++ plug 6 the well layer 5, 5' is split into two separate well layers 5, 5' on the

lateral sides of the plug 6. Therefore, the term well layer shall also cover two well

layers 5, 5', separated from each other by the plug 6 and the term channel layer

shall cover two channel layers 4, 4', separated from each other by the well layers

30   5, 5'.

In the process, shown in the FIGs 6 to 8, p channel layers 4, 4' and source

regions 3, 3' are formed in one MOS cell as separate regions (source regions 3, 3'

as separate regions by masking and channel layers 4, 4' by the region being

dominated in the central area by the higher doping concentration of the well layer

35   5, 5', wherein the well layers 5, 5' are first formed as one common layer 5 (FIG 8)

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and by the introduction of the p++ plug 6 the well layer 5 is split into two separate well layers 5, 5' on the lateral sides of the plug 6.

In another alternative manufacturing method, in step (b) a retrograde p doped layer as a common channel and well layer (4, 4', 5, 5') is formed and source

5   regions 3, 3' are formed before or after the retrograde layer (4, 4', 5, 5'). The retrograde layer (4, 4', 5, 5') has such doping concentration that on the outer lateral sides of the source regions 3, 3' the retrograde layer has a low doping concentration (i.e. channel layers 4, 4') at the first side 12, which then rises to greater depths (at least up to the source region depth 30) to a high doping

10   concentration below the source regions 3, 3' (i.e. well layers 5, 5'). By the later introduction of the plug 6 the common retrograde layer is split into a retrograde layer 4, 5 and 4', 5'. The retrograde layer may be formed by the process described above, i.e. by first forming the well layer 5, 5' and then forming the wider channel layer 4, 4'. Alternatively, for forming a common retrograde layer 4, 4', 5, 5' in step

15   (b) after having formed the source regions 3, 3', such part of the first mask 34, which is arranged between the two source regions 3, 3', thereby forming a second mask 54, and then performing an etching step on the first side 12, by which etching the first mask layer 35 is farther removed at the openings than the second mask layer 36, and removing the second mask layer 36, wherein the remaining

20   first mask layer 35' forming a third mask 46. Then the p third dopant 51 and the p first dopant 41 are applied as one common dopant for forming a retrograde channel and well layer in one step.

The plug 6 may also be formed as a retrograde layer having a lower doping concentration in shallow depth and a higher up to a maximum doping

25   concentration in greater depth, which depth may exemplarily be located as deep as the depth of the maximum doping concentration of the well layers 5, 5' or deeper.

The inventive structure and manufacturing method having a deep p++ plug may be applied to different semiconductor devices having MOS cell structures such as

30   MOSFETs and MOS controlled IGBTs.

In another embodiment, the conductivity types of the layers are switched, i.e. all layers of the first conductivity type are p type (e.g. the drift layer 2 and the source regions 3) and all layers of the second conductivity type are n type (e.g. channel layer 4, the well layer 5 and the plug 6).

35

Reference List

1	IGBT
1'	MOSFET
10	wide bandgap substrate product
12	first side
14	second side
2	drift layer
20	first main side
22	second main side
25	buffer layer
3, 3'	source region
31	second dopant
30	source region depth
34	first mask
35	first mask layer
35'	remaining first mask layer
36	second mask layer
4, 4'	channel layer
41	first dopant
40	channel layer depth
41	first dopant
44	polycrystalline silicon layer
45	oxide layer
46	third mask
47	non-depleted channel layer
48	depleted channel layer
49	top mask layer
49'	remaining top mask layer
5, 5'	well layer
50	well layer depth
51	third dopant
54	second mask
6	plug
60	plug depth
61	fourth dopant

62	fourth mask
65	contact layer
67	contact layer depth
7	gate electrode
70	gate layer
72	first insulating layer
74	second insulating layer
8	collector layer
80	drain layer
9	first main electrode
90	second main electrode

CLAIMS

1. A method of manufacturing a semiconductor device comprising following manufacturing steps:

(a) providing a wide bandgap substrate product (10) having a lowly doped layer of a first conductivity type forming a drift layer (2) in the semiconductor device, the substrate product (10) having a first side (12) and a second side (14) opposite to the first side (12), wherein the lowly doped layer is arranged on the first side (12),

(b) then forming in the wide bandgap substrate product on the first side (12) two source regions (3, 3') of the first conductivity type having higher doping concentration than the drift layer (2) up to a source region depth (30), two channel layers (4, 4') of a second conductivity type, which is different from the first conductivity type, having a channel layer depth (40) and surrounding the two source regions (3, 3') in a lateral direction, which direction is parallel to the first side (12), thereby separating the two source regions (3, 3') from the drift layer (2) in the lateral direction, and at least one well layer (5, 5') of the second conductivity type having a well layer depth (50), which is at least as large as the channel layer depth (40), and having a higher doping concentration than the at least one channel layer (4, 4'), wherein the at least one well layer (5, 5') separates the two source regions (3, 3') from the drift layer (2) on a side of the at least one well layer opposite to the first side (12), wherein applying a first mask (34) on the first side (12) having openings for the creation of the two source regions (3, 3'), which first mask (34) comprises a first mask layer (35) and a second mask layer (36) on top of the first mask layer (35), wherein the first mask layer (35) has a higher etching selectivity than the second mask layer (36), then applying a second dopant (31) of the first conductivity type for the creation of the two source regions (3, 3') up to the source region depth (30), then removing such part of the first mask (34), which is arranged between the two source regions (3, 3'), thereby forming a second mask (54), applying a third dopant (51) of the second conductivity type for forming the at least one well layer (5, 5') up to the well layer depth (50), performing an etching step on the first side (12), by which etching the first

mask layer (35) is farther removed at the openings than the second mask layer (36),

removing the second mask layer (36), wherein the remaining first mask layer (35') forming a third mask (46),

5   then applying a first dopant (41) of the second conductivity type for tforming two channel layers (4, 4') up to the channel layer depth (40).

(c) after step (b) applying a fourth mask, which at least covers the two source regions (3, 3') and the two channel layers (4, 4'),

then applying a fourth dopant of the second conductivity type for forming

10   a plug (6) having a plug depth (60), which is as least as great as the well layer depth (50), and having a higher doping concentration than the at least one well layer (5, 5'),

(d) after step (c) forming two gate electrodes (7) on the first side (12), each of which is separated from any doped layer by an insulating layer,

15   (e) after step (c) forming a first main electrode (9) as an ohmic contact on the first side (12), which at least contacts the two source regions (3, 3') and the plug (6).

2.   The method of manufacturing the semiconductor device according to a claim 1, characterized in, that

20   in step (c) applying the fourth mask such that the fourth mask projects a part of the well layer (5, 5') adjoining the two source regions (3, 3') such that the at least one well layer (5, 5') surrounds the plug (6) in the lateral direction and such that the at least one well layer (5, 5') separates the plug (6) from the two source regions (3, 3').

25   3.   The method of manufacturing the semiconductor device according to any of the claims 1 to 2, characterized in, that

in step (c) forming the plug (6) with a doping concentration, which is at least 10 times higher than the doping concentration of the at least one well layer (5, 5') or in that

30   forming the plug (6) with a doping concentration, which is between 10 times and 100 times higher than the doping concentration of the at least one well layer (5, 5').

4.   The method of manufacturing the semiconductor device according to any of the claims 1 to 4, characterized in, that

35   in step (b) forming the at least one well layer (5, 5') with a doping

concentration, which is at least 10 times higher than the doping concentration of the two channel layers (4, 4') or in that

in step (b) forming the at least one well layer (5, 5') with a doping concentration which is between 10 times and 100 times higher than the doping concentration of the two channel layers (4, 4').

5. The method of manufacturing the semiconductor device according to any of the claims 1 to 6, characterized in, that

in step (b) forming the at least one well layer (5, 5') with a doping concentration between $1 * 10^{17}$ and $1 * 10^{21}$ cm^{-3} or between $1 * 10^{18}$ and $1 * 10^{20}$ cm^{-3}.

6. The method of manufacturing the semiconductor device according to any of the claims 1 to 8, characterized in, that

in step (b) forming the two channel layers (4, 4') with a doping concentration between $1 * 10^{16}$ and $1 * 10^{18}$ cm^{-3}.

7. The method of manufacturing the semiconductor device according to any of the claims 1 to 9, characterized in, that

– in step (c) forming the plug (6) with a doping concentration between $2 * 10^{17}$ and $2 * 10^{21}$ cm^{-3} or between $1 * 10^{19}$ and $2 * 10^{21}$ cm^{-3}.

8. The method of manufacturing the semiconductor device according to any of the claims 1 to 11, characterized in, that in step (b) forming the at least one well layer (5, 5') and the two channel layers (4, 4') as a common layer (4, 5 and 4', 5') having a low doping concentration at the first side (12) in a region lateral to the source regions (3, 3'), and the doping concentration then rising to a higher doping concentration underneath the source regions (3, 3').

9. A wide bandgap semiconductor device comprising a lowly doped drift layer (2) of a first conductivity type between a first main side (20) and a second main side (22) of the device opposite to the first main side (20),

further comprising on the first main side (20) two source regions (3, 3') of the first conductivity type having a source region depth (30), which two source regions (3, 3') have higher doping concentration than the drift layer (2),

two channel layers (4, 4') of a second conductivity type, which is different from the first conductivity type, having a channel layer depth (40), which is at least as great as the source region depth (30), wherein each source region (3, 3') is separated from the drift layer (2) by a channel layer (4, 4') in a direction parallel to the first main side (20), and

two well layers (5, 5') of the second conductivity type having a well layer depth (50), which is at least as large as the channel layer depth (40), wherein the well layers (5) have a higher doping concentration than the channel layers (4, 4') and wherein the well layers (5, 5') separate the two source regions (3, 3') from the drift layer (2) on a side of the well layers opposite to the first main side (20),

a plug (6) of the second conductivity type having a plug depth (60), which is as least as great as the well layer depth (50), and having a higher doping concentration than the well layers (5, 5'), wherein the plug (6) is arranged between the two source regions (3, 3'),

wherein the two well layers (5, 5') surround the plug (6) in the lateral direction and the two well layers (5, 5') separate the plug (6) from the two source regions (3, 3')

two gate electrodes (7), each of which is arranged on the first main side (20), wherein each gate electrode (7) comprises a gate layer (70), which is separated from any doped layer by a first insulating layer (72),

and a first main electrode (9) as an ohmic contact on the first main side (20), which at least contacts the two source regions (3, 3') and the plug (6).

10. The wide bandgap semiconductor device according to claim 9, characterized in, that the two source regions (3, 3'), the channel layers (4, 4'), the well layers (5, 5') and the plug (6) form one planar plane on the first main side (20).

11. The wide bandgap semiconductor device according to any of the claims 9 or 10, characterized in, that the doping concentration of the plug (6) is at least 10 times higher than the doping concentration of the well layers (5, 5') or

in that the doping concentration of the plug (6) is between 10 times and 100 times higher than the doping concentration of the well layers (5, 5').

12. The wide bandgap semiconductor device according to any of the claims 9 to 11, characterized in, that the doping concentration of the well layers (5, 5') is at least 10 times higher than the doping concentration of the channel layers (4, 4') or

in that the doping concentration of the well layers (5, 5') is between 10 times and 100 times higher than the doping concentration of the channel layers (4, 4').

23

13. The wide bandgap semiconductor device according to any of the claims 9 to 12, characterized in, that at least one of

   – the plug (6) has a doping concentration between $2 * 10^{17}$ and $2 * 10^{21}$ cm^{-3} or between $1 * 10^{19}$ and $2 * 10^{21}$ cm^{-3},

   – the well layers (5, 5') have a doping concentration between $1 * 10^{17}$ and $1 * 10^{21}$ cm^{-3} or between $1 * 10^{18}$ and $1 * 10^{20}$ cm^{-3}, and

   – the channel layers (4, 4') have a doping concentration between $1 * 10^{16}$ and $1 * 10^{18}$ cm^{-3}.

14. The wide bandgap semiconductor device according to any of the claims 9 to 13, characterized in, that

   – the well layers (5, 5') and the channel layers (4, 4') being formed as common layers (4, 5 and 4', 5') having a low doping concentration at the first main side (20) in a region lateral to the source regions (3, 3'), and the doping concentration then rising to a higher doping concentration underneath the source regions (3, 3').

15. The wide bandgap semiconductor device according to any of the claims 9 to 14, characterized in, that the device is an insulated gate bipolar transistor or a metal-oxide semiconductor field-effect transistor.

74 70 7   4   72 30 3 9 50 60 6   1   3'   5'   4' 40   20

p

p+

p++

n++

n-

2

25

n

22

p+

8

90

FIG. 1

74 70   7   4   72 30 3 9 50 60 6   1'   3'   5'   4' 40   20

A

Lp

p+

p++

n++

B   B

C

n-

2

22

A   n+   C

80

90

FIG. 2

10

12

n-

2

8

p+

14

**FIG. 3**

FIG. 4

FIG. 5

FIG. 6
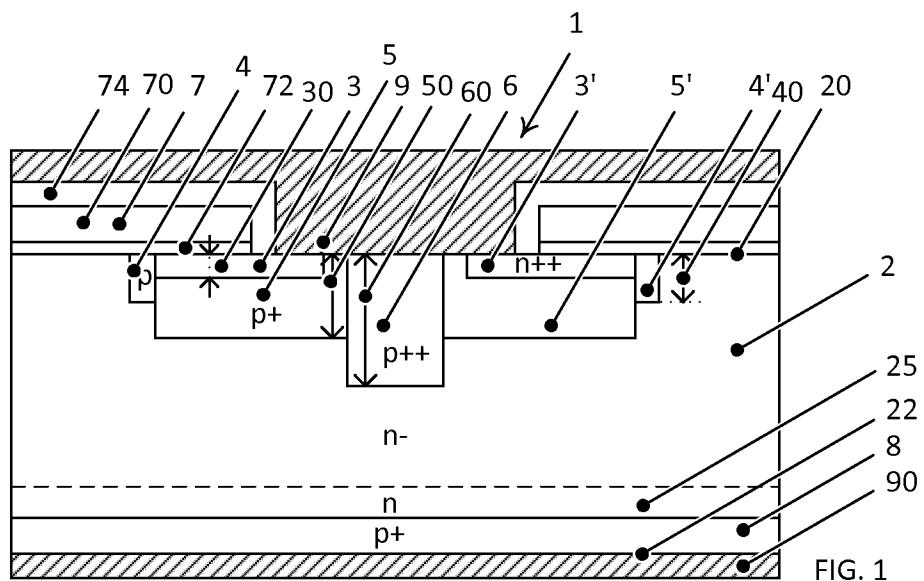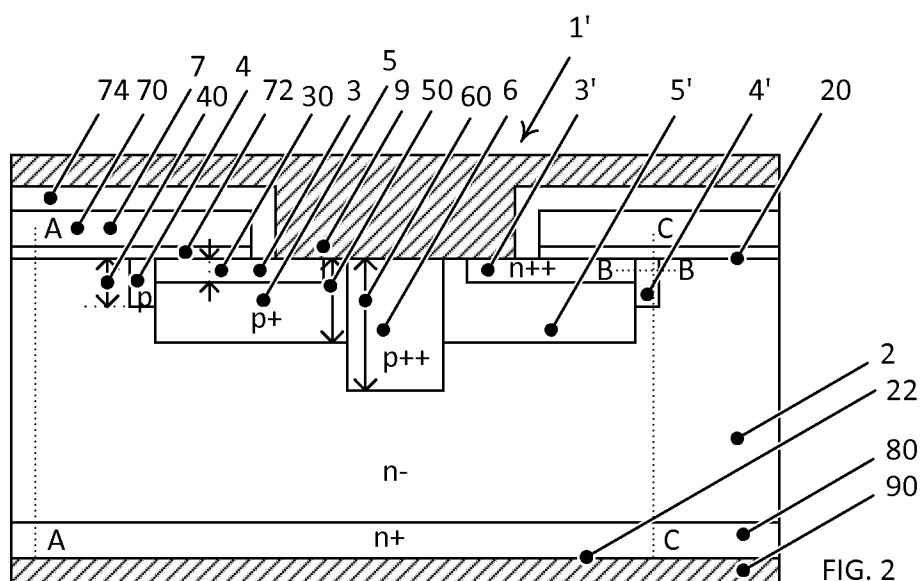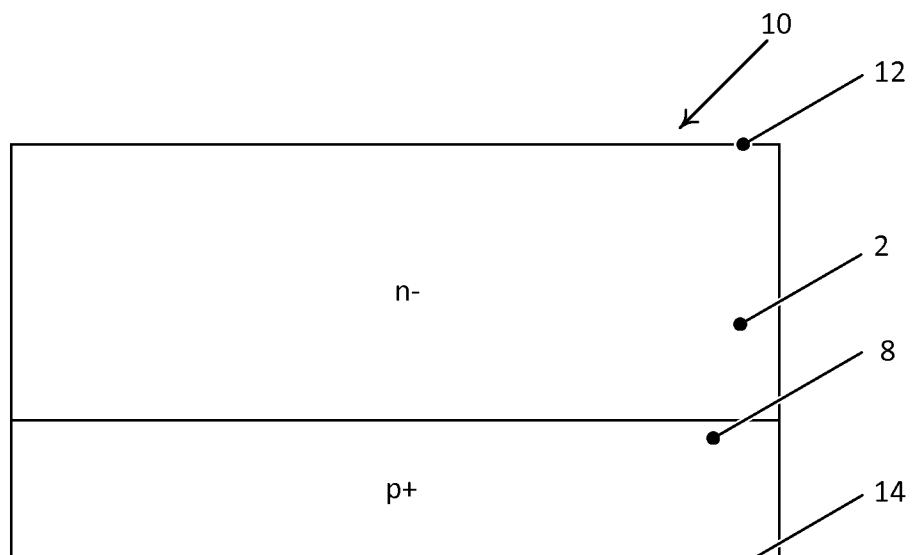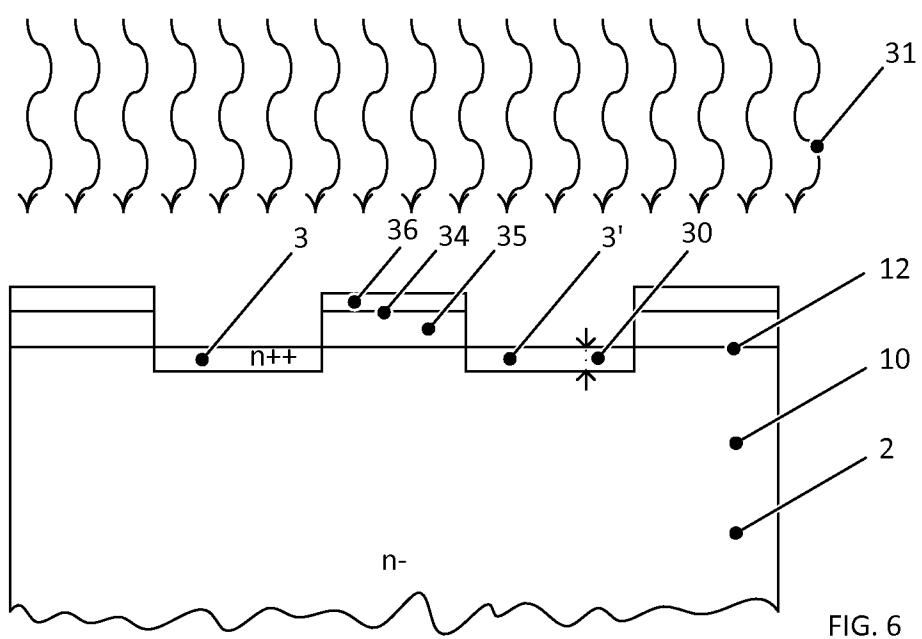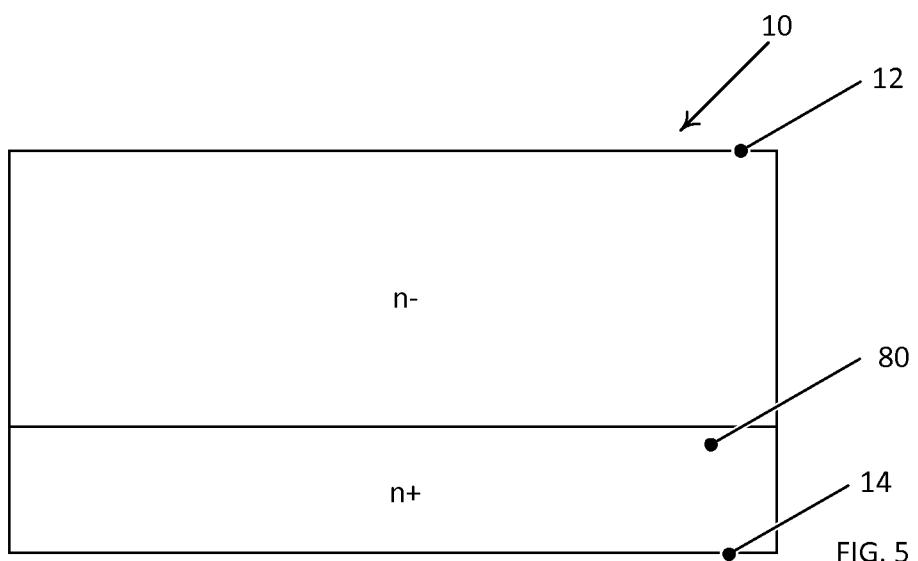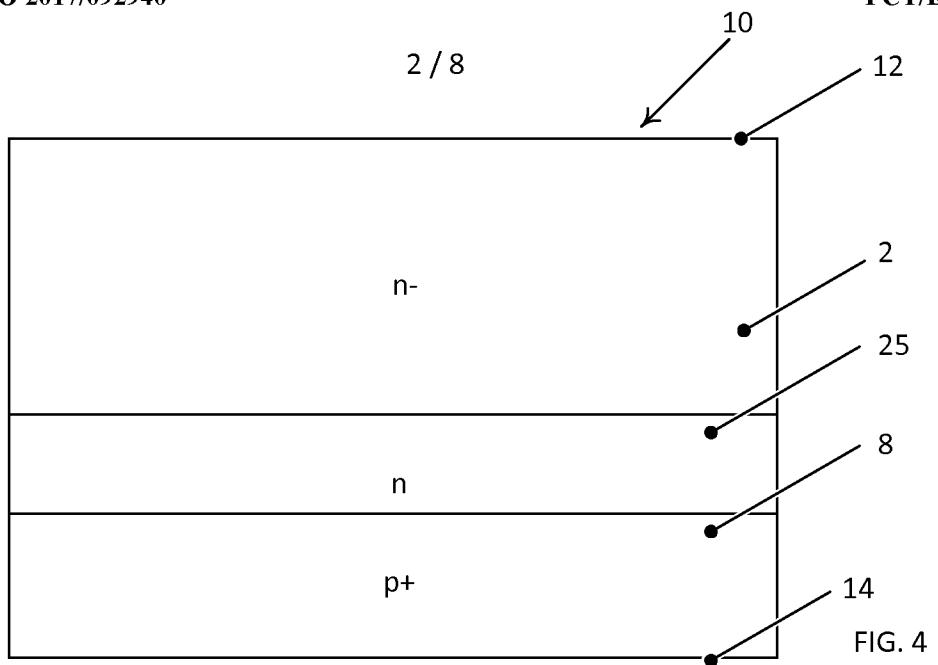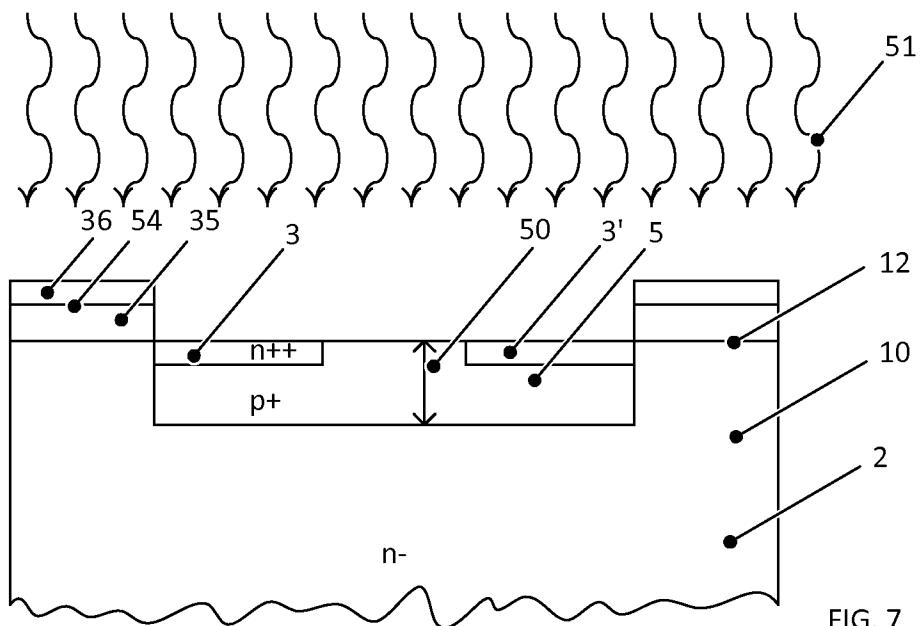
FIG. 7
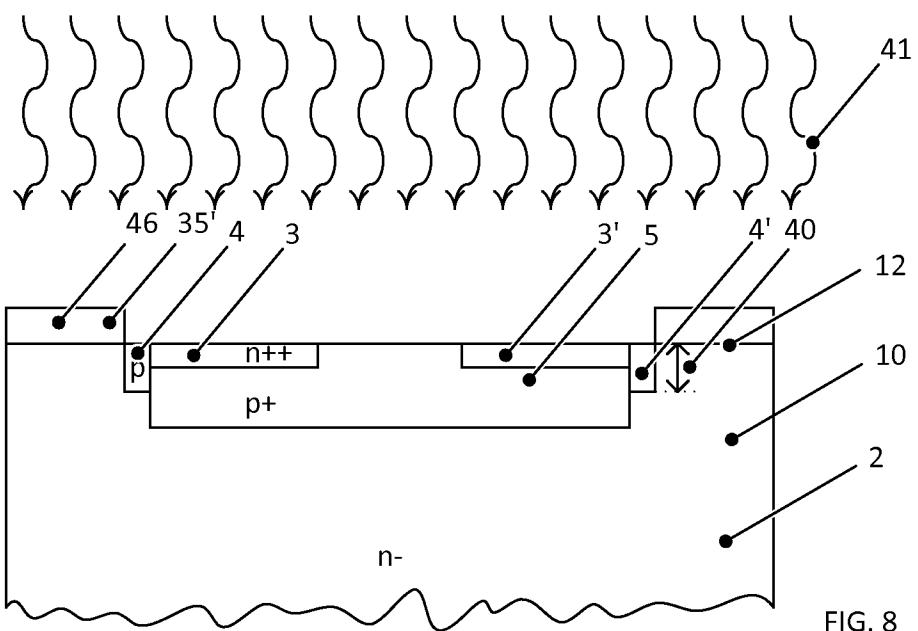
FIG. 8
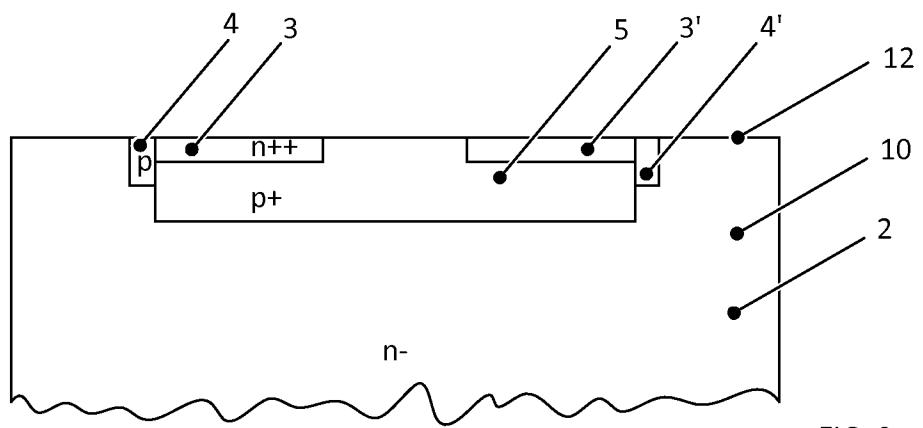
FIG. 9
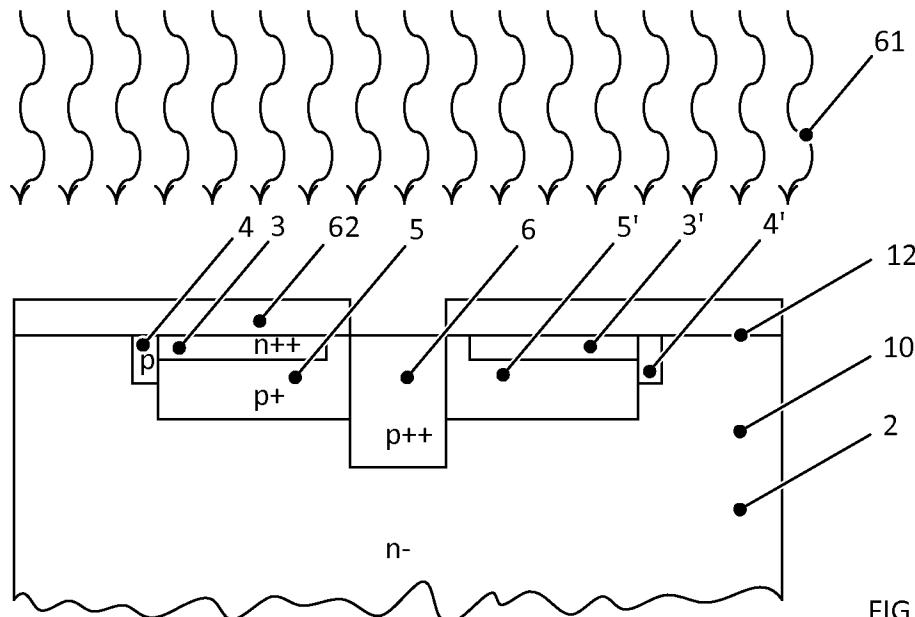
FIG. 10
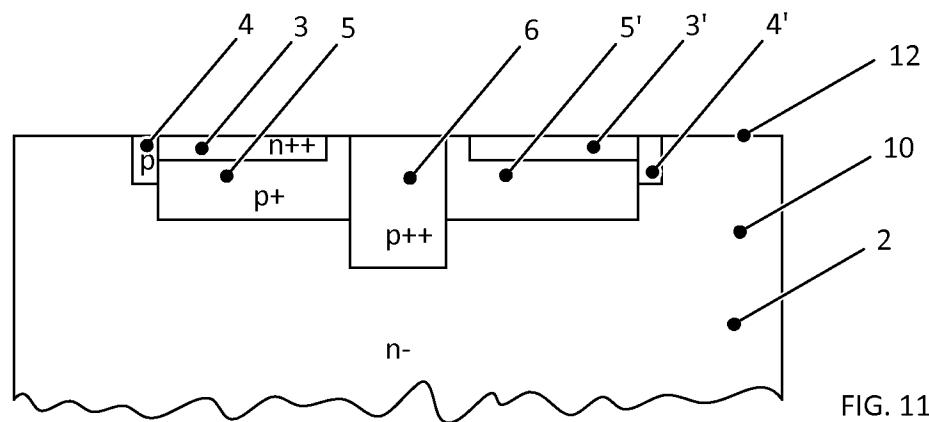
FIG. 11
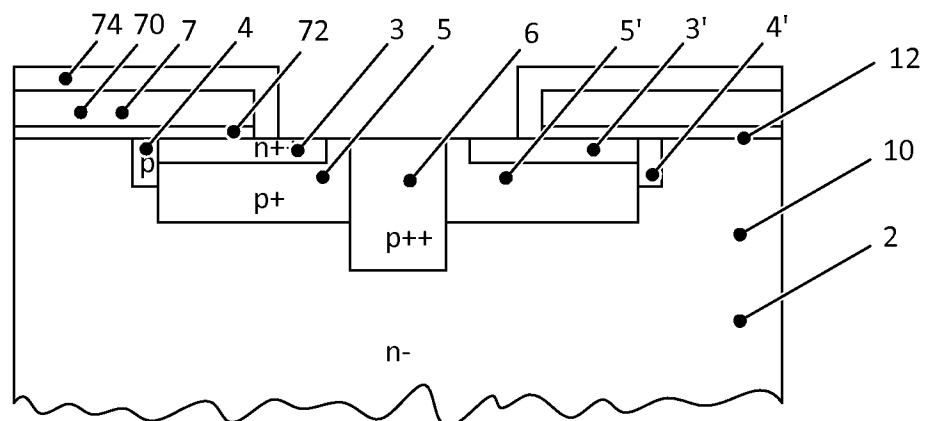
FIG. 12
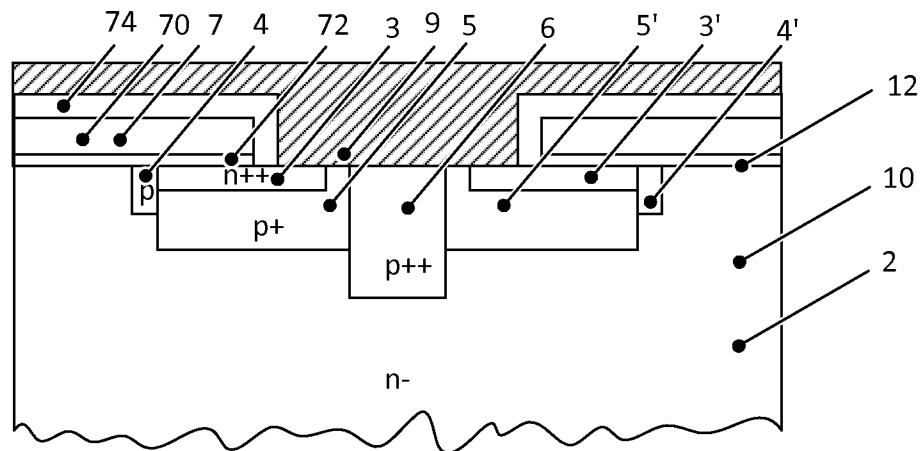
FIG. 13
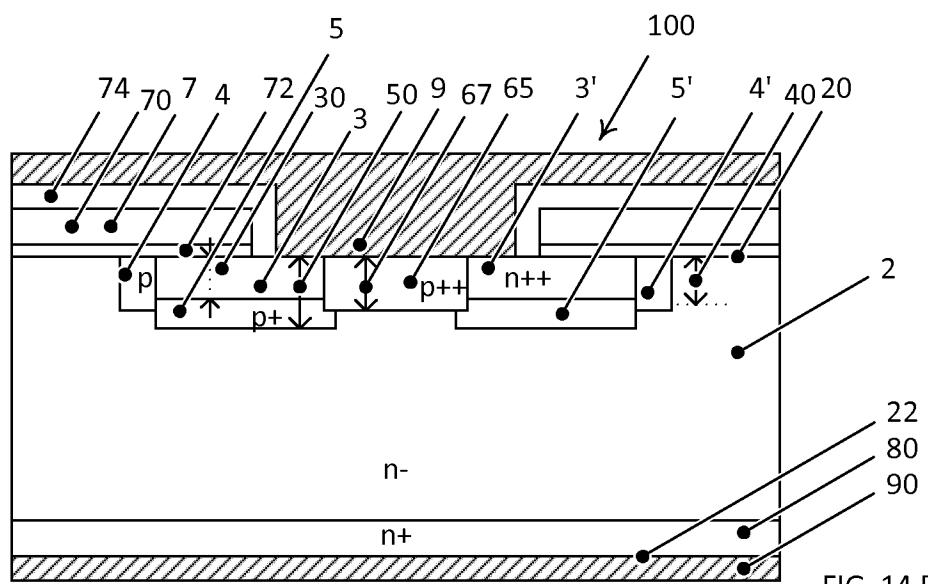
FIG. 14 Prior Art

FIG. 15

FIG. 16
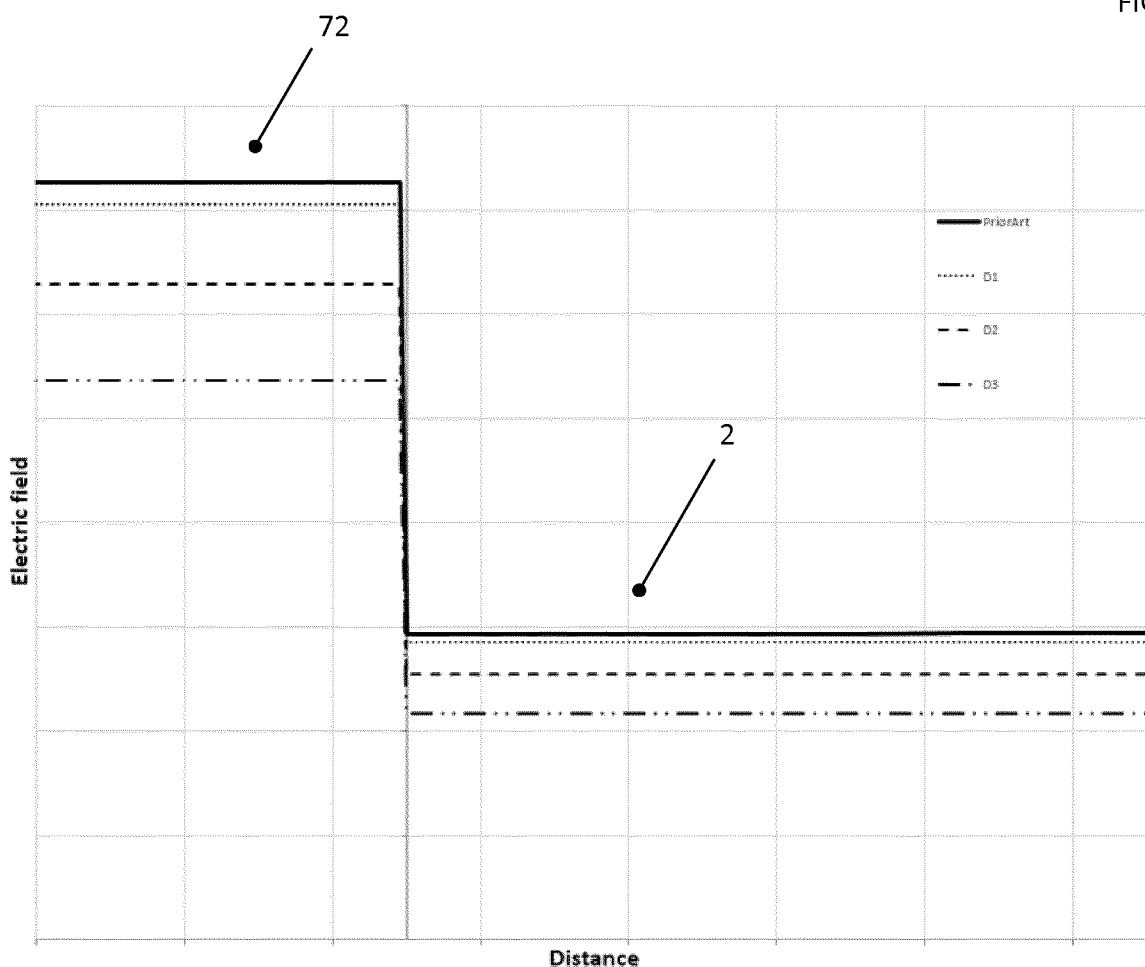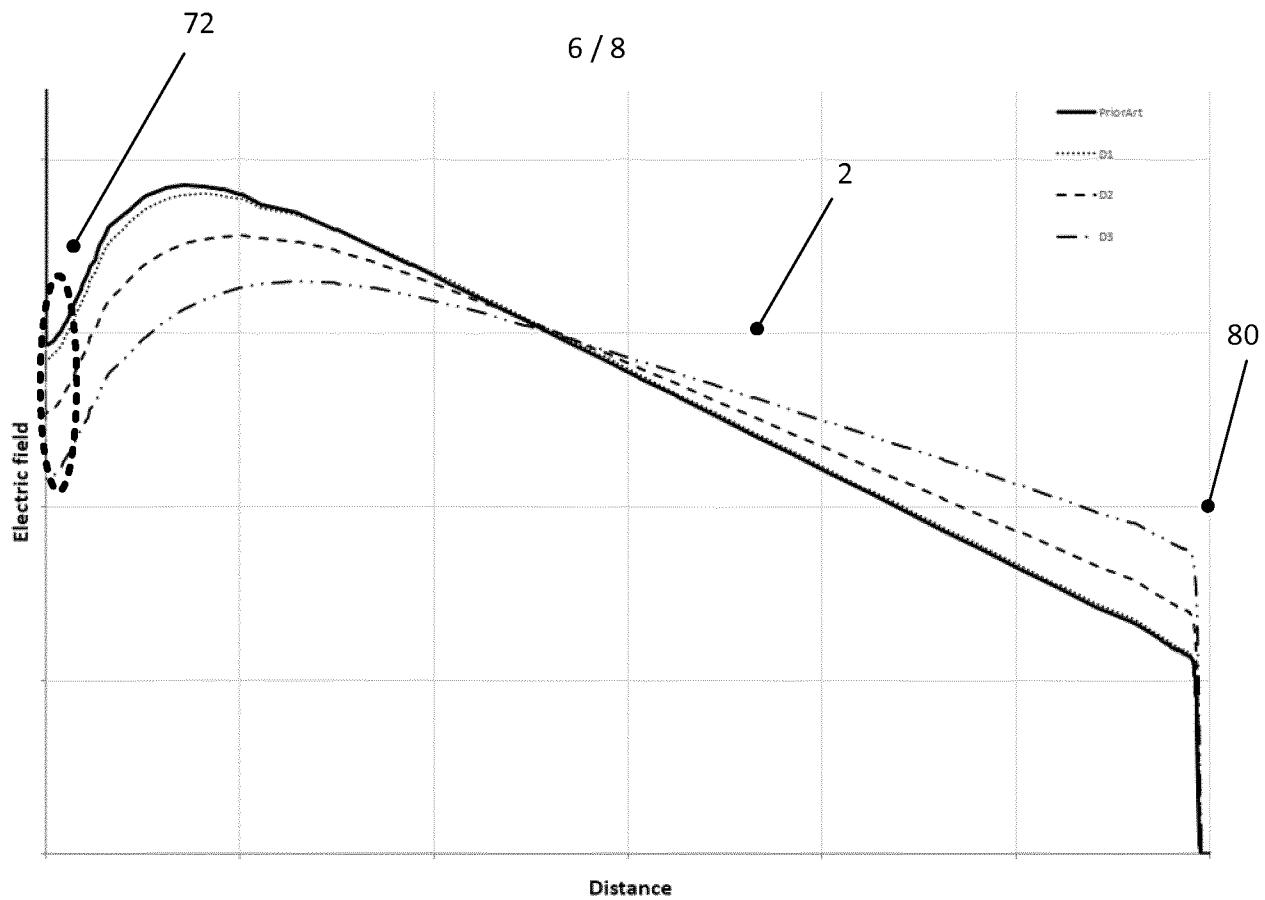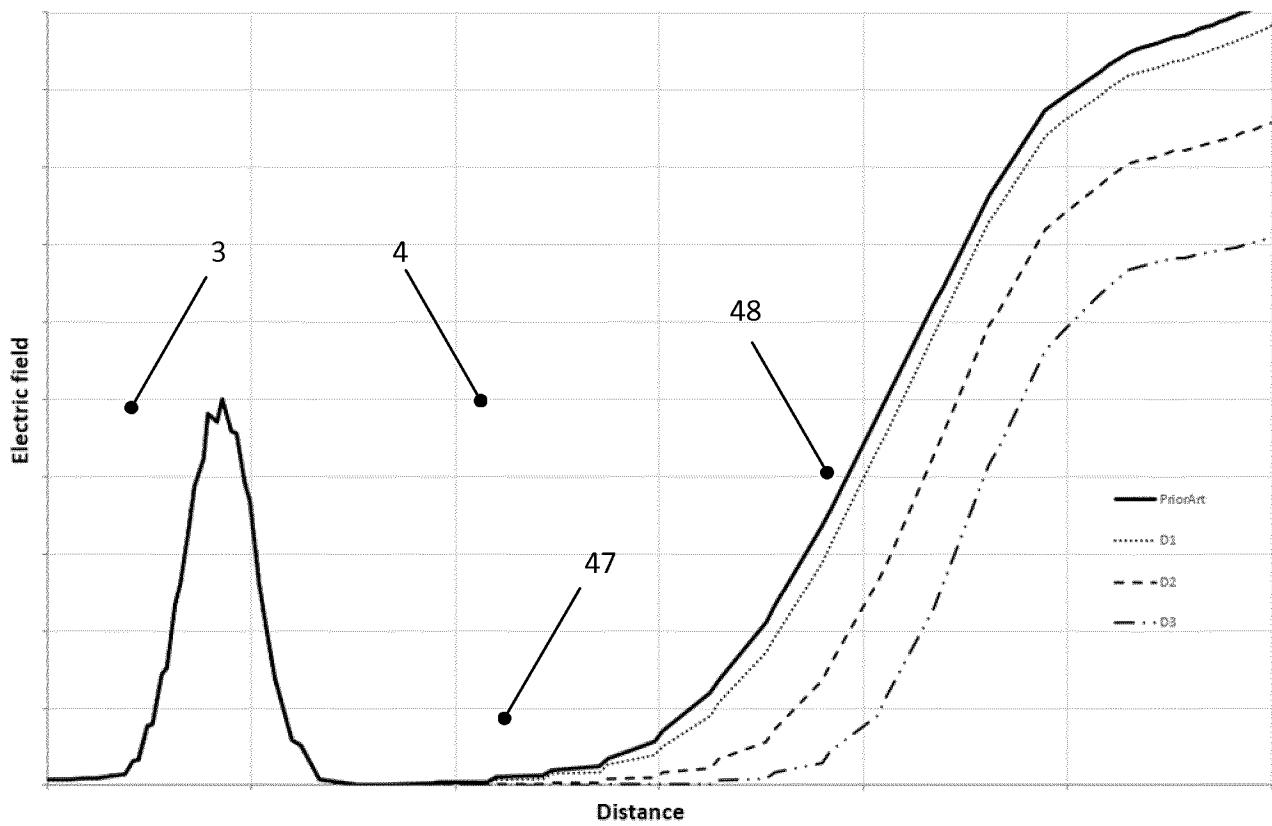
FIG. 17
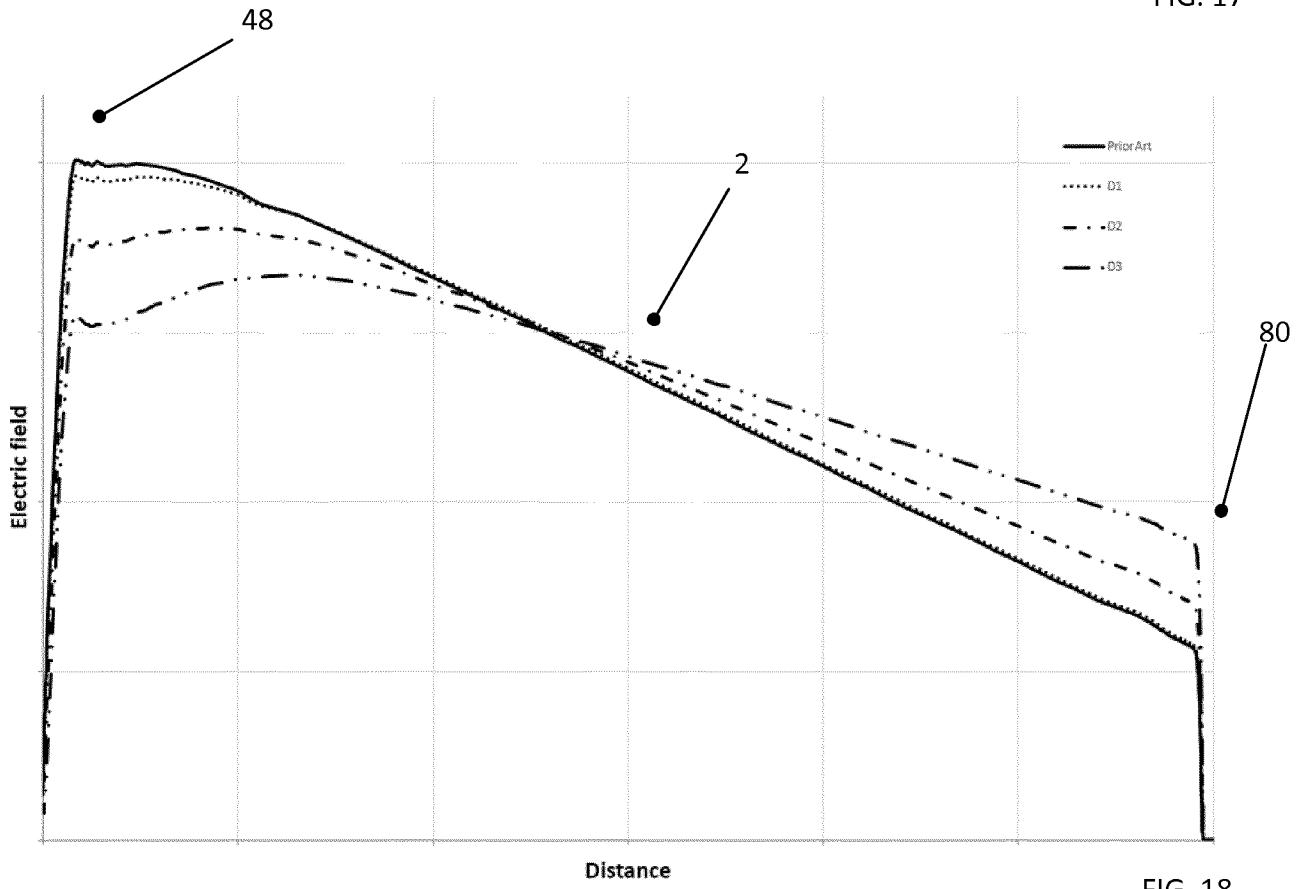
FIG. 18

FIG. 19

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/336   H01L29/78   H01L29/739   H01L29/10   H01L29/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	JP 2011 049267 A (MITSUBISHI ELECTRIC CORP) 10 March 2011 (2011-03-10) abstract; figures 1-10 -----	1-15
A	WO 2015/042146 A1 (CREE INC [US]) 26 March 2015 (2015-03-26) paragraph [0043] - paragraph [0047]; figure 5 paragraph [0066]; figures 12-20 -----	1-15

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[X] Further documents are listed in the continuation of Box C.   [X] See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 December 2016	13/12/2016

Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Lantier, Roberta

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation).	DOCUMENTS CONSIDERED TO BE RELEVANT	
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