Oct. 8, 1963

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3,106,701

FREQUENCY-CONVERSION TIME BASE GENERATOR
FOR SPEECH SOUND WAVES
Filed July 26, 1960

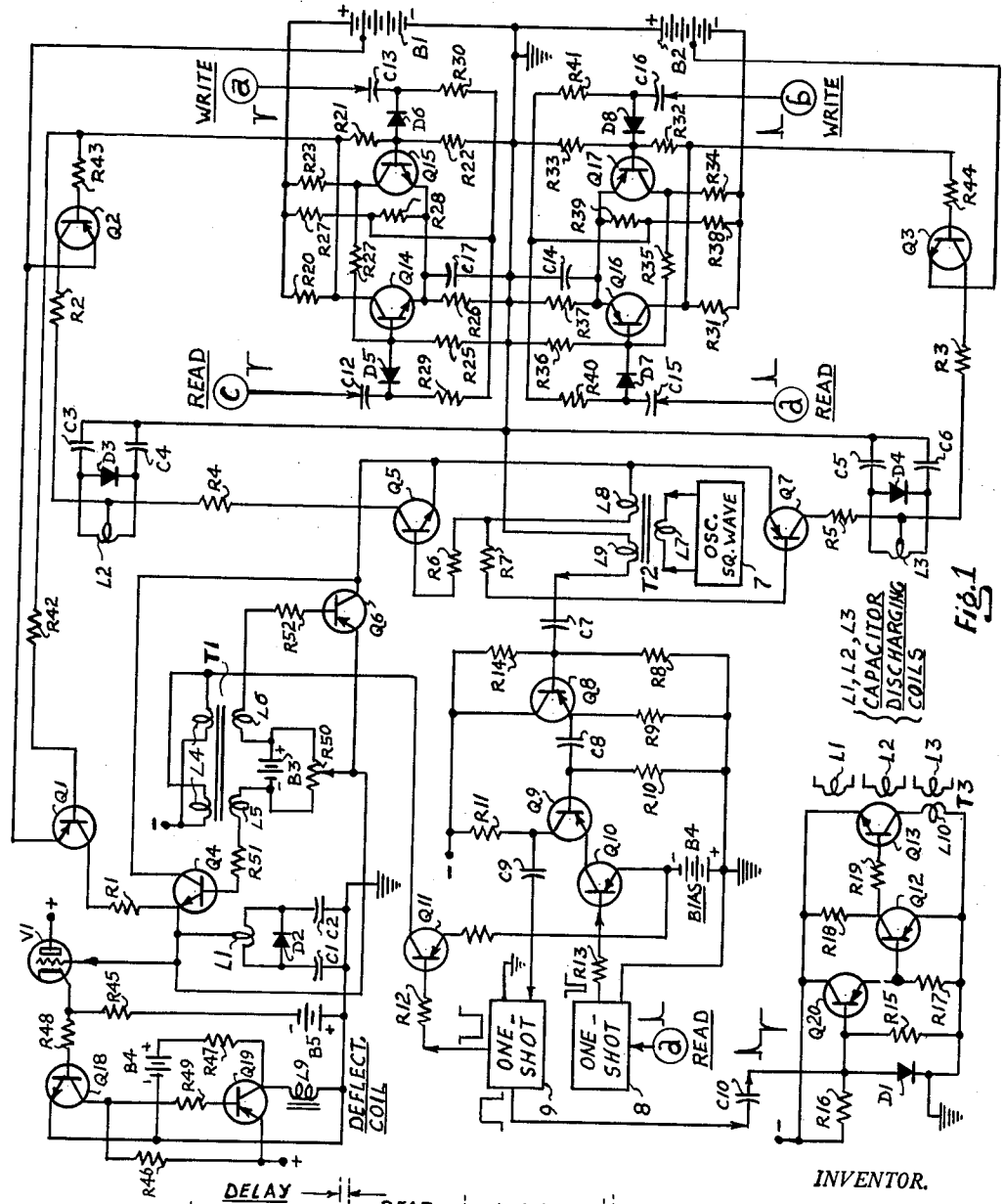

Fig. 1

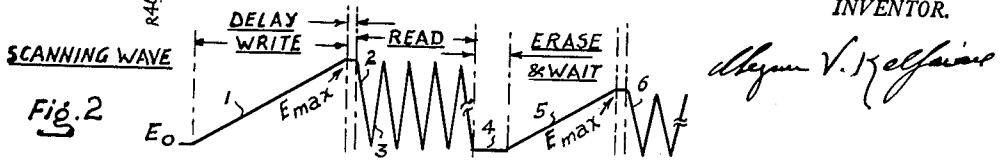

Fig. 2

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United States Patent Office 3,106,701 Patented Oct. 8, 1963

3,106,701

FREQUENCY-CONVERSION TIME BASE GENERATOR FOR SPEECH SOUND WAVES

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Filed July 26, 1960, Ser. No. 45,328
2 Claims. (Cl. 340—173)

This invention relates to a scanning system for shifting variably changing basic resonances in speech sound waves to predetermined reference frequency regions, for phonetic analysis of the spoken sound, and it is particularly an improvement over the systems disclosed in my U.S. Patents No. 2,705,260, March 29, 1955; No. 2,708,688, May 17, 1955; No. 2,921,133, January 12, 1960; No. 2,942,198, June 21, 1960; and patent application Serial No. 3,350, filed January 19, 1960. Its main object is to provide improved methods and means for standardizing the frequency positions of the basic resonances of the propagated speech sound waves, prior to analysis, for final translation into visible intelligible indicia, for example, by electric typing devices. A further object of the present invention is to provide a novel scanning system for said frequency conversion of the propagated speech sound waves.

In order that a machine, or the like, may be devised to simulate the interpretive mechanism of human intelligence, in printing spoken words, as spoken by all qualities and ranges of voices, without environmental control adjustments, or pre-adjustments to any particular voice, it is necessary that all environmental variables are first standardized during propagation of the sound waves, so that standard sets of parameters may be derived to collectively define different phonetic sounds of the spoken words. To accomplish such standardization, advantage is taken of the fact that all phonetic sounds are composed of definite sets of resonances whose ratios in frequency positions with respect to a fundamental remain constant, no matter what band of the voice spectrum they are produced in; this theoretical concept is disclosed in my above mentioned first three patents. Accordingly, the object of the present invention is to select the varying fundamental frequencies during propagation of the sound waves, and shift all frequency components to regions where their frequency ratios become constant with respect to a pre-assigned fundamental frequency. The said sets of parameters may then be derived, without variables, to collectively define each phonetic sound of the spoken words in speech.

Frequency standardizing methods and systems had been disclosed in my above mentioned patents. The systems utilized in these disclosures provide two storage tubes of the cathode ray type, in a manner that the wave pattern contained in one cycle portion of the selected fundamental (during propagation of the sound waves) is recorded in one storage tube, and the wave pattern contained in the following one cycle portion of the selected fundamental is recorded in the other storage tube. While the first recording is processed, its time length (from inception to termination of the wave pattern) is measured and stored in the form of a first signal quantity. Then, while the second recording is processed, the first recorded wave pattern is reproduced under control of the first quantity, so adjusted that the first recorded wave pattern is reproduced in a predetermined standard time base period. The same process is repeated with the second recorded wave pattern, so that the end result is a cyclic reproduction of the wave patterns of the propagated sound wave at a standard time base period. In order to allow time for reproduction of the recorded wave patterns prior to the arrival of successive wave patterns, the standard time base period is adjusted to be several times shorter than the shortest time base period occurring in ordinary sound waves. Thus, the number of reproduced wave patterns will be many more (randomly varying) than the actual recorded wave patterns, which condition is found to be more advantageous for more accurate resonance analysis of the wave patterns. Improved frequency conversion systems for the above noted purpose have been disclosed in my Patent No. 2,942,198, June 21, 1960; and patent applications Serial No. 781,103, Dec. 17, 1958; No. 857,121, Dec. 3, 1959; and Serial No. 3,350, Jan. 19, 1960.

It has been described in my above mentioned patents and patent applications that a wave pattern contained in one cycle time period of a fundamental frequency will yield all the information necessary for recognizing the particular phonetic sound. But since it is difficult to select the different resonances from a single wave pattern, the recorded wave pattern is reproduced a number of times so as to be capable of energizing a set of pre-tuned resonant circuits therefor. However, it is not necessary to render contiguity between succeedingly recorded wave patterns. In fact, such contiguity may sometimes cause ambiguity of resonance selection, as a succeeding wave pattern may change its shape from that of the preceding one. Thus, it is more desirable to energize the frequency selecting resonant circuits during reproduction of a wave pattern, and dissipate rapidly prior to selection of the resonances of a succeeding wave pattern. Also, the repeated reproduction of the recorded wave pattern does not have to be continually in forward direction, and accordingly, a back and forward sweeping scanning system may be utilized, with greater advantage of avoiding time lost during retrace period. Such time lost during retrace period may randomly cause sudden phase reversal of the reproduced wave pattern, and prevent proper energization of said pre-tuned resonant circuits by way of heavy filter action. Further yet, if the number of wave pattern reproduction is random, and less than the band pass of said pre-tuned resonant circuits, the amplitude built up in said resonant circuits, for each phonetic sound, may not be the same for different pitched voices. It is therefore more desirable to standardize the number of reproduction of a recorded wave pattern. Accordingly, it is an object of the present invention to provide a frequency conversion scanning system for first recording a wave pattern of the speech sound wave during propagation of same, and reproducing the recorded wave repeatedly in forward and backward sweeping directions at a predetermined reference time base period; including means for stopping said reproduction after reaching a predetermined number of counts. Such a system had been first disclosed in my patent application Serial No. 857,121, filed Dec. 3, 1959. An improvement over the circuitry of this system, utilizing transistors, instead of vacuum tubes, was disclosed in my patent application Serial No. 3,350, filed Jan. 19, 1960; and the present invention is contemplated as a further improvement over the transistorized version, as disclosed in last said patent application.

Briefly in accordance with the embodiments of the invention, there is provided a method which comprises the steps of producing a recording scanning wave rising in energy from zero value, the maximum level of last said wave representing the time dimension during which said recording occurs; producing repeated reproduction-scanning-waves at a constant predetermined reference time base period alternately falling and rising in energy coincident with said zero and maximum energy levels of the recording scanning wave; and stopping said re-

production of the waves after a predetermined number of counts.

The system utilized herein employs one small capacitor, and two substantially large capacitors. During *write* (recording) time period, the small capacitor is charged in positive direction with a linear rising potential for the production of the *write* scanning wave. During this *write* time period, the second capacitor is charged in positive direction with a linear but larger rising potential, and is isolated from the first. During this same period, the third capacitor is charged in negative direction with a linear but smaller rising potential, and it is also isolated from the first. At the end of this *write* time period, further charging of the three capacitors is stopped, and the stored charges in the two large capacitors are utilized as alternate charging and discharging potentials for the small capacitor, for the production of forward and backward scanning waves repeatedly during *read* time period. This condition is achieved by connecting the small capacitor to the two large capacitors alternately, in series with proper timing resistors, at a predetermined conversion frequency. The timing of these alternate connections is so arranged that the positively charged small capacitor is first connected to the negatively charged large capacitor, so that its charge will start falling to zero value linearly due to the larger potential across the larger capacitor than had been stored in the smaller capacitor. At the exact instant that the voltage across smaller capacitor has fallen to zero value, it is switched to the positively charged large capacitor to acquire a positively rising linear potential. In the previous mode, the positively rising potential in the small capacitor is linear due to the proportionally larger potential stored in the large capacitor. At the instant that the voltage in small capacitor has reached the same amplitude that it had acquired during *write* time period, it is again switched to the negatively charged large capacitor, and repeatedly on, until a timing element stops further oscillation. These exact timings are easily controlled by a fixed conversion frequency oscillator, and prefixed resistance capacitance time constant adjustments.

For further understanding of the objects and features of the present invention, reference is now made to the following specification in conjunction with the accompanying drawings, wherein: FIG. 1 is a schematic diagram in accordance with the invention; and FIG. 2 is a graph of waveforms involved in describing the arrangement of FIG. 1.

Referring now to the waveform of FIG. 2, the scanning waveform at A illustrates the mode of recording and reproducing a wave pattern of the speech sound waves. The sweeping wave **1** represents the recording, or *write*, saw tooth voltage, rising from zero voltage level to a maximum voltage level E_{max}. After the wave pattern is written during *write* period, symmetric saw teeth voltage waves **2**, **3**, etc. are produced during reproduction, or *read* period, at repetition of a reference conversion frequency rate. The fall **2** and rise **3** of these symmetric saw teeth voltages are produced in equal amplitudes as of the saw tooth voltage of wave **1**, and their maximums and minimums coincide exactly with that of zero and E_{max}. After a predetermined number of *read* saw teeth voltages are produced, they are stopped during waiting period **4**, until a new writing saw tooth voltage **5** is produced, the latter of which may have a different amplitude than the voltage of **1**; the rate of rise of voltages **1** and **5**, however, being always constant. After the writing scan voltage **5** is produced, the read scan voltages **6** follow in the previously explained manner. Due to certain inherent characteristics of the circuitry shown in FIG. 1, a slight variable delay is introduced between the ending of *write* period and the beginning of *read* period, as indicated in the graphical illustration at A. Such a delay, however, has no effect upon the operation of the system, and will not deteriorate any analytical conditions during reading time.

With the brief explanation of the presently disclosed scanning system, by way of the graphical illustration at A, in FIG. 2, reference is now made to the schematic arrangement of FIG. 1, wherein the scanning voltage waves at A are produced across capacitors C1, and C2, the two of which are connected in parallel, in series with inductance L1. The internal resistance of inductance L1 is negligibly low, and its A.-C. impedance is also negligibly low at the speed of scanning voltage change that takes place across C1 and C2, so that L1 acts as a short circuit for the parallel connection of capacitors C1 and C2; acting as a single capacitor. The parallel combination of capacitors C1 and C2 is connected to the positive terminal of battery B1 in series with timing resistor R1 and PNP transistor Q1. This transistor is utilized as an on-and-off switch, for example, during *write* period it is rendered conductive so that the capacitors C1 and C2 charge with a rising positive potential, at a time constant depending upon the RC time constant of resistor R1 and parallel connected capacitors C1 and C2; this rising potential representing the *write* scanning wave.

During *write* period, there are three sets of parallel connected capacitors charging at the same time, which are: the parallel combination of capacitors C1, C2 which are charged to positive potential in series with resistor R1, switching transistor Q1, and battery B1; the parallel combination of capacitors C3, C4 which are charged to positive rising potential in series with timing resistor R2, switching transistor Q2, and battery B1; and the parallel combination of capacitors C5, C6 which are charged in negative rising potential in series with timing resistor R3, switching transistor Q4, and negative potential of battery B2. The parallel connected capacitors C3, C4, and C5, C6 are in series with inductances L2 and L3, respectively, and functionally they behave as short circuits during rising potentials across said capacitors, as described in the foregoing.

After the *write* period has terminated, and the positive rising potential across capacitors C1, C2 is utilized as the recording scanning wave, the switching transistors Q1 through Q3 are switched off, so that the stored charges across capacitors C1, C2; C3, C4; and C5, C6 remain in steady states. The capacitive values of C3, C4 and C5, C6 are chosen much larger than the capacitive values of C1, C2, for example, 100 times larger, or more, so that the larger electrical quantities stored across C3, C4, and C5, C6 can be utilized to charge and discharge (without appreciable loss in quantity) the small capacitors C1, C2, for the production of reading scanning waves during *read* time period. This action is acomplished by alternately connecting the capacitors C1, C2 to the capacitors C3, C4 and C5, C6 in series with the timing resistors R4 and R5, by the alternate on-and-off switching action of transistors Q4, Q5 and Q6, Q7, respectively. This alternate switching operation is so timed that, the positively charged capacitors C1, C2 are first switched to the negatively charged capacitors C5, C6, for discharging in series with the timing resistor R5 until complete discharge to zero value is reached, whereupon, C1, C2 are switched to the positively charged capacitors C3, C4 in series with the timing resistor R4 until a positive charging voltage equal to the original value is reached; and thus repeating thereon. This performance is achieved as in the following.

The time constants of resistors R2, R3 and capacitors C3, C4 and C5, C6 are so adjusted that the amplitude of rising voltage across capacitors C3, C4 is at least 30% higher than the amplitude of rising voltage across capacitors C1, C2, and the amplitude of rising voltage in negative direction across capacitors C5, C6 is at least 30% of the amplitude of rising voltage across capacitors C1, C2. These higher stored voltages are to render linearity of the rising and falling voltages across capacitors C1, C2, for example, when the rising voltage across capacitors C1, C2 reaches the original amplitude that it had assumed during *write* period, the stored positive voltage across ca-

pacitors C3, C4 is still 30% higher for causing said linear rise; and similarly, when the voltage across capacitors C1, C2 falls to zero value, the stored negative voltage across capacitors C5, C6 is still 30% of the original amplitude in negative direction, for causing said linear fall. In order that the scanning voltages across capacitors C1, C2 rise and fall linearly coincident exactly at zero and E_{max} values during *read* time, as described by way of the graphical illustration at A, in FIG. 2, the values of timing resistors R4, R5, and the on-and-off switching time instants of transistors Q4, Q5 and Q6, Q7 must be accurate.

It will be noted that the transistors Q4 and Q5 are connected in series, and conduction of the series circuit may be cut off by either one of the transistors in an off state; this condition also pertaining to the series connected transistors Q6 and Q7. The on-and-off states of transistors Q5 and Q7 are alternately controlled by an oscillator 7, which produces output square waves, or approximation thereof, for abrupt switching of the Q5 and Q7 transistors at a preadjusted conversion frequency. When transistors Q4 and Q6 are in off states, by the normal cut-off bias voltage of battery B3 upon their base elements, the capacitors C1, C2 are electrically isolated from the capacitors C3, C4 and C5, C6, even though continuous production of alternate square waves from oscillator 7 causes on-and-off switchings of transistors Q5 and Q7. During *read* time, however, a square wave current flows through the primary coil L4 of transformer T1, which inductively causes a voltage to appear across the secondary coils L5 and L6. With the proper design of transformer construction, it is possible to hold the voltages across secondary coils L5 and L6 in steady states for a given period of time. Thus during *read* time period, a positive voltage is applied upon the base element of NPN switching transistor Q4, and a negative voltage is applied upon the base element of PNP switching transistor Q6, from secondary coils L5 and L6 of transformer T1, causing Q4 and Q6 to conduct. During conduction, the emitter to collector impedances of switching transistors Q4 to Q7 are negligibly low, and accordingly, the capacitors C1, C2 may be considered as directly connected to the capacitors C3, C4 and C5, C6, in alternate time periods, in series with switching transistors Q4, Q5 and Q6, Q7. The timing resistors R4 and R5 are connected in series with these series switching circuits, so that the timing of voltage rise or fall across capacitors C1, C2 is exactly equal to one square wave period of the oscillations produced in oscillator 7.

In operation, assume that transistors Q1, Q2, and Q3 are in on states during *write* time period. The capacitors C3, C4 start charging linearly in series with the timing resistor R2 in positive direction; the capacitors C5, C6 start charging linearly in series with the timing resistor R3 in negative direction; and the capacitors C1, C2 start charging linearly in series with the timing resistor R1 in positive direction, the rising voltage across capacitors C1, C2 being utilized as the *write* scanning wave. At the end of this *write* scanning time period, the transistors Q1, Q2 and Q3 are switched to off positions, and the stored charges in capacitors C1 through C6 are isolated from further charging. The switching transistors Q5 and Q6 are alternately switched to on-and-off positions at the conversion frequency of square wave oscillator 7. This oscillation continues without any phase control, and accordingly, no time coincidence of switching is established between transistors Q5 or Q7 and the exact ending of *write* time period. However, assuming for the moment that the transistor Q7 starts conducting at the instant that the *write* period has ended, the transistors Q4 and Q6 are rendered conductive. The capacitors C1, C2 are now electrically connected to the capacitors C5, C6, in series with the low impedance transistors Q6, Q7 and the high impedance timing resistor R5. The stored positive charge in capacitors C1, C2 starts discharging linearly at a time

constant depending upon the values of resistor R5 and the parallel connected capacitors C1, C2; this time constant being preadjusted equal to exactly the time period of one square wave of the oscillations produced by block 7. The discharging curve across capacitors C1, C2 is linear down to zero value, due to the fact that the negative voltage across capacitors C5, C6 is still at least 30% of the original magnitude that had been acquired in the capacitors C1, C2. Because of said accurate timings, the Q7 is rendered inoperative and the Q5 is rendered operative at the exact instant that the voltage across capacitors C1, C2 has dropped to zero value. These capacitors are now connected to the positively charged capacitors C3, C4 via low impedance transistors Q4, Q5 and timing resistor R4. The capacitors C1, C2 start charging in positive direction linearly up to an amplitude equal to the original amplitude that these capacitors had acquired at the end of said *write* period, due to the fact that the positive voltage across capacitors C3, C4 is still at least 30% higher at this point, whereupon, the transistors Q5 and Q7 switch conductive states for repetitive production of these *read* scanning waves. Having thus described the functions for producing *write* and *read* scanning waves, according to the embodiments of the present invention, the details of establishing the required timings and switching of different component parts of the arrangement in FIG. 1 is now made, as in the following.

The block 7 represents a square wave generator, preferably utilizing transistors, although vacuum tubes may also be used, if so desired. Square wave generators are commonly known in the art of electronics, and accordingly, special description of details is not needed herein. The output of square waves of block 7 is applied to a transformer T2 having a primary coil L7 and secondary coils L8, L9. With proper transformer design, it is possible to maintain square wave voltages across secondary coils L8 and L9, and such transformers are commercially available. The alternate square wave voltages across coil L8 are applied to the base elements of NPN transistor Q5 and PNP transistor Q7, in parallel so that when said square wave voltage is in positive polarity the Q5 becomes conductive and Q7 non conductive, and when said voltage is in negative polarity the Q7 becomes conductive and Q5 non conductive. The resistors R6 and R7 are used to limit the amount of currents passing through base to emitter of transistors Q5 and Q7, respectively. Due to continuous operation of the oscillator in block 7, the transistors Q5 and Q7 are in alternate on states at all times. But during *write* period, the transistors Q4 and Q6 are in off states, and accordingly, the three sets of parallel connected capacitors (C1 to C6) can be considered as completely isolated from each other during said period. Cross coupling between capacitors C3, C4 and C5, C6 is also accomplished by the high collector to emitter and collector to base cut off resistances of transistors Q5, Q7, and the high value series connected timing resistors R4, R5, in comparison with the large capacitive values of C3 to C6 and their low value series connected timing resistors R2 and R3.

At the end of a *write* period, it is desired that reading starts immediately, which can be established by switching the transistors Q4 and Q6 in on states simultaneously. However, it is necessary that the positively charged capacitors C1, C2 be first connected to the negatively charged capacitors C5, C6, and the transistor Q7, for this particular connection, may not be at its starting point of on condition; accordingly, a waiting period is introduced, as controlled by the voltage across secondary coil L9. The output voltages across secondary coils L8 and L9 are alike, and since these voltages are in square waveform, it is simple to derive a pulse signal across load resistor R8 by a small differentiating coupling capacitor C7 at the exact instant that the transistor Q7 has started to assume an on state. This negative pulse is applied to the base element of emitter follower Q8,

and further applied from its emitter circuit resistor R9, coupling capacitor C8, and load resistor R10, to the base element of gating transistor Q9. This gate circuit consists of transistors Q9 and Q10 connected in series, so that current is admitted therethrough only when forward biases are applied to their base elements simultaneously. At the end of *write* period, a narrow pulse voltage is applied to the one shot multivibrator circuit in block 8, the output of which produces a prolonged pulse and further applies to the base element of gating transistor Q10 in forward direction. The base elements of gating transistors Q9 and Q10 are normally biased in backward direction by the voltage from battery B4, and as mentioned above, both of the transistors must be forward biased simultaneously for conduction. Accordingly, the prolonged forward bias upon Q10 keeps the circuit in readiness until a pulse voltage in forward direction arrives upon the base element of gating transistor Q9 from secondary coil L9 of transformer T2, whereupon, current flows in the collector circuit resistor R11 causing a voltage drop across it, and finally applied to the input of one shot multivibrator in block 9, by way of coupling capacitor C9. The one shot multivibrator 9 produces an output square wave voltage which is applied in forward direction to the base element of normally cut-off transistor Q11, causing collector current through the primary coil L4 of transformer T1. A square wave voltage appears in the secondary coils L5 and L6, in oppsite polarities, which are applied in forward directions to the base elements of transistors Q4 and Q6, whereupon, production of *read* scanning wave starts, in the mode as described in the foregoing. Any phase delay that might occur between the operation of transistors Q4, Q6, and the exact start of operation of Q7, due to various stages of circuitry, may be corrected by pre-phasing the voltages across secondary coils L8 and L9 of transformer T2.

The frequency of oscillation in block 7 is prefixed, and crystal control may be utilized if precision is required. The exact frequency of oscillation may be determined for a specific use, and for practical purposes required herein the frequency may be adjusted to 7 kc.; producing 14 thousand symmetric forward and backward *read* saw tooth scanning waves per second across capacitors C1, C2. Once the frequency of this oscillation is fixed, the values of timing resistors R4 and R5 are so pre-adjusted that the rising and falling voltage across capacitors C1, C2 assume exact E_{max} and zero values at the switching instants of switching transistors Q5 and Q7 during production of *read* scanning waves. By the same token, the timing resistors R2 and R3 are also pre-adjusted to attain these correct proportions of voltages. Similarly, the correct ratios of voltages between batteries B1 and B2 must remain constant without variation. This condition, however, may be attained by using a single power supply (since B1 and B2 are in opposite polarities) and terminate the ground connection to a voltage dividing tap. Once this tap is pre-fixed, any voltage variation of this power supply will not impair operation of the system, as the system is dependent only on the correct voltage ratios.

With the above given example (oscillator 7 operating at 7 kc., the width of output pulse of the one shot multivibrator in block 8 may be adjusted to approximately 200 microseconds long, so that the gating transistor Q10 will be in on state long enough to coincide with the pulse signal arriving upon the base element of series connected gating transistor Q9, and thereby effect operation of the one-shot multivibrator in block 9. The width of the output pulse of block 9 may be adjusted to any desired value, for example, adjusted so that the pulse will fall after 14 forward and backward saw tooth waves are produced during *read* period. Various one-shot circuits are known and used both in commercial and specialized electronic devices, and accordingly, detailed circuitry is avoided herein for simplicity of drawing. A one-shot circuit, however, is known to change its state of conduction in response to an incoming pulse signal; remain in such state for a predetermined time period; and reset itself automatically to the original conductive state. The time period during which it stays in changed state depends upon the value of a capacitor contained therein, and it may be varied to any suitable time delay period, and due to the sharp rise and fall of the delayed output signal, either negative or positive pulses may be obtained by differentiation, for example, by coupling to associated circuits with a small capacitor. The resistors R12 and R13 are used as current limiters upon the base elements of transistors Q11 and Q10, respectively. The resistor R14 is used to provide normal bias upon the base element of emitter follower transistor Q8.

At the end of *read* period, the capacitors C1 through C6 must be discharged, to make ready for a new start of *write* scansion. A pulse signal is derived from the output of block 9 at the end of *write* scansion period, by a small differentiating coupling capacitor C10, and this pulse signal is applied to the base element of emitter follower transistor Q11 from across load resistor R15 and diode D1. The resistor R16 is used to provide a normal forward bias upon the base element of Q11. The pulse voltage developed across emitter circuit resistor R17 of Q11 is applied in forward direction to the base element of amplifier transistor Q12, and the voltage developed across collector circuit resistor R18 of Q12 is further applied to the base element of amplifier transistor Q13, in series with a current limiting resistor R19. The amplified pulse current in the collector circuit of Q13 is passed through the primary coil L10 of a high frequency transformer T3. The secondary coils L1, L2 and L3 of T3 are the same coils (as designated by like numerals) that are connected between the junctions of parallel connected capacitors C1, C2 and C3, C4 and C5, C6, respectively. Thus a pulse voltage is produced across the secondary coils L1 to L3 of high frequency transformer T3 at the end of *write* time period. These pulse voltages in coils L1 to L3 transform the like poled voltages in parallel connected capacitors C1, C2 and C3, C4 and C5, C6 to unlike poled voltages, and consequently, the unlike poled storages in these capacitors dissipate completely during homeward return of said pulse in the secondary coils L1 to L3; due to their extremely low value of impedances. The stored electrical quantities in these capacitors may be discharged by other means, for example, connecting across them low impedance thermionic devices, but it is contemplated herein, that, the secondary coils L1 to L3 are capable of introducing lower impedances than any thermionic devices avalaible at very low voltages. The diodes D2 to D3 in parallel with the secondary coils L1 to L4, respectively, are included to avoid oscillation across said coils.

The switching transistors Q2 and Q3 may be rendered in on-and-off states by flip-flop circuits, as shown in the drawing. Due to NPN and PNP characteristics of the transistors Q2 and Q3, two separate flip-flop circuits are used. One of the flip-flops consists of NPN transistors Q14, Q15; cross coupling resistors R20 through R25; emitter circuit resistor R26; bypass capacitor C11 across R26; and voltage dividing resistors R27, R28 from the junction terminal of which is obtained a positive bias for the diode inputs, by way of load resistors R29 and R30 to the diodes D5 and D6, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C12 and C13, only when their magnitudes are higher than said bias. The other flip-flop consists of PNP transistors Q16, Q17; cross-coupling resistors R31 through R36; emitter circuit resistor R37; bypass capacitor C14 across R37; and voltage dividing resistors R38, R39 from the junction terminal of which is obtained a negative bias for the diode inputs, by way of

load resistors R40 and R31 to the diodes D7 and D8, respectively, so that the flip-flop will operate by input signals, as received through coupling capacitors C15 and C16, only when their magnitudes are higher than said bias. These biases, although not necessary, are helpful in preventing operation of the flip-flops by noise signals. While these flip-flop circuits are shown in their specific forms, they may be devised in various forms, such as shown in various literature.

At the start of *write* time period, a negative pulse is applied to the terminal (*a*) of sufficient amplitude to drive the trigger transistor Q15 in off state, whereupon, the trigger transistor Q14 assumes a state of stable operation, delivering forward bias to the base element of switching transistor Q2 from across its collector circuit resistor R20. Simultaneously, a positive pulse is applied to the terminal (*b*) of sufficient amplitude to drive the trigger transistor Q17 in off state, whereupon, the trigger transistor Q16 assumes a state of stable operation, delivering forward bias to the base element of switching transistor Q3 from across its collector circuit resistor R31. At the end of said *write* time period, a negative and a positive pulse is applied to the terminal (*c*) and terminals (*d*), respectively, for resetting the two flip-flop circuits to read conditions. The resistors R42, R43, and R44 in series with the base elements of Q1, Q2 and Q3 are used as current limiters for said base elements. While these flip-flop trigger circuits are shown for rendering the switching transistors Q2 and Q3 in on-and-off states, such on-and-off states may also be accomplished by the use of a transformer having two split secondary coils, similar to the transformer T1. The split secondaries would then supply the required square wave forward bias voltages to the base elements of transistors Q2 and Q3 during the *write* time periods.

Still another transformer of this type is used in actual practice of the presently proposed system. According to the foregoing description it was mentioned that storage tubes of the cathode ray type are used for recording and reproducing the speech sound waves. Conventional storage tubes require different voltage settings during recording and reproducing states. When these different voltage settings are performed in square waveform, objectional output transients become unavoidable. Besides, during recording time period, it is desired for the particular purpose described herein, that the output of the storage tube is zero without the presence of switching transients. To achieve such ideal on-and-off output of the storage tube without the presence of switching transients, I have successfully used NPN and PNP transistors in parallel with a high impedance resistor capacitively coupled to the output resistor of the storage tube. Some storage tubes use low voltage in the output circuit, and accordingly, transistors are permissible with such low voltages. With high voltage storage tubes, however, I have first used a cathode follower, to render the system suitable for transistors. The said NPN and PNP transistors are normally biased in forward directions, so that any positive or negative voltage developed across the high impedance resistor is short circuited by the transistors. Thus, the voltage across the coupling capacitor is shunted at all times. Whereas, when the biases upon the base elements of said NPN and PNP transistors are changed in backward directions suddenly, the voltage across said coupling capacitor does not change suddenly, and accordingly, the output signal starts transmitting from a normal zero value, without producing transients. To achieve this condition, another transformer, such as T1, is operated and controlled by the output of block 9, so that said NPN and PNP transistors are rendered inoperative during *read* period of the written speech sound waves. Due to the very low output of storage tubes, I have used one such stage of signal shunting immediately after the output of the storage tube, and another stage of such signal shunting after amplification. Accordingly, such a novel system of signal shunting will be considered as part of the present invention.

It was mentioned in the foregoing that the parallel connected capacitors C1, C2 are preferably chosen having small capacitive values. The high impedance of these capacitors is not suitable for driving low impedance transistors, and accordingly, these capacitors are first coupled to the control grid of a cathode follower vacuum tube V1. The saw tooth voltage developed in the cathode circuit resistor R45 of V1 is then coupled directly to the base element of amplifier NPN transistor Q18 in forward direction, and the voltage developed across collector circuit resistor R46 of Q18 is further applied in forward direction to the base element of amplifier transistor Q19 for driving the beam deflection coil L9 of a cathode ray type of storage tube, for recording and reproducing the speech sound waves, as described in the foregoing. Existing storage tubes are usually made with the beam projected to the center of the storage screen. For the present purpose, however, the *write* scanning period may vary, and it is necessary that the *read* scanning wave coincide exactly with the minimum and maximum of the stored scanning line. It is therefore necessary that direct coupling is employed from the capacitors C1, C2 to the final deflection coil L9. Such direct coupling would require fixed deflection of the beam to one edge of the storage screen, for full utilization of the entire screen. Accordingly, a direct current is first passed through the deflection coil L9 in series with the battery B4 and resistor R47, for said deflection. Of course, a beam deflecting permanent magnet or a separate deflection coil with direct current passing therethrough may be utilized, or, the storage tube may be made with the beam normally projected to one edge of the storage screen. The resistors R48 and R49 are used as current limiters for the base elements of transistors Q18 and Q19. The resistor R50 is utilized to adjust the proper backward biases upon Q4 and Q6. Similarly, the resistors R51 and R52 are utilized as current limiters upon base elements of transistors Q4 and Q6. The battery B5 is used in opposition to the normal positive voltage that is developed across the cathode circuit resistor R45 of V1, so that the transistors Q18 and Q19 will normally draw minimum current for economy.

According to the foregoing descriptive matter, it is noted that the basic principles of the present invention is to produce scanning wave voltage in three separate storage devices: the first one being utilized as a *write* scanning wave in a frequency conversion system; and the other two being utilized as storages. During *read* scansion period, the first storage device is switched alternately to the said two storage devices at said conversion frequency, for producing the required *read* scansion waves. According to the description of the arrangement given in FIG. 1, the circuitry will satisfy the required functions. However, such circuitry is quite flexible, as is well known to the skilled in the art of electronics, and the specific arrangement may therefore be considered as exemplary. Also, the arrangement may be utilized for various other systems of frequency conversion. For example, instead of adjusting the *read* scansion frequency higher than the *write* frequency, each *read* period may be longer than the longest *write* period that may occur in the incoming signal wave. Such a system would be useful for bandwidth reduction, where all variably changing high frequency waves would be reduced in correct frequency ratios with respect to a low frequency reference fundamental frequency, such, for example, being useful for vocoder type systems. Accordingly, the descriptive matter contained herein, in conjunction with the drawings, and the purposes involved, are subject to various modifications, substitutions and adaptations, without departing from the true spirit and scope of the invention.

What I claim is:

1. The system for producing frequency conversion scan-

ning waves having a recording scanning wave rising from substantially a zero reference value to an unknown value, and a reproducing repetitive backward and forward symmetric scanning waves at a reference frequency rate with rise and falls coincident with said zero reference and unknown values, the system comprising first and second oppositely poled voltage sources; a first normally deenergized capacitor; second and third normally deenergized capacitors, having substantially larger values than the first capacitor; first, second, and third timing resistors; means for coupling the first and second capacitors to the first voltage source in series with the first and second resistors, respectively, and coupling the third capacitor to the second voltage source in series with the third resistor, thereby producing three separate recording scanning waves rising in potentials from zero value across said capacitors; means for stopping said coupling at the end of said recording scanning wave, thereby the voltages assumed across said capacitors at that instant to remain in steady states; fourth and fifth timing resistors; means for coupling the first capacitor to said second and third capacitors in series with said fourth and fifth resistors, respectively, alternately at said reference frequency rate, thereby causing fall and rise of the potential across said first capacitor by the opposite charges across the second and third capacitors; and means for adjusting both the values of said fourth and fifth resistors, and the timing of last said coupling, so that at the time the first capacitor is coupled to the third capacitor the first capacitor has assumed the same potential that it had assumed at the end of said recording scanning wave, and it has assumed zero potential when coupled to the second capacitor, thereby producing across the first capacitor the scanning waves aforesaid.

2. The system for producing frequency conversion scanning waves having a recording scanning wave rising from substantially zero reference value to an unknown value, and a reproducing repetitive backward and forward symmetric scanning waves at a reference frequency rate with rise and falls coincident with said reference and unknown values, the system comprising first and second oppositely poled voltage sources; a first normally deenergized capacitor; second and third normally deenergized capacitors, having substantially larger values than the first capacitor; first, second, and third timing resistors; first, second, and third normally inoperative switching means; means for coupling the first and second capacitors to said first voltage source in series with the first and second resistors, and the first and second switching means, respectively; means for coupling the third capacitor to said second voltage source in series with the third resistor and said third switching means; means for rendering said first, second, and third switching means operative, whereby producing first, second, and third rising potentials from zero value, representative of said recording scanning wave across said capacitors; a fourth timing resistor, and a normally inoperative fourth switching means; means for rendering the first, second, and third switching means inoperative at the end of said recording scanning wave, whereby the potentials assumed at that instant in said capacitors to remain in steady states thereafter; fourth and fifth timing resistors and a fourth normally inoperative switching means; means for coupling the first capacitor to said second capacitor in series with the fourth resistor and said fourth switching means; means for coupling the first capacitor to said third capacitor in series with the fifth resistor and said fifth switching means; means for producing repetitive waves at said reference frequency rate; means for apply last said repetitive waves to the fourth and fifth switching means alternately, for operation of same, so as to cause fall and rise of the voltage across the first capacitor, by virtue of alternate couplings to the oppositely poled charges across said second and third capacitors; and means for adjusting the values of all said timing resistors, and the timing of application of said alternate wave to the fourth and fifth switching means, so that at the time the first capacitor is coupled to the third capacitor the first capacitor has assumed the same potential as it had assumed at the end of said recording scanning wave, and it has assumed zero potential when coupled to the second capacitor, thereby producing across the first capacitor the scanning waves aforesaid.

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