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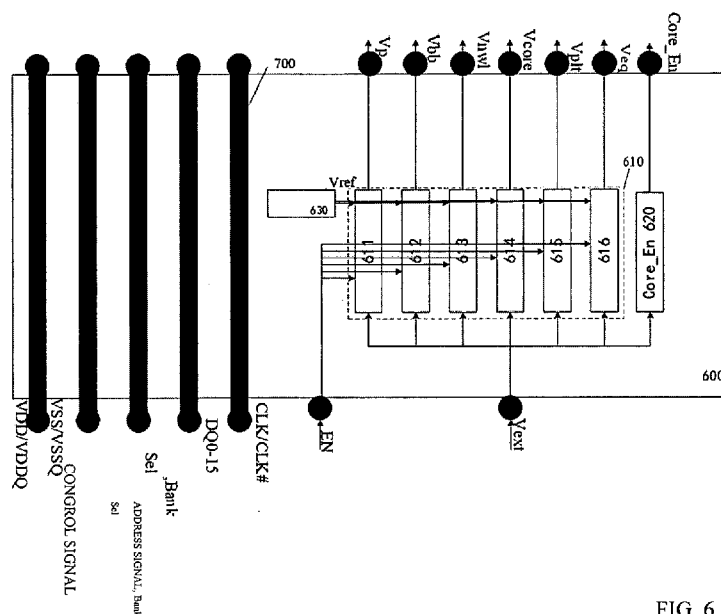


FIG. 6

(57) **Abstract:** An electronic device and a semiconductor package structure are provided. The electronic device includes a plurality of semiconductor dies stacked vertically over each other and a power supply system. The plurality of semiconductor dies are stacked over the power supply system, and the power supply system includes: a voltage generating circuit configured to generate at least one voltage; and a die enabling circuit configured to generate a die enable signal according to the at least one voltage. The at least one voltage is provided to the plurality of semiconductor dies through a power interconnecting structure, and the die enable signal is configured to enable synchronous input of the at least one voltage to the plurality of semiconductor dies.



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POWER SUPPLY SYSTEM AND SEMICONDUCTOR PACKAGE ASSEMBLY

CROSS-REFERENCE TO RELATED APPLICATION

[1] This application is based on and claims priority of the Chinese Patent Application No. 201811132407.4, filed on September 27, 2018 and entitled “POWER SUPPLY SYSTEM AND SEMICONDUCTOR PACKAGE ASSEMBLY.” The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[2] The present disclosure relates generally to the technical field of semiconductor technologies and, more specifically, to a power supply system and a semiconductor package structure.

BACKGROUND

[3] With the technical advancement in mobile consumer electronic devices, such as cellular phones, notebook computers and personal digital assistants, the demand for memory devices with compact structures and high performance has substantially increased. Modern developments in semiconductor memory devices can be viewed as a process of maximizing the storage capacity at the smallest area on a memory device at a specific operating speed. In this context, the term “smallest” generally refers to the smallest area occupied by a memory device in a “horizontal” X/Y plane (e.g., a plane defined by a main surface of a printed circuit board or template board). In general, the allowable horizontal area occupied by the memory device is limited, thus memory devices with vertically integrated structure are developed so that the storage capacity of the devices may be further increased.

[4] It is to be understood that the above information is only used to facilitate understanding the background of the present disclosure, and thus may include information that does not constitute prior art known to a person of ordinary skill in the art.

SUMMARY

[5] One aspect of the present disclosure is directed to an electronic device. The device may comprise a plurality of semiconductor dies and a power supply system. The power supply system may include a voltage generating circuit configured to generate at least one voltage and a die enable circuit configured to generate a die enable signal according to the at least one voltage.

[6] The voltage generating circuit may include at least one voltage regulator configured to generate the at least one voltage. The at least one voltage may be provided to the plurality of semiconductor dies through a power interconnecting structure, and the die enable signal may be configured to enable synchronous input of the at least one voltage to the plurality of semiconductor dies.

[7] In some embodiments of the present disclosure, the at least one voltage may be an internal voltage for the plurality of semiconductor dies.

[8] In some embodiments of the present disclosure, the plurality of semiconductor dies may be stacked over each other.

[9] In some embodiments of the present disclosure, the die enable circuit may comprise at least one voltage detection circuit and an AND gate circuit. Each of the at least one voltage detection circuit may be configured to detect a corresponding one of the at least one voltage, and an input of each of the at least one voltage detection circuit may be connected to a corresponding one of the at least one voltage. An output of each of the at least one voltage detection circuit may be connected to an input of the AND gate circuit, and an output of the AND gate circuit may be configured to output the die enable signal.

[10] In some embodiments of the present disclosure, the at least one voltage regulator may include a first charge pump circuit, a second charge pump circuit, a third charge pump circuit, a first low dropout linear regulator, a second low dropout linear regulator, and a third low dropout linear regulator. The first charge pump circuit, the second charge pump circuit, and the third charge pump circuit may be configured to output, respectively, a first voltage, a second voltage, and a third voltage according to an external voltage.

[11] The first low dropout linear regulator, the second low dropout linear regulator, and the

third low dropout linear regulator may be configured to output, respectively, a fourth voltage, a fifth voltage, and a sixth voltage according to the external voltage. The first voltage may be larger than the external voltage, and the second voltage and the third voltage may both be opposite to the external voltage in polarity. The fourth voltage, the fifth voltage, and the sixth voltage may each be less than or equal to the external voltage.

[12] In some embodiments of the present disclosure, in the aforementioned devices, the power supply system may further comprise a reference voltage generating circuit configured to generate a reference voltage. The at least one voltage regulator may be configured to output, respectively, the first voltage, the second voltage, the third voltage, the fourth voltage, the fifth voltage, and the sixth voltage according to the external voltage, the reference voltage, and a power enable signal.

[13] In some embodiments of the present disclosure, the at least one voltage regulator may include a first low dropout linear regulator, a first charge pump circuit, a second charge pump circuit, a second low dropout linear regulator, a third low dropout linear regulator, and a fourth low dropout linear regulator.

[14] The first low dropout linear regulator, the second low dropout linear regulator, the third low dropout linear regulator, and the fourth low dropout linear regulator may be configured to output, respectively, a first voltage, a fourth voltage, a fifth voltage, and a sixth voltage according to an external voltage. The first charge pump circuit and the second charge pump circuit may be configured to output, respectively, a second voltage and a third voltage according to the external voltage. The first voltage, the fourth voltage, the fifth voltage, and the sixth voltages may each be less than or equal to the external voltage. The second voltage and the third voltage may both be opposite to the external voltage in polarity.

[15] Another aspect of the present disclosure is directed to a semiconductor package structure. The semiconductor package structure may include a package substrate, at least one semiconductor die disposed on the package substrate, and the power supply system of any of the aforementioned embodiments. The power supply system may be disposed on the package substrate.

[16] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the at least one semiconductor die may comprise a plurality of

semiconductor dies, each having a same electrical function.

[17] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the plurality of semiconductor dies may be memory dies.

[18] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the plurality of semiconductor dies may be dynamic random-access memory (DRAM) dies.

[19] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the plurality of semiconductor dies may be stacked vertically on the power supply system.

[20] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the power interconnecting structure may comprise a through silicon via (TSV).

[21] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the plurality of semiconductor dies may be individually disposed on the package substrate directly, and the power supply system may be directly disposed on the package substrate.

[22] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the power interconnecting structure may comprise a metal wire.

[23] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, the plurality of semiconductor dies may be vertically stacked on the package substrate, and the power supply system may be directly disposed on the package substrate.

[24] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, a diameter of the power interconnecting structure may depend on a number of the at least one semiconductor die.

[25] In some embodiments of the present disclosure, the aforementioned semiconductor package structure may further comprise a signal interconnecting structure. The signal interconnecting structure may be configured to input an external control signal to each of the at least one semiconductor die and/or input a data signal to or receive a data signal from each of the at least one semiconductor die through the package substrate.

[26] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, each of the at least one semiconductor die and the power supply system may share a ground power source provided by the package substrate.

[27] In some embodiments of the present disclosure, in the aforementioned semiconductor package structure, a package size of the power supply system may be smaller than or equal to a package size of each of the at least one semiconductor die.

BRIEF DESCRIPTION OF THE DRAWINGS

[28] The various objectives, features and advantages of the present disclosure will become more apparent after reading the Detailed Description of the Embodiments in view of the accompanying drawings. The drawings are only illustrative diagrams of the present disclosure and are not necessarily drew to scale. In the drawings, the same reference indicates the same or similar parts.

[29] FIG. 1 is a schematic structural diagram of a semiconductor package structure in the related art.

[30] FIG. 2 is a schematic structural diagram of another semiconductor package structure in the related art.

[31] FIG. 3 is a schematic structural diagram of a semiconductor die in the related art.

[32] FIG. 4 is a schematic structural diagram of a semiconductor package structure in accordance with one embodiment of the present disclosure.

[33] FIG. 5 is a schematic structural diagram of another semiconductor package structure in accordance with one embodiment of the present disclosure.

[34] FIG. 6 is a schematic structural diagram of a power supply system in accordance with one embodiment of the present disclosure.

[35] FIG. 7 is a sequence diagram of the power supply system shown in FIG. 6.

[36] FIG. 8 is a schematic diagram of a die enable circuit based on the power supply system shown in FIG. 6.

[37] FIG. 9 is a schematic structural diagram of a first voltage detection circuit based on the die enable circuit shown in FIG. 8.

[38] FIG. 10 is a sequence diagram of the first voltage detection circuit shown in FIG. 9.

[39] FIG. 11 is a circuit diagram of a charge pump circuit based on the voltage V_p of the power supply system shown in FIG. 6.

[40] FIG. 12 is a sequence diagram of the charge pump circuit based on the voltage V_p shown in FIG. 11.

[41] FIG. 13 is a circuit diagram of the generation of the voltage V_{pclk} shown in FIG. 11.

[42] FIG. 14 is a circuit diagram of the generation of the voltage V_{pcklen} shown in FIG. 13.

[43] FIG. 15 is a circuit diagram of a charge pump circuit based on the voltage V_{bb} of the power supply system shown in FIG. 6.

[44] FIG. 16 is a circuit diagram of a charge pump circuit based on the voltage V_{nwl} of the power supply system shown in FIG. 6.

[45] FIG. 17 is a circuit diagram of a low dropout linear regulator based on the voltage V_{core} of the power supply system of FIG. 6.

[46] FIG. 18 is a circuit diagram of a low dropout linear regulator based on the voltage V_{eq} of the power supply system of FIG. 6.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[47] Exemplary embodiments embodying the features and advantages of the present disclosure will be described in details in the following description. It should be understood that the present disclosure can be modified based on various embodiments, which will not go beyond the scope of the present disclosure. Description and Drawings are not used for limiting but illustrating the present disclosure.

[48] In the following description of the various exemplary embodiments of the present disclosure, reference is made to the drawings which are parts of the disclosure, and some different exemplary structures, systems and steps according to various aspects of the disclosure are provided. It is understood that other specific components, structures, exemplary devices, systems and steps may be employed, and structural and functional modifications may be made without departing from the scope of the disclosure.

[49] FIG. 1 is a schematic structural diagram of a semiconductor package structure in the

related art.

[50] As shown in FIG. 1, a plurality of semiconductor dies (for example, the semiconductor memory dies A-D in FIG. 1) may be vertically stacked in a vertical plane Z relative to a horizontal plane X/Y. For example, the die A may be arranged on top of the die B, the die B may be arranged on top of the die C, and the die C may be arranged on top of the die D.

[51] A stacked semiconductor package structure may be one type of three-dimensional (3D) integrated circuit (IC). In other words, from a perspective of other systems (such as memory controllers), 3D memory devices may act as integrated memory devices. The data writing and reading operations may be performed by the 3D memory device so that data writing and reading methods that are generally applicable to non-stacked memory devices (i.e., 2D memory devices) may be used for 3D memory devices. Compared to non-stacked memory devices, 3D memory devices are capable of storing and providing a larger amount of data on a unit area of horizontal surface area.

[52] As shown in FIG. 1, a semiconductor package structure 100 having a plurality of stacked semiconductor dies may include a package substrate 101 and semiconductor dies A-D which are stacked on the package substrate 101 successively.

[53] Each semiconductor die may have a peripheral region on which electrode pads 102 may be disposed. The electrode pads 102 of the semiconductor dies A-D may be interconnected with electrode pads (not shown) on the package substrate 101 by bonding wires 103.

[54] In the semiconductor package structure 100 shown in FIG. 1, the width of each electrode pad 102 should satisfy certain requirements in order to achieve a reliable connection between the bonding wire 103 and the electrode pad 102. In addition, the distance between neighboring electrode pads 102 (the pitch) cannot be too small. As a result, the number of electrode pads 102 provided on the semiconductor die may be limited. Moreover, the bonding wires 103 increase the total horizontal area occupied by the stacked devices, and an intermediate layer, such as a Re-Distribution Layer (RDL) 104, may need to be provided between adjacent semiconductor dies in the stack.

[55] If the semiconductor dies A-D are Dynamic Random Access Memory (DRAM) dies, a large number of signal terminals, such as the address signal terminal, command signal terminal and data line terminal, should be provided with electrode pads 102, in addition to

the power supply terminal and the ground terminal. Therefore, the number of electrode pads 102 that can be assigned to the power supply terminal and the ground terminal may be limited.

[56] FIG. 2 is a schematic structural diagram of another semiconductor package structure in the related art.

[57] In FIG. 2, a 3D integrated circuit based on Through Silicon Via (TSV) is formed by vertically stacking multiple layers of dies with TSVs therethrough to achieve interconnection between dies for data communication. Thus, in addition to the horizontal area defined by the periphery of the largest die in the stack, no additional horizontal area needs to be occupied. In addition, TSVs may reduce the overall length of certain signal paths through the stacked structure of devices, thus helping to speed up operations. Thus, with the use of TSVs or similar stacking processes, devices, such as memory devices, formed by multiple vertically stacked dies can use a single integrated circuit with a relatively small horizontal surface area to store and provide large amounts of data.

[58] As shown in FIG. 2, the semiconductor package structure 200 may have a plurality of semiconductor dies A-D of the same size. The plurality of semiconductor dies A-D may be stacked one above another through a plurality of TSVs 202 and electrode pads 203, thereby achieving electrical connection between the semiconductor dies. This technique can reduce the size of the semiconductor package structure since it is not necessary to provide solder pads for each bonding wire.

[59] The semiconductor package structure 200 of FIG. 2 may be a DRAM device. Specifically, the semiconductor package structure 200 may include a package substrate 201 and four DRAM dies A-D successively stacked on the package substrate 201. In the DRAM dies and the peripheral regions of the package substrate 201, a plurality of TSVs 202 may be formed passing through the semiconductor dies from the top DRAM die to the bottom DRAM die along the Z direction.

[60] FIG. 3 is a schematic structural diagram of a semiconductor die in the related art.

[61] FIG. 3 is a schematic diagram of a single layer of DRAM die in the semiconductor package structure 200 as shown in FIG. 2. The DRAM dies A-D in FIG. 2 may each have the same ports or pins. For example, these ports or pins may include: BA0-2 (Bank Sel), A0-15

(Address signal), RAS/, CAS/, WE/(Command control signal), CLK, CLK/ (clock signal), CS/, RESET/ (reset signal), DQ[0:15] (data signal), and signals of the external power supplies VDD, VDDQ, VSS, VSSQ, VPP, etc. These ports or pins may be connected to the TSVs, metal wires or RDLs and may also be connected to package balls (PINs).

[62] Each of the control signals or address signals, such as Bank Sel, Address, Command, CLK, RESET/, may be electrically connected to and pass through each layer of the DRAM dies A-D. Signals of the external power supplies such as VDD, VDDQ, VSS, VSSQ, and VPP may be each electrically connected to and pass through each layer of the DRAM dies A-D.

[63] DRAM memory cell array 301 may include a plurality of single memory cells arranged corresponding to a matrix formed by signal lines arranged in rows and columns. Each memory cell may be capable of storing “write data” in response to a write command and providing “read data” in response to a read command received from an external device (not shown), such as a memory controller or processor. The read or write commands may generate certain control signals (e.g., row address, column address, enable signal, etc.), which may be applied to, along with certain control voltages, the memory cell array 301 through associated peripheral devices (e.g., row decoder 302 and column decoder 303).

[64] During a write operation, the “write data” (i.e., data to be stored in memory cell array 301) may be transmitted from an external circuit (e.g., external memory, external input device, processor, memory controller, memory switch, etc.) to a data register. Once stored in the data register, the “write data” may be written into the memory cell array 301 by conventional structures and techniques, which may include, for example, sense amplifiers and write driver circuits.

[65] During a read operation, the applied control voltage and the control signal outputs from row decoders 302 and column decoders 303 may typically cooperate to identify and select one or more memory cells in the memory cell array 301 and facilitate providing signals indicating the value of the data stored in the memory cells. The resulting “read data” may typically be transmitted by a read sense amplifier and stored in a data register. The “read data” stored in the data register then may be supplied to external circuits under the control of the read control circuit.

[66] As shown in FIG. 3, each layer of DRAM dies in FIG. 2 may include all logical blocks related to the DRAM operations, such as write/read control logic, refresh control, and power supply (e.g., V_p , V_{bb} , V_{nwl} , V_{core} , V_{eq} , V_{plt} , etc.). The power supply may need to be adjusted by the corresponding charge pump circuit or voltage regulator to obtain a desired voltage level.

[67] Each layer of the DRAM dies in the semiconductor package structure 200 shown in FIG. 2 may include a respective charge pump circuit and a voltage regulator. That is, the DRAM dies A-D may each have the same internal power supply circuit. Since the DRAM dies may need to be fabricated by advance nano-scale processes, and the power supply dies (Power IC) generally can be fabricated by micro-scale processes, the difference between the two processes, in term of feature size, may be up to 1000 times. If the power supply die is integrated in the DRAM dies, the efficiency of the power supply die may reduce (e.g., from 90% to 60% or so) since the manufacturing process for the DRAM dies may not be suitable for the power supply die. In addition, integrating the power supply die into the DRAM dies will occupy the die area and increase the cost of the DRAM dies. Moreover, the manufacturing process of the DRAM dies is an expensive process, while the manufacturing process of the power supply is relatively low in cost.

[68] FIG. 4 is a schematic structural diagram of a semiconductor package structure in accordance with one embodiment of the present disclosure.

[69] As shown in FIG. 4, this disclosure provides a semiconductor package structure 400. The semiconductor package structure 400 may include: a package substrate 401; a power supply system 402 which may be disposed on the package substrate 401; and at least one semiconductor die. In this embodiment, four semiconductor dies A-D may be provided as an example, but the number of dies can be adjusted according to specific needs, and the present disclosure is not limited thereto.

[70] In some embodiments, the at least one semiconductor die may include a plurality of semiconductor dies, and each of the plurality of semiconductor dies may have same electrical functions.

[71] In some embodiments, the plurality of semiconductor dies may be memory dies.

[72] In some embodiments, the plurality of semiconductor dies may be DRAM dies. The

semiconductor die, however, may be any type of die, and this disclosure is not limited thereto.

[73] In the embodiment shown in FIG. 4, the plurality of semiconductor dies may be vertically stacked on the power supply system 402 successively. For example, the DRAM die A may be vertically stacked on the DRAM die B, and the DRAM die B may be vertically stacked on the DRAM die C, and the DRAM die C may be vertically stacked on the DRAM die D.

[74] In the embodiment shown in FIG. 4, the power supply system 402 may send, through TSVs 403 acting as power interconnecting structures, the internal voltages to the respective semiconductor dies.

[75] It should be noted that FIG. 4 only shows one embodiment in which a plurality of semiconductor dies are vertically and successively stacked on the power supply system. In other embodiments, each of the plurality of semiconductor dies may be directly disposed on the package substrate 401. That is, the semiconductor dies may be arranged adjacent to each other in the horizontal plane of the package substrate 401 (i.e., side-by-side arrangement), and the power supply system may also be directly disposed on the package substrate 401. In other embodiments, the plurality of semiconductor dies may be vertically and successively stacked on the package substrate 401, and the power supply system may be directly disposed on the package substrate 401.

[76] In the embodiments in which the semiconductor dies are arranged adjacent to each other in the horizontal plane of the package substrate 401, the power supply system 402 may send, through metal wires acting as power interconnecting structures, the internal voltages to the respective semiconductor dies.

[77] FIG. 5 is a schematic structural diagram of another semiconductor package structure in accordance with one embodiment of the present disclosure.

[78] As shown in FIG. 5, at least one internal voltage output from the power supply system 402 may be input to each layer of the DRAM dies A-D through the corresponding TSVs 403, respectively. Three arrows are shown in FIG. 5 are for illustration purpose only and are not intended to limit the amount of internal voltages that may be output by power supply system 402.

[79] In some embodiments, the diameter of the power interconnecting structure may depend on the number of the at least one semiconductor die. For example, the larger the number of the semiconductor dies stacked on the power supply system 402, the larger the diameter of the corresponding TSV 403 may be. The higher the layer of the semiconductor dies to which the TSV 403s need to transmit the signal, the larger the voltage drop will be. In this case, the voltage drop may be decreased by increasing the diameter of the TSVs 403 or the number of TSVs 403 connected in parallel, so that the values of the same internal voltage received by the respective layers of the semiconductor dies may be substantially the same.

[80] In the embodiment shown in Fig. 5, each TSV 403 may have a diameter of, for example, about 20 μm and may be arranged at a pitch of about 50 μm , which is sufficient to prevent short-circuit failure between adjacent TSVs. However, the diameters and pitches can be reduced with the possible development of TSV technology.

[81] Referring to FIG. 5, the semiconductor package structure may further include: a signal interconnecting structure 404, which may be configured to input external control signals (e.g., Address, Command, etc.) to each of the semiconductor dies and/or input data signal (e.g., DQ [0-15]) to or output data signal (e.g., DQ [0-15]) from each of the semiconductor dies through the package substrate 401. In the embodiment of the present disclosure, the signal interconnecting structure 404 may also be a TSV.

[82] In the embodiment shown in FIG. 5, each of the semiconductor dies A-D and the power supply system 402 may share a ground power source (not shown) provided by the package substrate 401.

[83] In some embodiments, a package size of the power supply system may be less than or equal to a package size of each of the semiconductor dies.

[84] For example, in the embodiments shown in FIGs. 4 and 5, the package size of the power supply system 402 may be smaller than the package size of each of the semiconductor dies A-D.

[85] FIG. 6 is a schematic structural diagram of a power supply system in accordance with one embodiment of the present disclosure.

[86] As shown in FIG. 6, this disclosure provides a power supply system 600. The power supply system 600 may include an internal voltage generating circuit 610, which may be

configured to generate at least one internal voltage. The at least one internal voltage may be provided to at least one semiconductor die (such as the DRAM die in the aforementioned embodiments, but the disclosure is not limited thereto) through a power interconnecting structure (such as a TSV or bonding wire). The power supply system 600 may further comprise a circuit 620, which may configured to generate a die enable signal Core_En according to the at least one internal voltage. The die enable signal Core_En may be configured to enable synchronous input of the at least one internal voltage to the at least one semiconductor die.

[87] In some embodiments, the internal voltage generating circuit 610 may include at least one voltage regulator configured to generate the at least one internal voltage.

[88] In some embodiments, the at least one voltage regulator may include a first charge pump circuit, a second charge pump circuit, a third charge pump circuit, a first low dropout linear regulator, a second low dropout linear regulator and a third low dropout linear regulator. The first charge pump circuit, the second charge pump circuit, and the third charge pump circuit may be configured to output, respectively, a first internal voltage, a second internal voltage, and a third internal voltage according to an external voltage. The first low dropout linear regulator, the second low dropout linear regulators and the third low dropout linear regulator may be configured to output, respectively, a fourth internal voltage, a fifth internal voltage, and a sixth internal voltage according to the external voltage. The first internal voltage may be larger than the external voltage, the second internal voltage and the third internal voltage may both be opposite to the external voltage in polarity. The fourth internal voltage, the fifth internal voltage, and the sixth internal voltage may each be less than or equal to the external voltage.

[89] In some embodiments, a Low Dropout Regulator (LDO) may use a transistor or a Field Effect Transistor (FET) operating in its linear region to subtract the excess from the applied input voltage to produce a regulated output voltage. LDO has outstanding advantages in that it is cost-effective and has little noise and quiescent current. Moreover, LDO requires very few external components. For example, a LDO usually only requires one or two bypass capacitors. Thus a LDO may achieve high efficiency in cases in which the input voltage and the output voltage are very close. In such cases, the input current of the LDO is substantially

equal to the output current. If the voltage drop (the difference between the output voltage and the input voltage) is large, the energy consumed by the LDO may be large and the efficiency may deteriorate. In other embodiments, the LDO in the embodiment of the present disclosure may also be replaced by a DC-DC converter according to actual needs.

[90] In the embodiment shown in FIG. 6, as an example, the semiconductor dies may be DRAM dies, and it is assumed that each layer of the DRAM dies requires six internal voltages, which are V_p , V_{bb} , V_{nw1} , V_{core} , V_{plt} , and V_{eq} . The at least one voltage regulator may include a first charge pump circuit 611, a second charge pump circuit 612, a third charge pump circuit 613, a first low dropout linear regulator 614, a second low dropout linear regulator 615, and a third low dropout linear regulator 616. The first charge pump circuit 611 may be configured to output the first internal voltage V_p according to the external voltage V_{ext} . The second charge pump circuit 612 may be configured to output the second internal voltage V_{bb} according to the external voltage V_{ext} . The third charge pump circuit 613 may be configured to output the third internal voltage V_{nw1} according to the external voltage V_{ext} . The first low dropout linear regulator 614 may be configured to output a fourth internal voltage V_{core} according to the external voltage V_{ext} . The second low dropout linear regulator 615 may be configured to output the fifth internal voltage V_{plt} according to the external voltage V_{ext} . The third low dropout linear regulator 616 may be configured to output the sixth internal voltage V_{eq} according to the external voltage V_{ext} .

[91] In some embodiments, the first internal voltage V_p may be larger than the external voltage V_{ext} , and the second internal voltage V_{bb} and the third internal voltage V_{nw1} may be opposite to the external voltage V_{ext} in polarity. For example, these voltages may have the following values: $V_{ext}=1.2V$, $V_p=3.0V$, $V_{bb}=-0.5V$, $V_{nw1}=-0.3V$. The above voltage values are for illustrative purposes only, and the disclosure is not limited thereto.

[92] It should be noted that when the input voltage is opposite to the output voltage in polarity, the inverter in the corresponding charge pump can convert the input positive voltage into the output negative voltage.

[93] In some embodiments, the fourth internal voltage V_{core} , the fifth internal voltage V_{plt} , and the sixth internal voltage V_{eq} may each be less than or equal to the external voltage V_{ext} . For example, these voltages may have the following values: $V_{ext}=1.2V$, $V_{core}=1.0V$, and

$V_{plt}=V_{eq}=0.5V$. The disclosure is not limited thereto though.

[94] In some embodiments, the at least one voltage regulator may include a first low dropout linear regulator, a first charge pump circuit, a second charge pump circuit, a second low dropout linear regulator, a third low dropout linear regulator, and a fourth low dropout linear regulator. The first low dropout linear regulator, the second low dropout linear regulator, the third low dropout linear regulator, and the fourth low dropout linear regulator may be configured to output, respectively, a first internal voltage, a fourth internal voltage, a fifth internal voltage, and a sixth internal voltage according to an external voltage. The first charge pump circuit and the second charge pump circuit may be configured to output, respectively, a second internal voltage and a third internal voltage according to the external voltage. The first internal voltage, the fourth internal voltage, the fifth internal voltage, and the sixth internal voltage may each be less than or equal to the external voltage. Both the second internal voltage and the third internal voltage may be opposite to the external voltage in polarity.

[95] Taking FIG. 6 as an example, assuming that each layer of the semiconductor dies requires six internal voltages, which are V_p , V_{bb} , V_{nw1} , V_{core} , V_{plt} , and V_{eq} . The at least one voltage regulator may include the first low dropout linear regulator 611, the first charge pump circuit 612, the second charge pump circuit 613, the second low dropout linear regulator 614, the third low dropout linear regulator 615, and the fourth low dropout linear regulator 616. The first low dropout linear regulator 611 may be configured to output the first internal voltage V_p according to the external voltage V_{ext} . The first charge pump circuit 612 can be configured to output a second internal voltage V_{bb} according to the external voltage V_{ext} . The second charge pump circuit 613 can be configured to output a third internal voltage V_{nw1} according to the external voltage V_{ext} . The second low dropout linear regulator 614 can be configured to output a fourth internal voltage V_{core} in accordance with the external voltage V_{ext} . The third low dropout linear regulator 615 may be configured to output the fifth internal voltage V_{plt} according to the external voltage V_{ext} . The fourth low dropout linear regulator 616 may be configured to output the sixth internal voltage V_{eq} according to the external voltage V_{ext} .

[96] In some embodiments, the first internal voltage V_p , the fourth internal voltage V_{core} ,

the fifth internal voltage V_{pl1} and the sixth internal voltage V_{eq} each may be less than or equal to the external voltage V_{ext} . For example, these voltages may have the following values: $V_{ext} > 3.3V$, $V_p = 3.0V$, $V_{core} = 1.0V$, $V_{pl1} = V_{eq} = 0.5V$. The second internal voltage V_{bb} and the third internal voltage V_{nw1} may each be opposite to the external voltage V_{ext} in polarity. For example, these voltages may have the following values: $V_{ext} > 3.3V$, $V_{bb} = -0.5V$, $V_{nw1} = -0.3V$.

[97] Referring back to FIG. 6, the power supply system 600 may further include a reference voltage generating circuit 630 that may be configured to generate the reference voltage V_{ref} .

[98] In the embodiment shown in FIG. 6, each voltage regulator may be configured to output, respectively, the first internal voltage V_p , the second internal voltage V_{bb} , the third internal voltage V_{nw1} , the fourth internal voltage V_{core} , the fifth internal voltage V_{pl1} , and the sixth internal voltage V_{eq} according to the external voltage V_{ext} , the reference voltage V_{ref} and the power enable signal EN.

[99] In the embodiment shown in FIG. 6, the semiconductor package structure including the power supply system 600 may further include a signal interconnecting structure 700. The signal-die interconnection structure 700 may be configured to input external control signals (e.g., the external voltage V_{DD}/V_{DDQ} , V_{SS}/V_{SSQ} , the address signal Address, the command signal Command, the clock signal CLK or /CLK, etc.) to each of the semiconductor dies and/or input data signal (e.g., DQ [0-15]) to or output data signal (e.g., DQ [0-15]) from each of the semiconductor dies through the package substrate (not shown) of the semiconductor package structure. In the embodiment of the present disclosure, the signal interconnecting structure 700 may also be a TSV.

[100] It should be noted that the embodiment shown in FIG. 6 is described using an example in which the semiconductor die of the semiconductor package structure is a DRAM die. In other embodiments, the semiconductor die of the semiconductor package structure may be other type of die. Correspondingly, the number and type of internal voltages generated by the internal voltage generating circuit may also be changed accordingly. Similarly, the external control signals and/or data signals provided by the signal interconnecting structure may also be changed accordingly.

[101] FIG. 7 is a sequence diagram of the power supply system shown in FIG. 6.

[102]As shown in FIG. 7, when only the external voltage V_{ext} is at a high level, the internal voltage generating circuit will not work until the power enable signal EN is also at a high level. When both V_{ext} and EN are at a high level, the internal voltage generating circuit begins to work. After a certain delay, the internal voltage generating circuit may output, respectively, the first internal voltage V_p , the second internal voltage V_{bb} , the third internal voltage V_{nw1} , the fourth internal voltage V_{core} , the fifth internal voltage V_{plt} , and the sixth internal voltage V_{eq} .

[103]Since there may exist delays when outputting the high levels for various internal voltages (i.e., the high levels of various internal voltages may not be output synchronously), the die enable signal Core_En may be added to synchronize these internal voltages.

[104]FIG. 8 is a schematic diagram of a die enable circuit based on the power supply system shown in FIG. 6.

[105]In some embodiments, the die enable circuit 620 may include: at least one voltage detection circuit configured to detect a corresponding internal voltage, and an AND gate circuit. The input of each of the voltage detection circuits may be connected to a corresponding internal voltage, the output of each voltage detection circuit may be connected to the input of the AND gate circuit, and the output of the AND gate circuit may be configured to output the die enable signal Core-En.

[106]In the embodiment shown in FIG. 8, the die enable circuit 620 may include a first voltage detection circuit 621, a second voltage detection circuit 622, a third voltage detection circuit 623, a fourth voltage detection circuit 624, and a fifth voltage detection circuit 625, and a sixth voltage detection circuit 626. The first voltage detection circuit 621 may be configured to detect the first internal voltage V_p , and output the first detection signal Pwr_rdy1. The second voltage detection circuit 622 may be configured to detect the second internal voltage V_{bb} , and output the second detection signal Pwr_rdy2. The third voltage detection circuit 623 may be configured to detect the third internal voltage V_{nw1} and output the third detection signal Pwr_rdy3. The fourth voltage detection circuit 624 can be configured to detect the fourth internal voltage V_{core} , and output the fourth detection signal Pwr_rdy4. The fifth voltage detection circuit 625 may be configured to detect the fifth internal voltage V_{plt} , and output the fifth detection signal Pwr_rdy5. The sixth voltage

detection circuit 626 may be configured to detect the sixth internal voltage V_{eq} , and output the sixth detection signal Pwr_rdy6 . The first detection signal Pwr_rdy1 , the second detection signal Pwr_rdy2 , the third detection signal Pwr_rdy3 , the fourth detection signal Pwr_rdy4 , the fifth detection signal Pwr_rdy5 , and the sixth detection signal Pwr_rdy6 may all input to the AND gate circuit 627, and the AND gate circuit 627 may output the die enable signal $Core_En$.

[107]It should be noted that the number of voltage detection circuits included in the die enabling circuit and the received input signal can be adaptively adjusted according to the type of semiconductor die.

[108]FIG. 9 is a schematic structural diagram of a first voltage detection circuit based on the die enabling circuit shown in FIG. 8.

[109]Using the first voltage detection circuit 621 as an example, FIG. 9 shows a circuit diagram for the voltage detection circuit in FIG. 8. The circuit diagram of the other voltage detection circuits may be the same as the first voltage detection circuit 621 shown in FIG. 9.

[110]The first voltage detection circuit 621 may receive the power enable signal EN and the reference voltage V_{ref} . An input voltage terminal V_{in} may receive and divide the first internal voltage V_p , and the divided voltage may be sent to a positive input of a comparator, and be compared with the reference voltage V_{ref} on the negative input of the comparator. Then the comparison result may be sent to an input Set of a latch, and the power enable signal EN may be sent to an input Reset of the latch may. The latch may output the first detection signal Pwr_rdy1 .

[111]The power supply system and the semiconductor package structure according to the embodiments of the present disclosure may simultaneously provide internal voltages to each of the semiconductor dies in the semiconductor package structure from a same power supply system, and the power supply system does not need to be integrated in any of the individual semiconductor die. Thus the semiconductor dies can be manufactured by advance fabrication processes, while the power supply system may be manufactured by a regular process. Therefore, on one hand, the efficiency of the power supply system can be improved since the power supply system and the semiconductor dies may each be fabricated by corresponding proper manufacturing processes; and on the other hand, the cost of the DRAM dies

fabrication may be reduced as the power supply system does not occupy the die area inside the DRAM dies.

[112]FIG. 10 is a sequence diagram of the first voltage detection circuit shown in FIG. 9. FIG. 11 is a circuit diagram of a charge pump circuit based on the voltage V_p of the power supply system shown in FIG. 6. FIG. 12 is a sequence diagram of the charge pump circuit based on the voltage V_p shown in FIG. 11. FIG. 13 is a circuit diagram of the generation of the voltage V_{pclk} shown in FIG. 11. FIG. 14 is a circuit diagram of the generation of the voltage V_{pclken} shown in FIG. 13.

[113]As shown in FIG. 10, the reference voltage V_{ref} may reach a high level shortly after the voltage V_{ext} is supplied, and the external controller may provide the signal EN to enable the charge pump circuit in FIG. 11 to work (i.e., pump), which may cause the voltage V_p to gradually rise. When the voltage V_p reaches a target voltage, the first voltage detection circuit in FIG. 9 may, after detecting that the voltage V_p has reached the target voltage, generate the first detection signal Pwr_rdy1 , indicating that the voltage V_p has reached the target voltage. In FIG. 12, after the voltage V_p reaches the target voltage, the generation of the signal V_{pclk} may be stopped, causing the charge pump circuit in FIG. 11 to stop working. If the voltage V_p drops below the target voltage, the generation of the voltage V_{pclk} may begin, causing the charge pump circuit in FIG. 11 to begin working (i.e., pumping).

[114]FIG. 13 shows a voltage V_{pclk} generating circuit. When the signal V_{pclken} is at a high level, the generating of the voltage V_{pclk} starts. When the voltage V_{pclken} drops to a low level, the generation of the voltage V_{pclk} stops. FIG. 14 shows a voltage V_{pclken} generating circuit in which the voltage dividing resistors $R1$ and $R2$ can be designed according to specific application scenarios.

[115]FIG. 15 is a circuit diagram of a charge pump circuit based on the voltage V_{bb} of the power supply system shown in FIG. 6. FIG. 16 is a circuit diagram of a charge pump circuit based on the voltage V_{nwl} of the power supply system shown in FIG. 6. The principle of FIG. 15 and FIG. 16 is substantially the same as that of FIG. 11, and detailed descriptions are omitted for the sake of conciseness.

[116]FIG. 17 is a circuit diagram of a low dropout linear regulator based on the voltage V_{core} of the power supply system shown in FIG. 6. FIG. 18 is a circuit diagram of a low

dropout linear regulator based on the voltage V_{eq} of the power supply system shown in FIG. 6.

[117] Taking FIG. 17 as an example, the low dropout linear regulator may be an operational amplifier (OP), a positive input of the OP may be coupled to a voltage resulted from division of the voltage V_{ext} , and the value of the resistors R3 and R4 can be adjusted according to specific application scenarios. The negative input of the OP may be provided with a feedback voltage V_{core} , and the voltage V_{ext} supplied to the third input of the OP may be configured for amplification and rectification.

[118] It should be noted that the resistance values of the resistors R3 and R4 may be same or different. Similarly, the resistance values of the voltage dividing resistors R5 and R6 in FIG. 18 may be same or different.

[119] Exemplary embodiments of the power supply system and semiconductor package structure proposed by the present disclosure are described and/or illustrated in details above. However, embodiments of the present disclosure are not limited to the specific embodiments described herein, but rather, the components and/or steps of each embodiment can be used independently and separately from the other components and/or steps described herein. Each component and/or each step of an embodiment may also be used in combination with other components and/or steps of other embodiments. In the herein description or/and illustration of the elements/components/etc., the terms “one”, “the” etc. are used to indicate the presence of one or more elements/components/etc. The terms “comprising”, “including” and “having” are used for open-ended mode, which means additional elements/components or the like can also be provided or included in addition to the listed elements/components/etc. Moreover, the terms “first” and “second” and the like in the claims and the description are used only as a mark, not a numerical limit to the corresponding objects.

[120] While the power supply system and the semiconductor package structure according to the present disclosure have been described in terms of various specific embodiments, those skilled in the art will realize that the implementation of the present disclosure can be modified within the spirit and scope of the claims.

CLAIMS

1. An electronic device, comprising:
a plurality of semiconductor dies; and
a power supply system, comprising:
a voltage generating circuit configured to generate at least one voltage, wherein the voltage generating circuit comprises at least one voltage regulator configured to generate the at least one voltage; and
a die enable circuit configured to generate a die enable signal according to the at least one voltage, wherein the at least one voltage is provided to the plurality of semiconductor dies through a power interconnecting structure, and the die enable signal is configured to enable synchronous input of the at least one voltage to the plurality of semiconductor dies.
2. The device of claim 1, wherein the at least one voltage is an internal voltage for the plurality of semiconductor dies.
3. The device of claim 1, wherein the plurality of semiconductor dies are stacked over each other.
4. The device of claim 1, wherein the die enable circuit comprises:
at least one voltage detection circuit each configured to detect a corresponding one of the at least one voltage; and
an AND gate circuit, wherein an input of each of the at least one voltage detection circuit is connected to a corresponding one of the at least one voltage, an output of each of the at least one voltage detection circuit is connected to an input of the AND gate circuit, and an output of the AND gate circuit is configured to output the die enable signal.
5. The device of claim 1, wherein the at least one voltage regulator comprises a first

charge pump circuit, a second charge pump circuit, a third charge pump circuit, a first low dropout linear regulator, a second low dropout linear regulator, and a third low dropout linear regulator,

wherein the first charge pump circuit, the second charge pump circuit, and the third charge pump circuit are configured to output, respectively, a first voltage, a second voltage, and a third voltage according to an external voltage,

the first low dropout linear regulator, the second low dropout linear regulator, and the third low dropout linear regulator are configured to output, respectively, a fourth voltage, a fifth voltage, and a sixth voltage according to the external voltage,

and wherein the first voltage is larger than the external voltage, and the second voltage and the third voltage are both opposite to the external voltage in polarity, and the fourth voltage, the fifth voltage, and the sixth voltage are each less than or equal to the external voltage.

6. The device of claim 5, wherein the power supply system further comprises:

a reference voltage generating circuit configured to generate a reference voltage,

wherein the at least one voltage regulator are configured to output, respectively, the first voltage, the second voltage, the third voltage, the fourth voltage, the fifth voltage, and the sixth voltage according to the external voltage, the reference voltage, and a power enable signal.

7. The device of claim 1, wherein the at least one voltage regulator comprises a first low dropout linear regulator, a first charge pump circuit, a second charge pump circuit, a second low dropout linear regulator, a third low dropout linear regulator, and a fourth low dropout linear regulator,

wherein the first low dropout linear regulator, the second low dropout linear regulator, the third low dropout linear regulator, and the fourth low dropout linear regulator are configured to output, respectively, a first voltage, a fourth voltage, a fifth voltage, and a sixth voltage according to an external voltage,

the first charge pump circuit and the second charge pump circuit are configured to

output, respectively, a second voltage and a third voltage according to the external voltage,

and wherein the first voltage, the fourth voltage, the fifth voltage, and the sixth voltages are each less than or equal to the external voltage, the second voltage and the third voltage are both opposite to the external voltage in polarity.

8. A semiconductor package structure, comprising:

a package substrate;

at least one semiconductor die disposed on the package substrate; and

the power supply system of claim 1, wherein the power supply system is disposed on the package substrate.

9. The semiconductor package structure of claim 8, wherein the at least one semiconductor die comprises a plurality of semiconductor dies, each of the plurality of semiconductor dies having a same electrical function.

10. The semiconductor package structure of claim 9, wherein the plurality of semiconductor dies are memory dies.

11. The semiconductor package structure of claim 10, wherein the plurality of semiconductor dies are dynamic random-access memory (DRAM) dies.

12. The semiconductor package structure of claim 9, wherein the plurality of semiconductor dies are stacked vertically on the power supply system.

13. The semiconductor package structure of claim 12, wherein the power interconnecting structure comprises a through silicon via (TSV).

14. The semiconductor package structure of claim 9, wherein the plurality of semiconductor dies are individually disposed on the package substrate directly, and the power supply system is directly disposed on the package substrate.

15. The semiconductor package structure of claim 14, wherein the power interconnecting structure comprises a metal wire.
16. The semiconductor package structure of claim 9, wherein the plurality of semiconductor dies are vertically stacked on the package substrate, and the power supply system is directly disposed on the package substrate.
17. The semiconductor package structure of claim 8, wherein a diameter of the power interconnecting structure depends on a number of the at least one semiconductor die.
18. The semiconductor package structure of claim 8, further comprising:
a signal interconnecting structure,
wherein the signal interconnecting structure is configured to input an external control signal to each of the at least one semiconductor die and/or input a data signal to or receive a data signal from each of the at least one semiconductor die through the package substrate.
19. The semiconductor package structure according to claim 8, wherein each of the at least one semiconductor die and the power supply system share a ground power source provided by the package substrate.
20. The semiconductor package structure according to claim 8, wherein a package size of the power supply system is smaller than or equal to a package size of each of the at least one semiconductor die.

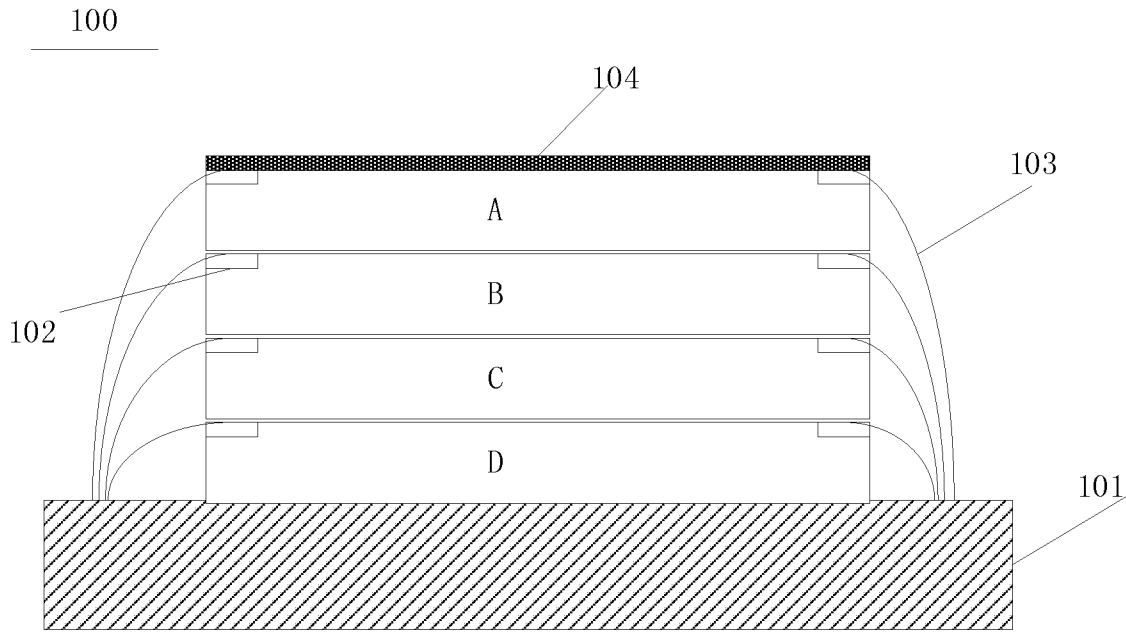


FIG. 1

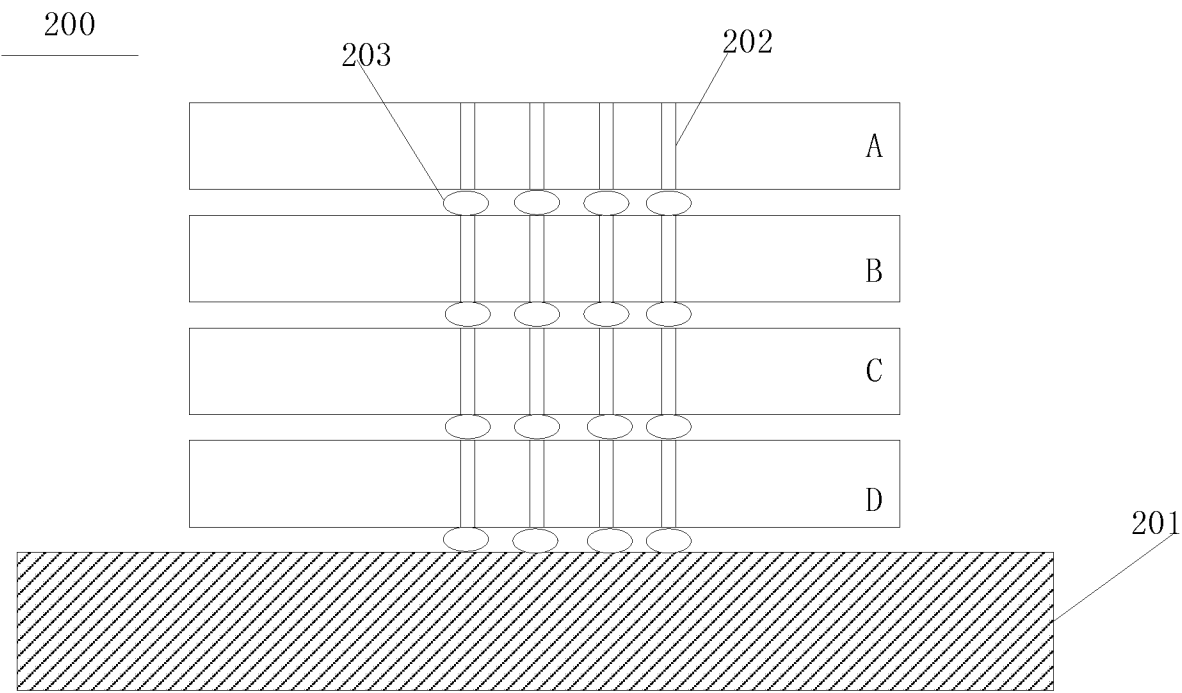


FIG. 2

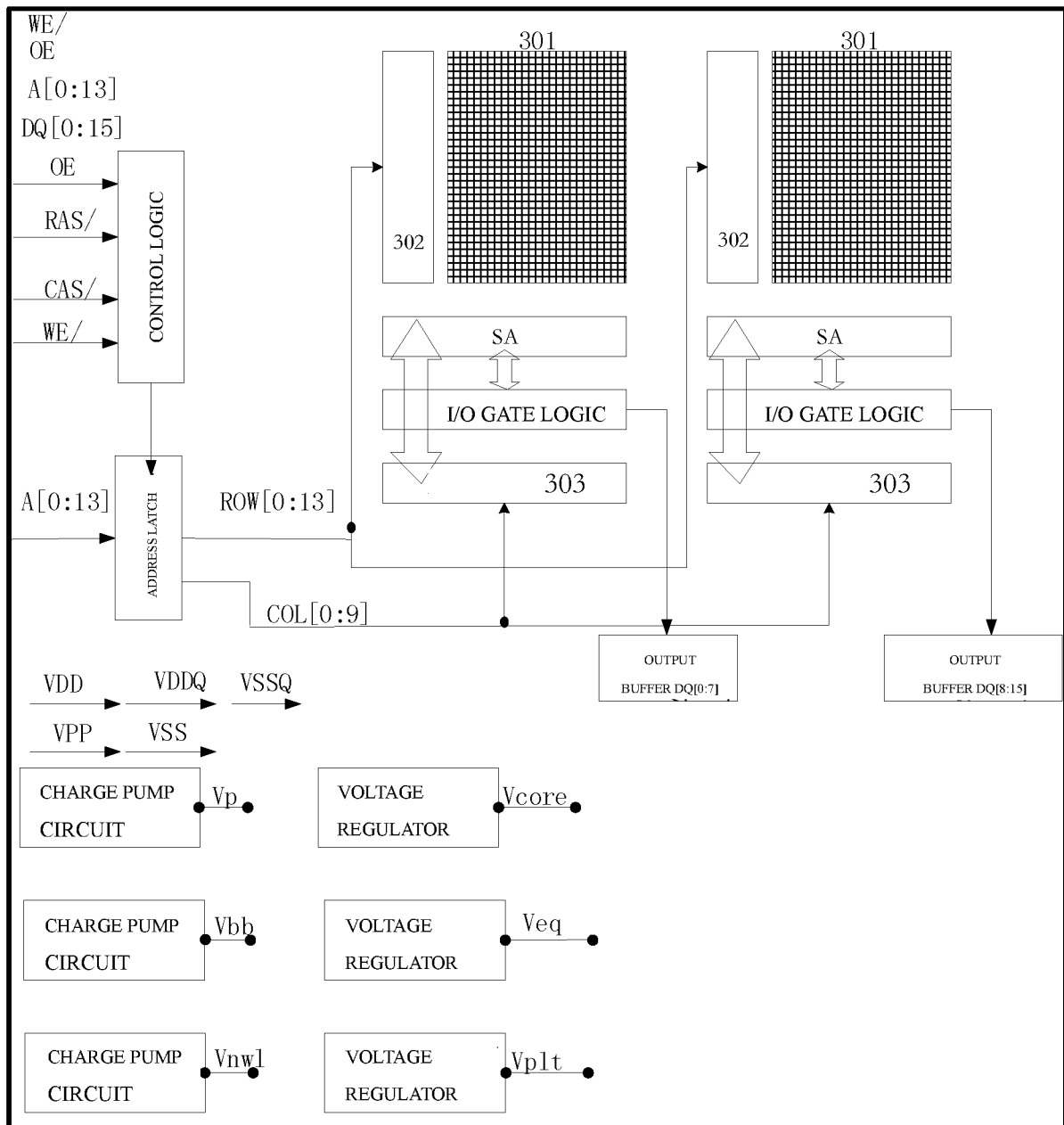


FIG. 3

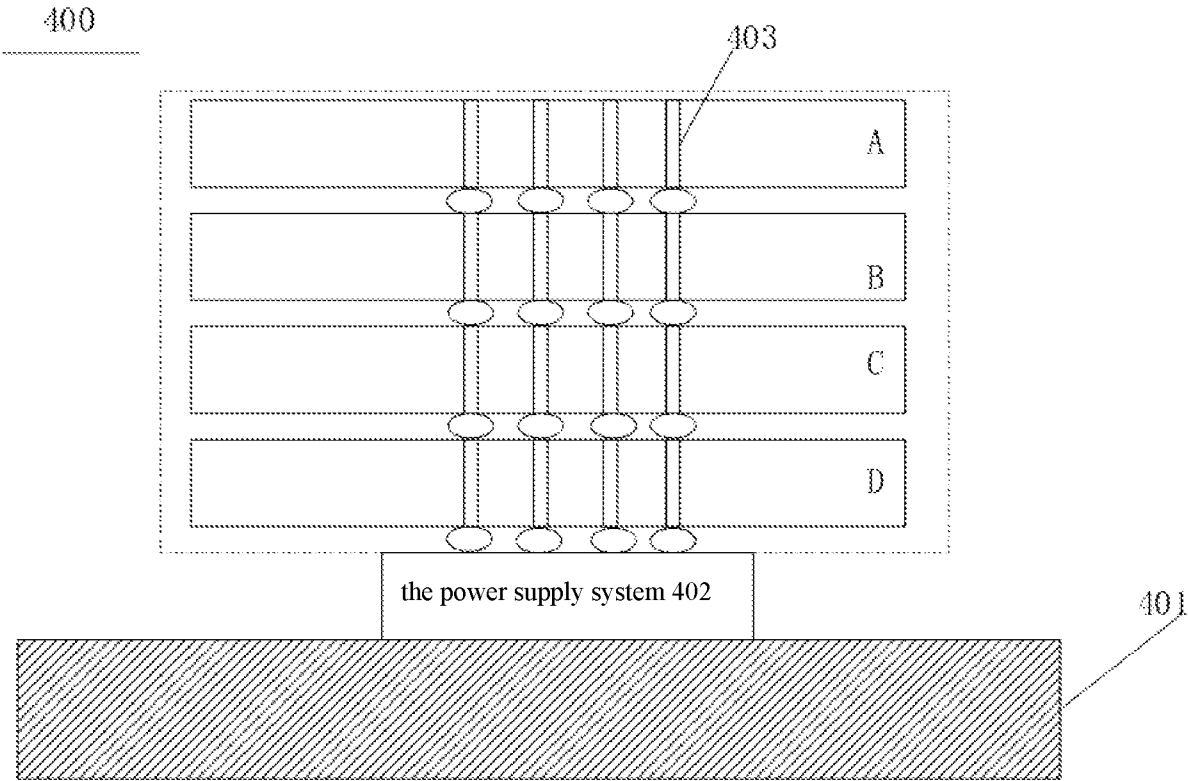


FIG. 4

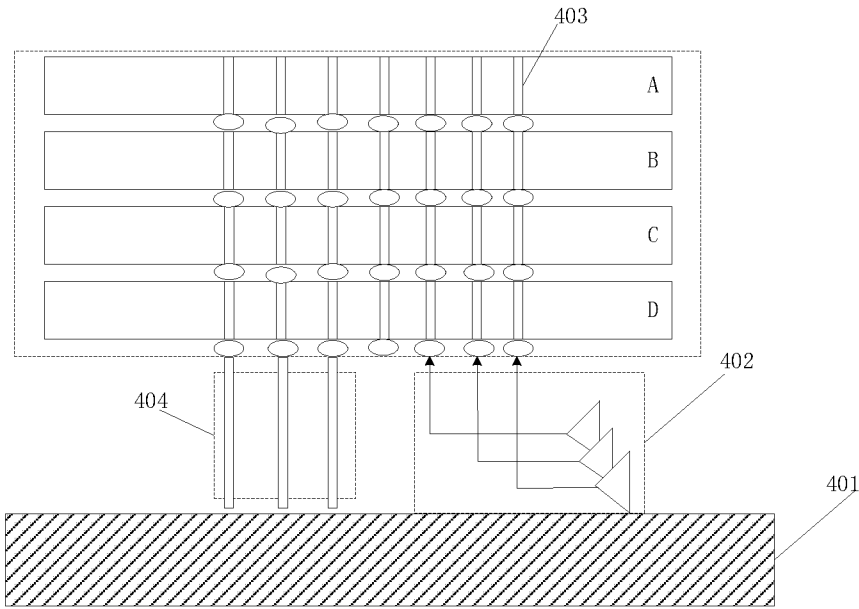


FIG. 5

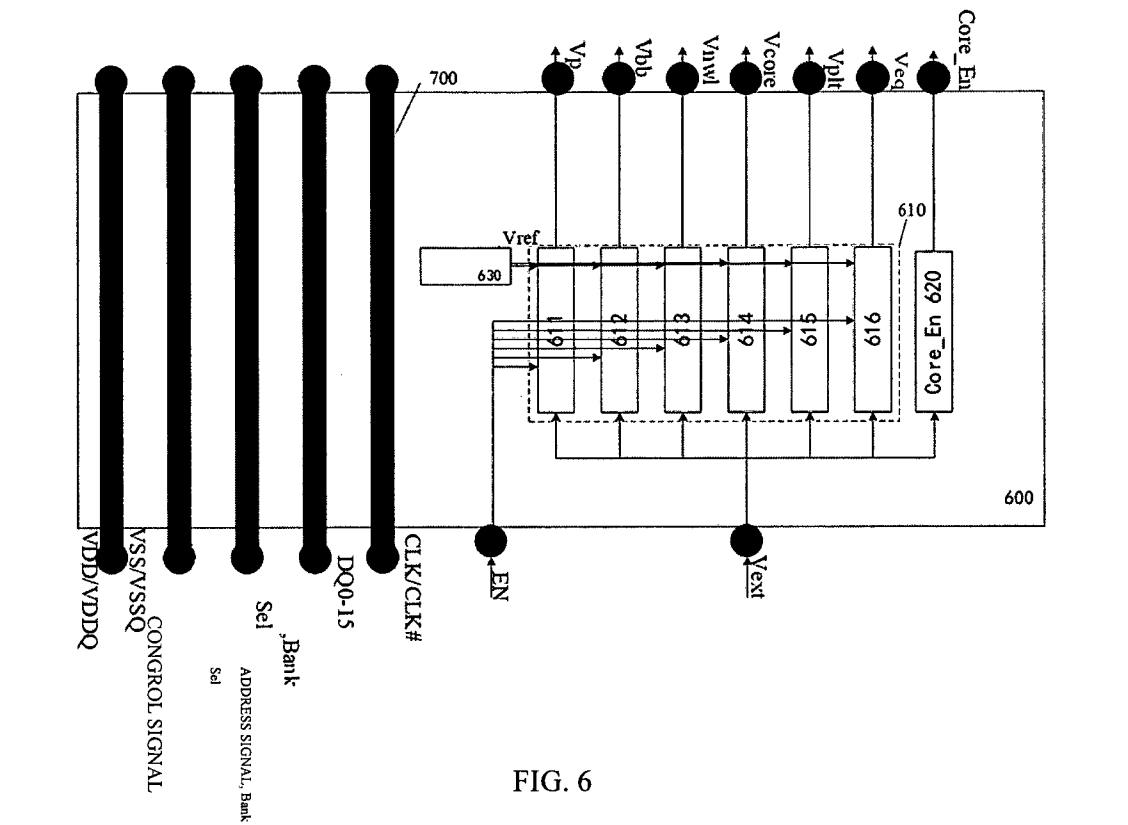


FIG. 6

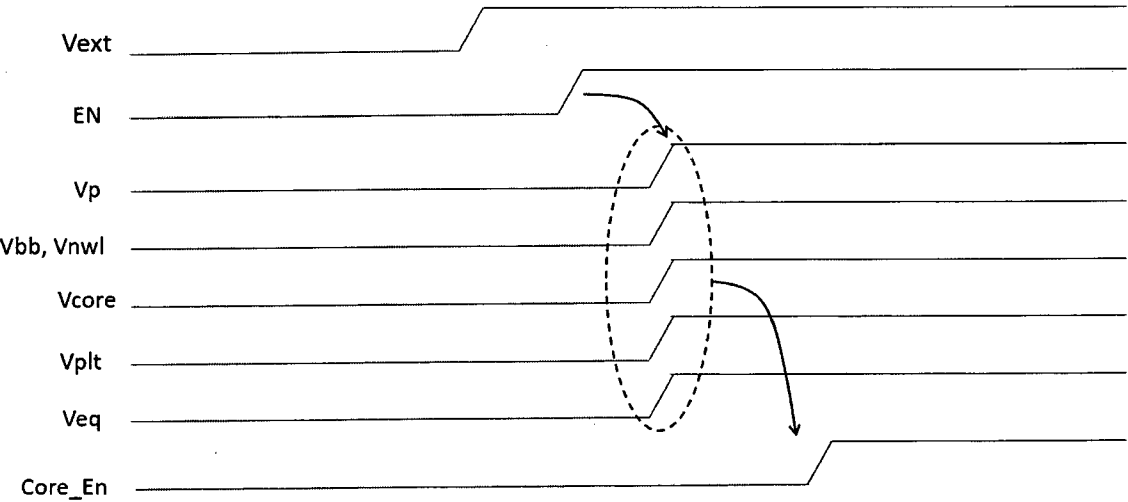


FIG. 7

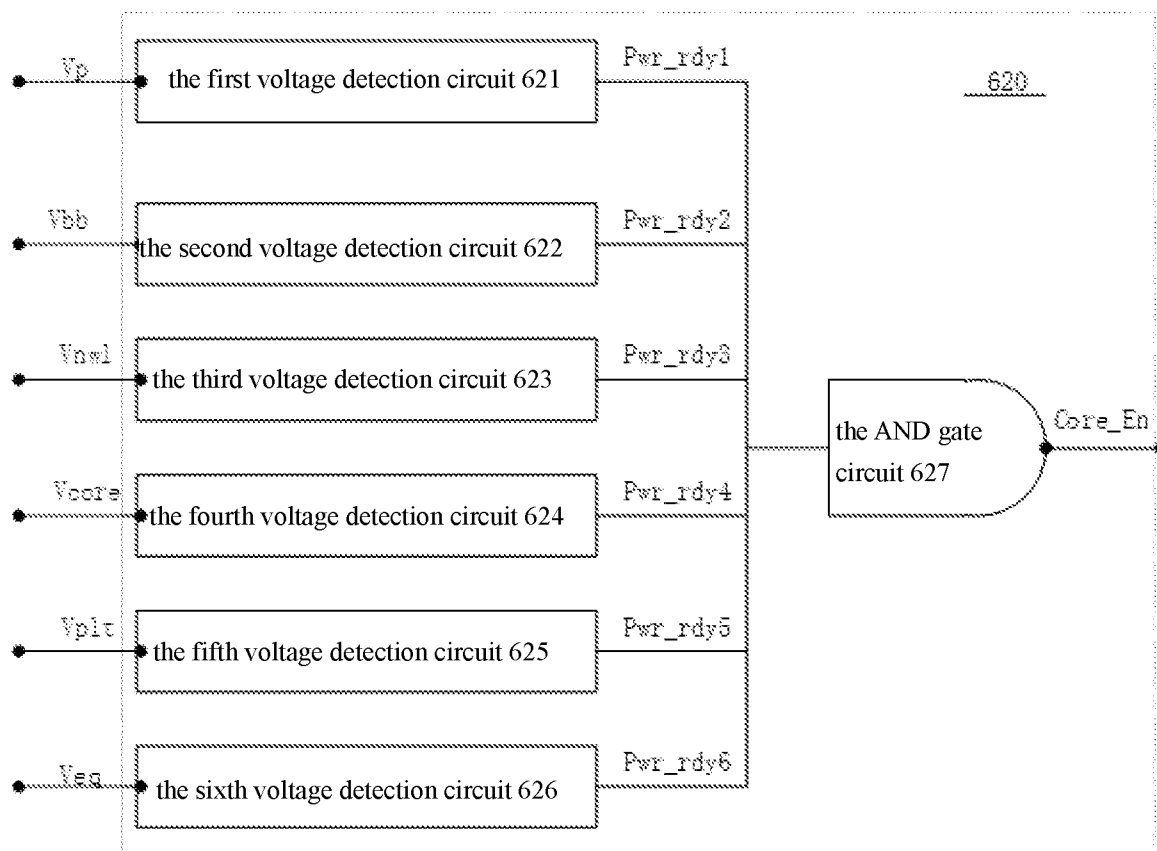


FIG. 8

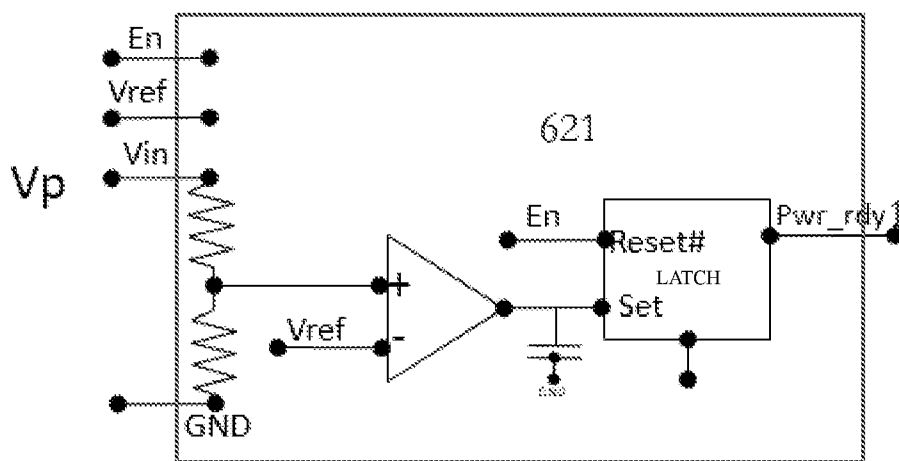


FIG. 9

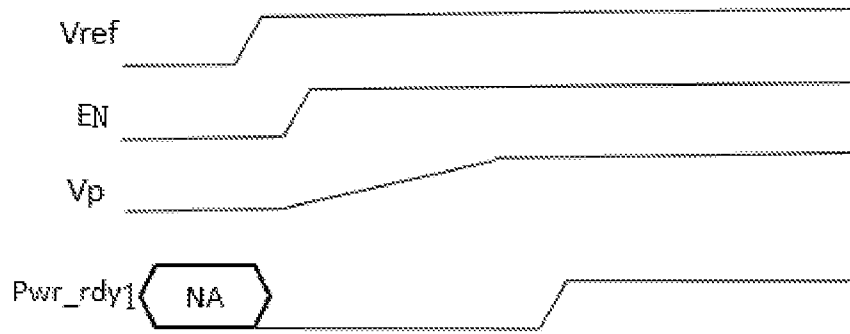


FIG. 10

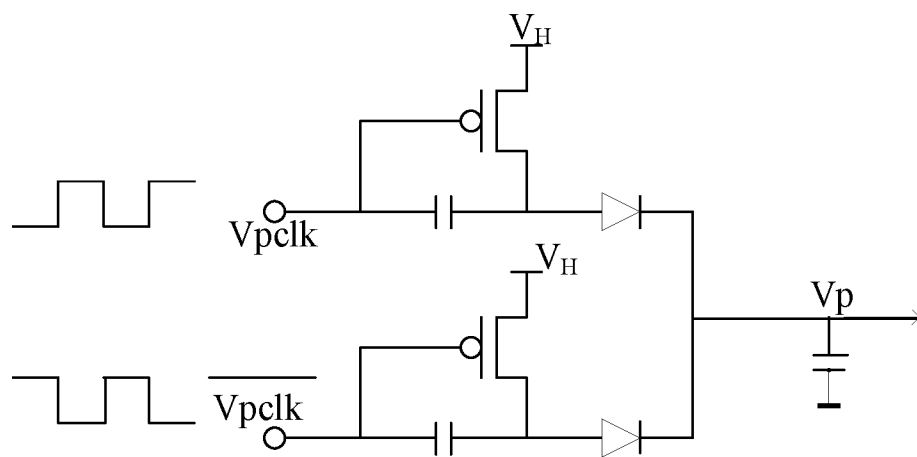


FIG. 11

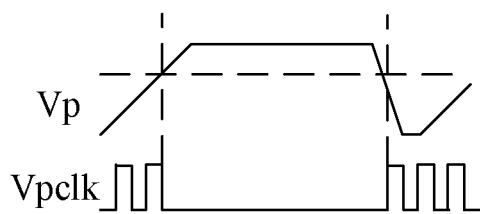


FIG. 12

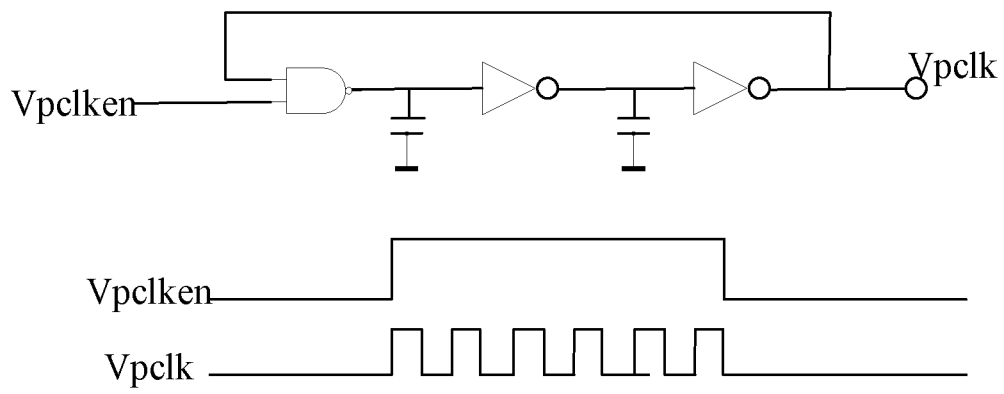


FIG. 13

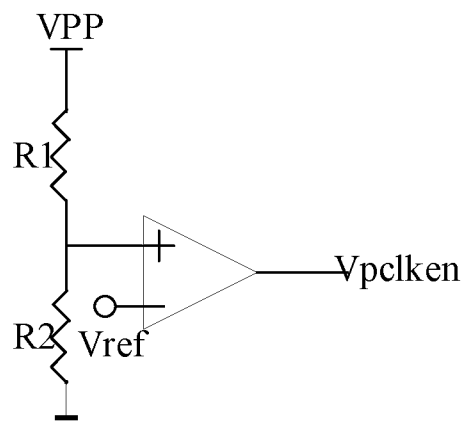


FIG. 14

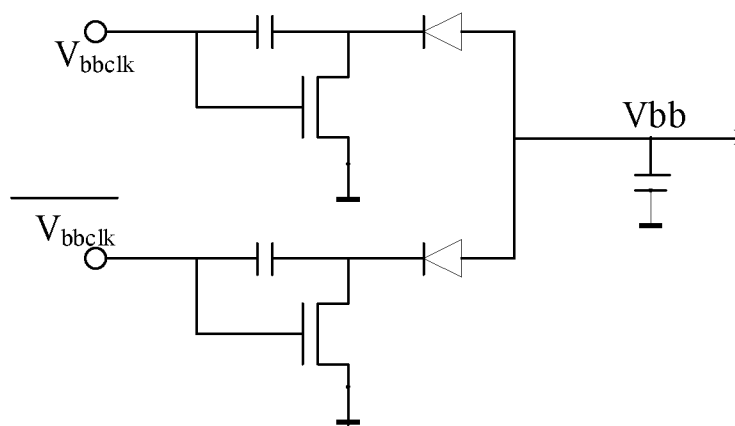


FIG. 15

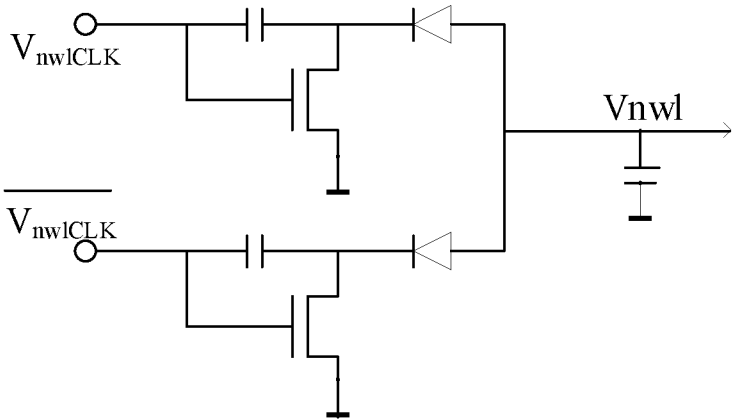


FIG. 16

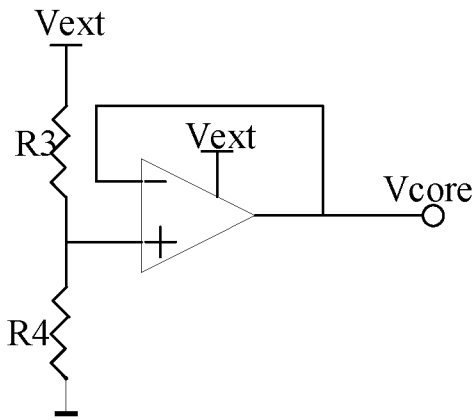


FIG. 17

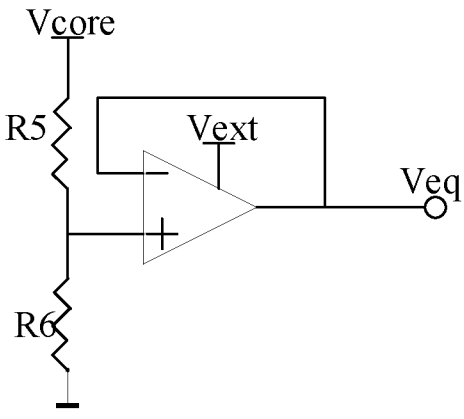


FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/108056

A. CLASSIFICATION OF SUBJECT MATTER

G11C 5/14(2006.01)i; G11C 11/4074(2006.01)i; H01L 25/18(2006.01)i; H01L 25/16(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C,H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI,EPODOC,CNPAT,IEEE,GOOGLE,CNKI:synchron+, storage, memory,voltage 1d generat+, power supply, enable circuit?, DRAM,TSV, interconnect, regulator

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 109147834 A (CHANGXIN STORAGE TECHNOLOGY CO., LTD.) 04 January 2019 (2019-01-04) description, paragraphs [0063]-[0113] and figures 4-18	1-20
PX	CN 109147835 A (CHANGXIN STORAGE TECHNOLOGY CO., LTD.) 04 January 2019 (2019-01-04) description, paragraphs [0059]-[0102] and figures 4-15	1-20
Y	US 2012250443 A1 (SARASWAT, Ruchir et al.) 04 October 2012 (2012-10-04) description, paragraphs [0011]-[0028] and figures 1-4	1-3, 8-20
Y	US 2008205183 A1 (SAMSUNG ELECTRONICS CO., LTD.) 28 August 2008 (2008-08-28) description, paragraphs [0014]-[0016], [0050] and figures 1-5	1-3, 8-20
A	US 9722597 B2 (SK HYNIX INC.) 01 August 2017 (2017-08-01) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

16 December 2019

Date of mailing of the international search report

08 January 2020

Name and mailing address of the ISA/CN

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100088
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LU,Ran

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961226

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/108056

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	109147834	A	04 January 2019	CN	208767022	U	19 April 2019
CN	109147835	A	04 January 2019	CN	208767023	U	19 April 2019
US	2012250443	A1	04 October 2012	WO	2012135772	A3	14 March 2013
				KR	20130133014	A	05 December 2013
				CN	103493137	B	16 March 2016
				CN	103493137	A	01 January 2014
				US	8547769	B2	01 October 2013
				KR	101566259	B1	05 November 2015
				CN	104900249	A	09 September 2015
				KR	20150006072	A	15 January 2015
				EP	2691957	A2	05 February 2014
				CN	104900249	B	15 December 2017
				EP	2691957	A4	24 June 2015
				KR	101592078	B1	18 February 2016
				WO	2012135772	A2	04 October 2012
US	2008205183	A1	28 August 2008	KR	100847315	B1	21 July 2008
				US	7649797	B2	19 January 2010
US	9722597	B2	01 August 2017	US	2017085261	A1	23 March 2017
				KR	20170034524	A	29 March 2017