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(54) Title: ADC NON-LINEARITY TESTING

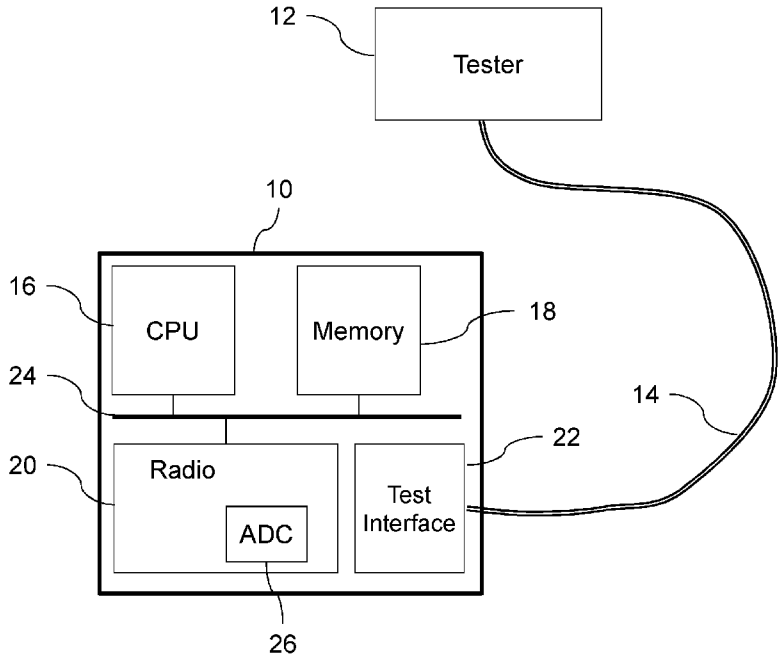

FIG. 1

(57) Abstract: An integrated circuit (10) comprises an analog-to-digital converter (ADC) (26), wherein: the ADC (26) is configured to receive a periodic analog test signal and to convert the periodic analog test signal into a sequence of digital codes during a test period. The integrated circuit (10) is configured to generate and store, on the integrated circuit (10), count data representative of, for each of one or more codes, a respective count of how often the ADC (26) outputs the respective code during the test period. The integrated circuit (10) is configured to output the count data from the integrated circuit (10), or is configured to process the count data on the integrated circuit (10) to determine a measure of non-linearity of the ADC (26).

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ADC Non-Linearity Testing

BACKGROUND OF THE INVENTION

This invention relates to methods and apparatus for testing the non-linearity of an analog-to-digital converter on an integrated circuit.

Integrated circuits (ICs), such as systems-on-chip (SoC), often contain one or more analog-to-digital converters for sampling analog signals. For instance, an SoC containing a digital radio, such as a Bluetooth radio, will use an ADC to generate a digital representation of a down-mixed received analog radio-frequency (RF) signal.

An ideal ADC is perfectly linear, such that every code (i.e. each possible binary sample value) that the ADC can output corresponds to a respective analog voltage interval of exactly the same size. In practice, however, ADCs exhibit some degree of non-linearity, with non-uniform step sizes between successive codes. The degree of non-linearity can vary even between individual integrated circuits fabricated to the same design, potentially on the same wafer, due to subtle process variations. For example, a charge-redistribution successive approximation register (SAR) ADC relies on a bank of binary-weighted switched capacitors that are switched in succession to perform the conversion, and any slightly mismatch between the individual capacitors of the bank can introduce non-linearity. The amount of non-linearity that can be tolerated may depend on the intended application, but in general ADCs that exhibit non-linearity above a tolerable threshold level—at least in a critical part of the ADC range—may need to be rejected as defective.

An ADC non-linearity test may therefore be included as part of a test regime that an integrated circuit die or chip has to pass, during or after fabrication (i.e. during wafer testing or package testing), before the device is released. Such a test may involve attaching test apparatus (e.g. a wafer prober or tester) to each integrated circuit via test probes, and controlling the test apparatus to provide a varying analog test signal as input to the ADC of the integrated circuit, while collecting corresponding code samples output by the ADC over a test period. The tester can then perform a statistical analysis of the codes to determine one or more measures of non-linearity of the ADC,

such as its differential non-linearity (DNL) and integral non-linearity (INL) at each code. However, such testing can be time-consuming and may limit production throughput. It also requires expensive test equipment, with good linearity and low noise.

Embodiments of the present invention seek to provide an alternative approach for testing ADC non-linearity.

SUMMARY OF THE INVENTION

From a first aspect, the invention provides an integrated circuit comprising an analog-to-digital converter (ADC), wherein:

the ADC is configured to receive an analog test signal and to convert the analog test signal into a sequence of digital codes during a test period;

the integrated circuit is configured to generate and store, on the integrated circuit, count data representative of, for each of one or more codes, a respective count of how often the ADC outputs the respective code during the test period; and

the integrated circuit is configured to output the count data from the integrated circuit, or is configured to process the count data on the integrated circuit to determine a measure of non-linearity of the ADC.

From a second aspect, the invention provides a method for testing an integrated-circuit analog-to-digital converter (ADC), the method comprising:

inputting an analog test signal to an ADC of an integrated circuit;

the integrated circuit generating and storing count data representative of, for each of one or more codes, a respective count of how often the ADC outputs the respective code during a test period; and

outputting the count data from the integrated circuit or processing the count data to determine a measure of non-linearity of the ADC.

Thus it will be seen that, in accordance with embodiments of the invention, count statistics for the ADC are collected by the integrated circuit itself. This can remove or reduce the dependence on external test equipment to receive ADC output codes for analysis, thereby making it quicker and/or easier to test ADCs since the volume of data that needs to be exported off the integrated circuit (IC) from the ADC can be reduced.

The analog test signal preferably has a known probability density function. It may be a non-repeating signal, such as a ramp signal (e.g. a linear slope), which may sweep across some or all of the ADC codes (e.g. relatively slowly). However, in a preferred set of embodiments, the analog test signal may be a periodic signal, such as saw-tooth or sine wave signal. In some preferred embodiments, it comprises a continuous-wave signal (i.e. a sine wave). The frequency of the analog test signal may be constant over the test period (e.g. being around 200 kHz).

The IC may, in some embodiments, receive the analog test signal directly from outside the IC (i.e. as a signal that has the same frequency spectrum as the analog test signal that is input to the ADC). In other embodiments, the IC may generate the analog test signal directly using an oscillator on the IC (i.e. such that the analog test signal has the same fundamental frequency as the oscillator).

However, in a preferred set of embodiments, the IC comprises a mixer and is configured to use the mixer (optionally in combination with one or more filters and/or gain stages, such as an anti-alias filter located between the mixer and the ADC) for generating the analog test signal. An input signal, e.g. a periodic square-wave or sinusoidal signal, having a component at an input frequency (e.g. having a fundamental frequency or a harmonic frequency of ~2.4 GHz), may be down-mixed by the IC to generate the analog test signal, which may have a frequency (i.e. an intermediate frequency) (e.g. 200 kHz) that is lower than said input frequency. The IC may comprise a local oscillator for generating a mixing signal for mixing with the input signal. The mixing signal may have a frequency that is offset from the input frequency by an intermediate frequency, which may determine the frequency of the analog test signal. The frequency of the mixing signal may be configurable (e.g. in software); this can enable a test signal to be generated at a user-selected frequency.

The input signal may be a radio-frequency (RF) signal. The IC may comprise radio receiver circuitry for receiving a radio-frequency (RF) signal. The mixer may be in the radio receiver. The IC may be configured to generate the analog test signal by down-mixing an RF test signal received at an antenna connection of the IC.

Deriving the test signal from an RF signal, on the IC, may have a number of advantages. For SoCs that already have a radio receiver, it enables an ADC test

signal to be generated without requiring significant additional circuitry. This can save design time and avoid expanding the area of the IC. This approach can also enable a wide range of test signal frequencies to be generated, providing significant flexibility. It can also enable a very clean (i.e. free from distortion) sinusoid to be generated.

The IC may comprise a test interface (e.g. one or more pads) for receiving and/or outputting analog signals and/or data with an external test apparatus (i.e. from apparatus that is not part of the IC).

The IC may be configured to output, to external test apparatus, the count data, or data representative of, or derived from, the measure of non-linearity of the ADC.

From a further aspect, the invention provides a system for testing an integrated-circuit analog-to-digital converter (ADC), the system comprising:

an integrated circuit; and

a test apparatus,

wherein:

the integrated circuit comprises an analog-to-digital converter (ADC);

the ADC is configured to receive an analog test signal and to convert the analog test signal into a sequence of digital codes during a test period;

the integrated circuit is configured to generate and store, on the integrated circuit, count data representative of, for each of one or more codes, a respective count of how often the ADC outputs the respective code during the test period; and

the integrated circuit is configured to output the count data from the integrated circuit, or is configured to process the count data on the integrated circuit to determine a measure of non-linearity of the ADC.

The test apparatus may be configured to receive the count data, or data representative of, or derived from, the measure of non-linearity of the ADC, from the IC.

In a first set of embodiments, the IC may be configured to receive an RF test signal (e.g. a signal having a fundamental or harmonic frequency at around 2.4 GHz), from outside the IC, at an antenna connection on the IC, during the test period, and to generate the analog test signal from the RF test signal. It may receive the RF test signal from the test apparatus.

In a second set of embodiments, the IC may comprise circuitry for generating an RF test signal (e.g. a signal having a frequency component at around 2.4 GHz) on the IC. In some embodiments, the RF test signal is a square-wave signal (e.g. a 32 MHz signal), comprising a harmonic at a desired RF frequency (e.g. at 2,432 MHz). The IC may comprise a filter for passing the harmonic, or a down-mixed signal generated from the harmonic, while attenuating other frequencies. The IC may be configured to provide the RF test signal to an antenna connection of a radio receiver of the IC, during the test period, and to generate the analog test signal from the RF test signal. In this way, it may advantageously be possible for the IC to generate count data without relying on external test apparatus to provide an input signal for the ADC, which may simplify or speed up the testing. It may allow more ICs to be tested in parallel than might be the case if an external test signal has to be provided.

The analog test signal may swing over a full-scale range of the ADC, but in preferred embodiments, during the test period, the test signal swings over (i.e. only over) a fraction of the full-scale range—e.g. over at most 50% or 30% or 10% of the full-scale range, such as a percentage between 5% and 30% (e.g. an interval corresponding to around 200 codes out of 2048 possible codes). (The swing may be determined by the difference between the highest and lowest levels in the test signal over the test period, and may represent a single sweep in the case of a non-repeating test signal, or multiple oscillations in the case of a periodic test signal.)

The analog test signal is preferably centred about the middle of the full-scale range (i.e. around mid-code), over the test period. A small-range, mid-scale test signal can be desirable in some embodiments as it can result in a higher proportion of counts near the mid-count of the ADC, which can provide statistically-significant count data quicker in situations where non-linearity around mid-scale is of particular interest. Also, a lower swing may result in a sinusoidal analog test signal that is less susceptible to distortion in embodiments in which the analog test signal is generated from an RF test signal by a radio receiver of the IC, as there may be less non-linearity in the radio receiver than if a higher-swing signal were being generated, resulting a more linear test signal.

The test period may have any duration, but in some embodiments it has a duration between 0.1 and 1 milliseconds, e.g. around 256 microseconds. The ADC may output any number of samples (i.e. individual codes) during the test period, but in some embodiments, it outputs between 100 and 100,000 samples, such as between 1,000 and 10,000 codes, e.g. 2048 or 8192 codes.

In some embodiments, the IC may generate and store count data for only a single code, which may be a mid-code of the ADC. The measure of non-linearity of the ADC may be determined from this mid-code count; in some embodiments it could equal the mid-code count, while in other embodiments it may be generated by an algorithm that comprises a step of dividing the mid-code count by an expected value. The algorithm may comprise one or more further steps, such as subtracting one from the result of the division. The expected value may be a predetermined constant value (e.g. if the swing of the test signal is well characterised). However, in a preferred set of embodiments, the IC is configured to calculate the expected value, e.g. from count data for each of a plurality of codes; this can allow the IC to adapt to the swing of the particular test signal.

In other embodiments, the IC may generate and store count data for each of a plurality of codes. The IC may generate count data for every code of the ADC, or only for every code within the swing of the analog test signal. However, in some embodiments, count data may be generated only for a subset of codes, which are preferably within the swing of the analog test signal over the test period. The subset may be centred around mid-code of the ADC. The subset may contain at most 50% or 20% or 10% of the codes within the swing of the analog test signal (e.g. between 5% and 20%), or at most 10% or 5% of all the codes of the ADC (e.g. between 2% and 5% of the total codes). For example, the total number of codes that the ADC can output may be 2048, with a test-signal swing of +/-100 codes around mid-code, and counts determined for the codes positioned -25 to +25 around mid-code. This can reduce processing load and/or storage requirements on the IC, if only these codes, or a further subset, are required for analysis. In some embodiments, only an analysis set of codes are analysed, which could be all the codes for which count data are determined, or a subset of these codes, which may contain only codes within an interval of at most 50% or 20% or 10% of the swing of the analog test signal (e.g. between 5% and 20%), or at most 10% or 5% of the total codes (e.g. between 2% and 5% of the total codes). Not

analysing every code may advantageously allow for simpler processing to be used to determine a measure of non-linearity of the ADC.

The ADC may comprise circuitry for sampling the analog test signal and for converting (i.e. quantizing) the analog test signal to a sequence of digital codes. The ADC may be any type of ADC, but in a preferred set of embodiments, the ADC is a successive-approximation-register (SAR) ADC. It preferably comprises one or more sets of capacitors—e.g. comprising a capacitor digital-to-analog converter (CDAC). Such ADCs are well suited to being analysed based only on one or more count values obtained around the mid-code of the ADC, as may be done in some embodiments disclosed herein. They can thus be particularly efficiently tested by some of the method disclosed herein.

The IC may comprise a memory (e.g. RAM or one or more registers) for storing the count data. The count data may be encoded in any appropriate way. The count data may represent a histogram of count values (also referred to herein as code hits).

In embodiments in which the count data is output from the IC to test apparatus, the test apparatus is preferably configured to process the count data to determine a measure of non-linearity of the ADC.

The measure of non-linearity of the ADC may comprise a differential non-linearity (DNL) value and/or an integral non-linearity (INL) value for one or more codes. This can provide useful statistical information about the matching for a capacitor array of the ADC. It may comprise a DNL value for mid-code and/or an INL value for mid-code.

The measure of non-linearity may be determined (by the IC or by test apparatus) from the count data for the plurality of codes. It may be calculated using an algorithm that assumes the expected number of counts for each code in an analysis set of codes will have the same value—i.e. which assume linearity of a histogram of count values over the analysis set—although this is not essential. A measure of non-linearity (e.g. DNL) for one or more codes in the analysis set of codes may be determined by an algorithm that comprises a step of dividing a count for the respective code by an expected value. The algorithm may comprise one or more further steps. The algorithm may further comprise subtracting one from the result of the division. The expected value may be a

predetermined constant value (e.g. if the swing of the test signal is well characterised). However, in a preferred set of embodiments, the IC is configured to calculate the expected value, e.g. from the count data; this can allow the IC to adapt to the swing of the particular test signal. The expected value may be calculated as the total number of counts across an analysis set of codes divided by the number of codes in the analysis set of codes.

However, in other embodiments, determining the measure of non-linearity (by the IC or by test apparatus) may comprise a step of linearizing the count data.

The integrated circuit may be on a die (e.g. on an uncut wafer, which may further comprise a plurality of other identical integrated circuits) or it may be in a chip (e.g. after packaging). It may be on a semiconductor substrate. It may be a system-on-chip. It may comprise a processor and memory. The memory may store software (e.g. firmware) comprising instructions for execution by the processor. The software may instruct the processor for performing one or more of the operations disclosed herein, such as storing the count data and/or processing the count data to determine the measure of non-linearity of the ADC.

The test apparatus may comprise a comprise a processor and memory. The memory may store software comprising instructions for execution by the processor. The software may instruct the processor for performing one or more of the operations disclosed herein, such as processing the count data to determine the measure of non-linearity of the ADC.

In some embodiments, the test apparatus may be configured to receive respective count data, or respective data representative of, or derived from, the count data, from each of a plurality of integrated circuits (e.g. a number of dies each implementing the same IC design). It may process the received data to determine a statistical measure of capacitor mismatch across the ADCs of the ICs.

Features of any aspect or embodiment described herein may, wherever appropriate, be applied to any other aspect or embodiment described herein. Where reference is made to different embodiments or sets of embodiments, it should be understood that these are not necessarily distinct but may overlap.

BRIEF DESCRIPTION OF THE DRAWINGS

Certain preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a test set-up for testing an IC chip embodying the invention;

Figure 2 is a schematic diagram of parts of the IC chip involved in methods of testing an ADC, embodying the invention;

Figure 3 is a graph of hits per code from a simulation of an ADC exhibiting no capacitor mismatch;

Figure 4 is a graph of hits per code from a simulation of an ADC exhibiting capacitor mismatch; and

Figure 5 is a close-up of the midscale of the graph of Figure 4.

DETAILED DESCRIPTION

Figure 1 shows an IC chip 10 being tested using an off-chip tester 12. The tester 12 is coupled to the chip 10 by test probes 14. Such testing may be performed at any time, but may be done as part of a fabrication process, e.g. while the chip 10 is still on a wafer, to determine whether the chip 10 passes quality control, or if it should be rejected and ultimately destroyed.

The chip 10 is a system-on-chip device comprising a system processor (CPU) 16, memory 18, a digital radio peripheral 20, and a test interface 22. Components are communicatively coupled by a bus system 24. The memory 18 may include volatile memory (e.g. RAM) and/or non-volatile memory (e.g. flash memory), and may be used to store data and software for execution by the processor 16. The test interface 22 may comprise a number of pads, located at various points across the chip 10 surface, to which a probe card of the tester 12 can be electrically coupled during wafer testing. The chip 10 may include other modules, not shown here, such as timers, cryptographic accelerators, input/output interfaces, general-purpose ADC and digital-to-analog (DAC) peripherals, further processors, power control logic, clock logic, etc. It may comprise pins or pads for temporary or permanent connection to other off-chip electronics, such as crystal oscillators, radio antennae, capacitors, resistors, other IC chips, etc.

The radio 20 includes digital and analog circuitry for receiving and transmitting radio-frequency signals. It may include an on-chip antenna and/or interface circuitry for connection to one or more off-chip antennae. It may support one or more standardised radio protocols, such as Bluetooth, Bluetooth Low Energy, ZigBee, LTE, WiFi, etc. The radio 20 may contain a local processor on the radio peripheral 20, or it may be controlled by software executing on the system processor 16.

Of particular relevance here, the radio peripheral 20 comprises a successive-approximation-register (SAR) ADC 26 for sampling received RF signals. The ADC 26 includes a capacitor digital-to-analog converter (CDAC), comprising a set of switched capacitors that are designed to have specific capacitances. Any mismatch between their capacitances can result in non-linear behaviour of the ADC 26.

Non-linearity of the ADC 26 can impair the performance of the radio 20, due to errors being introduced into the digital representations of received RF signals. If the non-linearity is excessive, the radio 20 may fail to meet minimum sensitivity standards and need to be rejected. Non-linearity around the midscale of the ADC 26 can be particularly problematic, since, in typical usage, this can be where a large proportion of the energy of analog signals sampled by the ADC 26 is concentrated, especially for small input signals.

Figure 2 shows some of the receive-path circuitry of the radio peripheral 20 in more detail. For simplicity, a single-ended implementation is shown, but some embodiments may use differential signals.

An antenna connection 30 of the radio 20 is arranged to receive radio-frequency signal from an antenna (not shown). The antenna may be integrated on the chip 10 or it may be located off-chip.

For testing purposes, the radio 20 in some embodiments comprises an on-chip signal generator 28, which is also switchably connectable to the antenna connection 30, as explained in more detail below.

When receiving a radio signal, signals received at the antenna connection 30 enter a low-noise amplifier (LNA) 32 which amplifies them and passes them to a passive mixer

34. The mixer 34 mixes the incoming RF signal with a local-oscillator (LO) signal generated by an all-digital phase-locked loop (ADPLL) 36. (In this example, the passive mixer 34 is configured to receive a square mixing signal which controls switches within the mixer; however, in alternative implementations, the mixer might be configured to receive a differently shaped mixing signal.) The LO frequency can be tuned to mix a desired radio channel (e.g. located in the 2.4 GHz band) to a non-zero intermediate frequency (IF). The down-mixed analog signal passes through IF gain circuitry 38, for further amplification, and through an anti-alias filter (AAF) 40, before entering the SAR ADC 26. The ADC 26 outputs digital samples that represent a tuned RF signal. These are output as a succession of multi-bit code words at a sampling rate—e.g. a succession of 12-bit words, having a mid-code value of 12'b1000 0000 0000. The voltage swing is monitored by automatic-gain-control circuitry (AGC) 42 at various points in the receive chain, and the AGC 42 controls the gain of the LNA 32 and the gain of the IF gain stage 38 led to provide a desired voltage swing to the ADC 26.

If the mixer 34 is a quadrature mixer, the radio 20 may contain two SAR ADCs 26, one for sampling an in-phase signal and another for sampling a quadrature signal. The mixer 34 may generate differential signals in some embodiments.

For testing the non-linearity of the radio ADC 26 to determine if its performance is acceptable, it may be sufficient to estimate small-signal non-linearity around the mid-code of the ADC 26, from a relatively small number of samples, rather than testing the ADC with a high-linearity large-scale input signal and a large sample size. In some embodiments, the chip 10 co-operates with external test apparatus 12 to perform this testing, while in other embodiments the analysis may be carried out entirely on the chip 10.

The test apparatus 12 may comprise a processor and memory storing software for execution by the processor. It may comprise an analog signal generator.

During testing, a continuous-wave analog RF test signal, of constant envelope, is provided to the antenna connection 30 and is passed through the radio receive chain from the antenna connection 30 to the ADC 26.

The RF test signal may be generated by an off-chip tester 12, but in some preferred embodiments it is generated by a continuous-wave signal generator 28 located on the chip 10 itself. The signal generator 28 may be implemented in any appropriate way—in some embodiments, the signal generator 28 comprises an on-chip oscillator or a PLL. The signal generator 28 may generate the RF test signal from a lower-frequency reference signal that the chip 10 receives over the test interface 22, e.g. from an off-chip crystal oscillator (e.g. a 32 MHz crystal). In some embodiments, the signal generator 28 receives or generates a square wave at a desired frequency (e.g. 32 MHz), which may be passed through one or more analog filters that pass only a single RF sine wave component of the square wave (e.g. a 2,432 MHz harmonic).

The radio 20 is configured, during testing of the ADC 26, to control the ADPLL 36 to mix the RF test signal to a desired intermediate frequency—e.g. of around 200 kHz or 1 MHz—which forms the analog test signal that is received by the ADC 26, after passing through the anti-alias filter (AAF) 40. The radio 20 also controls the AGC 42 to provide a desired voltage swing to the ADC 26, which is preferably kept uniform over the test period.

The AGC 42 is preferably set to give a swing of a size that means only a region around the mid-code of the ADC 26 is used. It may be configured to keep the swing between a negative threshold and a positive threshold around mid-code. The swing may be around 10% of the full-scale range of the ADC 26, although it could be 20% or any other value. Low swing, around the mid-code, can be beneficial for two reasons. First, it makes estimations better. This is because, for the codes that are reached, it leads to more hits (i.e. higher count values) per code for a given number of samples, resulting in a more accurate statistical analysis. Second, by keeping the swing low, it is more likely that the receive chain of the radio 20 is sufficiently linear that the down-mixed test signal that is received as input by the ADC 26 is a relatively-clean sinusoid (except for noise, which can be averaged out). The filtering of the receive chain preferably removes high-frequency signals that might otherwise contaminate the measurements.

The on-chip procedure for testing the ADC 26 may be controlled by software executing on the system processor 16, or in some embodiments by software executing on a radio processor located within the radio peripheral 20. The software controls receives

the code samples that are output from the ADC 26 over a test period, in which the approximately sinusoidal analog test signal is received by the ADC 26, through the receive path of the radio 20. The test period may cover any number of samples. In one example, 8192 samples are collected, which corresponds to a test period of 256 microseconds when using a 32 MHz sampling clock. However, more or fewer samples could be collected. The whole test procedure may last a few milliseconds, after allowing time for the AGC 42 to settle and for calculation time, as well as for potentially repeating the whole measurement and calculation process a plurality of times and averaging the results.

For each of a set of test codes, the software initialises a counter (e.g. in RAM 18) for each code at the start of the test period, and then increments the counter each time the respective code is output by the ADC 26 during the test period. At the end of the test period, the count values provide count data that can be analysed statistically to determine the non-linearity of the ADC 26, at one or more points in its range. This analysis may be carried out at least partly by the on-chip software, but some embodiments may instead output the count data from the chip 10, through the test interface 22, for the tester 12 to analyse.

It will be appreciated that, even if the count data is exported for off-chip processing, this is still less burdensome on the tester 12 compared with a chip for which the tester must receive raw output of the ADC 26, in real-time, over the test period. It can therefore allow for more efficient testing of dies or chips—e.g. by freeing up bandwidth on the test probes 14 so that other parts of the chip 10 can be tested in parallel, or by reducing processing load on the tester 12.

The set of codes for which count values are generated could include every code (e.g. from 12'b0000 0000 0000 to 12'b1111 1111 1111, for a 12-bit ADC), but it may only contain a subset of the codes. In some embodiments, a count value may be determined only for the one mid-code point (e.g. 12'b1000 0000 0000), since this may, in some situations, be sufficient to decide whether to pass or fail an ADC 26 with acceptably low false-pass and false-fail rates. In other embodiments, count values may be determined for a subset of the count values, which may be centred on the mid-code. This set may be sufficiently wide as to cover the full swing of the analog test signal received by the ADC 26. However, it may be narrower than this, such that some

codes that are output during the test period are not counted. In some examples, for instance, it may be +/- 20 or 25 codes around mid-code, which may represent under 5%, 10% or 20% of the full range of the ADC 26. The set of codes may span an interval in single-code steps, although it could contain gaps.

If the count data is analysed on the chip 10, the software may determine a differential non-linearity (DNL) value and/or an integral non-linearity (INL) value for one or more codes. It may determine a maximum DNL or INL value over an analysis set of codes (which may be all or only a subset of the set of codes for which count values were obtained). It may process the count values to evaluate a measure of capacitor mismatch in the capacitor array of the CDAC of the SAR ADC 26, e.g. as explained in more detail below.

If only codes in an analysis interval around mid-code are considered, where the analysis interval is significantly less than the full range of the ADC 26, then the calculation of DNL and INL may be able to assume that the histogram of count values over the analysis interval is linear, without significantly impacting the results, thereby simplifying the calculation. The on-chip software (or the tester 12) may thus evaluate DNL for a code by dividing the count value for the code by an expected number of hits for that code, over the time period, given the test signal that was provided to the ADC 26. It may subtract one from this result to get a DNL value—i.e. according to the equation:

$$DNL(code) = \frac{hits(code)}{\mathbb{E}(hits(code))} - 1$$

where $\mathbb{E}$ is expected number of hits. Under a linearity assumption, the expected value may be calculated as the total number of hits over the analysis interval divided by the number of codes in the analysis interval—i.e. the mean number of hits per code.

The software may calculate INL for one or more codes, e.g. by calculating a cumulative sum of DNL values over the analysis interval. It may optionally repeat the whole sampling and calculation process one or more times, and average the resulting DNL and INL values, to improve accuracy.

The software may calculate DNL(mid-code) and provide this (and optionally other statistics such as one or more INL values) as output to the tester 12, or it may further process one or more DNL values, e.g. to determine whether the ADC 26 meets a pass criterion (e.g. if DNL(mid-code) is below a predetermined threshold). More generally, the on-chip software may, in some embodiments, process the count data to determine whether the ADC 26 meets a pass criterion. The chip 10 may then signal to the tester 12 whether the ADC 26 passes or fails.

The software may calculate INL for one or more codes, e.g. by calculating a cumulative sum of DNL values over the analysis interval.

Figure 3 is a simulated histogram of codes output from the ADC 26, over a test period, assuming the ADC 26 contains a theoretically perfect CDAC that exhibits no capacitor array mismatch. However, the simulation does include noise and non-linearity in the receive chain of the radio 20 upstream of the ADC 26. A total of 8,192 samples were used to compute the histogram. In the simulation, an RF test signal of approximately 2.4 GHz was provided at the antenna connection 30, with a power of -75 dBm. The AGC 42 was locked to a predetermined gain setting, and the ADPLL 36 was set so that the mixer 34 would output an intermediate frequency of approximately 200 kHz to the ADC 26.

The code range output from the ADC 26 in the simulation was approximately ±150 codes, with code 0 representing mid-code. This is determined by the input RF power and gain settings.

As shown in from Figure 3, the histogram has a classic “bathtub” shape, but is slightly contaminated by noise from the receive chain.

Figure 4 shows a similar simulation, but with a +2 least-significant-bit (LSB) mismatch for the most-significant-bit (MSB) capacitor in the CDAC capacitor array of the ADC 26. There is now a significant spike at code 0, due to the mismatch introduced.

Instead of the analysis software on the chip 10 or the tester 12 mathematically processing the count data so as to linearize such a histogram, it may be possible to

estimate one or more non-linearity parameters directly, with acceptable accuracy, by considering only those count values close to the mid-count.

This is shown in Figure 5, which presents the same histogram as Figure 4, but truncated (i.e. zoomed-in) around mid-code. The histogram around the mid-code is quite linear, due to the fact that the rate of the change in gradient of the sinusoidal test signal (i.e. the second derivative) around mid-code is close to zero, or equivalently because $\sin(x) \simeq x$ for small values of x. There may thus be no need to linearize this part in order to obtain valid statistics from such a truncated interval. This can reduce the computational effort required, so that the DNL error for a code can be approximated by the number of hits for that code, divided by the expected numbers of hits per code (i.e. average hits per code), minus one, as shown above.

As already noted, non-linearity around the mid-code may be the most significant, especially for an SAR ADC 26, because the theoretical non-linearity is greatest around mid-code, when all the LSB and MSB capacitors in the CDAC are switched. Analysing the non-linearity around the mid-code can therefore give meaningful statistics about the capacitor matching inside the ADC 26.

The chip 10 may only determine count values over such a truncated code interval, since, over this interval, the histogram is already sufficiently close to linear that it can be used for non-linearity estimation directly, without needing to linearize the count values. However, in other embodiments, software on the chip 10 may implement a linearization algorithm to linearize a set of count values.

The following exemplary pseudo-code provides further details into how software on the chip 10 (or on the tester 12, or split between the chip 10 and the tester 12) may calculate DNL, DNL at mid-code, and INL.

```
{
Let samples from ADC be denoted as 'samples'
        Compute minimum bin,  minbin = min(samples)
        Compute maximum bin,  maxbin = max(samples)
        Compute histogram, hist_samples = hist(samples, minbin:1:maxbin)
        Chose integer truncation length n
        Compute truncated histogram, hist_samples_trunc = hist_samples(-minbin-n:1:-minbin+n)
        Estimate DNL, DNL = hist_samples_trunc/mean(hist_samples_trunc) - 1
        Calculate DNL at mid-code, DNL_mid = hist_samples_trunc(n+2)/mean(hist_samples_trunc) - 1
        Calculate INL, INL = cumsum(DNL)
}
```

In this code, the histogram is computed and truncated. The truncation is done since the histogram can be assumed to close to linear around the mid-code, which simplifies the computation. The whole histogram could be used, but then it may be necessary to linearize it in order to obtain meaningful statistics, because the probability density function of a sinusoid test signal is 'bathtub'-shaped, as shown in Figure 3, and not flat. This has some extra computation cost, and so may be less appropriate for on-chip CPUs. In some embodiments, only the DNL error at the ADC mid-code is of interest in any case, because the theoretical worst-case CDAC capacitor mismatch should occur at mid-code, and so this is useful to give a pass/fail criterion for the ADC in a production test.

There follows some further details on how, in some embodiments, DNL error at ADC mid-code, obtained from a plurality of different chips containing SAR-ADCs (e.g. chips like the chip 10 above), may also be analysed, preferably off-chip, to determine a measure of mismatch in a capacitor array of a SAR-ADC, such as the ADC 26. The usefulness of this measure are also explained below.

A SAR (successive approximation register) ADC (analog-to-digital converter) uses a large capacitor array to perform a binary search to map the analog input to a digital output code. A SAR ADC with resolution of *N* bits might have a capacitor array or arrays (e.g. two arrays for differential implementation) each consisting of 2^{N-1} unit capacitors (although not always, as this depends on the design). The ADC is designed assuming that all these capacitors are equal. However, in practice, these capacitors

will have some mismatch between them, which is random, due to imperfections in the manufacturing process, which might lower the linearity of the ADC. This mismatch is commonly described by the ratio

$$\frac{\sigma(C_u)}{C_u}$$

where $\sigma(C_u)$ is the standard deviation of a unit capacitance C_u. This is a useful design parameter, as it says something about the mismatch of a unit capacitor. For example, if $\frac{\sigma(C_u)}{C_u} = \alpha$, for some real number α, then the unit capacitor has a standard deviation of $\sigma(C_u) = \alpha C_u$.

Larger capacitors can be made by summing unit capacitors. If we assume that the unit capacitors have uncorrelated mismatch, then a capacitor of size nC_u, for some integer n, will have standard deviation of $\sigma(nC_u) = \sqrt{n}\alpha C_u$.

Here we have assumed that the distribution is also Gaussian, so the standard deviation scales as $\sqrt{n}$ when summing n uncorrelated distributions. So, given a ratio $\frac{\sigma(C_u)}{C_u}$, it is possible to model the capacitor array, since any larger capacitor is just a sum of unit capacitors. Generally, the SAR ADC capacitor arrays are custom made, so no number exists for $\frac{\sigma(C_u)}{C_u}$. It may be possible to try to 'guesstimate' this ratio, but this is not based on hard facts, and is therefore prone to error.

It is possible to estimate $\frac{\sigma(C_u)}{C_u}$ based on non-linearity measurements, but this typically requires many chips to be tested in order get a good estimate. In addition, non-linearity measurements typically are time consuming to obtain and require expensive external equipment.

However, using the non-linearity estimation methods disclosed herein, it's possible to test small-scale non-linearity for a large quantity of chips, with minimal test time, and requiring little or no external test equipment. Statistics of ADC mid-code DNL, collected from many chips, similar to the chip 10 described above, may be analyzed to estimate $\frac{\sigma(C_u)}{C_u}$.

If the DNL at ADC mid-code is denoted DNL_mid, then

$$\frac{\sigma(C_u)}{C_u} = \beta\sigma(\mathrm{DNL\_mid})$$

where β is a real constant that depends on the ADC design (for example, on the switching method of the SAR ADC), and $\sigma(\mathrm{DNL\_mid})$ is the standard deviation of $\mathrm{DNL\_mid}$. The constant β can be estimated from simulations. In some example embodiments, $\beta \simeq 0.21$ (based on simulations).

In other words, the mismatch of a unit capacitor is proportional to the standard deviation of DNL_mid. This is consistent with a higher mismatch for C_u giving a greater spread of DNL_mid across chips.

This analysis may be performed by off-chip test apparatus, processing data collected from a plurality of chips that each embody the invention disclosed herein. It can thus be seen that determining only the DNL error at the ADC mid-code may be sufficient, in some instances, to estimate $\frac{\sigma(C_u)}{C_u}$. This can be useful, as it may allow the manufacturer of a chip to gain useful insights into the capacitor array of its ADC design in practice, which may be useful when modifying the ADC design or when applying the same capacitor array structure to other chip designs.

It will be appreciated by those skilled in the art that the invention has been illustrated by describing one or more specific embodiments thereof, but is not limited to these embodiments; many variations and modifications are possible, within the scope of the accompanying claims.

CLAIMS

1. An integrated circuit comprising an analog-to-digital converter (ADC), wherein:

the ADC is configured to receive a periodic analog test signal and to convert the periodic analog test signal into a sequence of digital codes during a test period;

the integrated circuit is configured to generate and store, on the integrated circuit, count data representative of, for each of one or more codes, a respective count of how often the ADC outputs the respective code during the test period; and

the integrated circuit is configured to output the count data from the integrated circuit, or is configured to process the count data on the integrated circuit to determine a measure of non-linearity of the ADC.

2. The integrated circuit of claim 1, wherein the periodic analog test signal comprises a continuous-wave signal, having a frequency that is constant over the test period.

3. The integrated circuit of claim 1 or 2, comprising a mixer and a local oscillator, wherein the integrated circuit is configured to use the local oscillator and the mixer to generate the periodic analog test signal from an input signal by mixing the input signal with a mixing signal generated by the local oscillator.

4. The integrated circuit of any preceding claim, comprising radio receiver circuitry for receiving a radio-frequency (RF) signal, wherein the integrated circuit is configured to generate the periodic analog test signal by down-mixing a radio-frequency test signal received at an antenna connection of the integrated circuit.

5. The integrated circuit of claim 4, configured to receive the radio-frequency test signal from outside the integrated circuit during the test period.

6. The integrated circuit of claim 4, comprising circuitry for generating the radio-frequency test signal on the integrated circuit during the test period.

7. The integrated circuit of claim 6, comprising circuitry for generating the radio-frequency test signal as a square-wave signal comprising a harmonic at a predetermined radio frequency, and comprising a filter for passing the harmonic, or a down-mixed signal generated from the harmonic, while attenuating other frequencies.

8. The integrated circuit of any preceding claim, wherein, during the test period, the periodic analog test signal swings over a fraction of a full-scale range of the ADC, centred about a mid-code of the ADC.

9. The integrated circuit of any preceding claim, wherein, during the test period, the periodic analog test signal swings over at most 30% of the full-scale range of the ADC.

10. The integrated circuit of any preceding claim, configured to generate and store count data for only a single code, being a mid-code of the ADC.

11. The integrated circuit of any of claims 1 to 9, configured to generate and store count data only for a subset of all codes of the ADC, being a plurality of codes that are within a swing of the periodic analog test signal over the test period.

12. The integrated circuit of claim 11, configured to generate and store count data only for at most 5% of all the codes of the ADC.

13. The integrated circuit of any preceding claim, wherein the ADC is a successive-approximation-register ADC comprising a capacitor digital-to-analog converter.

14. The integrated circuit of any preceding claim, wherein the measure of non-linearity of the ADC comprises at least a differential non-linearity (DNL) value for a mid-code of the ADC.

15. The integrated circuit of any preceding claim, wherein the integrated circuit is configured to determine the measure of non-linearity for each of one or more codes by an algorithm that comprises a step of dividing a count for the respective code by an expected value.

16. The integrated circuit of any preceding claim, wherein the integrated circuit is configured to calculate the expected value from the count data as the total number of counts across an analysis set of codes divided by the number of codes in the analysis set of codes.

17. The integrated circuit of any preceding claim, comprising a processor and a memory storing software comprising instructions, for execution by the processor, for processing the count data to determine the measure of non-linearity of the ADC.

18. The integrated circuit of any preceding claim, comprising a test interface for outputting the count data, or data representative of or derived from the measure of non-linearity of the ADC, to an external test apparatus.

19. A system for testing an integrated-circuit analog-to-digital converter (ADC), the system comprising:

the integrated circuit of any preceding claim; and

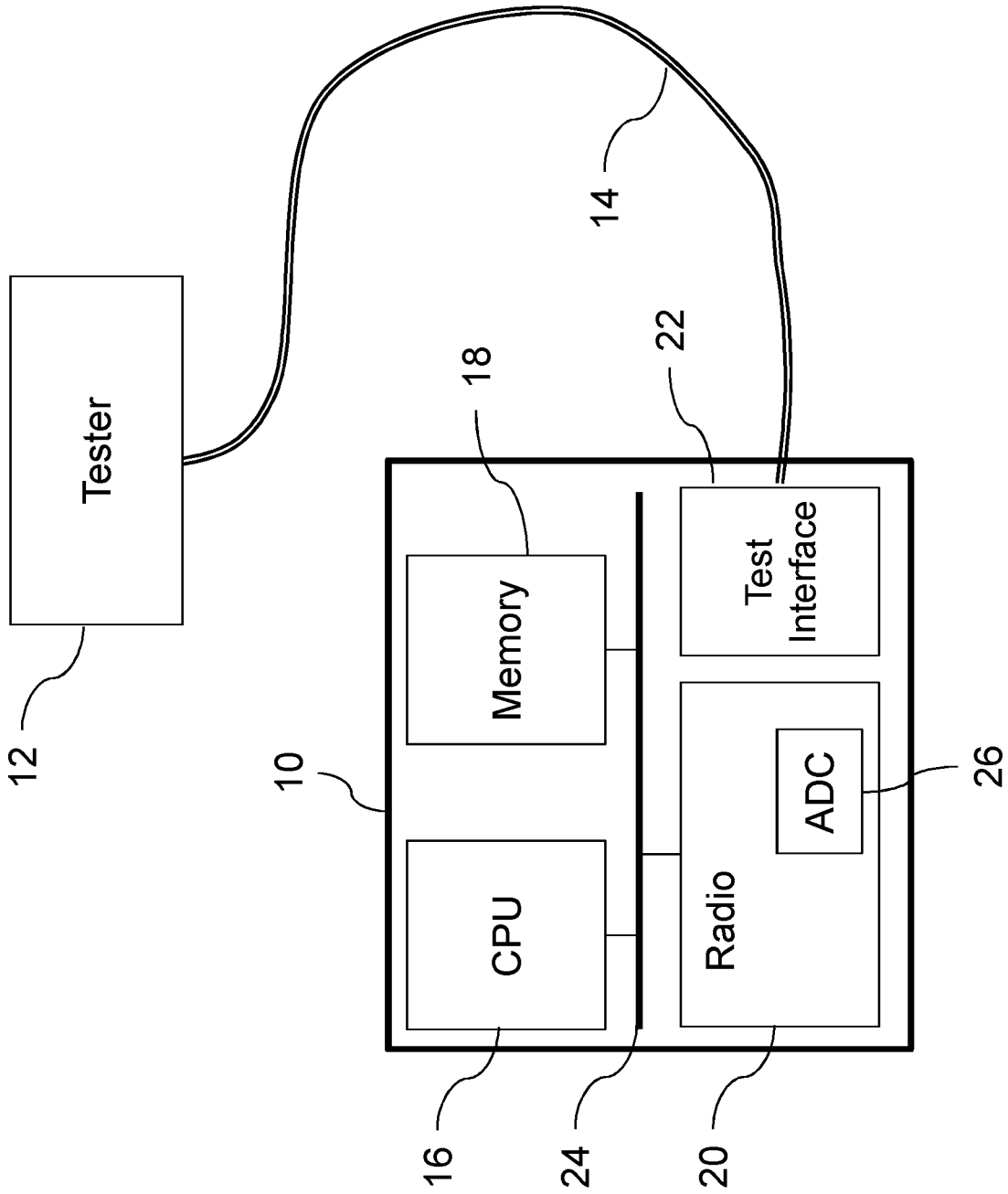
a test apparatus configured to receive the count data, or data representative of or derived from the measure of non-linearity of the ADC, from the integrated circuit.

20. A method for testing an integrated-circuit analog-to-digital converter (ADC), the method comprising:

inputting a periodic analog test signal to an ADC of an integrated circuit;

the integrated circuit generating and storing count data representative of, for each of one or more codes, a respective count of how often the ADC outputs the respective code during a test period; and

outputting the count data from the integrated circuit or processing the count data to determine a measure of non-linearity of the ADC.


Tester
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14
10
18
22
Memory
Test Interface
CPU
Radio
ADC
26
16
24
20

FIG. 1

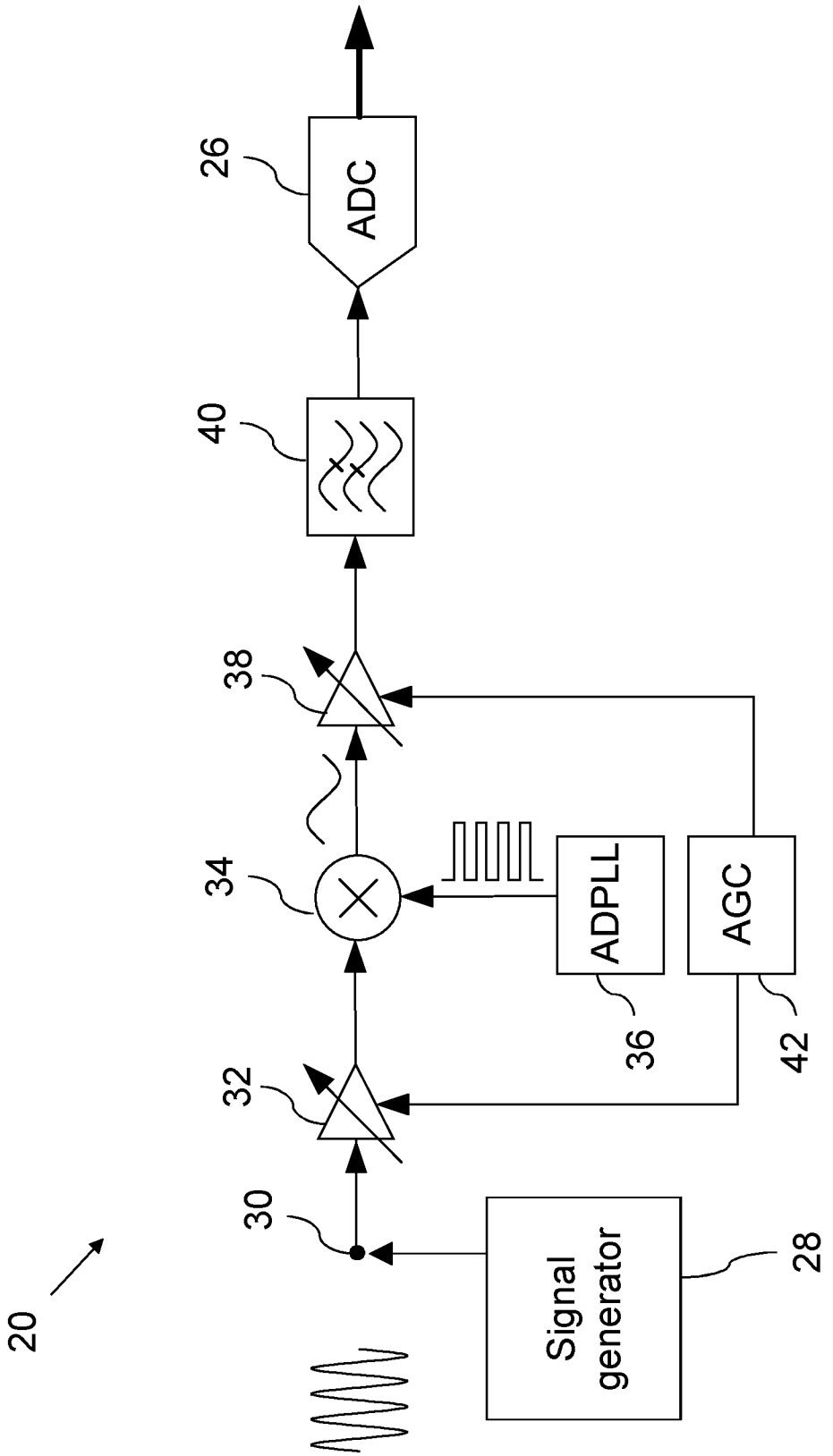
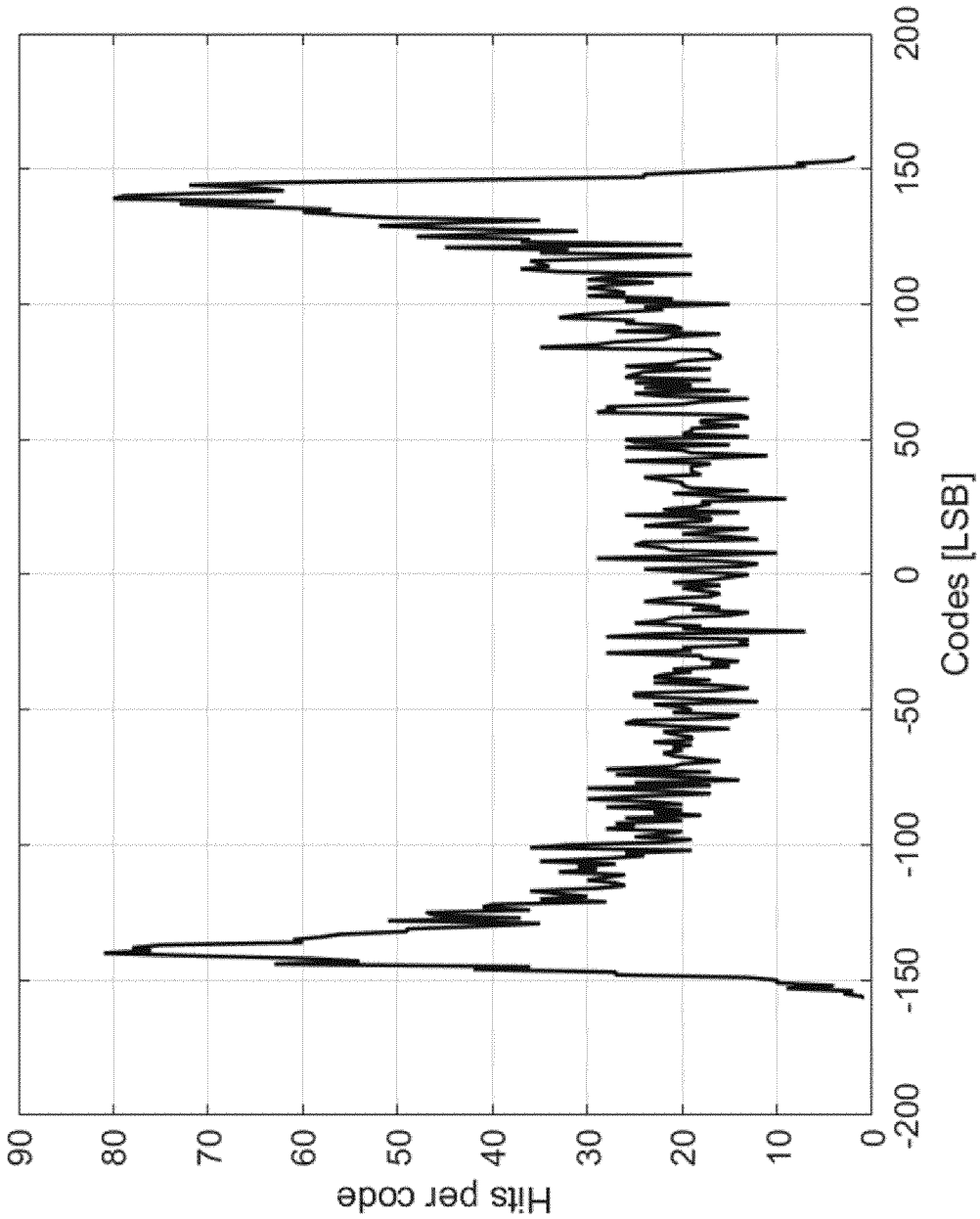


FIG. 2


Hits per code
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10
20
30
40
50
60
70
80
90
Codes [LSB]
-200
-150
-100
-50
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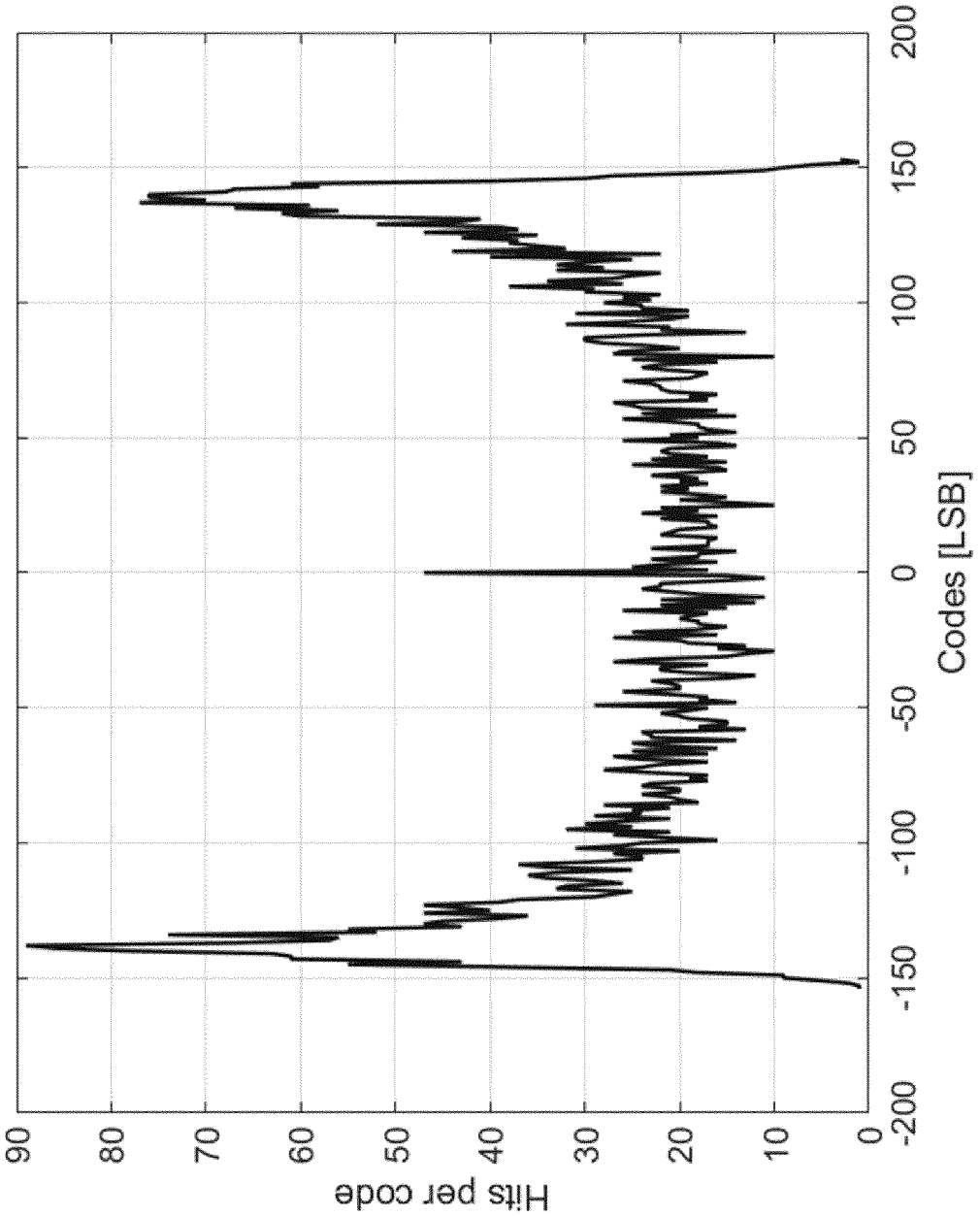
50
100
150
200

FIG. 3


Hits per code
0
10
20
30
40
50
60
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80
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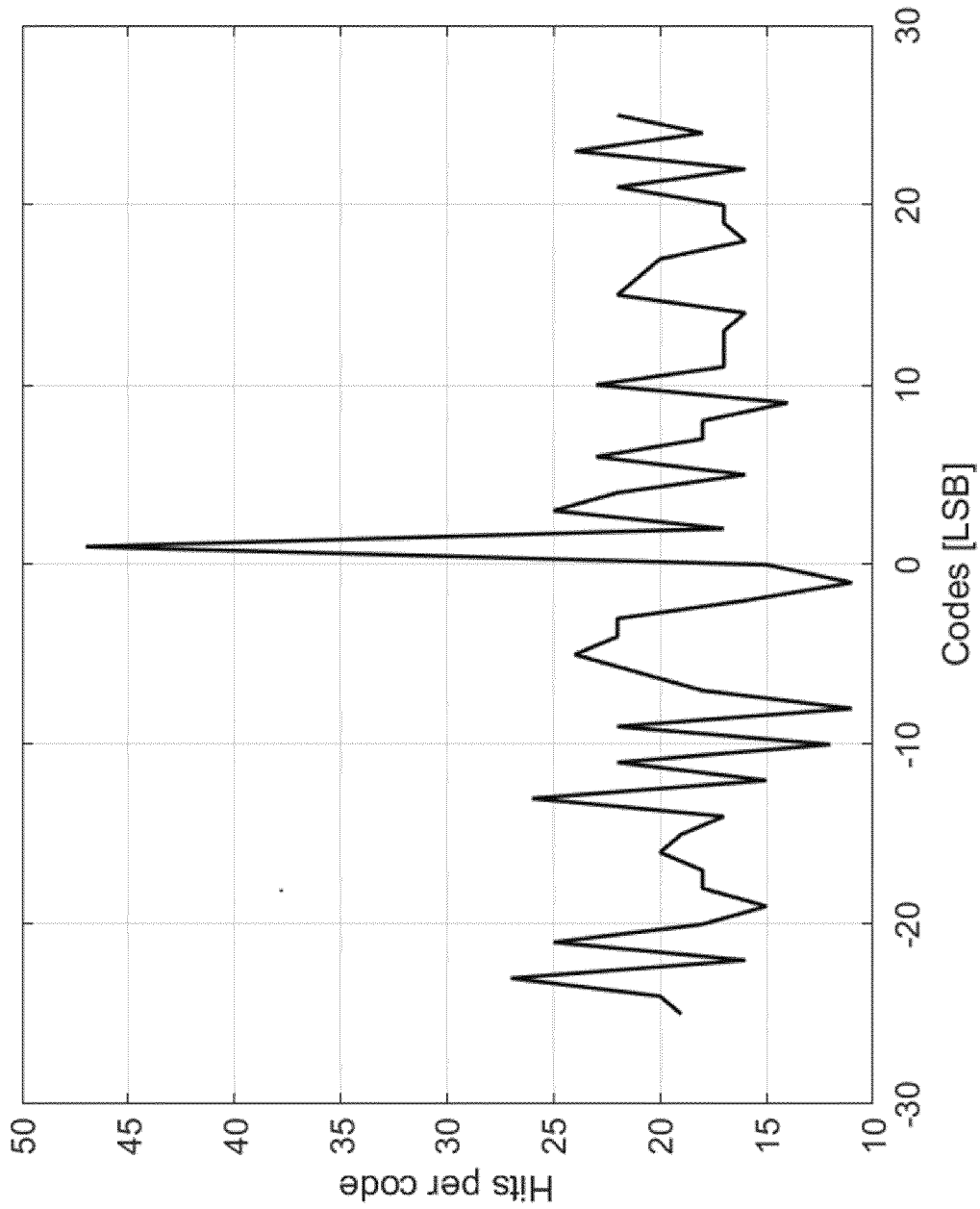
Codes [LSB]
-200
-150
-100
-50
0
50
100
150
200

FIG. 4


Hits per code
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45
40
35
30
25
20
15
10
-30
-20
-10
0
10
20
30
Codes [LSB]

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/069499

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/10 G01R31/316 H04B17/20 H03M1/46
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M G01R H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 793 642 A (FRISCH ARNOLD M [US] ET AL) 11 August 1998 (1998-08-11) column 2, lines 44-49 column 5, lines 6-16; figures 1,14,22 column 6, lines 16-26 column 6, lines 55-65 column 7, lines 55-65 claim 1	1-20
A	US 2014/092946 A1 (DHAYNI ACHRAF [FR] ET AL) 3 April 2014 (2014-04-03) paragraph [0079] - paragraph [0084]; figure 5	3
A	US 2014/162568 A1 (LASKAR JOY [US]) 12 June 2014 (2014-06-12) paragraphs [0002], [0005]; figure 1	3

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 November 2022	15/11/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Galardi, Leonardo

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/069499

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WO 2012/165940 A1 (MIMOS BERHAD [MY]; TAN KONG YEW [MY]) 6 December 2012 (2012-12-06) page 8, lines 11-17 figure 2 -----	9-12

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2022/069499

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		WO 2014089517 A1	12-06-2014
		WO 2014089520 A1	12-06-2014
		WO 2014089521 A1	12-06-2014
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WO 2012165940 A1	06-12-2012	NONE	