

[54] LATCHING SELECTOR FOR SELECTIVELY
DRAWING OUT A SINGLE SIGNAL FROM
AMONG A PLURALITY THEREOF[75] Inventors: Sigeiki Isii, Hamamatsu; Yasuji
Uchiyama, Hanakita, both of Japan[73] Assignee: Nippon Gakki Seizo Kabushiki
Kaisha, Shizuoka-ken, Japan

[22] Filed: Aug. 8, 1972

[21] Appl. No.: 278,824

[52] U.S. Cl. 340/147 LP, 84/1.01, 307/243,
328/104, 328/137, 328/154, 340/166 R

[51] Int. Cl. H04q 3/00

[58] Field of Search 340/147 LP, 166 R;
84/1.01; 328/104, 137, 154; 307/243

[56] References Cited

UNITED STATES PATENTS

2,918,576	12/1959	Munch, Jr.	307/243
3,112,353	11/1963	Campbell, Jr.	307/243
3,368,200	2/1968	McNicol	340/147 LP
3,488,515	1/1970	Hiyoshi	84/1.01

Primary Examiner—John W. Caldwell

Assistant Examiner—Robert J. Mooney

Attorney—Solon B. Kemon et al.

[57] ABSTRACT

A latching selector comprises a plurality of switching circuits each switching an assigned signal, a memory circuit including bistable circuits and controlling the respective switching circuits, and the same plurality of key switches triggering the memory circuit. The switching circuits have respective signal input terminals supplied with respective assigned signals, respective control terminals and a common signal output terminal. The memory circuit includes memory output terminals respectively connected to the control terminals, memory input terminals respectively connected to the key switches, a number of bistable circuits equal to the digit number sufficient for binary notation of the plurality number, and a coding and encoding matrix connecting the memory input and output terminals to the bistable circuits in binary relation. When a key switch is actuated, the bistable circuits memorize in binary notation which key switch has been actuated, and in turn keep the corresponding switching circuit to conduct the assigned signal to signal output terminal until another key switch is next actuated.

8 Claims, 5 Drawing Figures

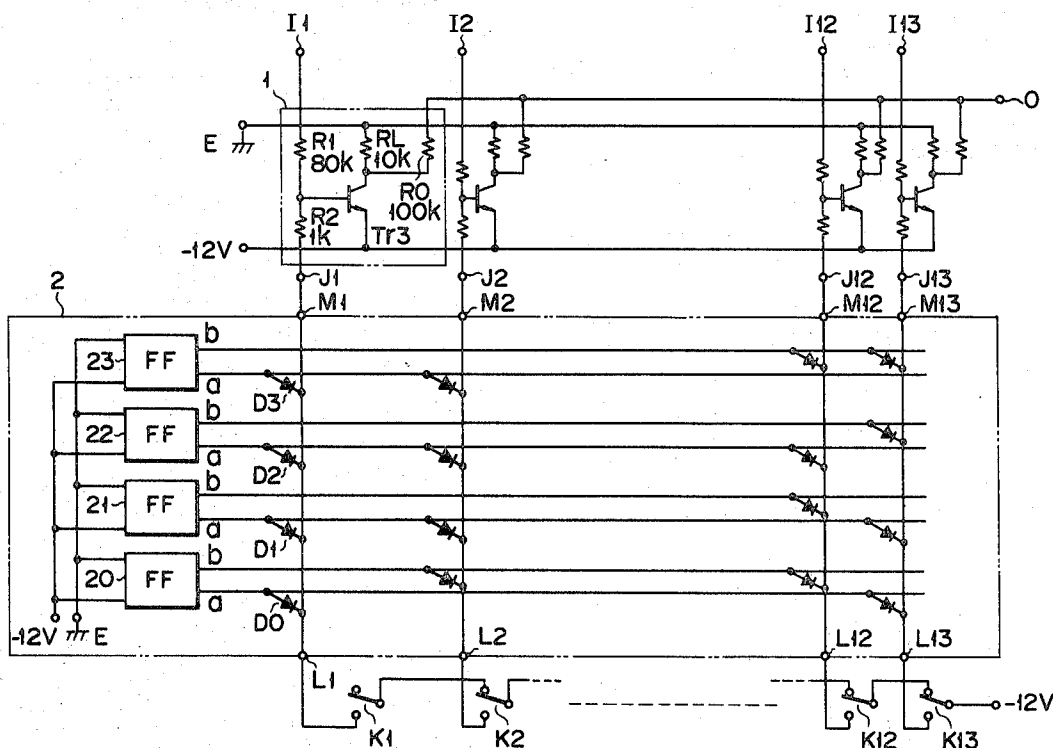


FIG. 1

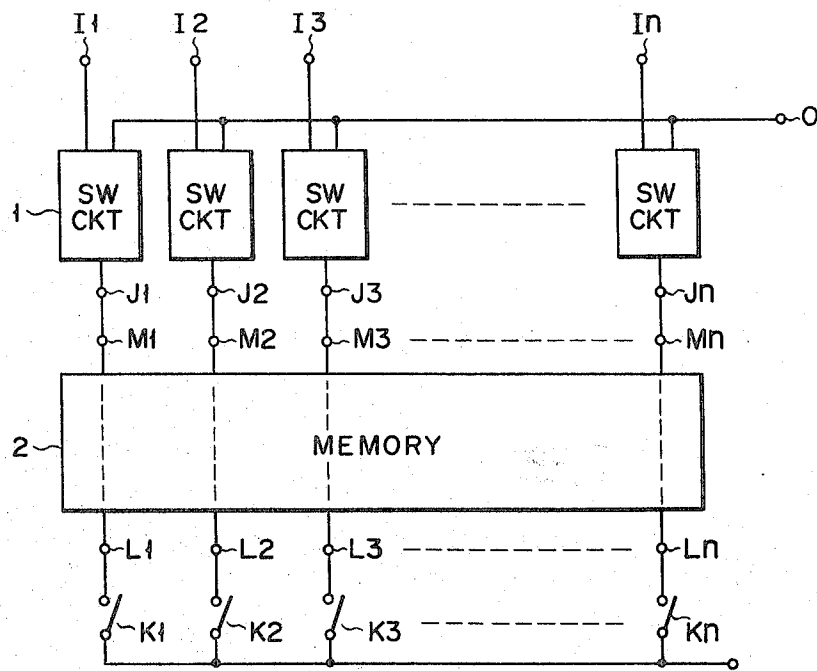


FIG. 2

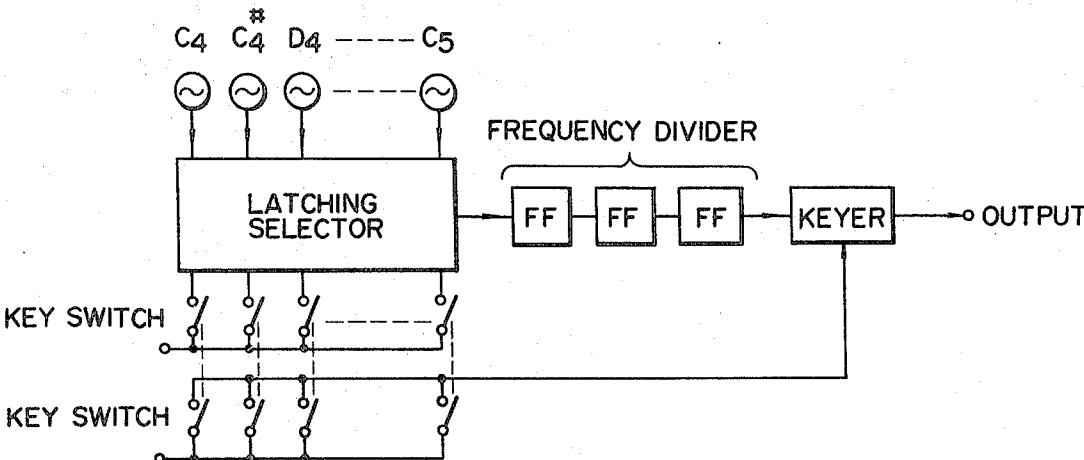


FIG. 3

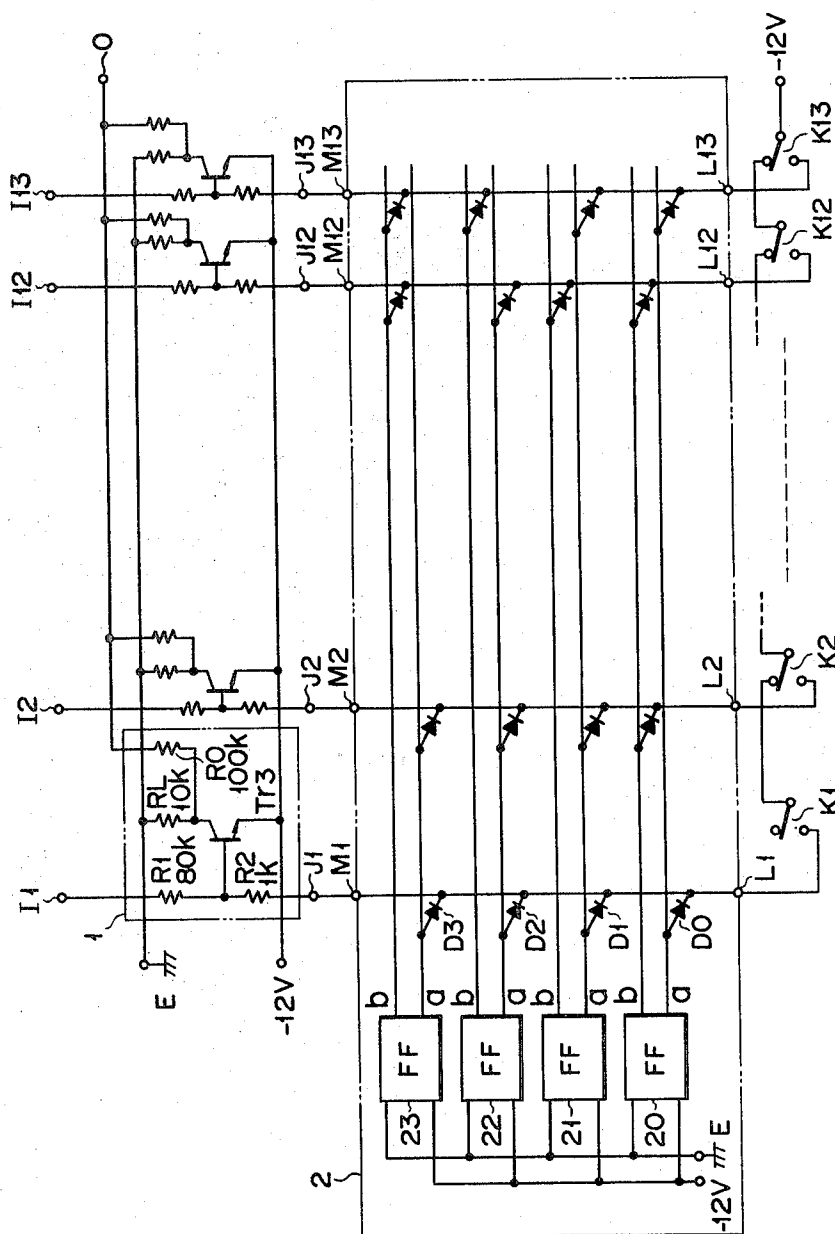


FIG. 4

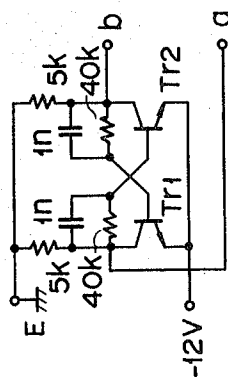
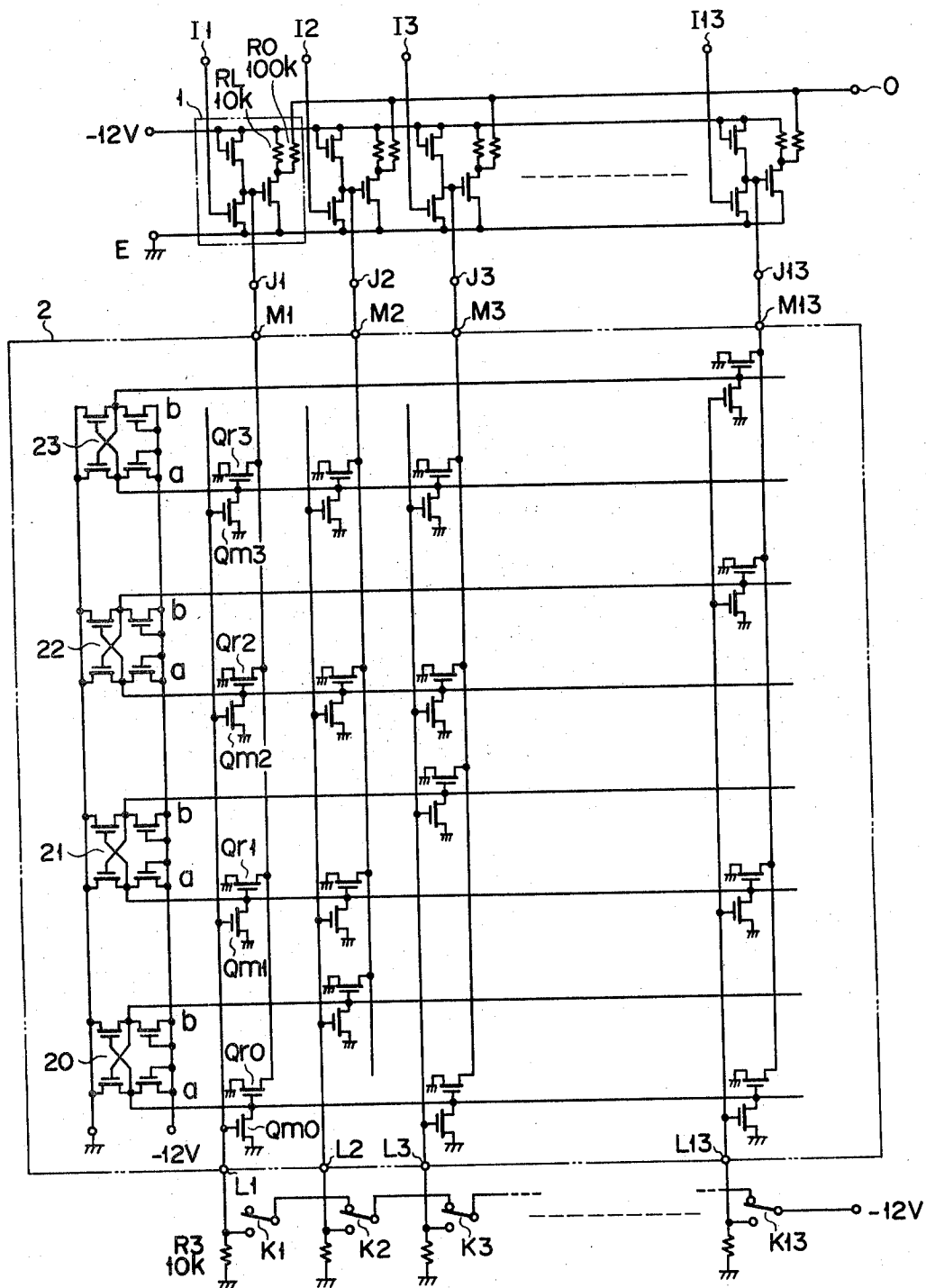


FIG. 5



LATCHING SELECTOR FOR SELECTIVELY DRAWING OUT A SINGLE SIGNAL FROM AMONG A PLURALITY THEREOF

BACKGROUND OF THE INVENTION

This invention relates to a latching selector for selectively drawing out a single signal from a plurality of signals and more particularly to a latching selector adapted for determining pedal tones in an electronic musical instrument.

The pedal tone generator arrangement of an electronic musical instrument is provided with a latching selector for selectively drawing out a tone signal from tone generators which corresponds to a depressed pedal key and sustaining the drawing out of the tone signal until another pedal key is next operated. The latching selector is so constructed that there can be derived from tone generators a single tone signal corresponding to only one of plural pedal keys even when they are simultaneously operated.

A prior art latching selector set forth, for example, in the U.S. Pat. No. 3,488,515 issued to Teruo Hiyoshi on Jan. 6, 1970 includes one bistable or flip-flop circuit for one tone, and is necessarily provided with 13 flip-flop circuits for 13 pedal keys. With the above-mentioned latching selector, operation of a pedal key reverses the state of the corresponding flip-flop circuit to derive a tone signal from the corresponding tone generator and prevents the flip-flop circuits corresponding to all the other pedal keys from delivering tone signal from the tone generators corresponding to the other pedal keys. However, a latching selector requiring a large number of flip-flop circuits as described above is unavoidably complicated in construction and destitute of reliability in operation. It is accordingly the object of this invention to provide a latching selector which well serves the purpose with a smaller number of bistable circuits than the tone generators and consequently admits of a much simpler arrangement.

SUMMARY OF THE INVENTION

According to one aspect of this invention there is provided a latching selector for selectively deriving an input signal from a plurality of input signals, which comprises a plurality of switching circuits each having a signal input terminal, a control terminal and a signal output terminal connected in common to all the switching circuits; a memory circuit including the same plurality of memory output terminals respectively connected to the control terminals of the switching circuits, the same plurality of memory input terminals, a number of bistable circuits equal to the digit number sufficient for binary notation of the plurality number and each having a first and a second line, and a coding and encoding matrix connecting the memory output and input terminals to either of the first and the second lines of the respective bistable circuits in a binary code fashion; the same plurality of key switches respectively connected to the respective memory input terminals; and a control voltage source connected to the key switches and having a voltage sufficient for deciding the stages of the bistable circuits.

In accordance with this invention the number of the bistable circuits can be less than that of the input signals from which a single input signal is selectively derived. The key switches may be comprised by switches each having a normally open contact, normally closed

contact and movable contact. The switches may be connected in preference circuit fashion in such a manner that a movable contact of one of the switches is connected to a normally closed fixed contact of the adjacent switch, the normally open fixed contacts of the respective switches being connected to the corresponding input terminals of the memory circuit, the movable contact of the rearmost switch being connected to the control voltage source. With such switch arrangement, even when several switches are simultaneously actuated a single input signal can be selected corresponding to one of the actuated switches.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an arrangement of a latching selector according to this invention;

FIG. 2 is an arrangement for producing bass tone signals of an electronic musical instrument including a latching selector;

FIG. 3 is a circuit diagram of a latching selector according to an embodiment of this invention;

FIG. 4 shows a circuit diagram of a bistable circuit usable for the latching selector of FIG. 3; and

FIG. 5 is a circuit diagram of a latching selector according to another embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, reference numeral 1 represents a plurality of switching circuits. The switching circuits 1 have signal input terminals I_1 to I_n , control terminals J_1 to J_n and a common signal output terminal O. The input terminals I_1 to I_n are connected to receive input signals from signal sources. Numeral 2 denotes memory circuit including memory input terminals L_1 to L_n and memory output terminals M_1 to M_n . The respective output terminals M_1 to M_n are connected to the respective control terminals J_1 to J_n of the corresponding switching circuits. The memory circuit 2 has its input terminals L_1 to L_n connected to key switches K_1 to K_n which in turn connected to a control voltage source, and includes, as later described, a smaller number of bistable or flip-flop circuits than the signal sources. The output terminals M_1 to M_n of the memory circuit 2 are connected to different selective combinations of one of the two output terminals of the respective flip-flop circuits in a binary coded fashion. Therefore, any one of the output terminals of the memory circuit 2 may be set at a different voltage level representing a so-called memorized state from those appearing at the remaining output terminals of the memory circuit 2. Accordingly, only one switching circuit that is connected to the above-mentioned one output terminal of the memory circuit 2 conducts an input signal supplied to the input terminal to the common output terminal O. The input terminals of the memory circuit 2 are connected to the same selective combinations of one of the two output terminals of the respective flip-flop circuits as those to which there are connected the corresponding output terminals of the memory circuit 2. Where, therefore, one of the switches K_1 to K_{13} is actuated, then there is impressed a control voltage on the corresponding lines of the flip-flop circuits which are connected to the actuated switch, setting the memorizing states of the flip-flop circuits. As a result, the output terminal of the memory circuit 2 corresponding to the actuated switch has a different voltage level from those of the other out-

put terminals of the memory circuit 2, causing the corresponding switching circuit to conduct an input signal from the input terminal to the output terminal. Thus this state is continued until another of the aforesaid switches K1 to K13 is operated.

The latching selector of this invention may be applied to an electronic musical instrument, for example, with an arrangement shown in FIG. 2. The latching selector is connected to thirteen signal sources or tone generators representing, for example, notes C4 through C5 and also to the key switches actuated by thirteen pedal keys. A tone signal picked up by the latching selector has its frequency divided by eight (i.e. stepped down by three octaves by three frequency dividers or flip-flop circuits and the divided tone signal or bass tone signal is conducted to a keyer. Since the latching selector has, as described above, a memorizing faculty, the tone signal selected thereby continues to be supplied to a keyer via the frequency dividers. The keyer is so controlled, as indicated in FIG. 2, by key switches as to produce the base tone signal at the output side thereof upon depression of a pedal key.

There will now be described a latching selector according to an embodiment of this invention shown in FIG. 3 with reference made to FIG. 1. The parts of FIG. 3 the same as those of FIG. 1 are denoted by the same numerals. The memory circuit 2 comprises four bistable circuits or flip-flop circuits 20, 21, 22 and 23, each having first and second lines *a* and *b*. Each flip-flop circuit may consist of an ordinary type including two transistors Tr1 and Tr2 as illustrated in FIG. 4. The first and second lines *a* and *b* are led out from the collectors of the transistors Tr1 and Tr2 respectively. These transistors Tr1 and Tr2 have their emitters connected to a negative power source (-12V) and their collectors to the ground terminal (E) through resistors. As is well known, while the first line *a* of the flip-flop circuit has a first voltage level, for example, -12V, its second line *b* indicates a second voltage level, for example, a ground potential, or vice versa.

The 13 output terminals M1 to M13 of the memory circuit 2 are connected through diodes to one of the two lines *a* and *b* of the respective flip-flop circuits with different selective combinations constituting an individual-to-binary convertor matrix. For example, the output terminal M1 of the memory circuit 2 is connected through diodes D0, D1, D2 and D3 to the first lines *a* of the flip-flop circuits 20, 21, 22 and 23, representing 0000 code. The output terminal M2 is connected through diodes to the second line *b* of the flip-flop circuit 20 and the first lines *a* of the flip-flop circuits 21, 22 and 23, representing 0001 code. Theoretically, one of the two lines of each of the four flip-flop circuits 20, 21, 22 and 23 can be selectively combined in 16 ways at maximum. In FIG. 3, however, there are used thirteen combinations in consideration of application to an electronic musical instrument.

The output terminals M1 to M13 of the memory circuit 2 are connected to the controls J1 to J13 of the switching circuits 1, each of which includes a transistor Tr3 having its base connected to the corresponding tone signal input terminal I through a resistor R1, its emitter connected to the power source (-12V) and its collector grounded through a load resistor RL. The collector of the transistor Tr3 is further connected to the common output terminal O through a take-out resistor RO.

The input terminals L1 to L13 of the memory circuit 2 are connected to its output terminals M1 to M13 and the key switches K1 to K13. Each of the key switches K1 to K13 may include a normally closed fixed contact, a normally open fixed contact and a movable contact. Further, these key switches K1 to K13 may be connected in a preference network fashion such that the movable contact of one of them is connected to the normally closed fixed contact of the adjacent key switch. The normally open fixed contact of the key switch is connected to the corresponding input terminal L of the memory circuit 2. In this case the movable contact of the rearmost key switch K13 is connected to the control voltage source (-12V).

There will now be described the operation of the latching selector of FIG. 3. Now let it be assumed that initially, the first lines *a* of the flip-flop circuits 20, 21, 22 and 23 have a first voltage level (-12V) and the second lines *b* indicate a second voltage level (0V). Under this condition, the first output terminal M1 connected only to the first lines *a* of the flip-flop circuits 20, 21, 22 and 23 becomes free from any urging voltages, whereas all the other output terminals M2 to M13 of the memory circuit 2 are given a ground potential via at least one diode connected to the *b* line(s). That is, the output terminal M2, for example, is connected to the second line *b* of the flip-flop circuit 20 now exhibiting the ground potential. And the output terminal M12 is connected to the second lines *b* of the flip-flop circuits 20, 21 and 23. Under such condition, the transistors Tr3 which are included in the switching circuits 1 corresponding to the output terminals M2 to M13 having a ground potential are brought in a saturated state. Accordingly, input tone signals supplied to the input terminals I2 to I13 can not be drawn out of the collectors of these saturated transistors Tr3.

On the other hand, the first output terminal M1 of the memory circuit 2 does not have a ground potential, and is consequence the transistor Tr3 of the switching circuit 1 connected to the first output terminal M1 is not saturated. Therefore, a tone signal supplied to the first input terminal I1 of the switching circuit 1 is conducted to the output terminal O from the collector of the transistor Tr3 through the take-out resistor RO.

Where the key switch K2 is operated by the corresponding pedal key (not shown), the input terminal L2 of the memory circuit 2 is impressed with control voltage (-12V). In this case, the memorizing state of the flip-flop circuit 20 whose second line *b* is connected to the input terminal L2 is reversed, that is, the first line *a* is set at the second voltage level (0V) and the second line *b* at the first voltage level (-12V). At this time, the states of the remaining flip-flop circuits 21, 22 and 23 remains unchanged. Accordingly, the output terminal M2 is released from the ground potential and the output terminal M1 is now brought to the ground potential. Therefore, a tone signal supplied to the input terminal I2 of the switching circuit 1 corresponding to the output terminal M2 is conducted to the common output terminal O. This state is maintained until another key switch is actuated. Where there is actuated next time, for example, the key switch K12, then there arises the reversion of the states of the other flip-flop circuits 21 and 23 whose second lines *b* is connected to the input terminal L12. As the result, the output terminal M2 is now brought to the ground potential, preventing the tone signal supplied to the input terminal I2 from

being conducted to the common output terminal O, but the output terminal M12 is released from the ground potential thereby permitting a tone signal impressed on the input terminal I12 corresponding to the output terminal M12 to appear at the common output terminal O.

If the key switches K1 to K13 are connected in a preference fashion as described above, then a tone signal supplied only to a signal input terminal corresponding to one of key switches actuated simultaneously nearest to K13 will be delivered to the common output terminal O even when several pedal keys are depressed at the same time.

FIG. 5 shows the arrangement of a latching selector according to a second embodiment of this invention using field effect transistors. According to this embodiment, the flip-flop circuits 20 to 23 and switching circuits 1, as well as the diodes D0 to D3 of FIG. 3 are comprised by MOS field effect transistors.

The output terminals M1 to M13 of the memory circuit 2 are connected through MOS field effect transistors Qr0, Qr1, Qr2 and Qr3 to the same selective combinations of the lines *a* and *b* of the four flip-flop circuits 20, 21, 22 and 23 as in FIG. 3. Between the output terminal M1 of the memory circuit 2 and the ground are connected conduction paths formed between the source and drain of the field effect transistors Qr0 to Qr3. The gates of the MOS field effect transistors Qr0 to Qr3 are connected to the first lines *a* of the flip-flop circuits 20 to 23. The other output terminals M2 to M13 are connected to either of the two lines of the respective flip-flop circuits 20 to 23 constituting a binary coding matrix.

The input terminals L1 to L13 of the memory 2 are connected through the MOS field effect transistors Qm0 to Qm3 to the same selective combinations of the two lines of the four flip-flop circuits 20 to 23 as in FIG. 3. The input terminal L1, for example, is connected to the gates of the MOS field effect transistors Qm0 to Qm3, whose conduction paths in turn are connected between the first lines *a* of the flip-flop circuits 20 to 23 and the ground. The input terminals L1 to L13 of the memory circuits 2 are grounded through the resistor R3 and connected to the normally open fixed contacts of the corresponding key switches K1 to K13.

The output terminals M1 to M13 of the memory circuit 2 are connected to the control terminals J1 to J13 of the switching circuits 1. These control terminals J1 to J13 are connected to the input signal paths of the switching circuits 1 such that the MOS field effect transistors Qr0 to Qr3 connected to the corresponding output terminals shunt the input signal paths of the switching circuits 1 to the ground.

There will now be described the operation of the latching selector of FIG. 5 arranged as described above. Let it be assumed that initially, the first lines *a* of the flip-flop circuits 20 to 23 are set at a first voltage level (now 0V) and the second lines *b* thereof at a second voltage level (now -12V). Under this condition, the MOS field effect transistors Qr0 to Qr3 connected to the output terminal M1 of the memory circuit 2 remain nonconducting. Accordingly, the signal path of the switching circuit 1 supplied with a tone signal through the input terminal I1 is not short-circuited, causing the tone signal supplied to the input terminal I1 to be drawn out to the common output terminal O. The remaining output terminals M2 to M13 of the

memory circuit 2 are shunted to the ground through at least one MOS field effect transistor which is rendered conductive by being connected to the second lines *b* of the flip-flop circuits 20 to 23. Under this condition, the signal path of the corresponding switching circuit is short-circuited to the ground, preventing an input tone signal from being conducted to the common output terminal O.

Where there is operated next time, for example, the key switch K2, the input terminal L2 of the memory 2 is impressed with a control voltage (-12V). As the result, the MOS field effect transistor connected to the input terminal L2 and the second line *b* of the flip-flop circuit 20 becomes conducting, causing the second line *b* to have a ground potential. Accordingly, the memorizing state of the flip-flop circuit 20 is reversed. That is, the first line *a* of the flip-flop circuit 20 is set at the second voltage level (-12V) and the second line *b* at the first voltage level (0V). Thus the MOS field effect transistor Qr0 which is connected to the output terminal M1 of the memory circuit 2 and has been remained nonconducting up to this time is now rendered conductive to short-circuit the signal path related to the input terminal I1 of the switching circuit 1 to the ground. On the other hand, that MOS field effect transistor which is connected to the output terminal M2 of the memory circuit 2 and the second line *b* of the flip-flop circuit 20 and has been kept conducting up to this time is now turned nonconducting. At this time, the states of the remaining flip-flop circuits 21 to 23 remains unchanged. As the result, the signal path related to the input terminal I2 of the switching circuit 1 is changed from the short-circuited to the nonshort-circuited state, permitting a tone signal supplied to the input terminal I2 to appear at the common output terminal O. This condition is sustained until another key switch is actuated.

What we claim is:

1. A latching selector for selectively drawing out a single signal from a plurality of signals comprising:
 - a. a plurality of switching circuits each having a signal input terminal, a control terminal and a signal output terminal;
 - b. a memory circuit including same said plurality of memory output terminals respectively connected to said control terminals, same said plurality of memory input terminals, bistable circuits in a number equal to the digit number sufficient for binary notation of said plurality number and each having a first and a second lines, and a coding and encoding matrix connecting said memory output terminals and said memory input terminals to either of said first and second lines of said respective bistable circuits in a binary code fashion;
 - c. same said plurality of key switches respectively connected to said respective memory input terminals; and
 - d. and a control voltage source connected to said key switches and having a voltage sufficient for deciding the states of said bistable circuits.
2. A latching selector according to claim 1 wherein said means for coupling said output and input terminals of said memory circuit to said lines of said bistable circuits are diodes.
3. A latching selector according to claim 1 wherein each said key switch includes a normally open fixed contact, a normally closed fixed contact and a movable

contact, and wherein said key switches are connected in a preference fashion in such a manner that said movable contact of the respective key switches is connected to the normally closed fixed contact of the adjacent key switch, and the movable contact of the rear-most switch to said control voltage source, said normally open contacts of the respective switches being connected to the corresponding input terminals of said memory circuit.

4. A latching selector according to claim 1 wherein each said switching circuit includes a transistor having a collector, an emitter and a base, and the respective input terminals of said switching circuit and the respective output terminals of said memory circuit are coupled to the bases of the corresponding transistors.

5. A latching selector according to claim 1 wherein said memory circuit includes four bistable circuits, thirteen output terminals and thirteen input terminals; and said key switches connected to said input terminals each including a normally open fixed contact, a normally closed fixed contact and a movable contact, said normally open fixed contact being connected to the corresponding input terminal of said memory circuit, said movable contact to the normally closed contact of the adjacent key switch and the movable contact of the rearmost key switch to said control voltage source.

6. A latching selector according to claim 1 wherein said coding and encoding matrix includes first coupling elements connected in a binary code matrix fashion between said memory output terminals and said lines of the bistable circuits and second coupling elements con-

nected in a binary code matrix fashion between said memory input terminals and said lines of the bistable circuits.

7. A latching selector according to claim 6 wherein said first and second coupling elements each have a conduction path and a control electrode for controlling the conductivity of said conduction path by the voltage impressed on said control electrode, the conduction path of said first coupling elements being connected between the corresponding memory output terminals and a circuit ground and their control electrodes being connected to the corresponding lines of said bistable circuits, said first coupling elements being rendered conductive when said lines of said bistable circuits to which said control electrodes are connected are set at a first voltage level, the conduction paths of said second coupling elements being connected between said lines of said bistable circuits and a circuit ground and their control electrodes being connected to said memory input terminals, said second coupling elements being rendered conductive when said memory input terminals to which said control electrodes are connected are impressed with the voltage from said control voltage source.

8. A latching selector according to claim 7 wherein said first and second coupling elements are field effect transistors each having a conduction path formed between a source and a drain and a gate for controlling the conductivity of said conduction path by a voltage impressed thereon.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,760,358 Dated September 18, 1973

Inventor(s) Sigeki Isii

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

[30] Priority Benefit:
Japanese Patent Application 59601/71, filed
August 9, 1971

Signed and sealed this 29th day of October 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

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