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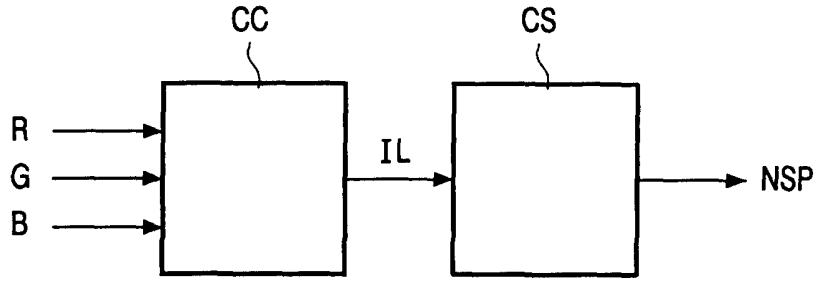

(57) Abstract: The display apparatus displays a color image by controlling a number of emissions (NSP) in accordance with primary video signals (R, G, B). A calculating circuit (CC, CS) calculates a weighted sum (IL) of the primary video signals (R, G, B) and limits the number of emissions (NSP) dependent on the weighted sum (IL). In the weighted sum (IL), at least one of the primary video signals (R, G, B) is weighted differently than another one of the primary video signals (R, G, B). This allows selecting the contribution of the different primary colors (R, G, B) to the weighted sum (IL) such that the number of emissions (NSP) is controlled differently for different primary colors (R, G, B). Consequently, the power (P) can be limited for each of the primary colors (R, G, B) at substantially the same value.

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Display apparatus

The invention relates to a display apparatus for displaying a color image by controlling a number of emissions in accordance with primary video signals, to a power consumption limiting circuit for use in such a display apparatus, and to a method of power consumption limiting.

The power consumption of a plasma display apparatus (further referred to as PDP) is largely determined by the power consumption of the plasma module which comprises the plasma panel and the drive electronics. Especially, the power consumption during the sustaining phase of the plasma module is large and variable. During the sustaining phase, the number of plasma cells (pixels) which have to generate light may vary between none and all. Consequently, variations of the power consumption as a function of the display load are very large. The display load is denoted as a percentage of a full-white image, thus, the average pixel gray value over the actual image divided by the maximum gray (is the full-white) value.

Usually, at average images to be displayed, the required power is substantially lower than the maximum required power when all pixels are emitting light. It is economically not justified to provide a power supply which is able to supply this maximum power requested by the plasma module. Thus, in practice, the power consumption of the plasma module is limited to a maximum power which the power supply of the display apparatus is able to deliver.

It is known to limit the power consumption of the plasma module based on the display load. In the known power limiting circuit, the display load is calculated as the average pixel value divided by the maximum possible value:

$$\text{display load} = ((R+G+B)/3)/255$$

wherein R, G, and B are 8 bit digital values which represent the three primary colors of the image, and which range from 0 to 255. If the digital values are represented by another

number of bits, the number 255 has to be replaced by the number of levels available at this another number of bits.

The power consumption of the plasma module is limited by decreasing the number of sustain pulses (the emissions) during the sustain phase as a function of an increasing display load.

It is a drawback of the prior art that the power consumption of the plasma module depends on the amount of each of the primary colors in the image. This is especially true in plasma displays with an asymmetric cell design wherein the cells corresponding to the different primary color phosphors have different areas.

It is an object of the invention to provide an improved power limiting.

To this end a first aspect of the invention provides a display apparatus as claimed in claim 1. A second aspect of the invention provides a power consumption limiting circuit as claimed in claim 6. A third aspect of the invention provides a power consumption limiting method as claimed in claim 7. Advantageous embodiments are defined in the dependent claims.

The matrix display apparatus displays a color image by controlling a number of emissions in accordance with primary video signals. The power consumed by the display apparatus is limited by calculating the display load of the primary video signals and by limiting the number of emissions based on the calculated display load. The limiting of the number of emissions is different for at least two of the primary video signals. The display load is an average pixel value over the pixels divided by a maximum pixel value of the pixels. In this manner, the number of emissions will be limited different for different primary video signals, which allows compensating for differences in the power consumed for the different primary colors when sustained at a same number of emissions.

In an embodiment as defined in claim 2, a calculating circuit calculates the display load as a weighted sum of the primary video signals and limits the number of emissions dependent on this weighted sum. In the weighted sum, at least one of the primary video signals is weighted differently than another one of the primary video signals.

This allows selecting the contribution of the different primary colors to the weighted sum such that the number of emissions is controlled differently for different primary colors. Consequently, the power can be limited for each of the primary colors at substantially the same value.

For example, the emissions may be caused by ignitions of plasma in a PDP display or a PALC (plasma addressed liquid crystal) display, or by the ignitions in an EL (electroluminescence) display.

In an embodiment as defined in claim 3, the limiting of the power consumption is applied to a plasma display panel (also referred to as PDP) with a matrix of pixels. In more recent PDPs, an asymmetric cell design is introduced to improve the color temperature. The known algorithm will limit the power such that in the worst case the maximum power of the power supply is not exceeded and will allow a large variation of the actual power as a function of the shares of the primary colors in the image. The power consumption limiting circuit in accordance with the invention limits the power for each one of the primary colors separately at substantially the same value.

For example, the plasma display panel is driven in a subfield manner. In each subfield, first all the pixels are selected line by line to prime the pixels such that an appropriate charge is present in those pixels which should produce light during the succeeding sustain phase of this subfield.

The display apparatus comprises a driver for priming the plasma cells and for driving the plasma display panel with sustain pulses to generate an amount of light dependent on a number of sustain pulses in the plasma cells primed to generate light. The primary video signals comprise R, G and B components, and the calculating unit calculates the image load signal IL = a*R+b*G+c*B wherein a, b, c are coefficients determining the weighted sum. At least one of the coefficients differs from the other coefficients.

In an embodiment as defined in claim 4, the calculating circuit limits the number of emissions by multiplying the function of the display load with a correction factor which is a function weighting the primary video signals. Also this allows to select the contribution of the different primary colors to the weighted sum such that the number of emissions is controlled differently for different primary colors. Consequently, the power can be limited for each of the primary colors at substantially the same value.

In an embodiment as defined in claim 5, the controlling circuit lowers the number of emissions as function of the display load to obtain a substantially linear increase of power consumed by the display apparatus as a function of the increase of the display load. This has the advantage that the power consumed increases with the display load, and does not show a maximum at about 60 to 70% of the display load as occurs with the known function which lowers the number of emissions linearly with the weighted sum.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows a block diagram of a prior art plasma display apparatus,

Fig. 2 shows a diagram for explaining a known example of a driving sequence of the plasma display apparatus,

Fig. 3 shows a diagram for explaining the relation between the image load, the number of sustain pulses, and the power consumption of a plasma display apparatus,

Fig. 4 shows a block diagram of a power limiting circuit in accordance with the invention, and

Fig. 5 shows examples of a control of the number of sustain pulses as a function of the display load.

Fig. 1 shows a block diagram of a prior art plasma display apparatus. The plasma display apparatus comprises a plasma display panel 1, a data driver DD, a scan driver SD, a common electrode driver CD, a controller CO, and a waveform generator WG.

The known three electrode plasma display panel 1 comprises scan electrodes SE1 to SEn, further referred to as SEi, common electrodes CE1 to CEn, further referred to as CEi, data electrodes DE1 to DEm, further referred to as DEj, and plasma cells PC11 to PCnm, further referred to as PCij.

The scan electrodes SEi and the common electrodes CEi are arranged substantially parallel. Neighboring scan electrodes SEi and common electrodes CEi are associated with the same plasma cells PCij. Usually, the plasma cells PCij are not physically separated but are areas in a plasma channel. The plasma channel is associated with the neighboring scan and common electrodes SEi and CEi. The areas forming the plasma cells PCij are associated with the neighboring scan and common electrodes SEi and CEi and a crossing data electrode DEj. The data electrodes DEj are arranged substantially perpendicular with respect to both the scan electrodes SEi and the common electrodes CEi.

The scan driver SD supplies scan voltages to the scan electrodes SEi. The common driver CD supplies a common voltage to the common electrodes CEi. The common driver may supply the same common voltage to all the common electrodes CEi, or to groups of the common electrodes CEi. The data driver DD receives input data ID to supply data voltages to the data electrodes DEj.

A controller CO receives synchronization signals SY belonging to the input data ID to supply a control signal CO1 to the scan driver SD, a control signal CO2 to the data driver DD, a control signal CO3 to the common electrode driver CD, and a control signal CO4 to the waveform generator WG. The controller CO controls the timing of the pulses and the signals supplied by these drivers.

The plasma display apparatus operates in a known manner. During an addressing period of the plasma display panel 1, the plasma channels usually are ignited one by one. An ignited plasma channel has a low impedance. The data voltages on the data electrodes DEj determine an amount of charge in each of the plasma cells PCij (the pixels) associated with the data electrodes DEj and the low impedance plasma channel. A pixel PCij preconditioned by this charge to produce light during the sustain period succeeding the addressing period will lit during this sustain period. A plasma channel which has a low impedance is further referred to as a selected line (of pixels). During the addressing phase, the data signals to be stored in the pixels PCij of a selected line are supplied line by line by the data driver DD.

During the sustaining phase, the scan driver SD and the common electrode driver CD supply select pulses and common pulses, respectively, to all the lines. The pixels pre-charged (or primed) to lit will produce light each time the associate plasma cells PCij are ignited. A plasma cell PCij will be ignited when it is pre-charged to do so and the sustain voltage supplied across the plasma cell PCij by the associated scan electrode SEi and common electrode CEi changes a sufficient amount. The total number of ignitions in a frame determine the total amount of light produced by a pixel PCij.

In a practical implementation, the sustain voltage comprises pulses of alternating polarity. The voltage difference between the positive and the negative pulses is selected to ignite the plasma cells PCij pre-charged to produce light, and to not ignite the plasma cells PCij pre-charged to not produce light. The sustain voltage is generated by the waveform generator WG which usually is a known energy recovery circuit. The waveform generator supplies a voltage VS to the scan electrodes SEi and the voltage VC to the common electrodes CEi.

During the sustain phase, the voltage across all the plasma cells PCij has to change polarity. All the plasma cells PCij arranged in parallel form the large panel capacitance CP. The polarity reversal has to take place within the quite short formative time lag FTL (the time between applying a sustain pulse slope and the ignition of the plasma) of the plasma cells PCij. By way of an example, in a practical situation wherein 120 rows of a

42" panel are connected in parallel, the panel capacitance is 15 nF, and the sustain voltage has to change from -170V to +170V in about 0,5 microseconds causing a current of about 45 Amperes.

The steep slopes of the sustain voltage are required because the panel capacitance has to be connected to the power supply before the large sustain current starts to flow. The start of the flow of the sustain current with respect to the start of the sustain slope is the formative time lag FTL. The value of the sustain current depends on the actual number of plasma cells that are ignited to produce light. It is this sustain current which is large and varies with the image information. For example, without a power limiting circuit, in a 42" panel, the sustain current may change to give rise to a power consumption change from almost zero to about 1000 Watts.

Fig. 2 shows a diagram for explaining a known example of a driving sequence of the plasma display apparatus. Fig. 2 shows the so called subfield driving method of a PDP. The video frame FR of the input data ID is divided into a plurality of subfields SF1 to SF4. Preferably, different subfields comprise different numbers of sustain pulses NSP. The grayscale of a pixel is obtained by selecting the appropriate subfields in which the pixel should be primed during the addressing period T1 to produce light during the sustain period T2.

Fig. 2 shows an example of a subfield drive wherein the frame FR is divided in four subfields SF1 to SF4 to display 16 gray levels when the number of sustain pulses NSP in the subfields SF1 to SF4 are a binary range of respectively 8:4:2:1. The scan period (also referred to as select or address period) T1 of each subfield is the period wherein the plasma channels are selected one by one to prime all the display cells PCij. R1 denotes the addressing of the first plasma channel (also referred to as row), and Rn denotes the addressing of the last row. During the scan period T1 the display cells are pre-charged to yes or no produce light during the succeeding sustain period T2. The sustain period T2 of each of the subfields SF1 to SF4 represents the length of time during which the selected cells emit light. It is possible to reproduce 16 gray levels by selecting the appropriate subfields in which a pixel PCij should produce light. Usually 8 to 10 subfields instead of 4 are present.

Fig. 3 shows a diagram for explaining the relation between the image load, the number of sustain pulses, and the power consumption of a prior art plasma display apparatus.

The horizontal axis shows the image load IL as a percentage, the left vertical axis shows the power consumption P in Watts, and the right vertical axis shows the total number of sustain pulses NSP in a frame FR. The dashed line PTOT shows the power

consumption P as a function of the image load IL if the power limiting circuit controls the number of sustain pulses NSP as a function of the image load IL as indicated by the graph NSP1. This dashed line is valid for a known PDP wherein the power consumed at a full red, full green, or full blue image is equal.

In the example shown in Fig. 3, the number of sustain pulses NSP is kept constant at 1024 for an image load IL varying between 0 and 15%. Above an image load IL of 15% the number of sustain pulses NSP decreases linearly to 300 at an image load IL of 100%. The power consumption P changes from 100 Watts at an image load IL of 0% to a maximum of about 430 Watts at an image load IL of about 65% and then decreases to about 300 Watts at an image load IL of 100%. Such a control of the number of sustain pulses NSP is generally applied in known PDPs with a symmetric cell design.

In a PDP with an asymmetric cell design wherein the cells corresponding to the different primary color phosphors Red R, Green G and Blue B have different areas, at a same particular number of sustain pulses NSP a different power consumption occurs. An example of different power consumptions for R, G, and B as function of the image load IL is illustrated by the graphs indicated by R, G, and B, respectively. These graphs start at an image load IL of 0% where the bit values of R, G, and B are zero and end at an image load of 33% at the maximum bit values of either R, G, or B.

The graphs are valid only if the image contains the respective color only. Thus, for R, the graph starts at a power of 100 Watts at an image load of 0% and ends, for example at 150 Watts at an image load of 33%. In this example, the graph of G ends at 170 Watts, and the graph of B ends at 210 Watts.

Consequently, in this example of an existing PDP with an existing power limiting algorithm which handles all the primary colors R, G, B in the same manner, a full red image, or a full green image, or a full blue image, all give rise to a same image load IL of 33% and the corresponding same number of sustain pulses NSP. However, at the same number of sustain pulses NSP, different powers are consumed: display of a full red image causes a power consumption of 150 Watts, of which 50 Watts is due to the sustain current. Display of a full green image causes a power consumption of 170 Watts, of which 70 Watts is due to the sustain current. Display of a full blue image causes a power consumption of 210 Watts, of which 110 Watts is due to the sustain current.

The consequence is that the power consumption P varies with the share of the primary colors R, G, B in images in which more than one primary color is present. The maximum power consumption has to be limited to the maximum power which can be

handled by the power supply. Thus, the power limiting circuit has to be designed to limit the maximum power in the worse case situation of shares of the primary colors to the maximum power which can be handled by the power supply. In all other situations, the limiting circuit will limit the power too much.

Fig. 4 shows a block diagram of a power limiting circuit in accordance with the invention. The power limiting circuit comprises a calculating circuit CC and a controlling circuit CS. The calculating circuit CC receives the primary color signals R, G, B to calculate the image load IL.

In an embodiment in accordance with the invention, the image load is calculated as a weighted sum of the primary color signals R, G, B:

$$IL = a * R + b * G + c * B$$

wherein a, b, and c are coefficients determining the weighted sum IL, and wherein at least two of the coefficients a, b, c differ from each other.

It is possible to select the coefficients a, b, c such that a power consumption occurring at a full red image, a full green image, or a full blue image become substantially equal. Consequently, the power limiting can be optimized for all images and is not dependent anymore on the shares of the primary colors in the image.

The controlling circuit CS receives the image load signal IL to supply a signal indicating the number of sustain pulses NSP in a frame FR. The function which defines the relation between the image load IL and the number of sustain pulses NSP may be selected in several ways, some examples are discussed with respect to Fig. 5.

The calculating circuit CC and the controlling circuit CS may be combined in one dedicated circuit or its functions may be performed by a suitably programmed micro computer. It is possible to calculate the number of sustain pulses NSP directly from the values of the primary color signals R, G, B and the predetermined coefficients a, b, c.

The compensation for the different power consumptions between the primary color signals R, G, B, which, for example, occurs in a PDP with cells having different areas may be performed in the image load function IL, as discussed above. However, usually, the relation between the image load IL and the power consumption P is a non-linear function:

$$P = (A * IL * LP * NSP * \pi)/\eta$$

$$NSP = f(IL)$$ wherein:

A is the total display area of the display panel, IL is the image load, LP is the average luminance per sustain pulse, NSP is the number of sustain pulses per field which is a function of the image load IL, and η is a constant representing the efficiency of the PDP.

Therefore, in a preferred embodiment in accordance with the invention a color correction factor CF is implemented in the display load algorithm:

$$NSP = CF * f(IL)$$

$$CF = IL / (r * RL + g * GL + b * BL)$$ wherein:

RL, GL, BL represent the respective image loads for the R, G, B cells, which are calculated similar to the image load, but now for each color component of each pixel, and the coefficients r, g, b denote the ratio of the power consumption for each color R, G, B with respect to the desired nominal power consumption.

To elucidate the above discussed algorithm, as an example only, it is assumed that a particular PDP without a display load algorithm displays a full red (R), green (G), blue (B) image, respectively, all with 200 sustain pulses. Due to the asymmetric cell design, the power consumption P will be 100 Watts for the full red image, 80 Watts for the full green image, and 120 Watts for the full blue image. If the desired nominal power is 100 Watts, the coefficients r, g, b are calculated to be r = 1, g = 0,8 and b = 1,2. These coefficients are substituted in the color correction factor CF which is used in the display load algorithm to calculate the number of sustain pulses NSP. Now, the number of sustain pulses NSP is different for the different primary colors R, G, B to obtain an equal power consumption P of 100 Watts for both a full red (R), a full green (G), and for a full blue (B) image. The number of sustain pulses NSP remains 200 for the full red image, for the full green and the full blue image, the number of sustain pulses NSP will become 250 and 167 respectively. Since the number of sustain pulses NSP is linear in the formula for the power consumption P, the power consumption P will increase or decrease with the same ratio as the number of sustain pulses NSP.

In this embodiment in accordance with the invention, the calculating circuit CC calculates the same image load IL as in the prior art, and the controlling circuit CS applies the color correction factor CF on the image load IL in calculating the number of sustain pulses NSP.

Fig. 5 shows examples of the control of the number of sustain pulses NSP as a function of the display load IL. As in Fig. 3, the horizontal axis shows the image load IL as a percentage, the left vertical axis shows the power consumption P in Watts, and the right vertical axis shows the total number of sustain pulses NSP in a frame FR.

The graph P1 shows the power consumption P as a function of the image load IL if the power limiting circuit controls the number of sustain pulses NSP as a function of the image load IL as indicated by the graph NS1. This relation between the image load IL and the

number of sustain pulses is known. However, it is not always desirable to have maximum power consumption between 60 and 70% of the image load IL. It may be important to have the maximum light output at 100% image load IL because in a specification of the display to customers the light output is specified at 100% image load.

The graph P2 shows the power consumption P as a function of the image load IL if the power limiting circuit controls the number of sustain pulses NSP as a function of the image load IL as indicated by the graph NS2.

The graph P3 shows the power consumption P as a function of the image load IL if the power limiting circuit controls the number of sustain pulses NSP as a function of the image load IL as indicated by the graph NS3.

If a maximum power consumption is desired at (or near to) 100% image load IL, a display load algorithm has to be determined which causes a more linear relation between the image load IL and the power consumption P.

If the number of sustain pulses NSP is a linear function of the image load IL, the light output for high light outputs of the PDP depends quadratically on the image load:

$$P = (A * IL * LP * NSP * \pi)/\eta$$

wherein, A is the total display area of the display panel, IL is the image load, LP is the luminance per sustain pulse, NSP is the number of sustain pulses per field which is a function of the image load IL, and η is a constant representing the efficiency of the PDP.

The quadratic term is introduced due to the product of the image load IL and the number of sustain pulses NSP which should be a linear function of the image load IL.

Consequently, a load algorithm with a relation of 1 over the image load IL will create a more linear behavior between the image load IL and the power consumption P.
An example of such an image load algorithm is:

$$NSP = d * (1 / IL) + e$$

wherein d and e are suitably selected coefficients.

However, since the black level power (the power required for charging and de-charging the panel capacitance during the sustaining period) is linearly related to the number of sustain pulses, a term with 1 over the image load is introduced. This term causes a dip in the total power function P3 near to the image load of 15%.

An algorithm based on a 1 over the square root of the image load IL provides a more linear relation between the image load IL and the total power consumption P as is shown by the graph indicated by P2. In an equation, this algorithm looks like:

$$NSP = f * (1 / \sqrt{IL}) + g$$

wherein f and g are suitably selected coefficients.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. For example, the invention is also useful in other displays in which a number of discrete emissions determine the light output of a pixel and in which full images of the primary colors cause different power consumptions.

It is also possible to select the weighted sum such that the number of sustain pulses NSP varies with the image load IL to keep the energy consumption constant.

Usually, the control of the number of sustain pulses NSP as a function of the image load is not direct in time but is delayed and/or averaged over time. This minimizes the visibility of the changes in the amount of light produced.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

To conclude, the display apparatus in accordance with a preferred embodiment of the invention displays a color image by controlling a number of emissions NSP in accordance with primary video signals R, G, B. A calculating circuit CC, CS calculates a weighted sum IL of the primary video signals R, G, B and limits the number of emissions NSP dependent on the weighted sum IL. In the weighted sum IL, at least one of the primary video signals R, G, B is weighted differently than another one of the primary video signals R, G, B. This allows selecting the contribution of the different primary colors R, G, B to the weighted sum IL such that the number of emissions NSP is controlled differently for different primary colors R, G, B. Consequently, the power P can be limited for each of the primary colors R, G, B at substantially the same value.

CLAIMS:

1. A display apparatus comprises a matrix of pixels for displaying a color image by controlling a number of emissions in accordance with primary video signals, the display apparatus comprises a calculating circuit for calculating a display load of the primary video signals and for limiting the number of emissions based on the calculated display load to limit a power required by the display apparatus, wherein the limiting of the number of emissions is different for at least two of the primary video signals, the display load being a function of a number of pixels emitting light divided by a total number of pixels of the display apparatus.

2. A display apparatus as claimed in claim 1, wherein
the calculating circuit is adapted for calculating the display load as a weighted sum of the primary video signals and for limiting the number of emissions dependent on the weighted sum, wherein at least two of the primary video signals are weighted differently.

3. A display apparatus as claimed in claim 1, wherein the display apparatus comprises a plasma display panel with a matrix of plasma cells, a driver for priming the plasma cells and for driving the plasma display panel with sustain pulses to generate an amount of light dependent on a number of sustain pulses in the plasma cells primed to generate light, the primary video signals comprise Red, Green and Blue components R, G, B and the calculating unit being coupled to receive the Red, Green and Blue components for calculating a display load substantially as IL = a*R+b*G+c*B, wherein a, b, c are coefficients for determining the weighted sum, and wherein at least two of the coefficients are not equal.

4. A display apparatus as claimed in claim 1, wherein the calculating circuit is adapted for limiting the number of emissions as function of the display load by calculating the number of emissions as a multiplication of a function of the display load and a correction factor being substantially CF = 1 / (r * RL + g * GL + b * BL), wherein RL, RG, RB represent respective display loads for the primary video signals, and r, g, b are coefficients determined by a ratio of a power consumption for each of the primary video signals with

respect to a nominal desired power consumption at a predetermined number of emissions, at least two of the coefficients have non-equal values.

5. A display apparatus as claimed in claim 1, wherein the calculating circuit is adapted for lowering the number of emissions as a function of the display load to obtain a substantially linear increase of power consumed by the display apparatus as a function of an increase of the display load.

6. A power consumption limiting circuit for use in a display apparatus comprising a matrix of pixels for displaying a color image by controlling a number of emissions in accordance with primary video signals, the power consumption limiting circuit comprises means for calculating a display load of the primary video signals and for limiting the number of emissions based on the calculated display load to limit a power required by the display apparatus, wherein the limiting of the number of emissions is different for at least two of the primary video signals, the display load being a function of a number of pixels emitting light divided by a total number of pixels of the display apparatus.

7. A method of power consumption limiting for use in a display apparatus comprising a matrix of pixels for displaying a color image by controlling a number of emissions in accordance with primary video signals, the power consumption limiting method comprises:

calculating a display load of the primary video signals, and

limiting the number of emissions based on the calculated display load to limit a power required by the display apparatus, wherein the limiting of the number of emissions is different for at least two of the primary video signals, the display load being a function of a number of pixels emitting light divided by a total number of pixels of the display apparatus.

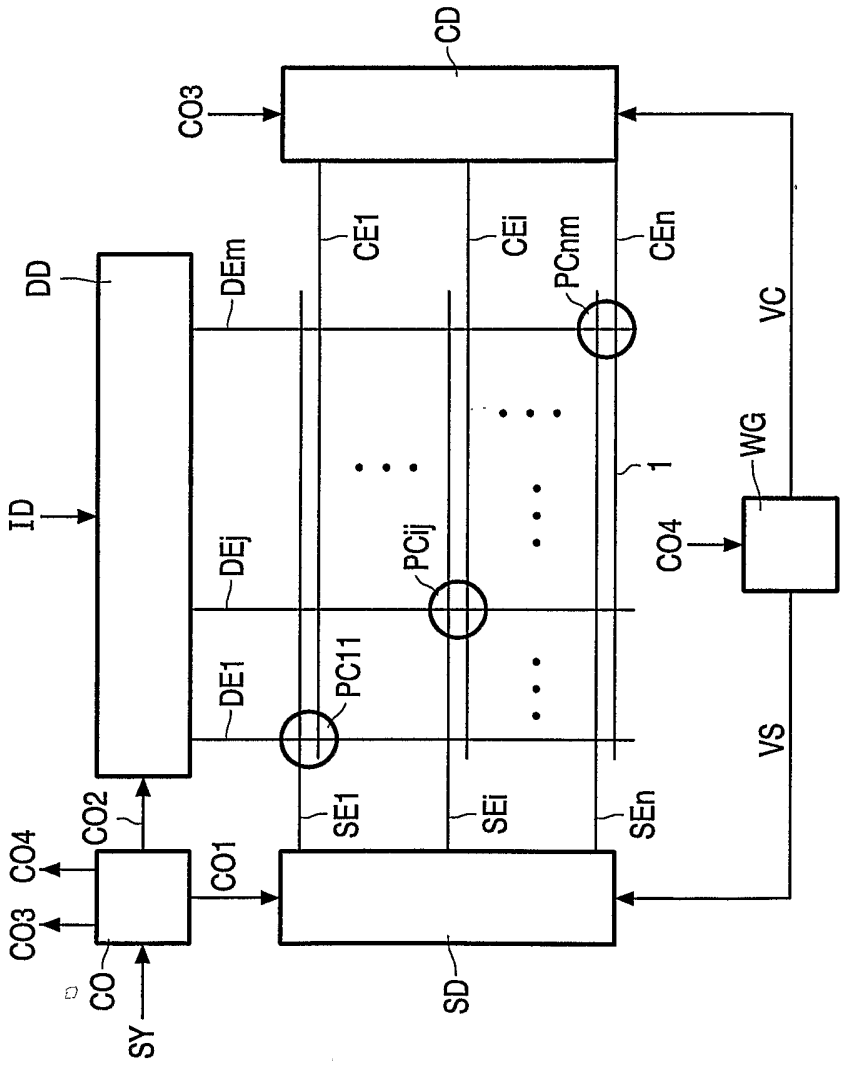

CD
CO3
CE1
CEi
CEn
PCnm
DD
DEm
VC
WG
ID
DEj
PCij
1
CO4
DE1
PC11
VS
CO2
SE1
SEi
SEn
CO4
CO1
CO3
CO
SY
SD

FIG. 1

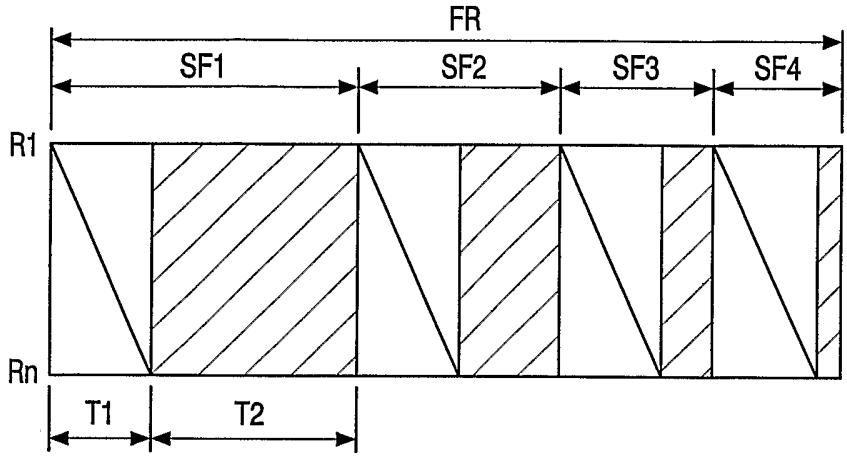
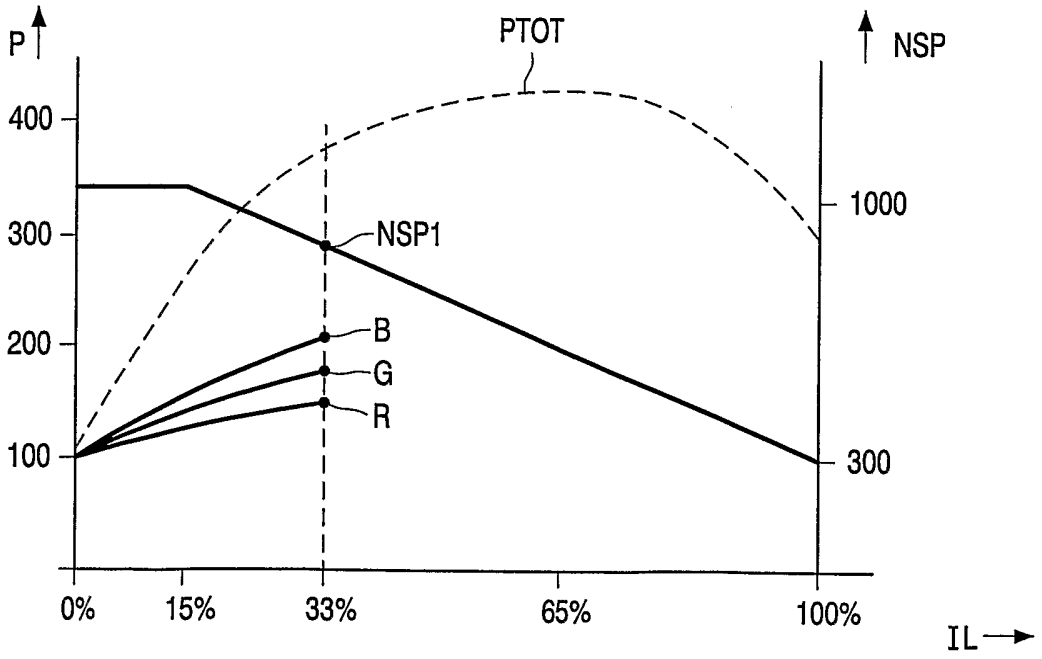

FR
SF1
SF2
SF3
SF4
R1
Rn
T1
T2

FIG. 2


P
PTOT
NSP
400
300
200
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1000
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NSP1
B
G
R
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15%
33%
65%
100%
IL

FIG. 3

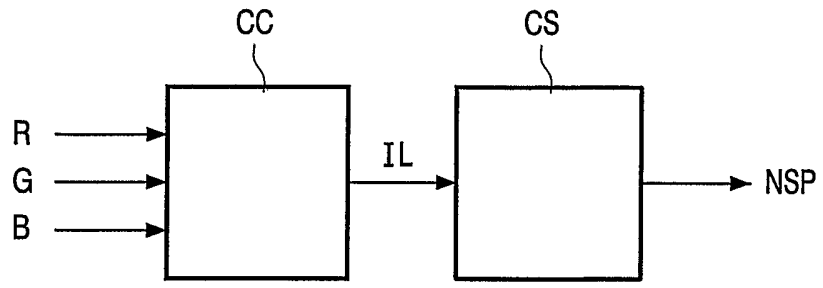
CC
CS
R
G
B
IL
NSP

FIG. 4

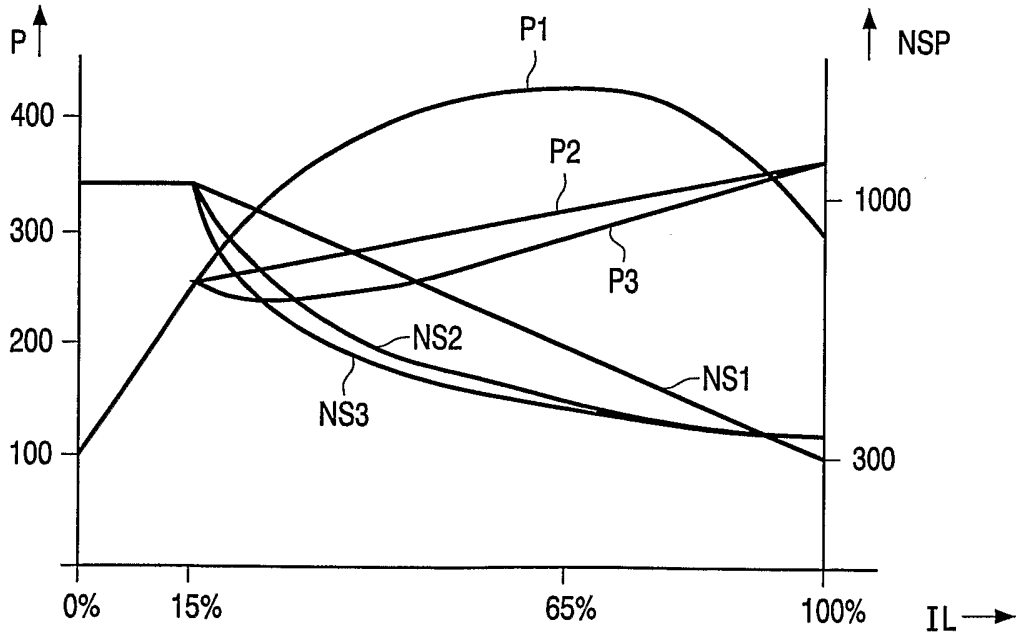
P
NSP
P1
P2
P3
NS1
NS2
NS3
400
300
200
100
1000
300
0%
15%
65%
100%
IL

FIG. 5

INTERNATIONAL SEARCH REPORT

PCT/IB 03/02897

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00 17845 A (MORITA TOMOKO ;ISHIKAWA YUICHI (JP); KASAHARA MITSUHIRO (JP); MATS) 30 March 2000 (2000-03-30) the whole document	1-7
X	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 02, 30 January 1998 (1998-01-30) -& JP 09 281927 A (FUJITSU GENERAL LTD), 31 October 1997 (1997-10-31) abstract	1,2,5
A	the whole document	3,4
E	EP 1 345 201 A (LG ELECTRONICS INC) 17 September 2003 (2003-09-17) the whole document	1-3,5-7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 November 2003	11/11/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Harke, M

INTERNATIONAL SEARCH REPORT

PCT/IB 03/02897

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