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(71) Applicant: **DIALOG SEMICONDUCTOR INC.**
[US/US]; 675 Campbell Technology Parkway, Suite 150,
Campbell, California 95008 (US).(72) Inventors: **GAO, Xiaolin**; 675 Campbell Technology
Parkway, Suite 150, Campbell, California 95008 (US).
CHEN, Yimin; 675 Campbell Technology Parkway, Suite
150, Campbell, California 95008 (US).(74) Agent: **HALLMAN, Jonathan W.**; Haynes and Boone,
LLP, 2323 Victory Avenue, Suite 700, Dallas, Texas
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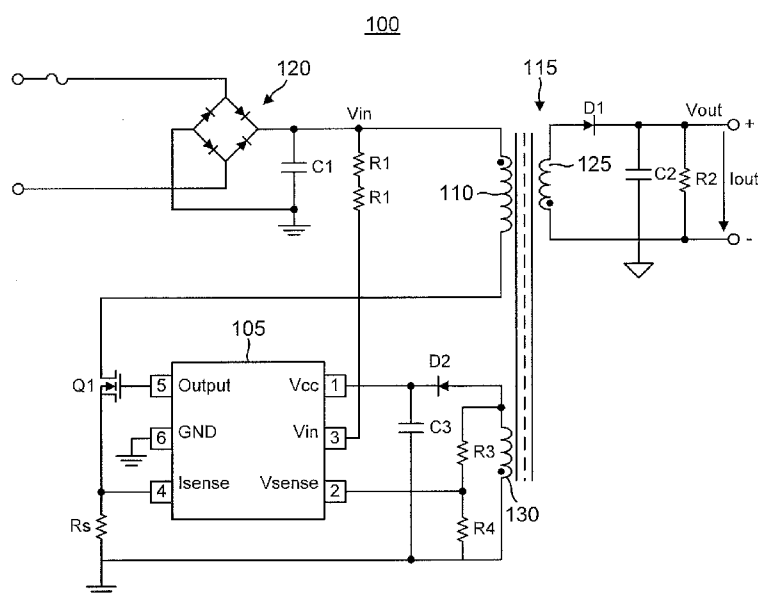


FIG. 1

(57) Abstract: A switching power con-
verter is provided that provides an ad-
aptive power factor correction using a
peak constant current mode and also a
constant on time mode during each cycle
of an input voltage.

FLYBACK PFC CONVERTER WITH ADAPTIVE POWER FACTOR CORRECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Non-Provisional Patent Application No. 14/752,700, filed June 26, 2015, which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] This application relates to switching power converters, and more particularly to a switching power converter with adaptive power factor correction.

BACKGROUND

[0003] A system's power factor relates to its efficiency because it is a ratio of the system's real power to its apparent power. For example, a non-linear load such as an electric motor presents a substantial amount of inductance to an AC power main. At startup, the input current must thus ramp up from zero whereas the AC voltage across the load continues to cycle with the AC power main voltage. The voltage and current into the load are thus out of phase with each other. A worst case with regard to power delivery occurs when the voltage and current are orthogonal to each other (90° out of phase) such that the power delivery is entirely reactive without any real power delivery. But apparent power is the magnitude of the product of the voltage and current (no phase dependence) such that such a device would continue to burn apparent power although the power factor would be zero. In contrast, a purely resistive load would produce no reactive power component such that the real power and the apparent power are equal,

producing an optimal power factor of one. As the reactive power component increases, the power factor drops from one towards zero.

[0004] The power factor is thus an important parameter for a switching power converter such as a flyback converter as its transformer inevitably presents a non-linear load to the AC power main. It is thus conventional to implement power factor correction in a flyback power converter. For example, a diode bridge and capacitor may be used to provide a rectified input voltage for a flyback power converter. Despite the rectification, the input voltage will still have a sinusoidal profile for relatively small (and thus inexpensive) input capacitors. To obtain a high power factor, the peak current through the primary winding in the flyback converter's transformer should also have a similar sinusoidal profile. This peak current through the primary winding is proportional to a product of the input voltage and the on time (t_{on}) for the corresponding switching cycle in the flyback converter. The on time is proportional to a ratio of the peak primary winding current to the input voltage. If the peak primary winding current amplitude is tied to the input voltage (as it should be for a high power factor), one can thus readily see that a constant on time achieves a high power factor.

[0005] But the resulting constant on time causes an undesirable ripple in the flyback converter's output voltage. In that regard, it can be shown that the output power of a flyback converter is proportional to a square of a product of the input voltage and the on time. Since the input voltage varies sinusoidally, the output power (and hence the output voltage) also varies sinusoidally for constant on time power factor correction. The flyback converter must then use a relatively large output capacitor at the secondary side of the transformer to filter the output ripple, which raises costs. To achieve high power factor correction yet also provide a tightly regulated output voltage, it is thus conventional to use a multi-stage approach such as by processing the output voltage

from the flyback converter through a DC-DC switching power converter. But such multi-stage approaches are expensive in terms of the extra components and increased control complexity. It is thus more economical to use a single-stage flyback converter architecture. But such users are then left with a choice of an improved power factor with a poorly-regulated output voltage or a tightly-regulated output voltage with a decreased power factor.

[0006] Accordingly, there is a need in the art for single-stage flyback converters with power factor correction and reduced output voltage ripple.

SUMMARY

[0007] A flyback switching power converter controller is provided with adaptive power factor correction. In this adaptive power factor correction, the controller institutes a period of constant peak current control and a period of constant switch on time control in each cycle of the input voltage. The flyback converter rectifies an AC main voltage to produce the rectified input voltage such that it still retains a rectified sinusoidal profile. The constant peak current control period may be centered about the sinusoidal peak in each cycle of the input voltage. In such embodiments, the controller would control a power switch for the flyback converter to have a constant on time during an initial portion of each input voltage cycle and during a final portion of each input voltage cycle.

[0008] Regardless of the relative timing of the constant on time periods versus the constant peak current period, the mixed usage of both these modes in each input voltage markedly reduces the resulting output voltage ripple at a cost of a relatively minor reduction in power factor. A suitably high power factor may thus be provided in combination with a relatively tightly regulated output voltage. These advantageous

features may be better appreciated through a consideration of the detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 illustrates an example flyback converter in accordance with an embodiment of the disclosure.

[0010] Figure 2 illustrates an example constant peak current control feedback circuit with adaptive power factor correction for the controller of Figure 1.

[0011] Figure 3 illustrates another example constant peak current control feedback circuit with adaptive power factor correction for the controller of Figure 1.

[0012] Figure 4 illustrates a clamped signal waveform for the feedback circuits of Figures 2 and 3.

[0013] Figure 5 illustrates the clamped signal waveforms for the feedback circuits of Figures 2 and 3 under a light load condition, a heavy load condition, and an overload condition.

[0014] Figure 6 illustrates an example constant on time control feedback circuit with adaptive power factor correction for the controller of Figure 1.

[0015] Figure 7 illustrates the ramp slope waveform for two cycles of the input voltage for the feedback circuit of Figure 6.

[0016] Embodiments of the present disclosure and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

[0017] To address the need in the art for improved power factor correction in a single-stage flyback converter with reduced output ripple, two different control modes are used across each cycle of the AC power main. During one portion of the AC power main cycle, the flyback converter uses a constant on time mode of operation. During a remaining portion of the AC power main cycle, the flyback converter uses a constant peak current mode of operation. The use of the constant on time mode during each AC power main cycle provides a high power factor but at the cost of relatively large output voltage ripple. Conversely, the use of the constant peak current mode of operation provides a tightly-regulated output voltage at the cost of a reduced power factor. The mixed mode operation thus provides an advantageous compromise between the conflicting goals of reducing the output voltage ripple and increasing the power factor.

[0018] The result is a power factor correction that is less than what would be achieved using a constant on time across the entire AC power main cycle. However, this reduction may be relatively mild such as resulting in a power factor of 0.7 instead of the nearly unitary value that strict constant on time would provide. Such a relatively high power factor is perfectly adequate for low-power applications such as an LED driver. At the same time, the output voltage level is substantially improved as compared to a strict constant on time mode of operation. Advantageously, the disclosed mixed-mode control provides the user an ability to select or tune the relative amounts of power factor correction and reduced output voltage ripple for a given application by varying the durations in each AC power main cycle dedicated to the constant on time mode period versus the constant peak current mode period.

[0019] The mixed mode control disclosed herein is independent of the control methodology traditionally used to achieve single-stage high power factor correction

using a flyback converter. For example, it is conventional to achieve single-stage high power factor correction using either a constant on time feedback loop methodology or a constant peak current feedback loop. Both of these control methodologies may be modified to practice the mixed-mode control (adaptive power factor correction) disclosed herein. Constant peak current control embodiments will be discussed first followed by a discussion of constant time-on embodiment.

Peak Current Feedback Control with Adaptive Power Factor Correction

[0020] An example single-stage flyback converter 100 configured to implement adaptive power factor correction using a modified constant peak current feedback control loop is shown in **Figure 1**. As will be explained further below, flyback converter 100 may also be modified to practice adaptive power factor correction using a modified constant on time feedback control loop. Flyback converter 100 is thus generic to both control methodologies. A controller integrated circuit 105 for flyback converter controls the switching of a power switch such as an NMOS transistor Q1. In alternative embodiments, the power switch may be implemented using a bipolar junction transistor. Controller 105 controls a gate voltage for power switch transistor Q1 through an output pin 5. When switched on, power switch transistor Q1 allows a primary current to flow through a primary winding 110 of a transformer 115 responsive to an input voltage V_{in} . A rectifier 120 including a diode bridge and a capacitor C1 rectifies the alternating line voltage carried on an AC main 125 to provide the input voltage V_{in} . In some embodiments, capacitor C1 is not an electrolytic capacitor such that it has a relatively small amount of capacitance. The input voltage V_{in} thus still retains a sinusoidal profile across each half of an AC main cycle.

[0021] For each cycle of power switch transistor Q1, the primary winding current ramps up from zero to a peak winding current value that depends upon the input

voltage V_{in} , the switch on time, and the inductance for primary winding 110. When power switch transistor Q1 cycles off, a secondary winding current flows across a second winding 125 in transformer 115, starting from a peak value and continuing to ramp down to zero. An output capacitor C2 and a resistor R2 stabilize a resulting output voltage V_{out} produced by the second winding current. A diode D1 prevents the secondary winding current from flowing while the primary winding conducts. The secondary winding current produces a reflected voltage across primary winding 110 and also across an auxiliary winding 130 for transformer 115. Diode D2 will have a voltage drop across it that prevents a direct relationship between the reflected voltage and the output voltage while the secondary current still flows. But when the secondary current ramps to zero (the transformer reset time), there is no voltage drop across diode D2 such the resulting reflected voltage at that time is directly related to the output voltage. By sampling the reflected voltage across auxiliary winding 130 at the transformer reset time, controller 105 thus may determine the output voltage V_{out} as known in the primary-only feedback arts. For example, controller 105 may include a V_{sense} pin 2 that samples the reflected voltage across auxiliary winding 130 through a voltage divider formed by a pair of resistors R3 and R4. The reflected voltage may also be rectified through a diode D12 and a capacitor C3 to form a power supply voltage VCC received by controller 105 at a power pin 1.

[0022] Controller 105 may include a ground pin 6 and a current sense (I_{sense}) pin 4 that samples the primary winding current through the voltage produced across a sampling resistor R_s coupled to a source of power switch transistor Q1. Since the input voltage V_{in} is proportional to a time rate of change of the primary winding current times the primary winding inductance, controller 105 may determine the input voltage V_{in} indirectly through the I_{sense} pin voltage. However, controller 105 may also

include a V_{in} pin 3 for directly sampling the input voltage V_{in} through one or more resistors R1.

[0023] Given the rectified sinusoidal profile for the input voltage V_{in} , the resulting primary winding current should also have a similar profile to provide a high power factor for flyback converter 100. Should controller 105 implement a constant on time for each cycle of power switch transistor Q1, the peak primary winding current will have a similar rectified sinusoidal profile across each cycle of the input voltage V_{in} (and hence across each half cycle of the AC main voltage) to provide a high power factor but at the cost of substantial output voltage ripple. Controller 105 is thus configured to practice an adaptive power factor correction in which both a constant on time mode of operation and a constant peak current mode of operation is used within each cycle of the input voltage V_{in} .

[0024] For example, controller 105 may include a first peak current control feedback circuit 200 as shown in **Figure 2**. In first peak current control feedback circuit 200, a comparator 205 (e.g. a differential) produces an error voltage (V_{error}) that equals the difference between a reference signal (e.g., a reference voltage such as produced by a band gap reference circuit 210) and a feedback signal (e.g., a feedback voltage I_{sense} as sampled at the transformer reset time). As discussed previously, the V_{sense} voltage has a direct relationship to the output voltage V_{out} for flyback converter 100 when sampled at the transformer reset time. After filtering through a compensation filter 215, the error voltage is multiplied with a clamped version 230 of the input voltage V_{in} in a multiplier 220. A voltage clamp circuit 225 clamps the input voltage V_{in} to produce clamped version 230, which may also be designated as a reference signal. A resulting peak winding current command 240 from multiplier 220 thus equals a product of the compensated error voltage and clamped version 230 of the input voltage V_{in} . A

comparator 245 asserts a power switch off command 250 when I_{sense} equals peak winding current command 240. Referring again to Figure 1, recall that I_{sense} represents the winding current. Since the power switch transistor Q1 will be turned off when I_{sense} equals peak winding current command 240, first peak current control feedback circuit 200 controls the peak winding current in each cycle of the power switch transistor Q1.

[0025] Should the input voltage not be clamped, it will have a sinusoidal profile 235, which shows the two sinusoidal peaks produced in sinusoidal profile 235 for every cycle of the AC main voltage. If multiplier 220 instead multiplies the compensated error voltage with V_{in} 235, a conventional constant time on mode of operation results using a peak current power factor correction feedback loop. In particular, note the peak primary winding current for a given power switch cycle is proportional to a product of the peak value for the input voltage V_{in} and the switch on time. The switch on time is thus proportional to a ratio of the peak primary winding current and the peak input voltage V_{in} . Since the peak primary winding current is tied to the peak input voltage through the multiplication, such a conventional peak current power factor correction feedback loop results in a constant on time for each power switch switching cycle. But the multiplication with clamped input voltage 235 only produces the constant on time mode of operation during the portions of each input voltage cycle that is not clamped.

[0026] During the clamped portion of a cycle for clamped input voltage 230, peak winding current command 240 is substantially constant. But input voltage 235 continues to peak sinusoidally during these clamped periods. Starting from a beginning time for each clamped period, the on time for successive power switch cycles will thus be shorter and shorter until a minimum on time is reached when input voltage 235 reaches its peak value. The switch on time for successive power switch cycles will then

begin to increase until the end of the clamped portion in the cycle for clamped input voltage is reached. It may thus be seen that the switch on time is inversely proportional to input voltage 235 during each clamped portion of clamped input voltage 230 such that the product of input voltage 235 and the on time is substantially constant. Since the output power for flyback converter 100 is proportional to a square of this product, the constant peak current mode of operation during each clamped period substantially reduces output voltage ripple as compared to conventional constant on time peak primary winding current control techniques. Such output voltage ripple reduction comes at the cost of a reduced power factor since input voltage 235 is varying across the clamped portion whereas the peak primary winding current is maintained constant. But as discussed previously, numerous applications such as an LED driver operate satisfactorily at lower power factors. Moreover, the resulting power factor from the adaptive power factor correction provided by first peak current control feedback circuit 200 is much better than what would be achieved if the primary winding current were maintained constant across the entire cycle of input voltage 235.

[0027] Rather than clamping the input voltage V_{in} , the I_{sense} voltage may be clamped to provide an adaptive power factor correction. For example, controller 105 may include a second peak current control feedback circuit 300 as shown in Figure 3. Band gap reference circuit 210, comparator 245, multiplier 220, compensation filter 215, and comparator 205 all function as discussed with regard to first peak current control feedback circuit 200. However, note that the input voltage V_{in} is no longer clamped. Instead, the I_{sense} voltage is clamped analogously by a voltage clamp circuit 315 to produce a clamped I_{sense} voltage 305 received by comparator 245. In that regard, it is conventional to clamp the I_{sense} voltage to provide over-current protection. But such conventional clamping occurs at a peak voltage level that exceeds that

produced by the peak primary winding current during normal operation. In contrast, voltage clamp circuit 315 clamps the Isense voltage at a level that is less than the peak Isense voltage produced by the peak primary winding current during normal operation. Moreover, in an over-current condition, a flyback converter will typically reset or shut down whereas controller 105 continues to cycle the power switch transistor Q1 despite the clamping of Isense voltage 310 to produce clamped Isense voltage 305 in second peak current control feedback circuit 300. Comparing first peak current control feedback circuit 200 with second peak current control feedback circuit 300, it may be seen that in both embodiments a clamp circuit is used to clamp a signal selected from a group consisting of a reference signal (e.g., clamped version 230) or an Isense signal.

[0028] Regardless of whether the adaptive feedback control is achieved using first peak current control feedback circuit 200 or second peak current control feedback circuit 300, the peak current control uses a clamped signal representative of the input voltage V_{in} . In other words, the clamped signal has a rectified sinusoidal profile in the absence of clamping that is in-phase with the input voltage V_{in} . Referring again to Figure 2, clamped version 230 of the input voltage V_{in} need not be derived directly from the input voltage V_{in} but instead could be a synthesized waveform. The synthesis would simply need to be synchronous with each cycle of the input voltage V_{in} . Similarly, clamped Isense voltage 305 in constant peak current control feedback circuit 300 need not be derived from Isense voltage 310 but instead could be synthesized so long as the resulting clamped waveform is synchronous with each cycle of the input voltage V_{in} . Regardless of how the clamped signal (V_{in} or Isense) is generated, the resulting mixed operation modes are as shown in **Figure 4** for a clamped signal 400. During each clamped portion of clamped signal 400, a period 405 of constant peak current operation occurs. Similarly, during each non-clamped portion in which the

clamped signal resumes its rectified sinusoidal profile, a period 410 of constant on time operation results. Referring again to Figures 2 and 3, voltage clamp circuit 225 and voltage clamp circuit 315 may each have their respective clamping voltage levels being responsive to a clamp command such that the respective percentages of when flyback converter 100 operates in a constant peak current mode or a constant on time mode may be tuned accordingly. This tuning may be performed automatically by controller 105 responsive to operating conditions or may be responsive to a user's command.

[0029] In embodiments in which the clamping voltage level is controlled by controller 105, the Verror voltage may be used to determine the load level such the clamping level is scaled proportional to the determined load level. The resulting clamped signal is shown in **Figure 5**. A first clamped signal 500 represents a low load condition in which the clamping voltage is lowered to a nominal value (V_{nom}). As the load is increased, controller 105 continues to increase the clamping voltage level until a maximum value (V_{clamp}) is reached as shown for a second clamped signal 505 (a high load condition). At this point, no further increases in the clamping voltage level can be achieved such that the feedback loop can only supply more power by increasing the percentage of time in which the constant peak current mode of operation is used as shown for a third clamped signal 515. This provides an ability to detect an over-current condition, which is especially useful for second peak current control feedback circuit 300 since a conventional over-voltage clamp is replaced by voltage clamp circuit 315. In that regard, the constant peak current period in each cycle of the clamped signals has a nominal duration (T_{nom}). As this duration is exceeded for third clamped signal 515, an overload condition may be detected accordingly.

Constant On Time Feedback Control with Adaptive Power Factor Correction

[0030] An example constant on time feedback circuit 600 with adaptive power correction is shown in **Figure 6**. A first comparator 605 such as a differential amplifier receives a ramped voltage (or current) signal 630 from a ramp generator 610. A second comparator 615 (which also may comprise a differential amplifier) provides an error signal (Verror) to first comparator 605 based upon the difference between a reference voltage Vref and the Vsense signal. A suitable reference voltage generator such as a band gap reference circuit 620 may be used to provide the reference voltage Vref. If ramp generator 610 generated the ramp voltage using a constant slope, a conventional constant on time control loop results. This is so because the error signal Verror may be considered to be relatively constant over any given cycle of the input voltage Vin. The comparison of a constant slope ramp signal with the relatively static error signal Verror will thus produce a constant on time for each cycle of the power switch transistor Q1 as is conventional to result in a high power factor at the cost of relatively high output voltage ripple. To provide markedly reduced voltage ripple (e.g., a reduction of 50%) while still providing a relatively high power factor such as 0.7 or greater), a slope control module 625 varies a slope for ramp generator 610 over a constant peak current mode of operation in each cycle of the input voltage Vin. Slope control module 625 maintains the slope constant over a remaining portion of each cycle of the input voltage Vin. A compensation filter (not illustrated) may be used to filter error signal Verror to prevent constant on time feedback circuit 600 from responding to the slope modulation provided by slope control module 625. Alternatively, the bandwidth of comparator 615 may be made relatively low to provide the desired compensation.

[0031] A resulting waveform for ramp signal 630 may be as shown in **Figure 7**. In each cycle of the input voltage Vin (and thus each ramp slope cycle), the ramp slope

is maintained constant over an initial constant on time period and a final constant on time period. In between these two periods, the slope is sinusoidally peaked in each ramp slope cycle. During these peaking portions, the increasing ramp slope results in shorter and shorter switch on times until a shortest switch on time is reached. The switch on times would then be increased until the ramp slope is again made constant. The switch on times during the sinusoidally peaked portion of each ramp slope cycle are thus consistent with a constant peak current mode of operation. The remaining constant slope portions of each ramp slope cycle correspond to a constant on time mode of operation. With regard to synchronizing the generation of the constant slope periods with the constant peak current period in each ramp slope cycle, slope control module 625 may receive a timing command derived from the cycling of the input voltage V_{in} . In addition, controller 105 may command slope control module 625 to vary the relative proportions of the constant peak current portion as compared to the constant on time portions in each ramp slope period responsive to changing load conditions analogously as discussed with regard to Figure 5. Slope control module 625 may generate the changing ramp slope command using, for example, selectable resistors R . Moreover, the changing ramp slope may be conducted in a piece-wise linear fashion that approximates the desired sinusoidal profile during the constant peak current periods.

[0032] As those of some skill in this art will by now appreciate and depending on the particular application at hand, many modifications, substitutions and variations can be made in and to the materials, apparatus, configurations and methods of use of the devices of the present disclosure without departing from the spirit and scope thereof. In light of this, the scope of the present disclosure should not be limited to that of the particular embodiments illustrated and described herein, as they are merely by way of

some examples thereof, but rather, should be fully commensurate with that of the claims appended hereafter and their functional equivalents.

CLAIMS

We claim:

1. A flyback converter controller, comprising:
 - a multiplier configured to multiply an error signal with a reference signal to produce a peak current command signal;
 - a comparator configured to compare the peak current command signal corresponding to a desired peak value for a primary winding current to an Isense signal that represents a primary winding current amplitude, the comparator configured to generate a power switch off command responsive to an amplitude for the primary winding current equaling the desired peak value, and
 - a clamp circuit configured to clamp a signal selected from the reference signal and the Isense signal such that a peak value for the primary winding current amplitude is maintained constant for a constant peak current period of each cycle of an input voltage and such that a power switch on time is maintained constant in a remaining constant on time period of each cycle of the input voltage.
2. The flyback controller of claim 1, wherein the clamp circuit is configured to clamp the reference signal during each constant peak current period, and wherein the reference signal is proportional to a rectified sinusoidal profile for the input voltage during each constant on time period.
3. The flyback controller of claim 2, further comprising an error signal generator configured to compare a feedback signal representative of an output voltage to a reference voltage to generate the error signal.

4. The flyback controller of claim 3, further comprising a band gap reference circuit configured to generate the reference voltage as a band gap reference voltage.
5. The flyback controller of claim 3, wherein the error signal generator further comprises a compensation filter configured to filter the error signal.
6. The flyback controller of claim 3, wherein the flyback controller is configured to vary a duration of the constant peak current period responsive to a load level.
7. The flyback controller of claim 7, wherein the flyback controller is further configured to trigger an over-current condition responsive to the duration of the constant peak current period exceeding a threshold value.
8. The flyback controller of claim 1, wherein the clamp circuit is configured to clamp the I_{sense} signal, and wherein the peak value for the primary winding current is less than an over-current peak value for the primary winding current.
9. The flyback controller of claim 1, wherein the flyback controller is incorporated into a flyback converter including the power switch, and wherein the power switch comprises a MOSFET transistor.
10. The flyback controller of claim 1, wherein the flyback controller is incorporated into a flyback converter including the power switch, and wherein the power switch comprises a bipolar junction transistor.
11. A flyback controller, comprising:

an error signal generator configured to generate an error signal that is proportional to a difference between a reference signal and a feedback signal;

a ramp generator configured to cyclically generate a ramp signal;

a comparator configured to switch off a power switch responsive to the ramp signal equaling the error signal; and

a ramp slope control circuit configured to control a ramp slope for the ramp signal such that the ramp slope has a substantially sinusoidally peaked period for each cycle of an input voltage and such the ramp slope is maintained constant during a remaining portion of each cycle of the input voltage.

12. The flyback controller of claim 11, further comprising a band gap reference circuit configured to generate the reference signal as a band gap reference voltage.

13. The flyback controller of claim 11, wherein the ramp slope control is further configured to control the ramp slope by selecting from a plurality of selectable resistors to generate a ramp slope command.

14. The flyback controller of claim 11, wherein the ramp slope control circuit is further configured to control the ramp slope such that the substantially sinusoidally peaked period is a piecewise linear period.

15. A switching power converter control method, comprising:

generating a reference signal having a rectified sinusoidal profile in each cycle of an input voltage;

clamping the reference signal to generate a clamped reference signal;

multiplying the clamped reference signal with an error signal to generate a peak current command; and

in each cycle of a power switch, turning off the power switch responsive to a primary winding current equaling the peak current command.

16. The switching power converter control method of claim 15, wherein turning off the power switch comprises turning off a MOSFET transistor.

17. The switching power converter control method of claim 15, wherein turning off the power switch comprises turning off a bipolar junction transistor.

18. A switching power converter control method, comprising:

generating a ramp signal having at least one constant slope portion and a remaining sinusoidally peaked period for each cycle of an input voltage;

cycling a power switch for the switching power converter on and off during each cycle of the input voltage, wherein switching off the power switch is responsive to the ramp signal equaling an error signal.

19. The switching power converter control method of claim 1, further comprising generating the error signal responsive to a comparison of a reference signal to a feedback signal.

20. The switching power converter control method of claim 19, further comprising generating the reference signal as a band gap reference voltage using a band gap reference circuit.

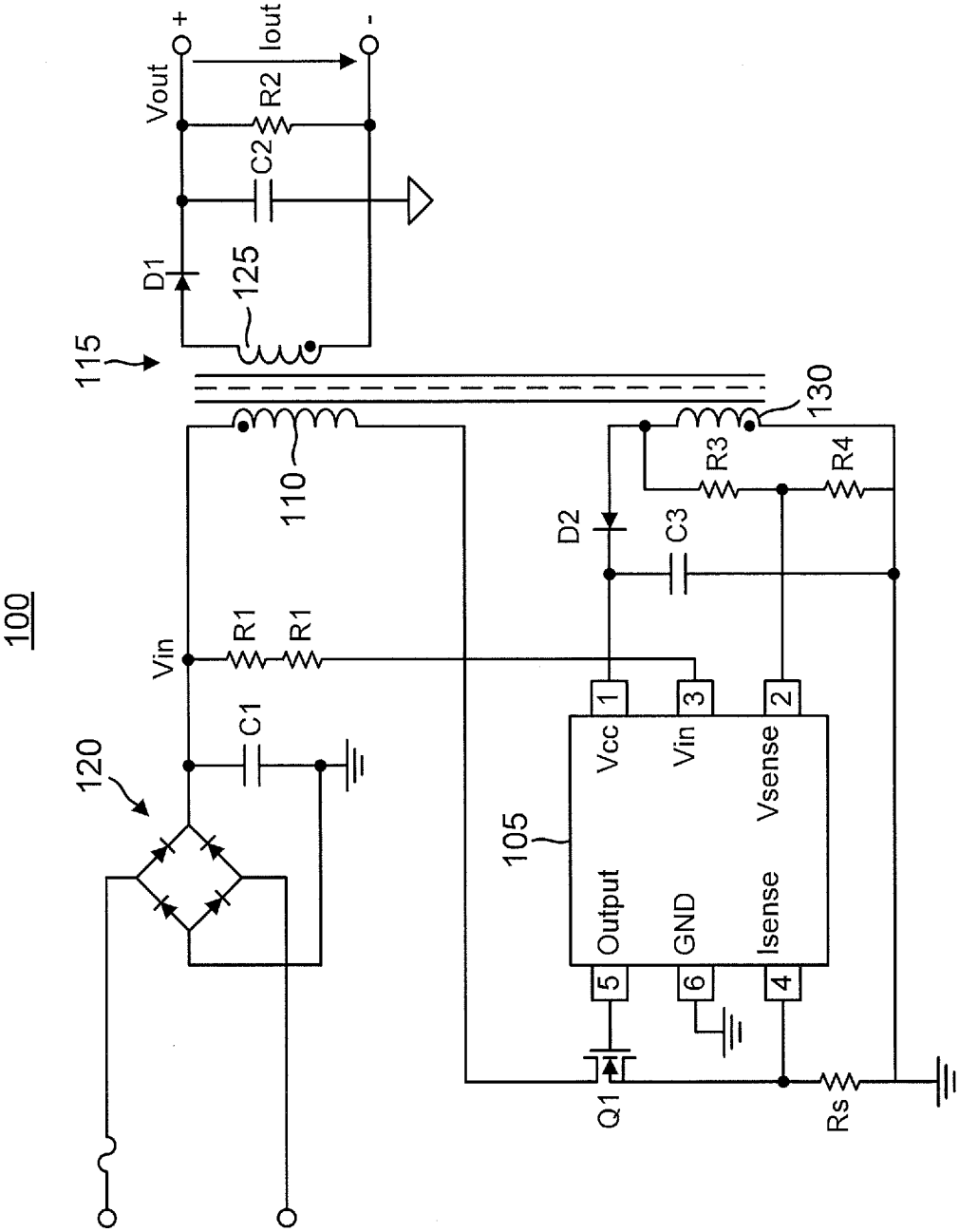


FIG. 1

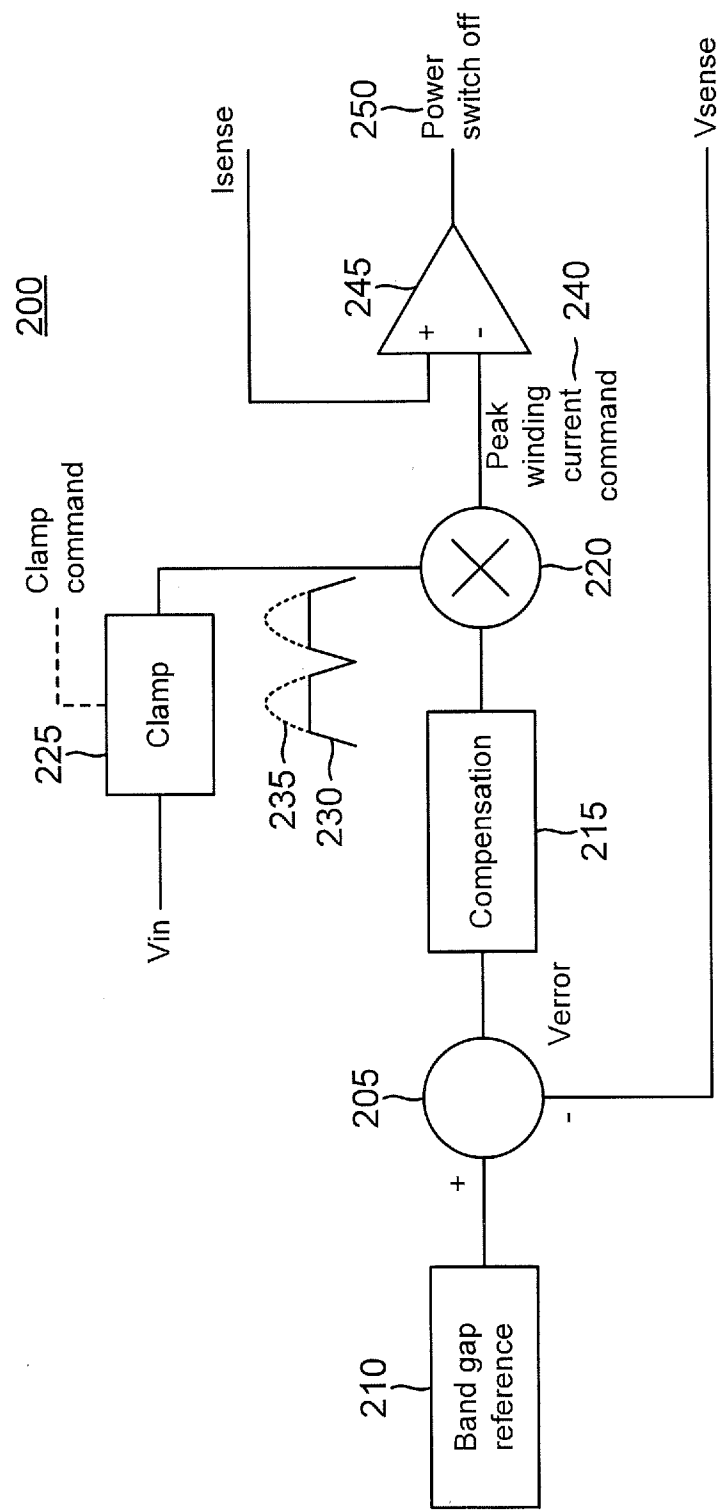


FIG. 2

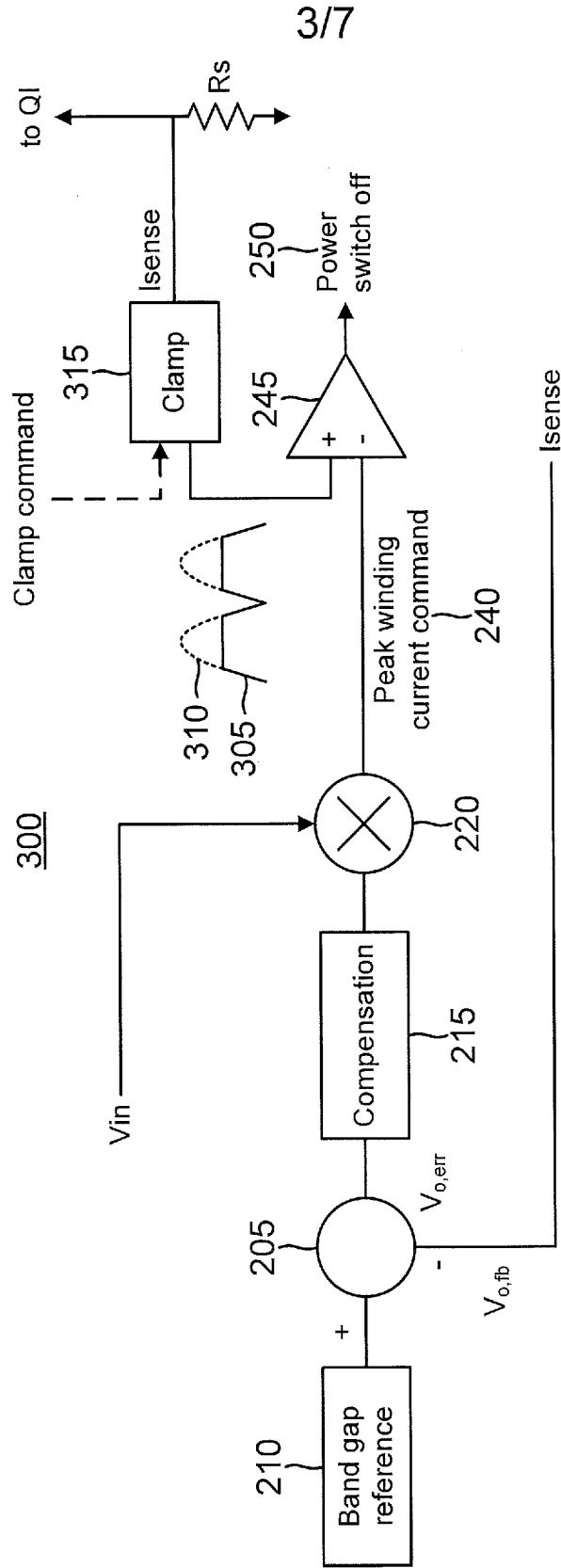


FIG. 3

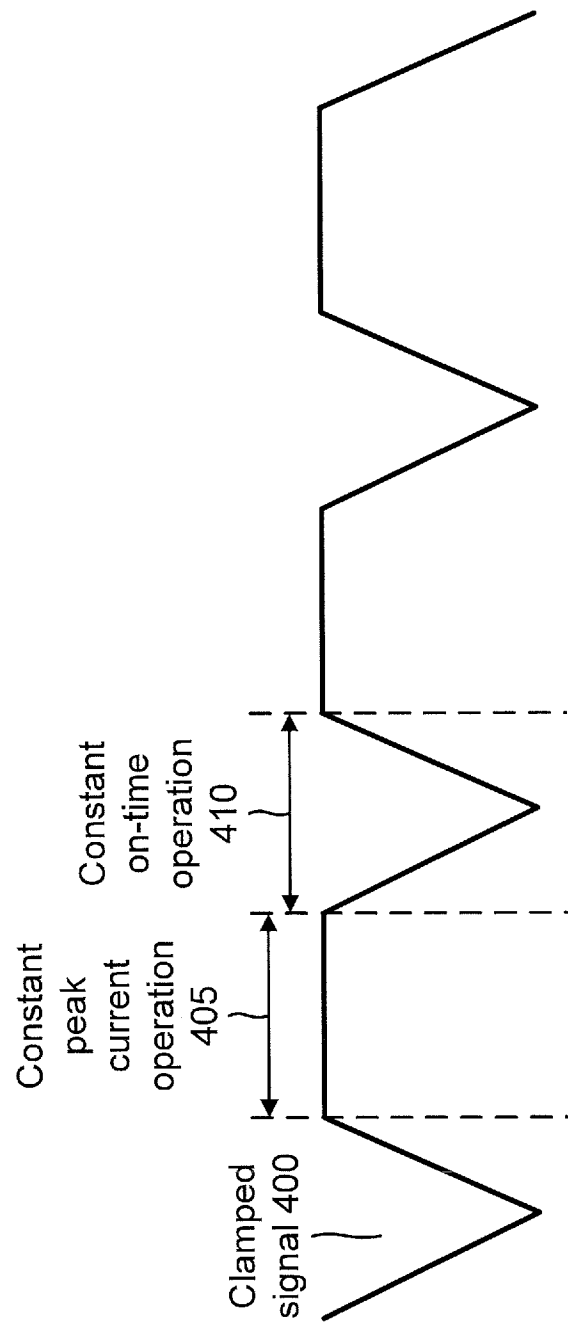


FIG. 4

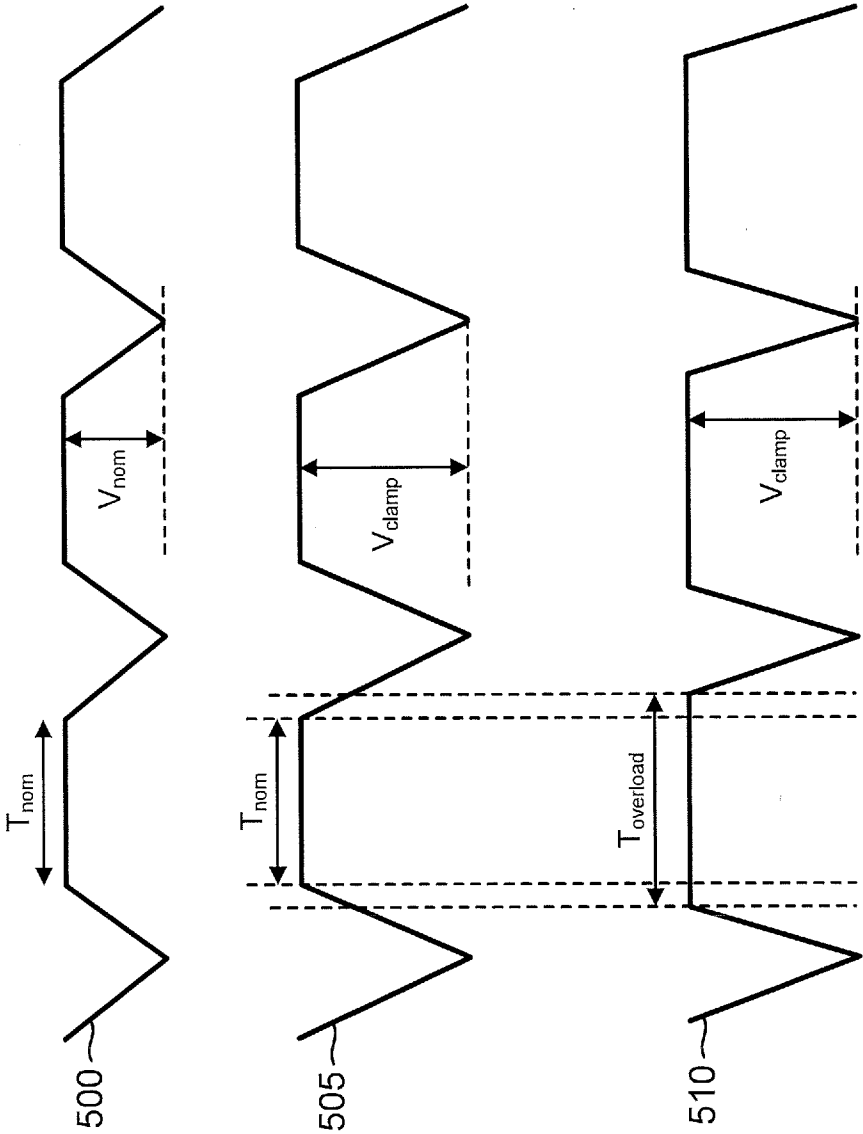


FIG. 5

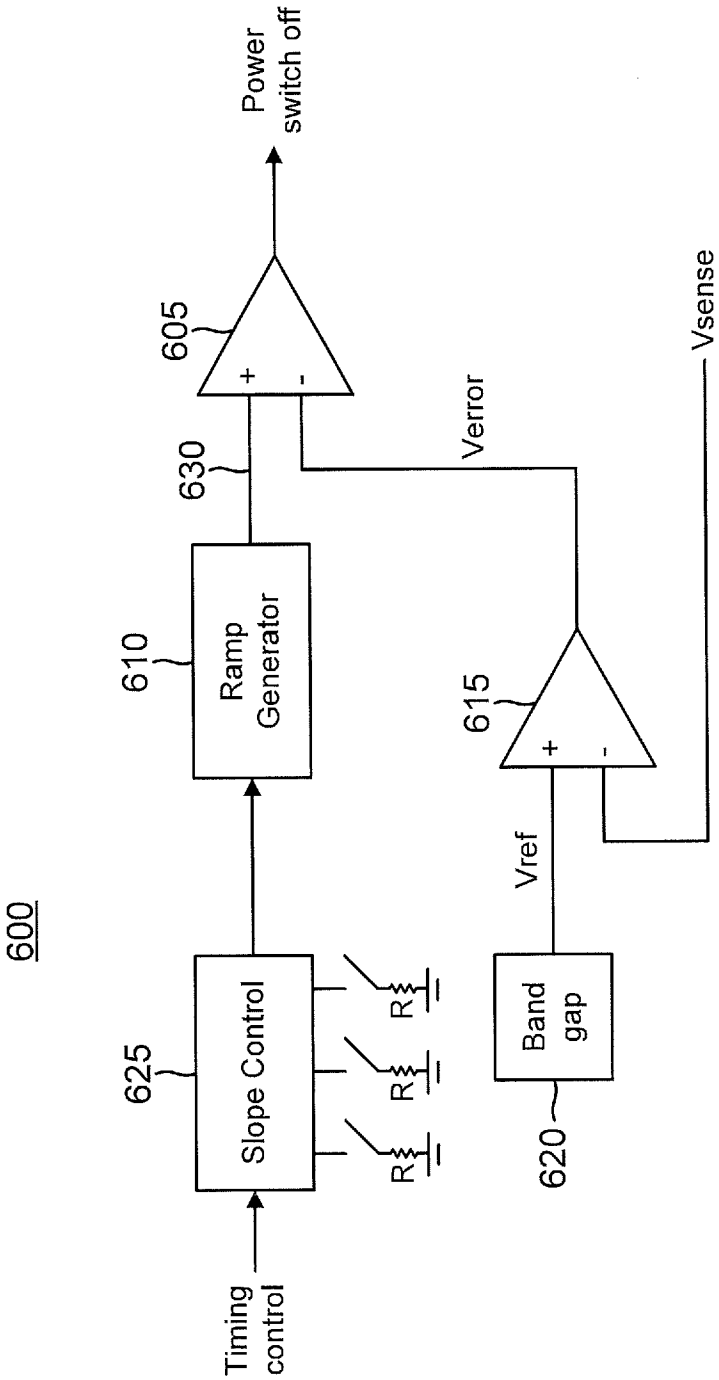


FIG. 6

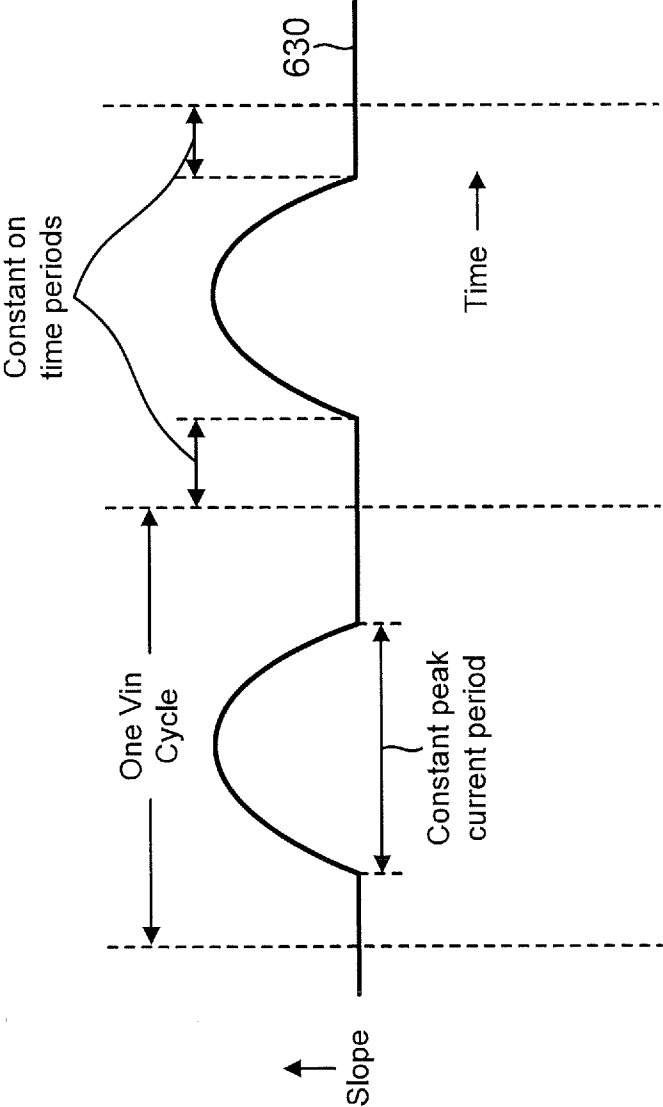


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/061053

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/42 H02M1/15
ADD. H02M1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/077370 A1 (GU LIN-LIN [CN] ET AL) 28 March 2013 (2013-03-28)	1-6, 8-10, 15-17
Y	figure 9	11-14, 18-20
A	-----	7
X	CN 102 332 814 B (SILERGY CORP) 18 December 2013 (2013-12-18)	1-6, 8-10, 15-17
Y	figures 2-7	11-14, 18-20
A	-----	7
Y	US 2005/219871 A1 (LI HONG-CHUN [TW] ET AL) 6 October 2005 (2005-10-06) figures 9, 10, 11 paragraphs [0033] - [0036] -----	11-14, 18-20
	-/-	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

Date of the actual completion of the international search

10 March 2016

Date of mailing of the international search report

18/03/2016

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Kail, Maximilian

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2015/061053

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2009/156891 A1 (NXP BV [NL]; KOOLEN GERT-JAN [NL]; VASTERINK MARTIN [NL]) 30 December 2009 (2009-12-30) figures 1-3 page 2 - page 4	11-14, 18-20
Y	----- EP 2 688 189 A1 (IWATT INC [US]) 22 January 2014 (2014-01-22) abstract; figures 1,4,5 paragraphs [0005] - [0007] -----	11-14, 18-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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			JP	5722959 B2		27-05-2015
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