MULTIPLE DATA RATE RAM MEMORY CONTROLLER

A memory controller for a multiple data rate RAM memory module is provided. Said controller comprises a PLL unit (PLL) for generating different clock phases (clk, clk90, clk180) from a reference clock (ref clk). In addition, a controllable delay unit (CDU) for delaying a strobe signal (dqs) is provided.
Multiple data rate RAM memory controller

FIELD OF THE INVENTION
The invention relates to multiple data rate RAM memory controller and a data processing system comprising such a memory controller.

BACKGROUND OF THE INVENTION
With the increasing processing speed of microprocessors the memory architecture has to improve accordingly. For example a controller for Double Data Rate (DDR) Synchronous Dynamic Random Access Memory SDRAM typically comprises an interface to standard DDR SDRAM memory devices. The controller is provided to control the access to the SDRAM and serves to deal with the bus arbitration, the command interpreting, bank-interleaving and timing. The controller instructs the DDR interface when to perform writes and reads from the DDR data bus. The interface, i.e. the DDR interface, serves to maintain the bi-directional DDR data bus and assert all addresses and command signals to the SDRAM.

In Fig. 6 a basic representation of the interface between the DDR SDRAM and the controller ASIC is shown. In particular, the well known interface signals are shown. The controller ASIC issues the clock signals clkp, clkn, the address and command signal addr/cmd and the mask signal dqm. The strobe dqs as well as the data signal dq may originate from the controller ASIC for a write command or from the SDRAM for a read command.

Fig. 7 shows the corresponding timings of the interface signals of Fig. 6. In particular, the timings of a write and a read command wrt, rd are depicted. For every clock cycle two bits per pin are transferred. The rising and falling edge of the clock signal is used to capture the data with a strobe signal dqs. This strobe has the same frequency as the clock clkp. To realize a compensation for delays the strobe dqs travels with the data. Hence, the interface can be operated at speeds up to 450 Mbit/s/pin or even higher. The strobe signal dqs is generated by the data source. Therefore, for reading data the memory device SDRAM and for writing data the controller generates the strobe signal dqs. It should be noted that the alignment between strobe signal dqs and data dq is different for read and write commands.
In Fig. 8 a schematic block diagram of the relevant parts of the DDR SDRAM controller for generating multiple clock phases according to the prior art are shown. In particular, a Phase Locked Loop PLL unit PLL and a Delay Locked Loop DLL unit DLL is depicted. The PLL unit and the DLL unit are connected in series and the PLL unit outputs the clock signal clk to the DLL unit. The DLL unit serves to remove the clock skew between a processor and the SDRAM and to generate multiple clock phases from the clock signal clk to generate the write signals as described in Figs 6 and 7 or to capture the read data. The phases required in an interface logic (not shown) are the clock signals clk, clk90 (90°), clk180 (180°), and the strobe signals dqs90 (90°), dgs270 (270°). The strobe signal DQS originates from the external memory and is only present during reading data.

The DLL unit DLL comprises a master DLL unit MDLL and a slave DLL unit SDLL. The master DLL is a DLL unit having a feedback loop and is therefore able to lock to the incoming clock signal clk of the PLL unit PLL. Accordingly, the delay of the delay line of the DLL unit will be matched to the delay of a clock period. The delay line in the slave DLL unit SDLL is then matched to the delay line in the master DLL unit MDLL.

The slave DLL unit SDLL is used to shift the incoming strobe signal DQS by 90 degrees in phase, i.e. a quarter of a clock period, such that it can be used for capturing the incoming data. As a result, the phase shift of the strobe signal is very accurately equal to a quarter of a clock period, which is vital as the timing becomes very critical.

It should be noted, that all the above shown clock phases are required in the interface logic, which consists mainly of flip-flops. This logic serves to generate the write signals and to capture the read data. As the specific purpose of the respective clock phases is not relevant for the generation thereof, a detailed description thereof will be omitted.

However, the DLL units in the solution described above consume a considerable amount of chip area and power. This is increasingly becoming a problem especially for the interface solutions for Mobile DDR SDRAM's.

It is therefore an object of the invention to provide a memory controller for a multiple data rate RAM with a reduced required chip area and a reduced power dissipation.

This object is solved by an a multiple data rate RAM memory controller according to claim 1 and a data processing system according to claim 8.

Therefore, a memory controller for a multiple data rate RAM memory module is provided. Said controller comprises a PLL unit PLL for generating different clock phases clk, clk90, clk180 from a reference clock REFCLK. In addition, a controllable delay unit CDU for delaying a strobe signal dqs is provided.
Accordingly, the different clock phases clk, clk90 and clk180 are generated
from the PLL in stead of the DLL unit as in the prior art. In addition, the prior art DLL units
are replaced by single delay elements and is therefore cheaper to implement.

According to an aspect of the invention, the delay of the controllable delay
unit CDU is matched to the delay of said PLL unit PLL. Accordingly, a cheap
implementation is realized without sacrificing the required accuracy.

According to a preferred aspect of the invention said controllable delay unit
CDU is adapted to delay a strobe signal dqs by 90 degree.

According to a further aspect of the invention said PLL unit PLL comprise a
4-phase oscillator OSC having two single delay units CDU1. Hence, the provision of the 4
phases may be implemented requiring less chip area.

According to still a further aspect of the invention said PLL unit PLL further
comprises a phase comparator COMP which outputs a control signal V_{ctrl}, wherein all delay
units CDU, CDU1 receive said control signal V_{ctrl} as input signal. Therefore, the signals in an
interface towards a DDR SDRAM can be timed accurately.

The invention also relates to a data processing system comprising one of the
above memory controller.

Further aspects of the invention are described in the dependent claims.

These and other aspects of the invention are apparent from and will be
elucidated with reference to the embodiment(s) described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a basic block diagram of the relevant parts of a DDR SDRAM
controller for generating multiple clock phases according to a first embodiment;

Fig. 2 shows a schematic block diagram of an oscillator of the PLL unit of Fig.
1;

Fig. 3 shows the timings of the oscillator of Fig. 2;

Fig. 4 shows a schematic block diagram of the relevant parts of the DDR
SDRAM controller for generating multiple clock phases according to a second embodiment;

Fig. 5 shows a schematic block diagram of a PLL unit of Fig. 1;

Fig. 6 shows a basic representation of the interface between the DDR SDRAM
and the controller;

Fig. 7 shows the corresponding timings of the interface signals of Fig. 6; and
Fig. 8 shows a schematic block diagram of the relevant parts of the DDR SDRAM controller for generating multiple clock phases according to the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 Fig. 1 shows a basic block diagram of the relevant parts of a DDR SDRAM controller for generating multiple clock phases according to a first embodiment. Such a controller is e.g. arranged between a processor and a DDR SDRAM memory module in a data processing system on a single chip or on multiple chips. The controller comprises a PLL unit PLL and a controlled delay unit CDU. These units perform the same function as the corresponding units of Fig. 8, namely to provide the different clock phases clk, clk90, and clk180 and the different phases of a strobe signal dq90, dq270, when data is read from the memory. Here, the delay of the controllable units CDU is matched to the delay of the 90 degree delay element in the PLL unit.

10 Fig. 2 shows a schematic block diagram of an oscillator OSC of the PLL unit of Fig. 1. The oscillator comprises two delay units CDU. The delay of the two controlled equal delay units CDU is controlled by the control voltage $V_{ctrl}$. Each delay unit can introduce a delay of $\frac{1}{4}T$, i.e. 90 degree with regard to the input clock clk. The frequency of the oscillator will be 4 times the delay of the single delay element CDU.

15 Fig. 3 shows the timings of the oscillator of Fig. 2. In particular, the signals at the nodes, i.e. the clock signal clk, the signal clk90 (being the clock signal shifted by 90 degrees), the signal clk180 (being the clock signal shifted by 180 degrees) and the signal clk270 (being the clock signal shifted by 270 degree), are shown.

20 Fig. 4 shows a block diagram of the relevant parts of a DDR SDRAM controller for generating multiple clock phases according to a second embodiment. Here, the oscillator OSC of Fig. 2 and a controlled delay unit CDU is shown. The purpose of this arrangement corresponds to the purpose of the arrangement of Fig. 8, namely to accurately time the signals in an interface between a processor and a DDR SDRAM memory with each other. The oscillator OSC generates the clock signals clk, clk90, clk180, clk270, i.e. the clock signal and signals shifted by 90, 180, and 270 degree, respectively. The delay unit CDU receives the control signal $V_{ctrl}$ and the strobe signal DQS as input signals and outputs dq90 and dq270. Preferably, the controlled delay unit CDU is a simple $\frac{1}{4} T$ delay unit. Hence, the incoming strobe signal is delayed to generate the dq90 and dq270 signals (being the strobe signal shifted by 90 and 270 degree), respectively. Therefore, all the phases originally shown in Fig. 8 are present. The control voltage $V_{ctrl}$ is controlled by the feedback loop in the PLL.
The buffers B1 – B7 are added to translate the differential (analog) signals of the delay units CDU in real rail-to-rail logic signals. Those signals can be used in the (not shown) interface logic mentioned above.

As the control signal $V_{ctl}$ is used for all three delay units CDU1, CDU, the delay unit CDU is matched to the delay in the PLL unit.

Fig. 5 shows a schematic block diagram of a PLL unit of Fig. 1. A phase comparator COMP and the oscillator OSC is shown. The output of the oscillator OSC, which may be implemented according to Fig. 2, is feed back to the input of the phase comparator COMP, where it is compared to a reference clock ref_clk. The phase comparator COMP outputs the control voltage $V_{ctl}$. The control voltage $V_{ctl}$ also serves as control input for the delay units CDU1, CDU.

Accordingly, the DDR SDRAM interface signals, like the strobe signal dq, can be timed accurately. Additionally, simple T/4 delay elements can be employed instead of a DLL unit as in the prior art.

In other words, a solution for the physical interface towards external DDR SDRAM memories is provided, that is more efficient in terms of power and area than existing solutions. In the physical interface usually a PLL and a number of DLL’s are required. The number of DLL’s required, depends on the width of the external interface. As one DLL is required per byte, 4 DLL’s are needed for a 32 bits interface. However, according to the invention, the DLL’s are replaced by single delay elements. Since those delay elements are more power and area efficient, this improves the efficiency of the solution. Typically, the DLL’s (and not standard delay elements) are used to achieve high timing accuracy. However, this accuracy is hardly influenced according to the invention.

Therefore, the area and power efficiency of the physical implementation of a DDR SDRAM interface is improved. The usual physical implementation comprises a PLL unit and 4 DLL units. According to the invention, the PLL unit comprises a 4-phase oscillator with single delay elements. As the DLL units are replaced by single delay units the area and power is approximately 8 times lower than that of 4 DLL units. While in the interfaces according to the prior art the DLL units are used to provide a very accurate delay of a fixed fraction of the clock period, the single delay units according to the invention are matched to the delay in the PLL unit to maintain the accuracy thereof.

The above described controller may be implemented for a Mobile DDR SDRAM as it has the same physical interface concept as a standard DDR SDRAM, namely
two bits are transferred per clock cycle, a strobe per byte is used and the alignment between strobe and data is equal.

As the prior art DLL units contains 8 comparable delay elements, 4 in the master DLL and 4 in the slave DLL, the provision of merely one delay unit results in an area gain of 8. The delay of the single delay elements that replace the DLL's is matched to a delay element in the PLL with a delay of a quarter of a clock cycle.

According to a further embodiment of the invention the arrangement and the operation of the memory controller as described in the first and second embodiment is further adapted or implemented for a Quad Data Rate QDR SRAM. For more detailed information regarding QDR memory modules please refer to http://www.qdrsramp.com.

Alternatively, the arrangement and the operation of the memory controller according to the first and second embodiment may also be implemented for other multiple data rate RAM memory controller in particular for multiple data rate SRAM memory controller.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Furthermore, any reference signs in the claims shall not be construed as limiting the scope of the claims.
CLAIMS:

1. Memory controller for a multiple data rate RAM memory module, comprising a PLL unit (PLL) for generating different clock phases (clk, clk90, clk180) from a reference clock (ref_clk); and a controllable delay unit (CDU) for delaying a strobe signal (dqs).

2. Memory controller according to claim 1, wherein said memory controller is adapted for double data rate SDRAM memory modules.

3. Memory controller according to claim 1 or 2, wherein the delay of the controllable delay unit (CDU) is matched to the delay of said PLL unit (PLL).

4. Memory controller according to claim 1, 2 or 3, wherein said controllable delay unit (CDU) is adapted to delay a strobe signal (dqs) by 90 degree.

5. Memory controller according to claim 3 or 4, wherein said PLL unit (PLL) comprise a 4-phase oscillator (OSC) having two single delay units (CDU1).

6. Memory controller according to claim 5, wherein said PLL unit (PLL) further comprises a phase comparator (COMP) which outputs a control signal (V_{ctrl}), wherein all delay units (CDU, CDU1) receive said control signal (V_{ctrl}) as input signal.

7. Memory controller according to claim 1, wherein said memory controller is adapted for quad data rate RAM memory modules.
8. Data processing system comprising a memory controller according to claims 1 – 7.
FIG. 7

FIG. 8
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G11C7/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>X</td>
<td>US 2002/190772 A1 (MOSHE DAVID ET AL) 19 December 2002 (2002-12-19) page 1, paragraph 9 - page 2, paragraph 17; figures 1-3</td>
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Further documents are listed in the continuation of box C. Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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