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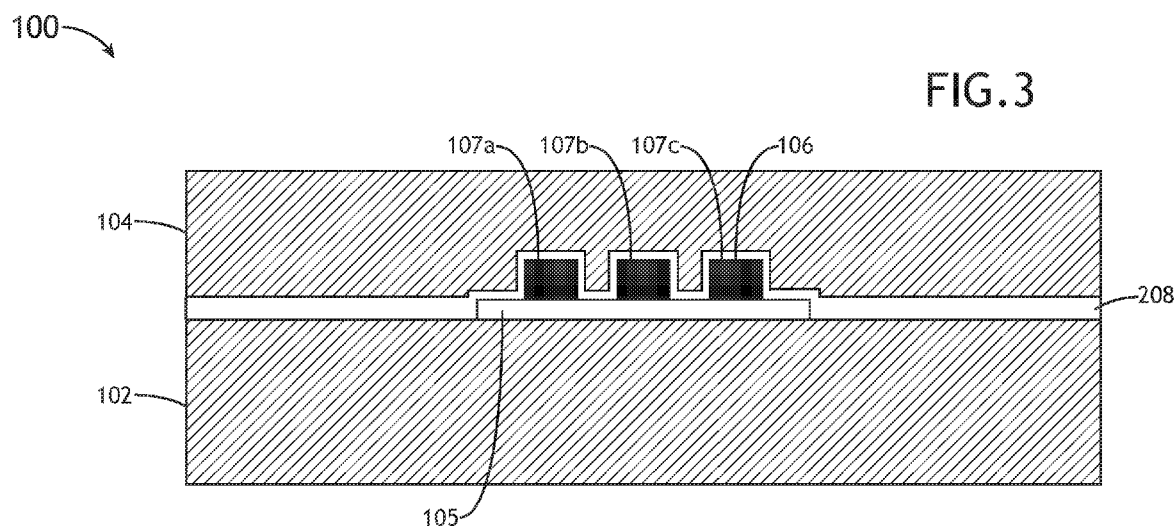
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(54) Title: PROCESS TEMPERATURE MEASUREMENT DEVICE FABRICATION TECHNIQUES AND METHODS OF CALIBRATION AND DATA INTERPOLATION OF THE SAME



(57) Abstract: A process condition measurement wafer assembly is disclosed. In embodiments, the process condition measurement wafer assembly includes a bottom substrate and a top substrate. In another embodiment, the process condition measurement wafer assembly includes one or more electronic components disposed on one or more printed circuit elements and interposed between the top substrate and bottom substrate. In another embodiment, the process condition measurement wafer assembly includes one or more shielding layers formed between the bottom substrate and the top substrate. In embodiments, the one or more shielding layers are configured to electromagnetically shield the one or more electronic components and diffuse voltage potentials across the bottom substrate and the top substrate.



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***PROCESS TEMPERATURE MEASUREMENT DEVICE FABRICATION TECHNIQUES
AND METHODS OF CALIBRATION AND DATA INTERPOLATION OF THE SAME***

CROSS-REFERENCE TO RELATED APPLICATION

[0002] The present application claims priority under 35 U.S.C. § 119(e) to United States Provisional Patent Application Serial No. 62/727,633 entitled PROCESS TEMPERATURE MEASUREMENT DEVICE FABRICATION TECHNIQUES AND METHODS OF CALIBRATION AND DATA INTERPOLATION OF THE SAME, filed September 6, 2018, naming Farhat A. Quli, Andrew Nguyen, and James Richard Bella as inventors, which is incorporated herein by reference in the entirety.

TECHNICAL FIELD

[0003] The present invention generally relates to monitoring of wafers along a semiconductor process line, and, in particular, to a system and method for a process condition measurement wafer assembly.

BACKGROUND

[0004] As tolerances on process conditions in semiconductor device processing environments continue to narrow, the demand for improved process monitoring systems continues to increase. Thermal uniformity within a processing system is one such condition. Current methods are unable to monitor temperature under the extreme conditions (e.g., high temperature) required of current processing techniques without contaminating the associated chamber. One previous approach to monitoring process conditions involves the use of a process condition measurement wafer. Conventional process condition measurement wafers may include wireless data acquisition systems which measure and record process conditions, such as temperature. However, conventional process condition measurement wafers are often subject to temperature inaccuracies attributable to internal construction variation, and may not be able to withstand the energy flux of current and future processing systems (e.g., epitaxy chambers, plasma etch chambers). Therefore, it would be desirable to provide a system

and method to allow for high temperature measurement using an instrumented wafer to monitor the conditions of a semiconductor device processing line.

SUMMARY

[0005] A process condition measurement wafer assembly is disclosed. In embodiments, the process condition measurement wafer assembly includes a bottom substrate and a top substrate. In another embodiment, the process condition measurement wafer assembly includes one or more electronic components disposed on one or more printed circuit elements and interposed between the top substrate and bottom substrate. In another embodiment, the process condition measurement wafer assembly includes one or more shielding layers formed between the bottom substrate and the top substrate. In embodiments, the one or more shielding layers are configured to electromagnetically shield the one or more electronic components and diffuse voltage potentials across the bottom substrate and the top substrate.

[0006] A process condition measurement wafer assembly is disclosed. In embodiments, the process condition measurement wafer assembly includes a bottom substrate and a top substrate. In another embodiment, the process condition measurement wafer assembly includes one or more electronic components disposed on one or more printed circuit elements and interposed between the top substrate and the bottom substrate. In another embodiment, at least one of the bottom substrate or the top substrate are configured to electromagnetically shield the one or more electronic components and diffuse voltage potentials across the bottom substrate and the top substrate.

[0007] A method is disclosed. In embodiments, the method may include: acquiring, under isothermal conditions, a set of temperature measurements from a set of temperature sensors and a set of heat flux measurements from a set of heat flux sensors distributed across a process condition measurement wafer; calibrating the set of temperature measurements and the set of heat flux measurements acquired under isothermal conditions; apply a known heat flux to the process condition measurement wafer; acquiring, during application of the known heat flux, an additional set of

temperature measurements from the set of temperature sensors and an additional set of heat flux measurements from the set of heat flux sensors; identifying temperature variation observed across the set of temperature sensors during application of the known heat flux; identifying a heat flux-temperature variation relationship by correlating the known heat flux with the identified temperature variation of the set of temperature sensors; acquiring, under unknown heat flux conditions, a test set of temperature measurements from the set of temperature sensors and a test set of heat flux measurements from the heat flux sensors; and adjusting the test set of temperature measurements based on the test set of heat flux measurements and the identified heat flux-temperature variation relationship.

[0008] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not necessarily restrictive of the invention as claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The numerous advantages of the disclosure may be better understood by those skilled in the art by reference to the accompanying figures in which:

[0010] FIG. 1A is a simplified cross-sectional view of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0011] FIG. 1B is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0012] FIG. 1C is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0013] FIG. 1D is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0014] FIG. 1E is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0015] FIG. 1F is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0016] FIG. 2A is a simplified cross-sectional view of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0017] FIG. 2B is a simplified cross-sectional view of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0018] FIG. 3 is a simplified cross-sectional view of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0019] FIG. 4A is a simplified cross-sectional view of a process condition measurement wafer assembly communicatively coupled to a remote data system, in accordance with one or more embodiments of the present disclosure.

[0020] FIG. 4B is a simplified block diagram view of a process condition measurement wafer assembly communicatively coupled to a remote data system, in accordance with one or more embodiments of the present disclosure.

[0021] FIG. 5 is a simplified cross-sectional view of a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

[0022] FIG. 6 is a flowchart of a method for calculating temperatures across a process condition measurement wafer assembly, in accordance with one or more embodiments of the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

[0023] Reference will now be made in detail to the subject matter disclosed, which is illustrated in the accompanying drawings.

[0024] Referring generally to FIGS. 1A through 5, a system and method for a process condition measurement wafer assembly is shown and described, in accordance with one or more embodiments of the present disclosure.

[0025] Conventional process condition measurement wafers include measurement electronics disposed between silicon wafers. The silicon wafers are designed to shield the measurement electronics from extreme conditions (e.g., high RF, high heat flux, high electromagnetic radiation) within process chambers. The silicon wafers within these conventional process condition measurement wafers are typically coupled via one or more discrete ohmic contacts between the respective silicon wafers. However, these ohmic contacts result in high current density within and around the contacts, and may result in high potentials across the process condition measurement wafers. Additionally, complex internal construction of conventional process condition measurement wafers may further result in temperature inaccuracies due to the internal construction of the wafers themselves.

[0026] Accordingly, embodiments of the present disclosure are directed to a system and method which cure one or more of the shortfalls of the previous approaches identified above. Embodiments of the present disclosure are directed to a process condition measurement wafer assembly which improves the accuracy, precision, and construction of wafer-based process condition measurement devices. Additional embodiments of the present disclosure are directed to a process condition measurement wafer assembly including one or more electromagnetic shielding layers disposed between a top substrate

and a bottom substrate. Further embodiments of the present disclosure are directed to a process condition measurement wafer assembly including one or more thermal pillars configured to facilitate heat transfer throughout the apparatus.

[0027] Embodiments of the present disclosure are directed to a process condition measurement wafer assembly capable of operating up to high temperature (e.g., 600 °C to 800 °C). Such a process condition measurement wafer assembly may be utilized with semiconductor processing chambers (e.g., epitaxy chamber, plasma etch chamber) operating at high temperature. In some embodiments, the process condition measurement wafer assembly of the present disclosure includes a top substrate, a bottom substrate, and one or more shielding layers, whereby the on-board electronic components (e.g., sensors, processors, memory, power supply) and/or other sensitive devices are interposed between the top substrate and the bottom substrate, and shielded by the one or more shielding layers. The use of an instrumented substrate is described in U.S. Patent Application No. 15/277,753, filed on September 27, 2016, which is incorporated herein by reference in the entirety. Instrumented substrates are described in further detail in U.S. Patent No. 7,540,188 B2, filed May 1, 2016 entitled PROCESS CONDITION MEASURING DEVICE WITH SHIELDING, and in U.S. Patent Application No. 15/277,792, filed September 27, 2016 entitled ENCAPSULATED INSTRUMENTED SUBSTRATE APPARATUS FOR ACQUIRING MEASUREMENT PARAMETERS IN HIGH TEMPERATURE PROCESS APPLICATIONS, both of which are incorporated herein by reference in the entirety.

[0028] FIG. 1A is a simplified cross-sectional view of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure. The process condition measurement wafer assembly 100 may include, but is not limited to, a top substrate 104 and a bottom substrate 102. The process condition measurement wafer assembly 100 may include one or more electronic components 106.

[0029] As shown in FIG. 1A, the top substrate 104 may be mechanically coupled to the bottom substrate 102. The top substrate 104 and/or the bottom substrate 102 of the process condition measurement wafer assembly 100 may include any substrate known

in the art. In some embodiments, the top substrate 104 and/or the bottom substrate 102 of the process condition measurement wafer assembly 100 may include a wafer. For example, the top substrate 104 and/or the bottom substrate 102 may include, but are not limited to, a semiconductor substrate, a glass wafer (e.g., fused silica glass wafer, borosilicate glass wafer), a crystalline wafer (e.g., crystalline quartz wafer, silicon wafer), a wafer formed from one or more compounds (e.g., silicon carbide, silicon nitride), and the like. For instance, the process condition measurement wafer assembly 100 may include any substrate causing negligible contamination in a semiconductor processing environment, such as, but not limited to, a wafer formed from one or more of silicon, silicon carbide, silicon nitride, gallium nitride, gallium arsenide, germanium, gallium, indium, or silicon dioxide (e.g., quartz).

[0030] In one embodiment, the process condition measurement wafer assembly 100 may include one or more cavities 107 between the top substrate 104 and the bottom substrate 102. For example, as shown in FIG. 1A, the process condition measurement wafer assembly 100 may include a cavity 107 within the bottom substrate 102. It is noted herein that the process condition measurement wafer assembly 100 may include one or more cavities 107 within the top substrate 104 and/or the bottom substrate 102. For example, a cavity 107 may include a portion of a cavity 107 within the top substrate 104, and a portion of a cavity 107 within the bottom substrate 102.

[0031] In another embodiment, the one or more electronic components 106 may be interposed between the top substrate 104 and the bottom substrate 102. For example, as shown in FIG. 1A, the one or more electronic components 106 may be disposed within the one or more cavities 107. In embodiments, the one or more electronic components 106 are disposed between the top substrate 104 and the bottom substrate 102 such that the one or more electronic components 106 are sealed (e.g., hermetically sealed) between the top substrate 104 and the bottom substrate 102. The one or more electronic components 106 may include any electronic components which are configured to monitor process conditions within a process system (e.g., epitaxy chamber, plasma etch chamber). In this regard, the one or more electronic components 106 may include any

electronic components known in the art including, but not limited to, sensor devices (e.g., temperature sensors, pressure sensors, chemical sensors, radiation sensors, heat flux sensors, voltage sensors), a power source, one or more processors, a memory, communication circuitry, and the like.

[0032] In some embodiments, a plurality of electronic components 106 may be communicatively coupled to one another within the process condition measurement wafer assembly 100. In another embodiment, the one or more electronic components 106 may be disposed on one or more printed circuit elements 105 interposed between the top substrate 104 and the bottom substrate 102. In this regard, the one or more electronic components 106 may be communicatively coupled via the one or more printed circuit elements 105. The one or more printed circuit elements 105 may include any electronic components known in the art including, but not limited to, a printed circuit board, a printed wiring board, and the like. Similarly, the one or more printed circuit elements 105 may be formed from any material known in the art including, but not limited to, a ceramic, silicon, an inorganic material, and the like.

[0033] FIG. 1B is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure.

[0034] As noted previously herein, the top substrate 104 and the bottom substrate 102 may be mechanically coupled to one another. In some embodiments, the process condition measurement wafer assembly 100 may further include one or more shielding layers 108. The one or more shielding layers 108 may be formed between the top substrate 104 and the bottom substrate 102. For example, the one or more shielding layers 108 may include one or more films disposed/deposited on a surface of the top substrate 104 and/or bottom substrate 102. For instance, as shown in FIG. 1B, the one or more shielding layers 108 may be disposed across at least a portion of an upper surface of the bottom substrate 102 and/or across at least a portion of a lower surface of the top substrate 104.

[0035] It is contemplated herein that the one or more shielding layers 108 may include any layers/films known in the art configured to electromagnetically shield the one or more electronic components 106 and/or diffuse voltage potentials across the top substrate 104 and/or bottom substrate 102. In some embodiments, the one or more shielding layers 108 may be formed from an electrically conductive material. In additional and/or alternative embodiments, the one or more shielding layers 108 may include a light-blocking film. In this regard, the one or more shielding layers 108 may include one or more opaque films. For example, the one or more shielding layers 108 may include, but is not limited to, a material that is absorptive of radiation traversing the top substrate 104 to the bottom substrate 102.

[0036] The one or more shielding layers 108 may be further understood with reference to FIGS. 1C-1F.

[0037] FIG. 1C is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure. As shown in FIG. 1C, the one or more shielding layers 108 may include, but are not limited to, an adhesive layer 110 and a plurality of conductive particles 112.

[0038] In some embodiments, a shielding layer 108 formed between at least a portion of the top substrate 104 and the bottom substrate 102 may include an adhesive layer 110. The adhesive layer 110 may be formed from any adhesive material known in the art configured to mechanically couple substrates. In another embodiment, the shielding layer 108 may include conductive particles 112 suspended within the adhesive layer 110. For example, as shown in FIG. 1C, the shielding layer 108 may include a plurality of conductive particles 112 suspended within an adhesive layer 110. In some embodiments, the conductive particles 112 may be distributed evenly throughout the adhesive layer 110. In embodiments, the inclusion of conductive particles 112 within the shielding layer 108 may create electrical contact between at least a portion of the top substrate 104 and at least a portion of the bottom substrate 102. Accordingly, the conductive particles 112 may be formed using any conductive material known in the art. Similarly, the adhesive layer

110 may be formed from an electrically conductive material in order to further facilitate electrical contact between the top substrate 104 and the bottom substrate 102.

[0039] It is contemplated herein that the inclusion of conductive particles 112 within the shielding layer 108 may create electrical contact between the top substrate 104 and the bottom substrate 102, and/or between conductive layers deposited on these respective substrates. These electrical contacts may facilitate the diffusion of voltage potentials throughout the process condition measurement wafer assembly 100 and/or between the top substrate 104 and the bottom substrate 102. Furthermore, these electrical contacts and conductive particles/layers may provide electrical and electromagnetic shielding to the electronic components 106 of the process condition measurement wafer assembly 100.

[0040] FIG. 1D is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure. As shown in FIG. 1D, the one or more shielding layers 108 may include, but are not limited to, an adhesive layer 110 and a plurality of conductive electrically conductive structures 114.

[0041] In additional and/or alternative embodiments, electrical contact between portions of the top substrate 104 and the bottom substrate 102 may be facilitated by the use of conductive electrically conductive structures 114. For example, as shown in FIG. 1D, a plurality of electrically conductive structures 114 may be fabricated on a surface of at least one of the top substrate 104 or bottom substrate 102 such that the electrically conductive structures 114 electrically couple at least a portion of the top substrate 104 and at least a portion of the bottom substrate 102. The plurality of electrically conductive structures 114 may include any shape or type of electrically conductive structures known in the art. For example, the plurality of electrically conductive structures 114 may include a plurality of protrusions formed on a surface of at least one of the top substrate 104 or the bottom substrate 102. By way of another example, the plurality of electrically conductive structures 114 may include a plurality of conic sections (e.g., cones) and/or bumps formed

on a surface of the top substrate 104 and/or a surface of the bottom substrate 102. The plurality of electrically conductive structures 114 may be formed using any material known in the art including, but not limited to, one or more conductive metals.

[0042] The plurality of conductive electrically conductive structures 114 may be formed/fabricated on a surface of the top substrate 104 and/or bottom substrate 102 using any technique known in the art. For example, the electrically conductive structures 114 may be deposited onto a surface of the top substrate 104 and/or bottom substrate 102 through an electroplating process or a wire bond bumping process. In another embodiment, the adhesive layer 110 may be formed around the plurality of electrically conductive structures 114.

[0043] FIG. 1E is a simplified cross-sectional view of a portion of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure.

[0044] In one embodiment, the one or more shielding layers 108 are formed via direct wafer-to-wafer bonding. For example, as shown in FIG. 1E, the one or more shielding layers 108 may be formed via an adhesive-less silicon-to-silicon bonding between the top substrate 104 and the bottom substrate 102. In some embodiments, the top substrate 104 and/or the bottom substrate 102 may serve as the one or more shielding layers 108. Thus, the top substrate 104 and/or the bottom substrate 102 may be configured as the one or more shielding layers 108. In this regard, the top substrate 104 and/or the bottom substrate 102 may serve to electromagnetically shield the one or more electronic components 106 and diffuse voltage potentials in addition to, or in lieu of, the one or more shielding layers 108. For example, as shown in FIG. 1E, the top substrate 104 direct bonded to the bottom substrate 102 may include a doped silicon substrate such that the top substrate 104 serves as a shielding layer 108.

[0045] It is contemplated herein that shielding layers 108 formed via direct wafer-to-wafer bonding (e.g., silicon-to-silicon bonding) may be carried out with one or more

intermediate films 116 interposed between the top substrate 104 and the bottom substrate 102.

[0046] In some embodiments, the as shown in FIG. 1F, one or more shielding layers 108 of the process condition measurement wafer assembly 100 include one or more intermediate films 116 and one or more metal contacts 118. It is contemplated herein that electrical coupling between the top substrate 104 and the bottom substrate 102 may be further facilitated with direct metal-to-metal thermo-compression bonding at discrete locations in order to improve conductivity. Accordingly, conductivity may be improved through the inclusion of one or more additional metal contacts 118 within the adhesive-less silicon-to-silicon bonding. For example, as shown in FIG. 1F, the one or more intermediate films 116 interposed between the top substrate 104 and the bottom substrate 102 may include a plurality of metal contacts 118. By way of another example, the one or more intermediate films 116 may include one or more metal film layers in order to improve electrical coupling between the top substrate 104 and the bottom substrate 102.

[0047] In additional and/or alternative embodiments, the one or more shielding layers 108 may include one or more films deposited on at least one of the top substrate 104 or the bottom substrate 102 via a transient liquid phase bonding process. For example, metal films deposited on a surface of the top substrate 104 and the bottom substrate 102 may react with one another to form an alloy in order to form the one or more shielding layers 108 and bond the top substrate 104 and bottom substrate 102.

[0048] FIG. 2A is a simplified cross-sectional view of a process condition measurement wafer assembly 100. The process condition measurement wafer assembly 100 may include, but is not limited to, a top substrate 104, a bottom substrate 102, one or more electronic components 106, one or more printed circuit elements 105, and one or more layers 208. It is noted herein that the one or more layers 208 may include one or more adhesive layers and/or one or more shielding layers 108 discussed previously herein with respect to FIGS. 1B-1F.

[0049] As noted previously herein, one issue associated with conventional process condition measurement wafers is poor thermal management and the build-up of heat, which may lead to the failure of electronic components, adhesive layers, or both. For example, as shown in FIG. 2A, a process condition measurement wafer assembly 100 may be exposed to a high heat flux 202. While efficient thermal conductivity pathways may exist between direct couplings of the top substrate 104 and the bottom substrate 102, thermal conductivity pathways may be substantially diminished in locations with electronic components 106 and/or printed circuit elements 105 interposed between the top substrate 104 and the bottom substrate 102. These diminished thermal conductivity pathways may therefore result in high-temperature areas 203 and the build-up of heat, as shown in FIG. 2A.

[0050] Accordingly, some embodiments of the present disclosure are directed to a process condition measurement wafer assembly 100 with improved thermal management construction in order to improve the thermal robustness of the process condition measurement wafer assembly 100. This may be further understood with reference to FIG. 2B.

[0051] FIG. 2B is a simplified cross-sectional view of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure.

[0052] In some embodiments, the process condition measurement wafer assembly 100 may include one or more thermal pillar structures 206a, 206b configured to facilitate efficient thermal conductivity pathways between at least a portion of the top substrate 104 and at least a portion of the bottom substrate 102. For example, the one or more thermal pillar structures 206a, 206b may be machined into at least one of the top substrate 104 or the bottom substrate 102. By way of another example, the one or more thermal pillar structures 206a, 206b may be metal plated onto at least one of the top substrate 104 or the bottom substrate 102. In embodiments, the one or more printed circuit elements 105 may include one or more ports, holes, or apertures configured to receive the one or more pillar structures 206a, 206b. Accordingly, the one or more pillar structures 206a, 206b

may be configured to create efficient thermal conductivity pathways from the top substrate 104 to the bottom substrate 102 through one or more ports (e.g., holes, apertures, or the like) within the printed circuit elements 105. The one or more pillar structures 206a, 206b may be formed from any material known in the art including, but not limited to, semiconductor materials, metal materials, or the like. For example, the one or more pillar structures 106a, 206b may include silicon pillars, conductive metal pillars, and the like.

[0053] FIG. 3 is a simplified cross-sectional view of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure. The process condition measurement wafer assembly 100 may include, but is not limited to, a top substrate 104, a bottom substrate 102, one or more electronic components 106, one or more printed circuit elements 105, and one or more layers 208. It is noted herein that the one or more layers 208 may include one or more adhesive layers and/or one or more shielding layers 108 discussed previously herein with respect to FIGS. 1B-1F.

[0054] In one embodiment, the one or more printed circuit elements 105 may be coupled to at least one of the top substrate 104 or the bottom substrate 102. For example, the one or more printed circuit elements 105 may be brazed and/or direct bonded to at least one of the top substrate 104 or the bottom substrate 102. For instance, as noted previously herein, an inorganic printed circuit element 105 may be direct bonded to the bottom substrate 102. It is noted herein that direct bonding the one or more printed circuit elements 105 to the top substrate 104 and/or the bottom substrate may improve thermal conductivity and thermal management of the process condition measurement wafer assembly 100.

[0055] FIG. 4A is a simplified cross-sectional view of a process condition measurement wafer assembly 100 communicatively coupled to a remote data system 402, in accordance with one or more embodiments of the present disclosure. FIG. 4B is a simplified block diagram view of a process condition measurement wafer assembly

communicatively coupled to a remote data system, in accordance with one or more embodiments of the present disclosure.

[0056] In some embodiments, as noted previously herein, the process condition measurement wafer assembly 100 includes one or more electronic components 106, which may include one or more sensors. In another embodiment, one or more electronic components 106 may be disposed at one or more locations across the printed circuit elements 105 and communicatively coupled to one another via one or more wireline and/or wireless connections. The one or more electronic components 106 may include, but are not limited to, communication circuitry 410, one or more processors 412, a memory 414, one or more sensors 416, and a power supply 418. In some embodiments, the power supply 418 may include any power source known in the art including, but not limited to, batteries, wirelessly rechargeable batteries, and the like.

[0057] For the purposes of the present disclosure, the term 'processor' may be broadly defined to encompass any device having one or more processors (e.g., CPU) or logic elements (e.g., ASICs), which execute instructions from an internal or external memory 414. In this sense, the one or more processors 412 may include any microprocessor-type or logic device configured to execute algorithms and/or instructions. It should be recognized that the steps described throughout the present disclosure may be carried out by a single processor 412, or, alternatively, multiple processors 412. The memory 414 may include a read-only memory, a random-access memory, a solid-state drive, flash, EPROM, EEPROM, and the like.

[0058] In embodiments, the one or more processors 412 are configured to execute a set of program instructions stored in memory 414, the set of program instructions configured to cause the one or more processors 412 to carry out various steps/functions of the present disclosure. For example, the one or more processors 412 may be configured to: generate one or more control signals configured to cause the one or more sensors 416 to acquire one or more measurement parameters; store acquired measurement parameters in memory 414; calculate one or more values based on the one or more measurement parameters; and transmit the one or more measurement parameters and/or

the one or more determined values to a remote data system 402 via the communication circuitry 410. Each of these steps will be addressed herein.

[0059] In one embodiment, the one or more processors 412 of the process condition measurement wafer assembly 100 are configured to generate one or more control signals configured to cause the one or more sensors 416 to acquire one or more measurement parameters. In this regard, the one or more sensors 416 located at one or more locations within the process condition measurement wafer assembly 100/printed circuit elements 105 may be configured to acquire one or more measurement parameters (e.g., thermocouple voltage, resistance from resistance temperature device, voltage/signal from a pressure sensor, voltage/signal from a radiation sensor, voltage/signal from a chemical sensor, and the like). It is noted herein that the one or more sensors 416 may be configured to acquire measurement parameters associated with any parameter or characteristic which is to be monitored throughout a processing system (e.g., temperature, heat flux, pressure, and the like).

[0060] It is noted that the one or more sensors 416 may be formed so as to have any shape and be distributed in any manner across the process condition measurement wafer assembly 100 (e.g., across the bottom substrate 102). In this regard, the one or more sensors 416 may be selectively distributed across the process condition measurement wafer assembly 100 so as to acquire measurement parameters in the selected locations associated with each sensor 416. It is further contemplated herein that the one or more sensors 416 may include discrete sensor devices, and/or may be integrated into the top substrate 104 and/or bottom substrate 102.

[0061] It is further noted that the one or more sensors 416 may include any measurement device known in the art. For example, the one or more sensors 416 may include, but are not limited to, a thermal/temperature sensor, a pressure sensor, a radiation sensor, a chemical sensor, a voltage sensor, a heat flux sensor, and the like. For instance, in the case of temperature measurements, the one or more sensors 416 may include, but are not limited to, one or more thermocouple (TC) devices (e.g., thermoelectric junction) or one or more resistance temperature devices (RTDs) (e.g., thin

film RTD). In another instance, in the case of pressure measurements, the one or more sensors 416 may include, but are not limited to, a piezoelectric sensor, a capacitive sensor, an optical sensor, a potentiometric sensor and the like. In another instance, in the case of radiation measurements, the one or more sensors 416 may include, but are not limited to, one or more light detectors (e.g., photovoltaic cell, photoresistor and the like) or other radiation detectors (e.g., solid state detector). In another instance, in the case of chemical sensors, the one or more sensors 416 may include, but are not limited to, one or more chemiresistors, gas sensors, pH sensors and the like.

[0062] In another embodiment, the one or more processors 412 of the process condition measurement wafer assembly 100 are configured to store acquired measurement parameters in memory 414.

[0063] In another embodiment, the one or more processors 412 of the process condition measurement wafer assembly 100 are configured to calculate one or more values based on the one or more acquired measurement parameters. The one or more processors 412 may be configured to calculate any value known in the art based on the acquired measurement parameters. For example, in the case of temperature, the one or more sensors 416 may be configured to acquire thermocouple voltages (measurement parameters) indicative of temperature, and the one or more processors 412 may be configured to calculate a temperature based on the thermocouple voltages.

[0064] In another embodiment, the one or more processors 412 of the process condition measurement wafer assembly 100 are configured to transmit the one or more measurement parameters and/or the one or more determined values to a remote data system 402 via the communication circuitry 410. In this regard, the one or more electronic components 106 of the process condition measurement wafer assembly 100 may be communicatively coupled to a remote data system 402 via communication circuitry 410. The one or more electronic components 106 of the process condition measurement wafer assembly 100 may be communicatively coupled to a remote data system 402 using any wireline or wireless communication protocols known in the art.

[0065] In embodiments, the one or more electronic components 106 of the process condition measurement wafer assembly 100 may be wirelessly communicatively coupled to the remote data system 402. The one or more electronic components 106 may be wirelessly communicatively coupled to the remote data system 402 in any suitable manner. The communication circuitry 410 may include any communication circuitry and/or communication device known in the art of communication. For instance, the communication circuitry 410 may include, but is not limited to, one or more communication antennas (e.g., communication coil).

[0066] In one embodiment, the communication circuitry 410 is configured to establish a communication link between the process condition measurement wafer assembly 100 and the off-substrate remote data system 402. Further, the communication circuitry 410 may be communicatively coupled to the one or more processors 412, memory 414, one or more sensors 416, and power supply 418. In this regard, the one or more processors 412 may be configured to generate one or more control signals configured to cause the communication circuitry 410 to transmit the one or more measurement parameters and/or the one or more determined values to the remote data system 402.

[0067] In one embodiment, the remote data system 402 includes communication circuitry 404 suitable for establishing the communication link between the on-substrate communication circuitry 410 and the remote data system 402. For example, the communication circuitry 404 may establish the communication link between the on-substrate communication circuitry 410 and the remote data system 402 using a radio frequency (RF) signal, 3G, 4G, 4G LTE, 5G, WiFi protocols, Bluetooth protocols, and the like.

[0068] As discussed previously herein, the one or more processors 412 of the process condition measurement wafer assembly 100 may be configured to determine values associated with the acquired measurement parameters. In additional and/or alternative embodiments, values associated with the acquired measurement parameters may be determined/calculated by one or more processors 420 of the remote data system 402. For example, the communication circuitry 410 may transmit acquired measurement

parameters to the remote data system 402, and the one or more processors 420 of the remote data system 402 may calculate one or more values based on the acquired measurement parameters acquired by the sensors 416.

[0069] In another embodiment, the remote data system 402 may be configured to map (or correlate) the one or more values calculated by the processors 412 and/or the remote data system 402 based on the one or more measurement parameters acquired by sensors 416. The remote data system 402 may be configured to map (or correlate) the one or more values to the position of acquisition on the process condition measurement wafer assembly 100 (e.g., "measurement locations"). In another embodiment, the remote data system 402 reports the mapped values to a user interface. For example, the remote data system 402 may report mapped values to one or more of a desktop computer, laptop, tablet, handheld device, memory, or a server.

[0070] As noted previously herein, some conventional process condition measurement wafers are often subject to temperature inaccuracies attributable to internal construction variation. For example, with conventional process condition measurement wafers, temperature readings (e.g., measurement parameters) may be collected at 65 discreet locations across wafer. When these acquired temperature readings are displayed in a 2-D map, the temperature of the wafer may be simply interpolated between sensor locations/measurement locations. Depending on the source and magnitude of temperature non-uniformity within the conventional process condition measurement wafers (e.g., chuck temperature, heat flux, wafer cooling) the accuracy of the interpolated temperature may vary, leading to inaccurate temperature measurements.

[0071] Accordingly, some embodiments of the present disclosure are directed to a process condition measurement wafer assembly 100 and technique for improving the accuracy of temperature readings by calibrating out conduction variations. This may be further understood with reference to FIG. 5.

[0072] FIG. 5 is a simplified cross-sectional view of a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure.

[0073] As shown in FIG. 5, a first electronic component 106a (e.g., first sensor 416a) disposed on a first printed circuit element 105a may be disposed within a first cavity 107a between the top substrate 104 and the bottom substrate 102. Similarly, a second electronic component 106b (e.g., second sensor 416b) disposed on a second printed circuit element 105b may be disposed within a second cavity 107b between the top substrate 104 and the bottom substrate 102. Comparing the relative arrangement of the cavities 107a, 107b and electronic components 106a, 106b, it may be seen that the first cavity 107a is larger than the second cavity 107b. In this regard, the first electronic component 106a is further removed/spaced from the bottom substrate 102, and is therefore further decoupled from the bottom substrate 102 by a larger thermal resistance as compared to the second electronic component 106b.

[0074] In a perfect isothermal environment, the first electronic component 106a (e.g., first sensor 416a) and the second electronic component 106a (e.g., second sensor 416b) would acquire identical temperature measurements (e.g., measurement parameters). However, fabrication processes typically are not carried out in perfect isothermal environments. During fabrication processes (e.g., etch processes), the bottom substrate 102 may be cooled while heat flux 202 is applied to the top substrate 102. In this case, the first sensor 416a would read higher than second sensor 416b, as it is further removed from the cooled bottom substrate 102, and therefore more decoupled from cooling.

[0075] Thus, it may be seen that construction variations (e.g., varying size of cavities 107a, 107b) may result in errors/discrepancies in acquired measurement parameters. Other construction variations which may result in discrepancies between acquired measurement parameters and/or calculated values may include, but are not limited to, variations in size/shape of electronic components 106, adhesion to varying surfaces (e.g., coupling to top substrate 104, coupling to bottom substrate 102), variations in adhesive and/or conductive properties, and the like. Furthermore, as temperature gradients and

heat fluxes 202 become greater, such construction variations may lead to increased discrepancies between acquired measurement parameters and/or calculated values.

[0076] Accordingly, some embodiments of the present disclosure are directed to quantifying and calibrating effects of construction variations on acquired measurement parameters and/or calculated values. By quantifying effects of construction variations on acquired measurement parameters, and calibrating out (e.g., removing) determined effects, the system and method of the present disclosure may enable more efficient and accurate process monitoring.

[0077] In embodiments, the one or more processors 420 of the remote data system 402 are configured to execute a set of program instructions stored in memory 422, the set of program instructions configured to cause the one or more processors 420 to carry out various steps/functions of the present disclosure. For example, the one or more processors 420 may be configured to: acquire, under isothermal conditions, a set of temperature measurements from a set of temperature sensors and a set of heat flux measurements from a set of heat flux sensors distributed across the process condition measurement wafer assembly 100; calibrate the set of temperature measurements and the set of heat flux measurements acquired under isothermal conditions; apply a known heat flux to the process condition measurement wafer assembly 100; acquire, during application of the known heat flux, an additional set of temperature measurements from the set of temperature sensors and an additional set of heat flux measurements from the set of heat flux sensors; identify temperature variation observed across the set of temperature sensors during application of the known heat flux; identify a heat flux-temperature variation relationship by correlating the known heat flux with the identified temperature variation of the set of temperature sensors; acquire, under unknown heat flux conditions, a test set of temperature measurements from the set of temperature sensors and a test set of heat flux measurements from the heat flux sensors; and adjust the test set of temperature measurements based on the test set of heat flux measurements and the identified heat flux-temperature variation relationship. Each of these steps/functions will be addressed in further detail herein.

[0078] In one embodiment, the processors 420 may be configured to acquire, under isothermal conditions, a set of temperature measurements from a set of temperature sensors 416 and a set of heat flux measurements from a set of heat flux sensors 416 distributed across the process condition measurement wafer assembly 100. For example, a process condition measurement wafer assembly 100 may be fabricated to include a plurality of temperature sensors 416 and a plurality of heat flux sensors 416 distributed at varying locations throughout the process condition measurement wafer assembly 100. Under isothermal conditions, the plurality of temperature sensors 416 and the plurality of heat flux sensors 416 may be configured to acquire a set of temperature measurements and heat flux measurements, respectively. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410.

[0079] In another embodiment, the processors 420 may be configured to calibrate the set of temperature measurements and the set of heat flux measurements acquired under isothermal conditions. For example, the processors 420 may be configured to set the measurements acquired under isothermal conditions as a baseline against which subsequent measurements may be compared and/or adjusted.

[0080] In another embodiment, the processors 420 may be configured to generate one or more control signals configured to cause a heat source to apply a known heat flux to the process condition measurement wafer assembly 100. For example, in a processing environment, the processors 420 may be communicatively coupled to one or more heat sources (not shown). The processors 420 may be configured to generate one or more control signals configured to cause the one or more heat sources to apply a known heat flux to the process condition measurement wafer assembly 100. Parameters/characteristics associated with known heat fluxes may be stored in memory 422 and retrieved by the processors 420.

[0081] In another embodiment, the processors 420 may be configured to acquire, during application of the known heat flux, an additional set of temperature measurements from the set of temperature sensors 416 and an additional set of heat flux measurements from

the set of heat flux sensors 416. For example, during application of the known heat flux, the plurality of temperature sensors 416 and the plurality of heat flux sensors 416 may be configured to acquire an additional set of temperature measurements and heat flux measurements, respectively. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410. The processors 420 may be configured to store the acquired measurements in memory 422.

[0082] In another embodiment, the processors 420 may be configured to identify one or more temperature variations observed across the set of temperature sensors during application of the known heat flux. For example, as noted previously herein with respect to FIG. 5, construction variations (e.g., varying size of cavities 107a, 107b, variations in size/shape of electronic components 106, adhesion to varying surfaces, variations in adhesive and/or conductive properties, and the like) may cause a first temperature sensor 416a to acquire varying readings as compared to an additional temperature sensor 416b. In this regard, the processors 420 may be configured to identify one or more temperature variations observed across the set of temperature sensors 416 during application of the known heat flux.

[0083] In another embodiment, the processors 420 may be configured to identify a heat flux-temperature variation relationship by correlating the known heat flux with the identified temperature variation of the set of temperature sensors 416. For example, the processors 420 may be configured to associate the known heat flux with the identified temperature variation in order to identify the heat flux-temperature variation relationship. It is contemplated herein that the identified heat flux-temperature variation relationship may take any form known in the art including, but not limited to, a relationship represented by a mathematical equation(s), a list of associated heat flux values and related temperature variation values, and the like.

[0084] In order to more thoroughly model a heat flux-temperature variation relationship, the processors 420 may be configured to collect readings at multiple isothermal conditions, as well as during a plurality of varying known heat flux conditions. By collecting measurements under these varying conditions, the processors 420 may be configured to

generate a model which represents the identified heat flux-temperature variation relationship of the process condition measurement wafer assembly 100.

[0085] After identification of the heat flux-temperature variation relationship, the process condition measurement wafer assembly 100 may subsequently be used in one or more processes (e.g., processes within epitaxy chambers, processes within plasma etch chambers). While conditions within the respective chambers may be generally known, the exact temperature and heat flux conditions, as experienced by the process condition measurement wafer assembly 100, may be unknown. Accordingly, the processors 412 may be configured to acquire a test set of temperature measurements and a test set of heat flux measurements from the sensors 416.

[0086] For example, under unknown heat flux conditions, the set of temperature sensors 416 may be configured to acquire a test set of temperature measurements, and the set of heat flux sensors 416 may be configured to acquire a test set of heat flux measurements. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410. The processors 420 may be configured to store the acquired measurements in memory 422.

[0087] In another embodiment, the processors 420 may be configured to adjust the test set of temperature measurements based on the test set of heat flux measurements and the identified heat flux-temperature variation relationship. For example, based on the heat flux-temperature variation relationship, the processors 420 may be configured to identify a sub-set of temperature sensors 416 read higher temperatures under a particular set of heat flux conditions. In this regard, the processors 420 may be configured to adjust (e.g., lower) the temperature measurements of the test set of temperature measurements collected by the sub-set of temperature sensors 416 based on the heat flux-temperature variation relationship. It is noted herein that the processors 420 may be configured to adjust the test set of temperature measurements using any mathematical technique known in the art.

[0088] In another embodiment, the processors 420 may be configured to map the adjusted test set of temperature measurements to one or more measurement locations of the process condition measurement wafer assembly 100. For example, the locations of each of the temperature sensors 416 on the process condition measurement wafer assembly 100 may be known and stored in memory 422. These known locations of temperature sensors 416 are locations in which temperature measurements are acquired by the process condition measurement wafer assembly 100, and may be referred to as measurement locations. In this regard, the processors 420 may be configured to map the adjusted test set of temperature measurements to the respective known locations of each temperature sensor 416 (e.g., measurement locations).

[0089] In another embodiment, the processors 420 may be configured to interpolate a set of temperature values at locations between the one or more measurement locations based on the adjusted test set of temperature measurements and one or more interpolation functions. For example, the processors 420 may be configured to map a first adjusted temperature value to a first measurement location and a second adjusted temperature value to a second measurement location. In this example, the processors 420 may be configured to interpolate between the first measurement location and the second measurement location. For instance, the processors 420 may be configured to assign one or more temperature values to one or more locations between the first measurement location and the second measurement location.

[0090] Depending on the source and magnitude of temperature non-uniformity between various measurement locations, the accuracy of interpolated temperature values may vary. In order to improve the accuracy of the interpolated temperature values between temperature sensors 416 (e.g., between measurement locations), the processors 420 may be configured to model the effects of different types of construction variation/non-uniformity (e.g., varying size of cavities 107a, 107b, variations in size/shape of electronic components 106, adhesion to varying surfaces, variations in adhesive and/or conductive properties, and the like) on acquired temperature values. For example, known construction variations/non-uniformities may be considered and included in the heat flux-

temperature variation relationship discussed above. In this regard, the processors 420 may be configured to account for construction variations within the process condition measurement wafer assembly 100 when generating the heat flux-temperature variation relationship model.

[0091] After accounting for construction variations in the heat flux-temperature variation relationship model, the process condition measurement wafer assembly 100 may be used in a chamber to be tested. Subsequently, process non-uniformities may be identified by a number of techniques including, but not limited to: measurement of pre-plasma chuck non-uniformity, steady state temperature data (e.g., temperature measurements from temperature sensors 416), determining a derivative of temperature measurements over time (dT/dt) to estimate heat flux and cooling non-uniformity, concurrent acquisition of temperature measurements with heat flux measurements, and the like. In some embodiments, the processors 420 may be configured to utilize known effects of construction variation (e.g., heat flux-temperature variation relationship model based at least partially on construction variations) and identified process non-uniformities to more accurately predict process temperature values between measurement locations (e.g., between temperature sensors 416).

[0092] In additional and/or alternative embodiments, measurement parameters and/or values acquired by the process condition measurement wafer assembly 100 may be used in a feedforward or feedback loop in order to adjust one or more upstream or downstream process tools. For example, upon acquiring measurement parameters in a semiconductor device process, the one or more processors 420 may be configured to receive the acquired measurement parameters and/or determined values, and generate one or more control signals configured to selectively adjust one or more characteristics of one or more process tools within the semiconductor device process. Process tools which may be adjusted may include, but are not limited to, lithography tools, deposition tools, etching tools, and the like.

[0093] It is noted herein that the one or more components of the process condition measurement wafer assembly 100 and associated system may be communicatively

coupled to the various other components of process condition measurement wafer assembly 100 and associated system in any manner known in the art. For example, the communication circuitry 410, 404 may be communicatively coupled to each other and other components via a wireline (e.g., copper wire, fiber optic cable, and the like) or wireless connection (e.g., RF coupling, IR coupling, 3G, 4G, 4G LTE, 5G, WiFi, WiMax, Bluetooth and the like).

[0094] In one embodiment, the one or more processors 412, 420 may include any one or more processing elements known in the art. In this sense, the one or more processors 412, 420 may include any microprocessor-type device configured to execute software algorithms and/or instructions. In one embodiment, the one or more processors 412, 420 may consist of a desktop computer, mainframe computer system, workstation, image computer, parallel processor, or other computer system (e.g., networked computer) configured to execute a program configured to operate the process condition measurement wafer assembly 100 and associated system, as described throughout the present disclosure. It should be recognized that the steps described throughout the present disclosure may be carried out by a single computer system or, alternatively, multiple computer systems. Furthermore, it should be recognized that the steps described throughout the present disclosure may be carried out on any one or more of the one or more processors 412, 420. In general, the term "processor" may be broadly defined to encompass any device having one or more processing elements, which execute program instructions from memory 414, 422. Moreover, different subsystems of the process condition measurement wafer assembly 100 and associated system (e.g., sensors 416, remote data system 402) may include processor or logic elements suitable for carrying out at least a portion of the steps described throughout the present disclosure. Therefore, the above description should not be interpreted as a limitation on the present disclosure but merely an illustration.

[0095] The memory 414, 422 may include any storage medium known in the art suitable for storing program instructions executable by the associated one or more processors 412, 420 and the data received from the process condition measurement wafer assembly

100/sensors 416. For example, the memory 107, 118, 124 may include a non-transitory memory medium. For instance, the memory 107, 118, 124 may include, but is not limited to, a read-only memory (ROM), a random-access memory (RAM), a magnetic or optical memory device (e.g., disk), a magnetic tape, a solid-state drive and the like. It is further noted that memory 414, 422 may be housed in a common controller housing with the one or more processors 412, 420. In an alternative embodiment, the memory 414, 422 may be located remotely with respect to the physical location of the processors 412, 420. In another embodiment, the memory 414, 422 maintains program instructions for causing the one or more processors 412, 420 to carry out the various steps described through the present disclosure.

[0096] FIG. 6 is a flowchart of a method 600 for calculating temperatures across a process condition measurement wafer assembly 100, in accordance with one or more embodiments of the present disclosure.

[0097] In a step 602, a set of temperature measurements from a set of temperature sensors and a set of heat flux measurements are acquired under isothermal conditions from a set of heat flux sensors distributed across a process condition measurement wafer. For example, a process condition measurement wafer assembly 100 may be fabricated to include a plurality of temperature sensors 416 and a plurality of heat flux sensors 416 distributed at varying locations throughout the process condition measurement wafer assembly 100. Under isothermal conditions, the plurality of temperature sensors 416 and the plurality of heat flux sensors 416 may be configured to acquire a set of temperature measurements and heat flux measurements, respectively. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410.

[0098] In a step 604, the set of temperature measurements and the set of heat flux measurements acquired under isothermal conditions are calibrated. For example, the processors 420 may be configured to calibrate the set of temperature measurements by adjusting one or more of the acquired temperature measurements. By way of another

example, the processors 420 may be configured to set the measurements acquired under isothermal conditions as a baseline against which subsequent measurements may be compared and/or adjusted.

[0099] In a step 606, known heat flux is applied to the process condition measurement wafer. For example, in a processing environment, the processors 420 may be communicatively coupled to one or more heat sources (not shown). The processors 420 may be configured to generate one or more control signals configured to cause the one or more heat sources to apply a known heat flux to the process condition measurement wafer assembly 100.

[00100] In a step 608, during application of the known heat flux, an additional set of temperature measurements are acquired from the set of temperature sensors and an additional set of heat flux measurements are acquired from the set of heat flux sensors. For example, during application of the known heat flux, the plurality of temperature sensors 416 and the plurality of heat flux sensors 416 may be configured to acquire an additional set of temperature measurements and heat flux measurements, respectively. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410. The processors 420 may be configured to store the acquired measurements in memory 422.

[00101] In a step 610, a temperature variation observed across the set of temperature sensors during application of the known heat flux is identified. For example, as noted previously herein with respect to FIG. 5, construction variations (e.g., varying size of cavities 107a, 107b, variations in size/shape of electronic components 106, adhesion to varying surfaces, variations in adhesive and/or conductive properties, and the like) may cause a first temperature sensor 416a to acquire varying readings as compared to an additional temperature sensor 416b. In this regard, the processors 420 may be configured to identify one or more temperature variations observed across the set of temperature sensors 416 during application of the known heat flux.

[00102] In a step 612, a heat flux-temperature variation relationship is identified by correlating the known heat flux with the identified temperature variation of the set of temperature sensors. For example, the processors 420 may be configured to associate the known heat flux with the identified temperature variation in order to identify the heat flux-temperature variation relationship. It is contemplated herein that the identified heat flux-temperature variation relationship may take any form known in the art including, but not limited to, a relationship represented by a mathematical equation(s), a list of associated heat flux values and related temperature variation values, and the like.

[00103] In a step 614, under unknown heat flux conditions, a test set of temperature measurements is acquired from the set of temperature sensors, and a test set of heat flux measurements is acquired from the heat flux sensors. For example, under unknown heat flux conditions, the set of temperature sensors 416 may be configured to acquire a test set of temperature measurements, and the set of heat flux sensors 416 may be configured to acquire a test set of heat flux measurements. The processors 420 may then be configured to receive the acquired measurements via communication circuitry 404, 410. The processors 420 may be configured to store the acquired measurements in memory 422.

[00104] In a step 616, the test set of temperature measurements is adjusted based on the test set of heat flux measurements and the identified heat flux-temperature variation relationship. For example, based on the heat flux-temperature variation relationship, the processors 420 may be configured to identify a sub-set of temperature sensors 416 read higher temperatures under a particular set of heat flux conditions. In this regard, the processors 420 may be configured to adjust (e.g., lower) the temperature measurements of the test set of temperature measurements collected by the sub-set of temperature sensors 416 based on the heat flux-temperature variation relationship. It is noted herein that the processors 420 may be configured to adjust the test set of temperature measurements using any mathematical technique known in the art.

[00105] All of the methods described herein may include storing results of one or more steps of the method embodiments in memory. The results may include any of the results described herein and may be stored in any manner known in the art. The memory may include any memory described herein or any other suitable storage medium known in the art. After the results have been stored, the results can be accessed in the memory and used by any of the method or system embodiments described herein, formatted for display to a user, used by another software module, method, or system, and the like. Furthermore, the results may be stored "permanently," "semi-permanently," temporarily," or for some period of time. For example, the memory may be random access memory (RAM), and the results may not necessarily persist indefinitely in the memory.

[00106] It is further contemplated that each of the embodiments of the method described above may include any other step(s) of any other method(s) described herein. In addition, each of the embodiments of the method described above may be performed by any of the systems described herein.

[00107] As used herein, directional terms such as "top," "bottom," "over," "under," "upper," "upward," "lower," "down," "downward," and similar terms, are intended to provide relative positions for purposes of description, and are not intended to designate an absolute frame of reference. Various modifications to the described embodiments will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[00108] The herein described subject matter sometimes illustrates different components contained within, or connected with, other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein

combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "connected," or "coupled," to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "couplable," to each other to achieve the desired functionality. Specific examples of couplable include but are not limited to physically interactable and/or physically interacting components and/or wirelessly interactable and/or wirelessly interacting components and/or logically interactable and/or logically interacting components.

[00109] Furthermore, it is to be understood that the invention is defined by the appended claims. It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," and the like). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to inventions containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should typically be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means at least two

recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to “at least one of A, B, and C, and the like” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., “a system having at least one of A, B, and C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, and the like). In those instances where a convention analogous to “at least one of A, B, or C, and the like” is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., “a system having at least one of A, B, or C” would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, and the like). It will be further understood by those within the art that virtually any disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” will be understood to include the possibilities of “A” or “B” or “A and B.”

[00110] It is believed that the present disclosure and many of its attendant advantages will be understood by the foregoing description, and it will be apparent that various changes may be made in the form, construction and arrangement of the components without departing from the disclosed subject matter or without sacrificing all of its material advantages. The form described is merely explanatory, and it is the intention of the following claims to encompass and include such changes. Furthermore, it is to be understood that the invention is defined by the appended claims.

CLAIMS

What is claimed:

1. A process condition measurement wafer assembly comprising:
a bottom substrate;
a top substrate;
one or more electronic components disposed on one or more printed circuit elements and interposed between the top substrate and the bottom substrate; and
one or more shielding layers formed between the bottom substrate and the top substrate, wherein the one or more shielding layers are configured to electromagnetically shield the one or more electronic components and diffuse voltage potentials across the bottom substrate and the top substrate.
2. The assembly of Claim 1, wherein the one or more shielding layers comprise:
one or more films disposed on at least one of a surface of the bottom substrate or a surface of the top substrate, wherein the one or more films are electrically conductive and opaque.
3. The assembly of Claim 1, wherein the one or more shielding layers comprise:
an adhesive layer; and
a plurality of conductive particles suspended within the adhesive layer, wherein the plurality of conductive particles is configured to establish electrical contact between a portion of the top substrate and a portion of the bottom substrate.
4. The assembly of Claim 1, wherein the one or more shielding layers comprise:
an adhesive layer; and
a plurality of electrically conductive structures formed on at least one of a surface of the top substrate or a surface of the bottom substrate, wherein the adhesive layer is formed around the electrically conductive structures.

5. The assembly of Claim 4, wherein at least one electrically conductive structure of the plurality of the electrically conductive structures comprises a protrusion formed on at least one of the surface of the top substrate or the surface of the bottom substrate.
6. The assembly of Claim 5, wherein at least some of the electrically conductive structures are at least one of conic sections or bumps formed on at least one of the surface of the top substrate or the surface of the bottom substrate.
7. The assembly of Claim 4, wherein the plurality of electrically conductive structures is formed via an electroplating process.
8. The assembly of Claim 4, wherein the plurality of electrically conductive structures is formed via a wire bond bumping process.
9. The assembly of Claim 1, wherein the one or more shielding layers is formed via an adhesive-less silicon-to-silicon bonding of the top substrate to the bottom substrate.
10. The assembly of Claim 9, wherein the one or more shielding layers comprise: one or intermediate films interposed between the top substrate and the bottom substrate.
11. The assembly of Claim 10, wherein the one or more intermediate films include one or more metal contacts.
12. The assembly of Claim 1, wherein the one or more shielding layers comprise:
one or more films deposited on at least one of the top surface or the bottom surface via a transient liquid phase bonding process.
13. The assembly of Claim 1, further comprising:
one or more pillar structures formed on at least one of the top substrate or the bottom substrate, wherein the one or more pillar structures are configured to establish

thermal conductivity pathways through one or more portions of the one or more printed circuit elements.

14. The assembly of Claim 13, wherein the one or more pillar structures are formed from at least one of a semiconductor material or a metal.

15. The assembly of Claim 1, wherein the one or more printed circuits are formed from an inorganic material.

16. The assembly of Claim 15, wherein the one or more printed circuits are direct bonded to at least one of the top substrate or the bottom substrate.

17. The assembly of Claim 1, wherein at least one of the top substrate or the bottom substrate comprise a semiconductor substrate.

18. The assembly of Claim 17, wherein the at least one of the top substrate or the bottom substrate comprises:

at least one of, a silicon substrate, a silicon carbide substrate, a silicon nitride substrate, a gallium nitride substrate, a gallium arsenide substrate, a germanium substrate, or a substrate of gallium and indium.

19. The assembly of Claim 17, wherein at least one of the bottom substrate or the top substrate is configured as the one or more shielding layers

20. The assembly of Claim 1, wherein the one or more electronic components comprise:

at least one of one or more temperature sensors, one or more pressure sensors, one or more chemical sensors, or one or more radiation sensors.

21. The assembly of Claim 19, wherein the one or more electronic components comprises:

one or more processors;
communication circuitry;
memory; and
a power source.

22. The assembly of Claim 20, wherein the one or more electronic components are configured to calculate one or more values from one or more acquired measurement parameters.

23. The assembly of Claim 1, further comprising:

a remote data system communicatively coupled to the one or more electronic components, wherein the one or more electronic components are configured to transmit one or more acquired measurement parameters to the remote data system, wherein the remote data system is configured to calculate a value from the one or more acquired measurement parameters.

24. The assembly of Claim 22, wherein the remote data system is configured to map the one or more values to the one or more locations of at least one of the top substrate or the bottom substrate.

25. The assembly of Claim 23, wherein the remote data system is configured to report the mapped one or more values to a user interface.

26. A process condition measurement wafer assembly comprising:

a bottom substrate;

a top substrate; and

one or more electronic components disposed on one or more printed circuit elements and interposed between the top substrate and the bottom substrate,

wherein at least one of the bottom substrate or the top substrate are configured to electromagnetically shield the one or more electronic components and diffuse voltage potentials across the bottom substrate and the top substrate.

27. A method comprising:

acquiring, under isothermal conditions, a set of temperature measurements from a set of temperature sensors and a set of heat flux measurements from a set of heat flux sensors distributed across a process condition measurement wafer;

calibrating the set of temperature measurements and the set of heat flux measurements acquired under isothermal conditions;

apply a known heat flux to the process condition measurement wafer;

acquiring, during application of the known heat flux, an additional set of temperature measurements from the set of temperature sensors and an additional set of heat flux measurements from the set of heat flux sensors;

identifying temperature variation observed across the set of temperature sensors during application of the known heat flux;

identifying a heat flux-temperature variation relationship by correlating the known heat flux with the identified temperature variation of the set of temperature sensors;

acquiring, under unknown heat flux conditions, a test set of temperature measurements from the set of temperature sensors and a test set of heat flux measurements from the heat flux sensors; and

adjusting the test set of temperature measurements based on the test set of heat flux measurements and the identified heat flux-temperature variation relationship.

28. The method of Claim 27, further comprising:

mapping the adjusted test set of temperature measurements to one or more measurement locations of the process condition measurement wafer.

29. The method of Claim 28, further comprising:

interpolating a set of temperature values at locations between the one or more measurement locations based on the adjusted test set of temperature measurements and one or more interpolation functions.

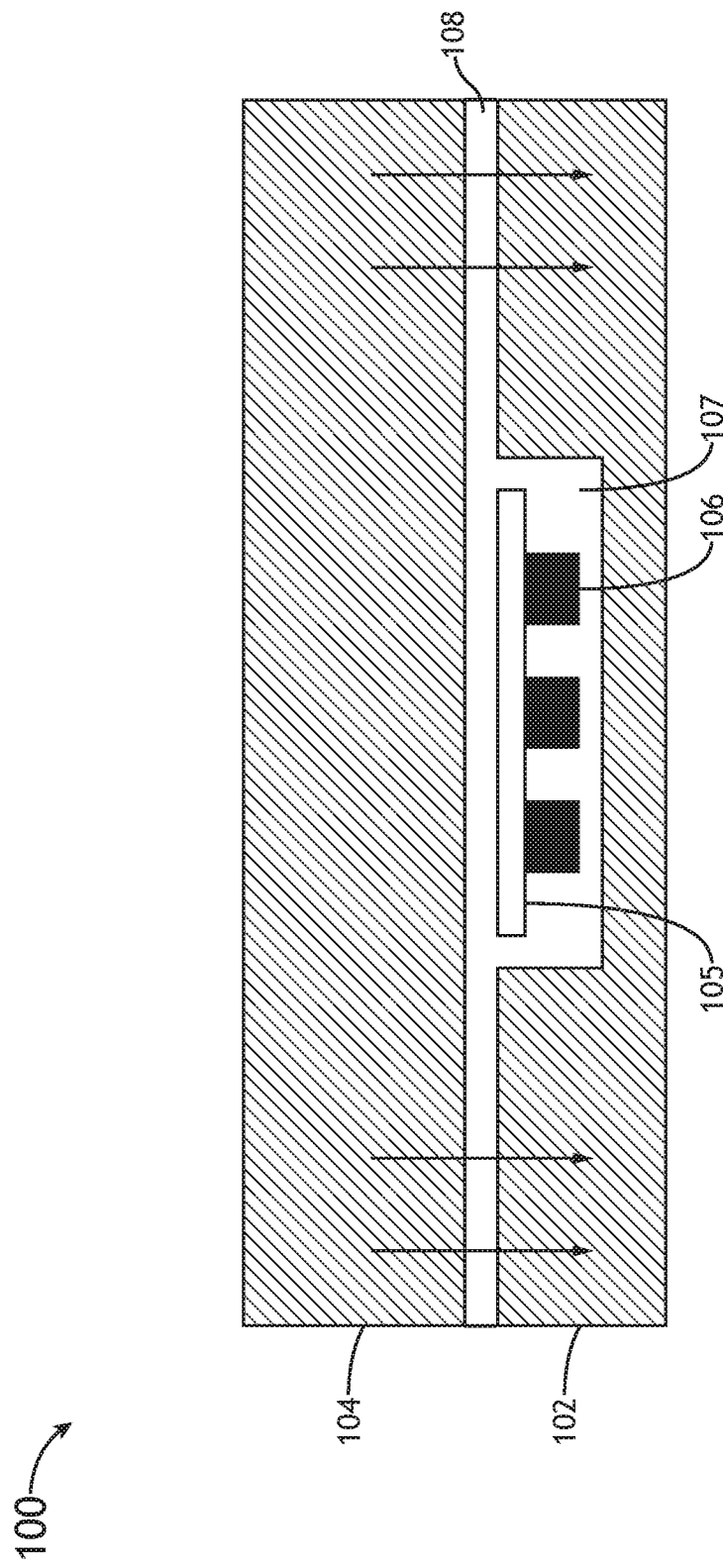


FIG.1A

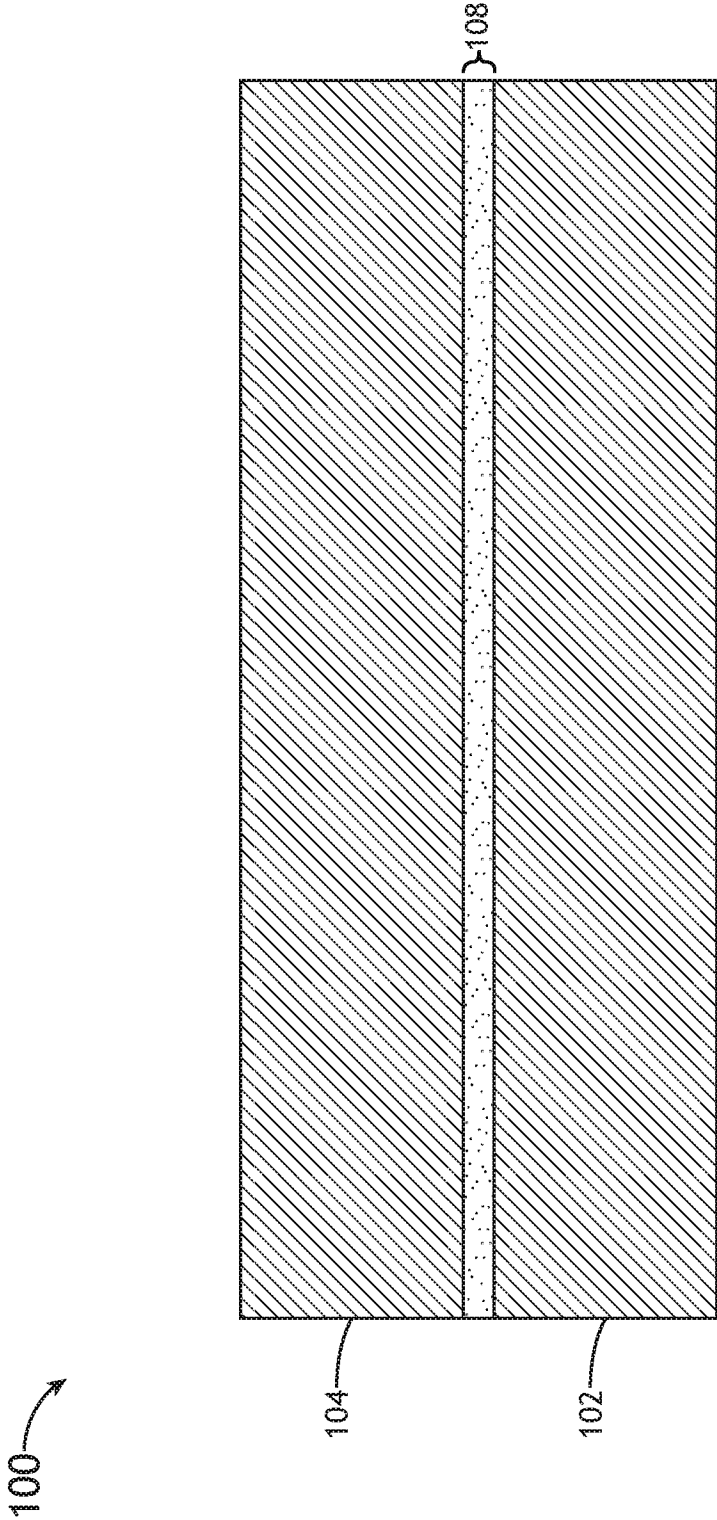


FIG. 1B

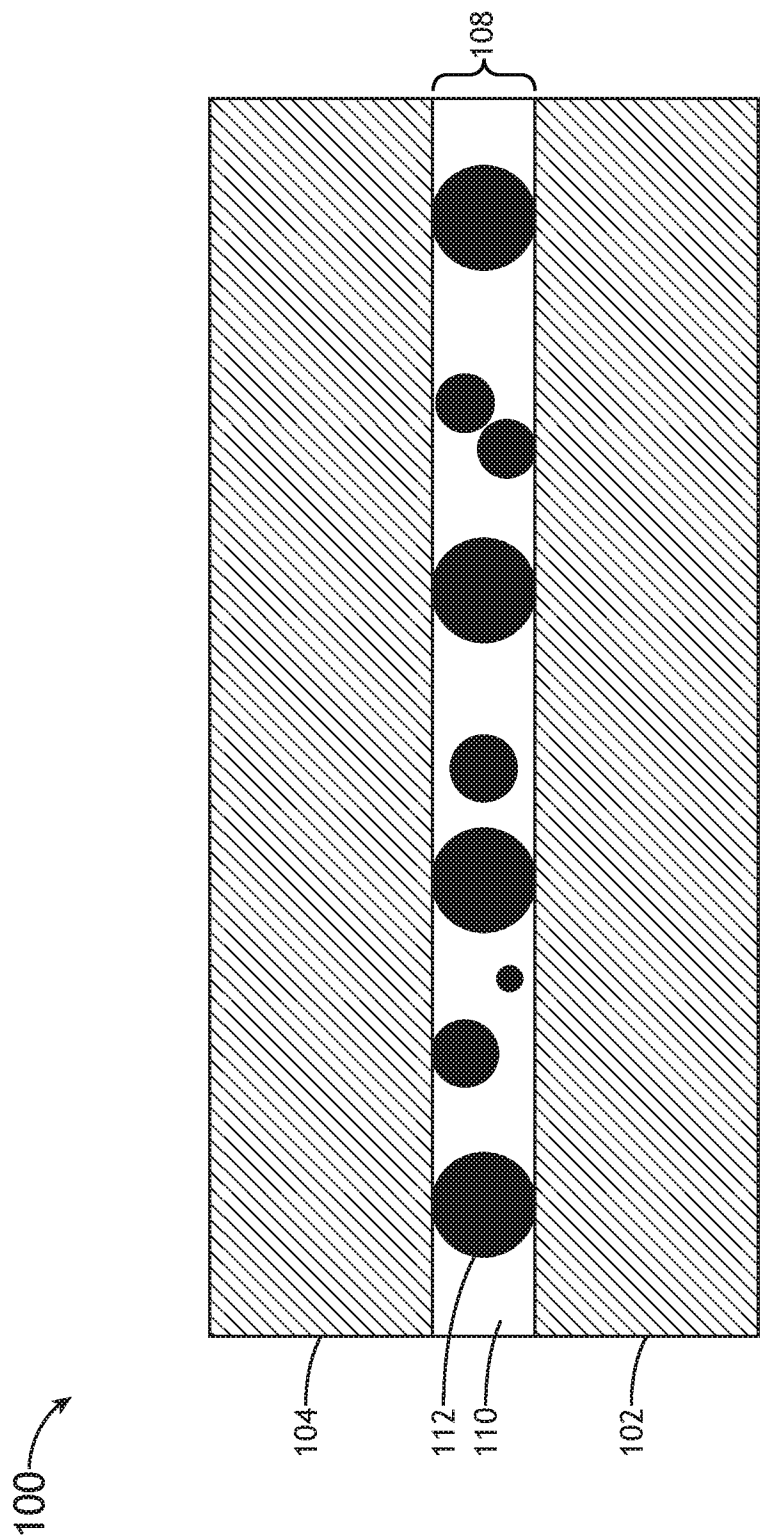


FIG.1C

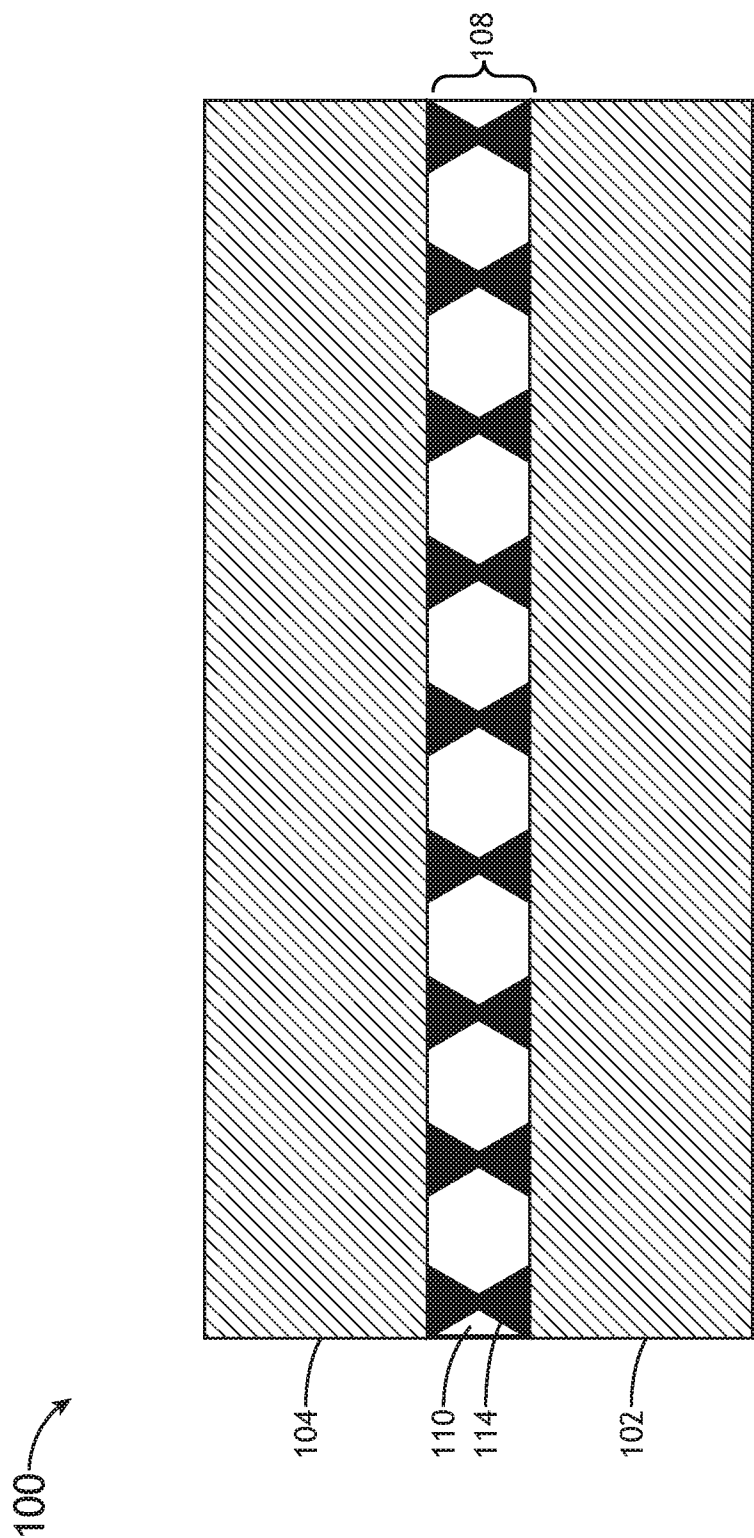


FIG.1D

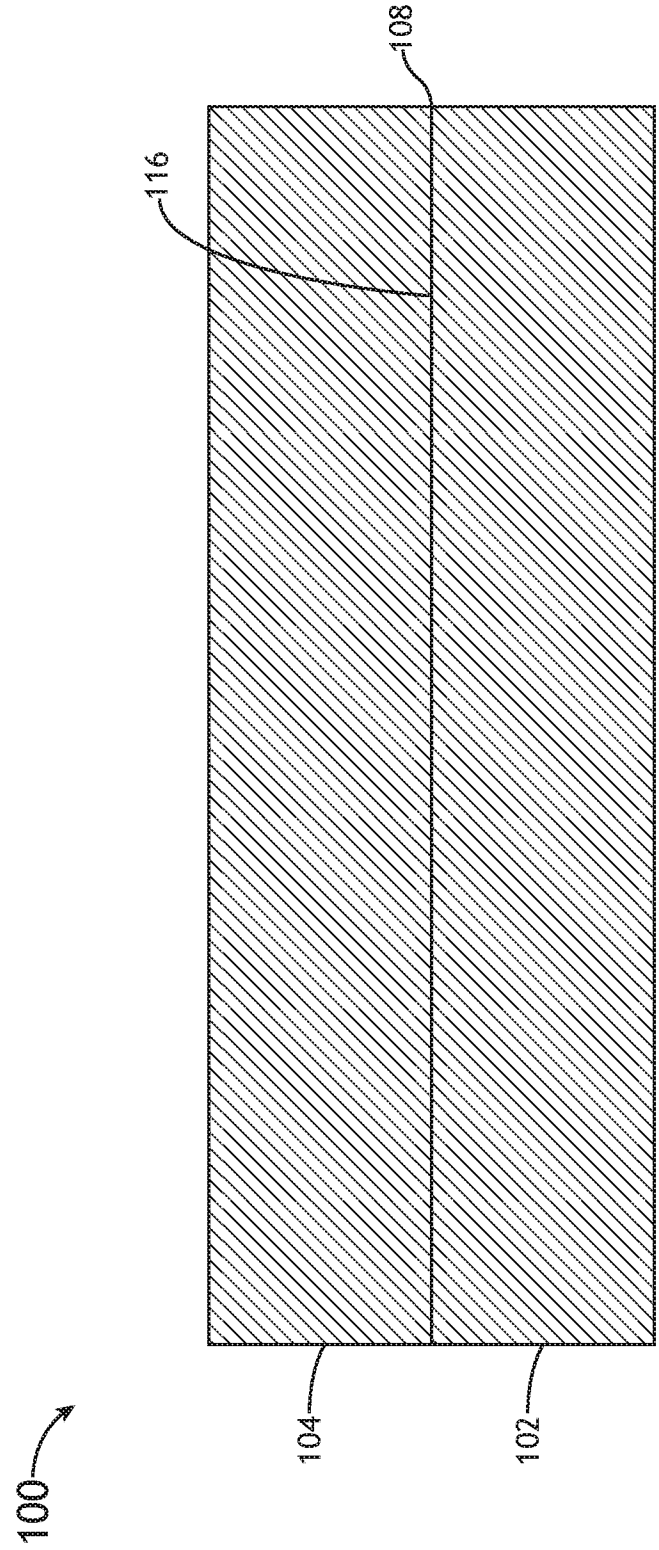


FIG. 1E

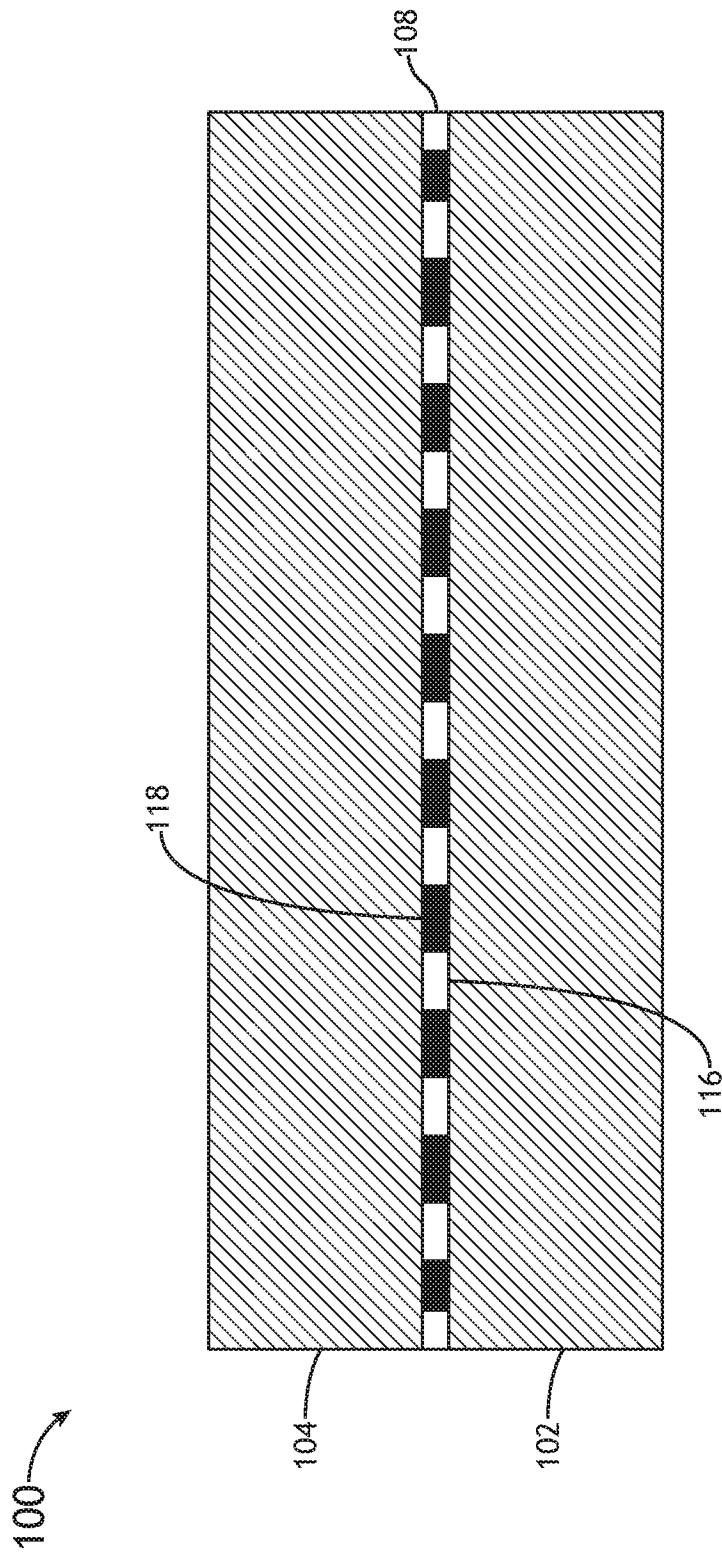


FIG.1F

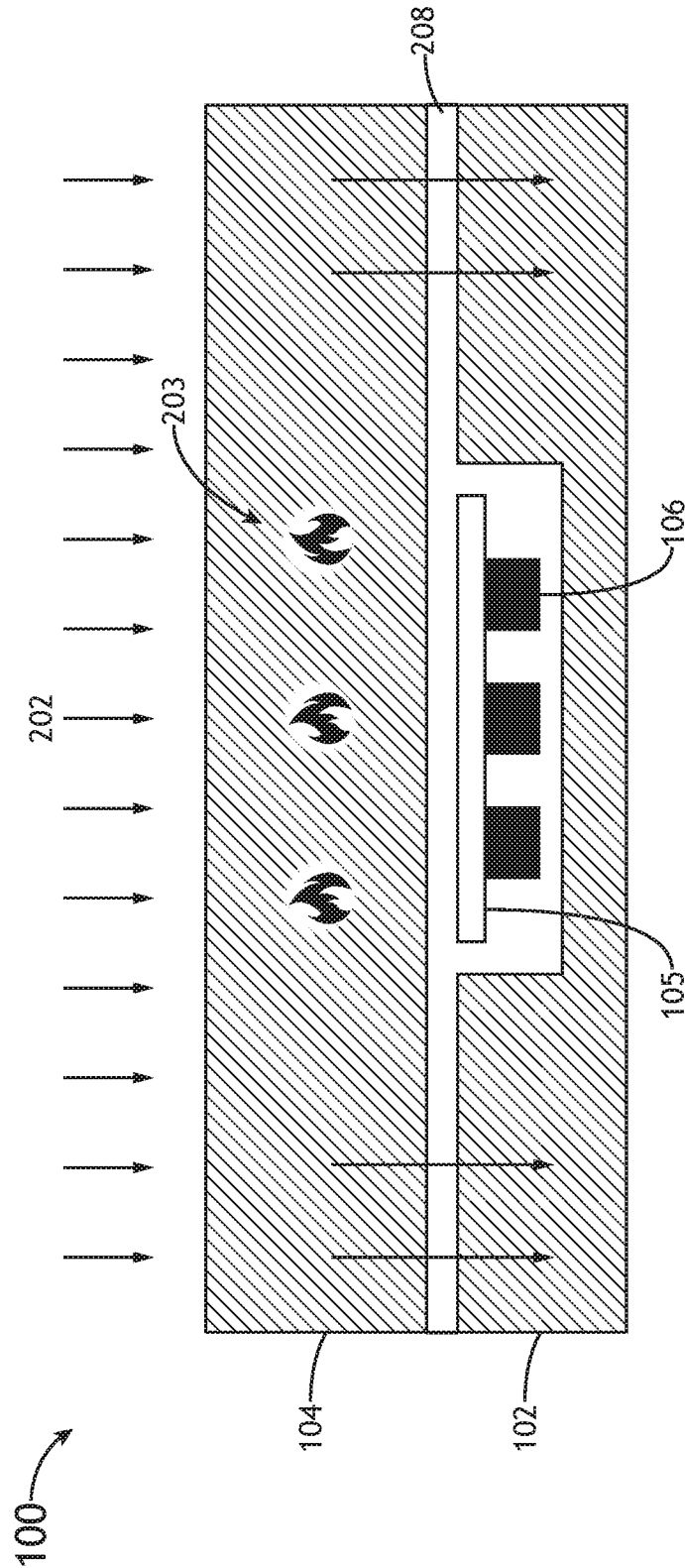


FIG. 2A

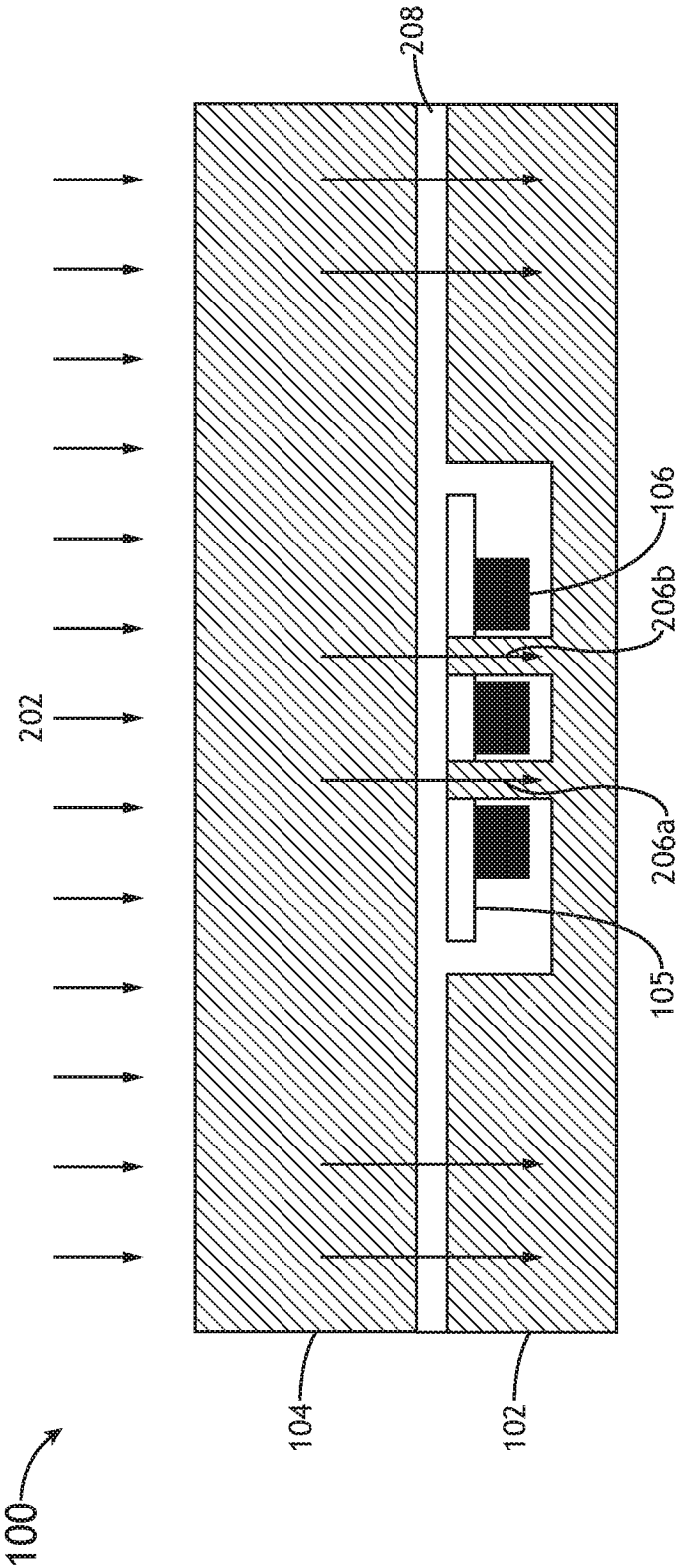


FIG.2B

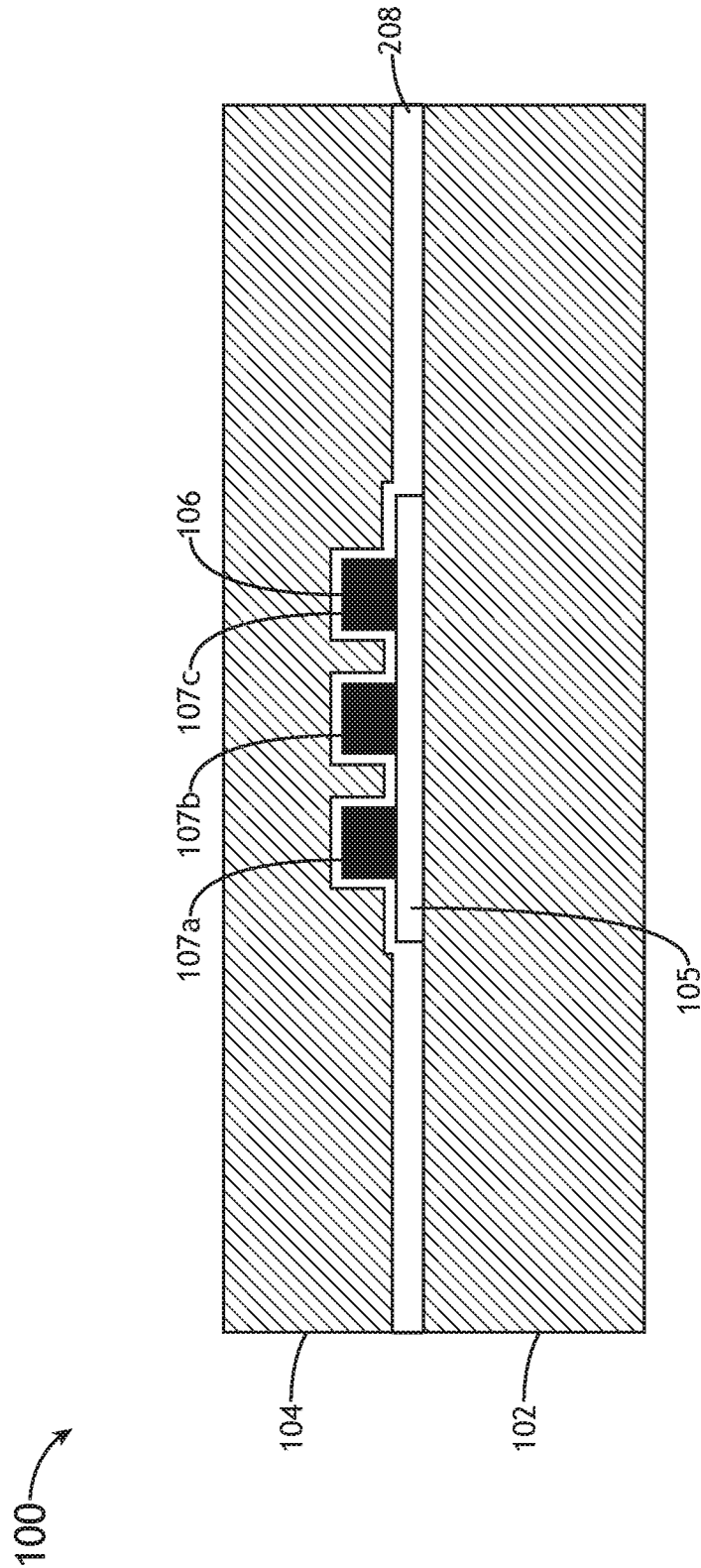


FIG.3

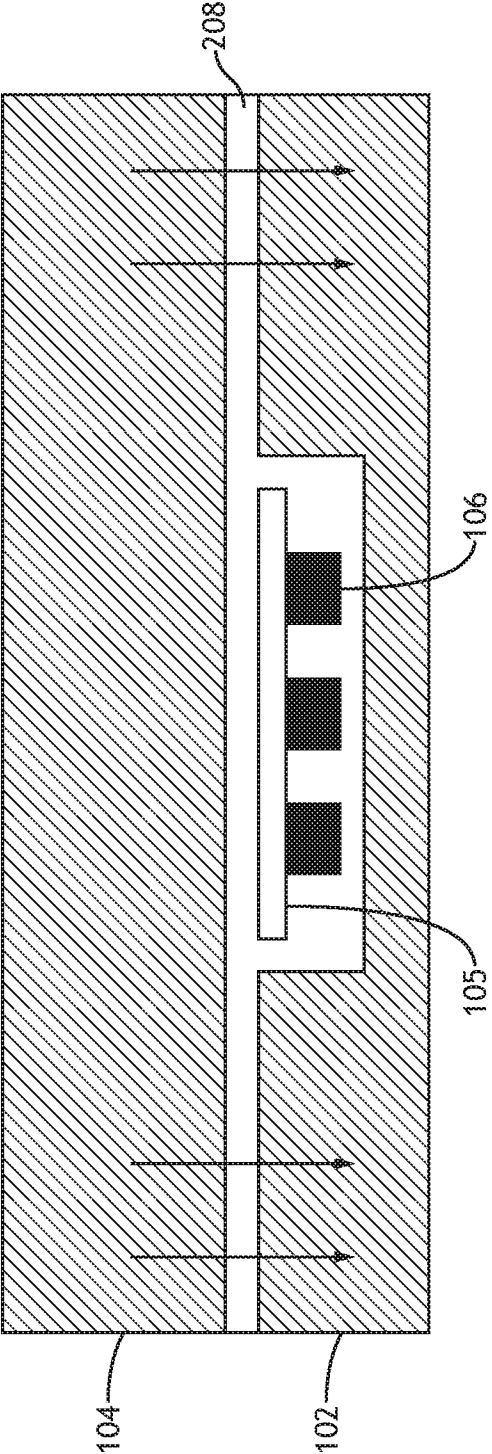
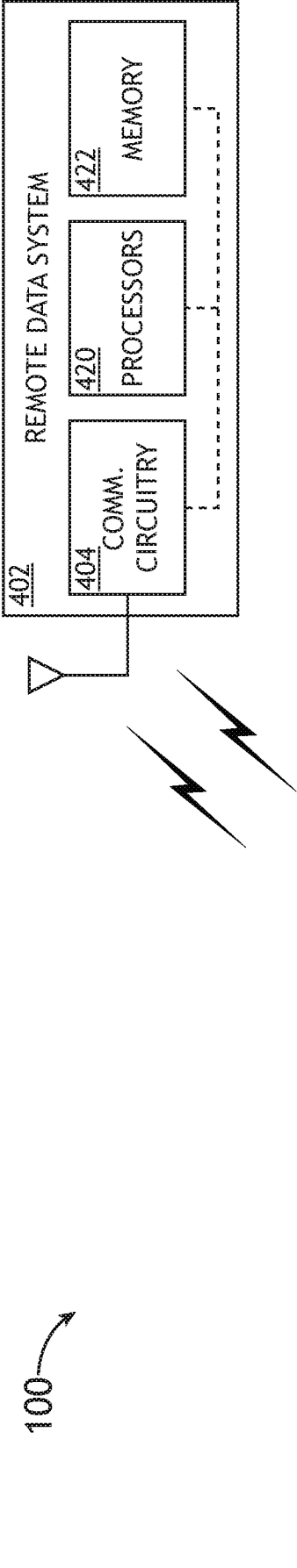


FIG. 4A

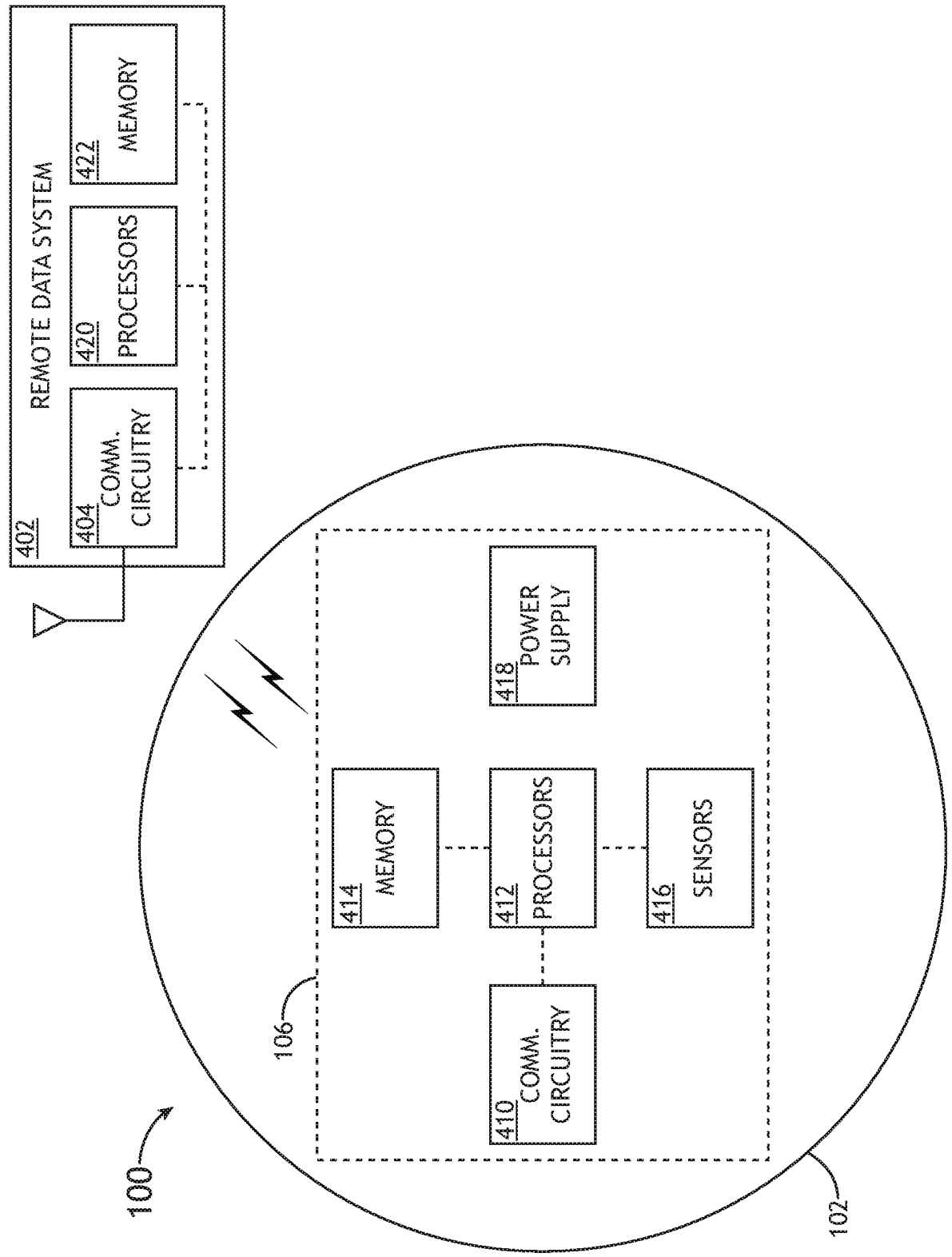


FIG. 4B

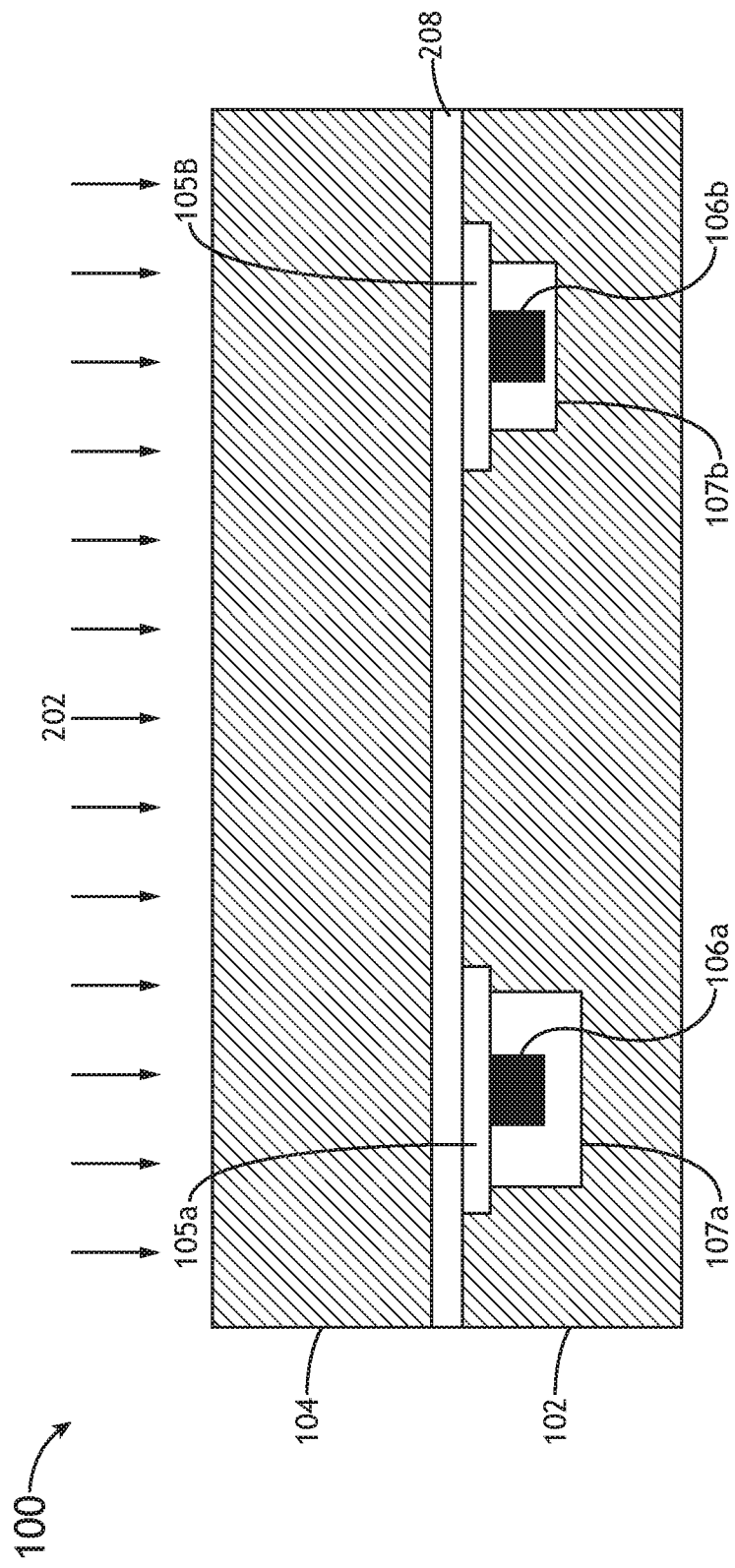


FIG.5

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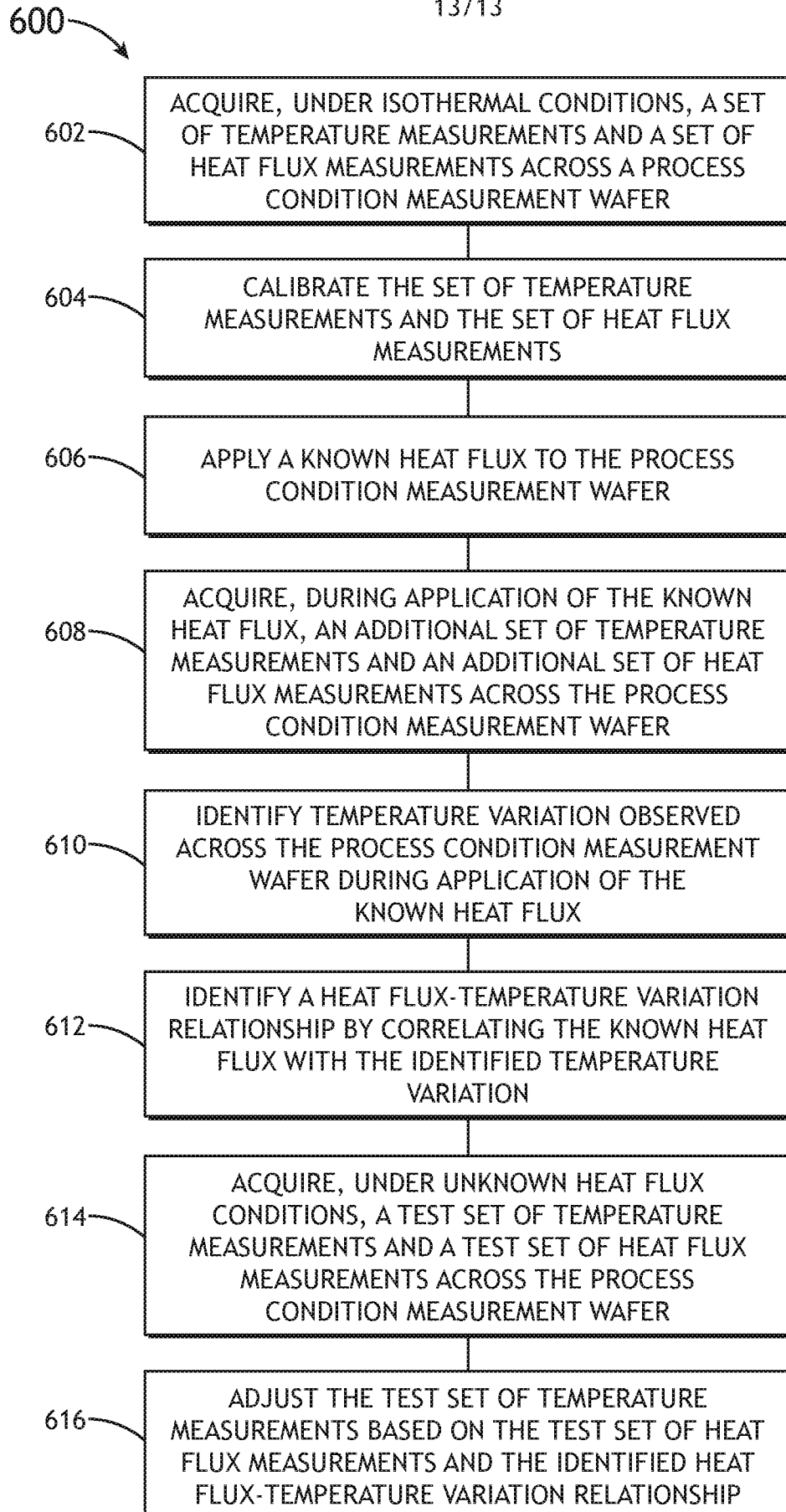


FIG.6

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/66(2006.01)i, H01L 23/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/66; G01D 11/00; G01K 7/00; G01K 7/16; G01L 27/00; G01L 9/12; G01N 21/95; H01L 23/00; H01L 23/552; H01L 23/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: test wafer, electronic component, printed circuit element, shielding layer, conductive particle, adhesive layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0056441 A1 (MEI H. SUN et al.) 05 March 2009 paragraphs [0018]–[0040], figures 1A–3F	1, 2, 9, 12–26
Y		3–8, 10, 11
A		27–29
Y	US 2016-0172309 A1 (ZHIWEI GONG et al.) 16 June 2016 paragraph [0044] and figure 10	3–8, 10, 11
A	US 2012-0269229 A1 (HISAKI ISHIDA et al.) 25 October 2012 paragraphs [0039]–[0060] and figures 1–5	1–29
A	KR 10-2017-0129602 A (KOREA RESEARCH INSTITUTE OF STANDARDS AND SCIENCE) 27 November 2017 paragraphs [0033]–[0038] and figure 2	1–29
A	US 2016-0131550 A1 (AMS INTERNATIONAL AG) 12 May 2016 paragraphs [0024]–[0026] and figure 2	1–29



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

19 December 2019 (19.12.2019)

Date of mailing of the international search report

20 December 2019 (20.12.2019)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

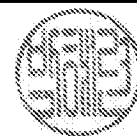
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/049833

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