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(54) Title: MULTILEVEL CONVERTER

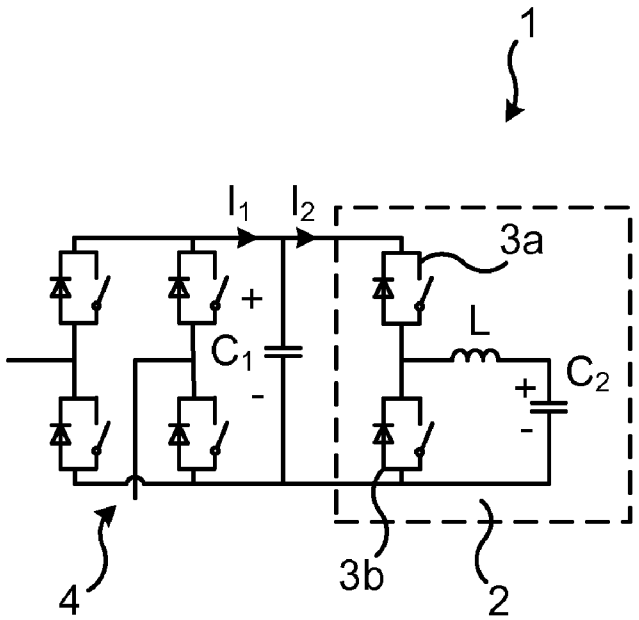

Fig. 2

(57) Abstract: The present disclosure relates to a multilevel electrical converter comprising a plurality of chain-linked cells (1). Each cell comprises a primary capacitive storage element (C_1) and a secondary capacitive storage element (C_2), connected in parallel with the primary capacitive storage element. The secondary capacitive storage element is connected in the cell via at least first and second series connected semiconductor switches (3a) and (3b) connected in parallel with the primary capacitive storage element. The first series connected semiconductor switch (3a) is connected in series with the secondary capacitive storage element and the second series connected semiconductor switch (3b) is connected in parallel with the secondary capacitive storage element. The series connected semiconductor switches are configured for high frequency switching of at least ten times the fundamental frequency of the converter.

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MULTILEVEL CONVERTER

TECHNICAL FIELD

The present disclosure relates to a multilevel electrical converter comprising a plurality of chain-linked cells wherein each cell comprises a capacitive storage element.

BACKGROUND

Multilevel converters are found in many high power applications in which medium to high voltage levels are present in the system. By virtue of their design, multilevel converters share the system voltage, eliminating the need of series connection of devices.

In particular, modular converters have become popular, where a number of cells, each containing a number of switching elements and an energy storage element in the form of a Direct Current (DC) capacitor, are connected in series to form a variable voltage source. These converters can be used for Drive, High Voltage DC (HVDC) and Flexible Alternating Current (AC) Transmission System (FACTS) applications. The converter can be a chain-link converter constructed with series connections of full-bridge (H-bridge) cells in which each cell comprises a DC capacitor in parallel with two legs of series connected switches. Alternatively, the cells may be half-bridge cells each of which comprises a single leg of series connected switches in parallel with the DC capacitor.

In a cascaded converter utilized in grid connected applications, a second order harmonic (100 Hz) component will be present on the DC link during normal operation. In the case of the modular multi-level converter (MMC) a 50 Hz component will also be present on the DC capacitors. These harmonic components significantly increase the required size of the DC capacitors. There are at least two reasons why the DC capacitance must be increased:

1. The peak voltage on each capacitor must not be not exceeded. Exceeding maximum voltages can destroy the capacitor and also increases protection

requirements in the event of a fault necessitating cell bypass (due to increased peak energy).

2. The sum of capacitor voltages at their minimum values must always be capable of synthesizing the required converter output voltages. Otherwise converter current control is affected.

These points imply that the purpose of cell capacitance is not only to absorb (and later in the fundamental cycle re-supply) 50/100Hz energy variations, but also to restrict capacitor voltages to a certain bounds. Typically these bounds are set at ±10% of the nominal DC value.

Figure 1 illustrates a squared relationship between a capacitor's energy and voltage. The top dashed line indicates the peak per unit energy (1.21) in a cell capacitor which has been sized such that the maximum instantaneous voltage is 1.1 pu. The middle dashed line shows the minimum per unit energy (0.81) in a cell capacitor which has been sized such that the minimum instantaneous voltage is 0.9 pu.

This means that each cell is absorbing/supplying an amount of energy equal to 1.21 - 0.81 = 0.4 pu. So if the full range of capacitor voltage could be utilized there is 0.81 pu extra available. If the required energy to be absorbed is 0.41, then there is a three times increase in available energy storage capacity. Stated another way, the cell capacitance could be reduced by up to a factor of 3 if the full range of capacitor voltage can be utilized. What inhibits the converters from utilizing the full range is the need to satisfy point 2 shown above.

Capacitors make up a significant proportion of total converter cost. Additionally, the physical size of a converter cell is mainly dependent on the amount of stored capacitor energy and the cell's mechanical layout. The volume occupied by semiconductor (silicon) area within the cell is quite small. Therefore savings in cell capacitance can significantly reduce cell volume and make the converter more compact.

It can be shown that for normalized phase-leg waveforms associated with the modular multi-level converter there is an indication that when the converter is required to supply both active and reactive power, the minimum capacitor voltage can be very close to the period of time when maximum converter output voltage is required. This means an extra 20% over-rating, in the number of cells in each phase-leg, would be required due to effect of capacitor voltage ripple.

SUMMARY

It is an objective of the present invention to provide a multilevel converter in which can utilize a larger range of the capacitor voltage, thereby allowing the cells to be made smaller and more compact.

The present invention reduces required cell capacitance. To achieve this, a new type of cell is used in multilevel converter topologies. The typical single phase AC/DC converters such as full-bridge and half-bridge cells are modified to include an extra sub-unit comprising an additional leg of series connected switches and a secondary capacitive storage element (e.g. a capacitor) which is connected in parallel with the regular capacitive storage element (typically a DC capacitor), herein called the primary capacitive storage element.

US 2003/133317 discloses a converter circuit with parallel capacitors. However, the circuit is not part of a multilevel converter, nor are the semiconductor switches configurable for high-power applications where losses need to be reduces or for the high switching frequencies required for the present invention.

The extra leg of switches is responsible for controlling the amount of stored energy in the secondary capacitive storage element. In order to achieve this control, the switches of the leg of the sub-unit are configured for a much higher switching frequency than the fundamental frequency (e.g. 50 Hz) which the other switches of the cell are typically configured for. The higher switching frequency may e.g. be at least ten times the fundamental frequency,

such as at least 500 Hz or 1 kHz. Such high switching frequencies are not possible without intolerable losses when using regular semiconductor materials which are not suitable for high switching frequencies. A small inductor may also be comprised in the sub-unit to effectively control the current flow between the primary and secondary capacitive storage elements.

According to an aspect of the present invention, there is provided a multilevel electrical converter comprising a plurality of chain-linked cells. Each cell comprises a primary capacitive storage element and a secondary capacitive storage element, connected in parallel with the primary capacitive storage element. The secondary capacitive storage element is connected in the cell via at least first and second series connected semiconductor switches (3a, 3b) connected in parallel with the primary capacitive storage element. The first series connected semiconductor switch is connected in series with the secondary capacitive storage element and the second series connected semiconductor switch is connected in parallel with the secondary capacitive storage element. The series connected semiconductor switches are configured for high frequency switching of at least ten times the fundamental frequency of the converter.

According to another aspect of the present invention, there is provided a use of a cell in an electrical multilevel converter. The cell comprises a primary capacitive storage element and a secondary capacitive storage element, connected in parallel with the primary capacitive storage element. The secondary capacitive storage element is connected in the cell via at least first and second series connected semiconductor switches connected in parallel with the primary capacitive storage element. The first series connected semiconductor switch is connected in series with the secondary capacitive storage element and the second series connected semiconductor switch is connected in parallel with the secondary capacitive storage element. The series connected semiconductor switches are operating at a switching frequency which is at least ten times the fundamental frequency of the converter.

In some embodiments, the series connected semiconductor switches each comprises a wide-bandgap semiconductor material, e.g. having a band gap of at least three electron volts, such as silicon carbide, aluminium nitride, gallium nitride or boron nitride, preferably silicon carbide.

In some embodiments, the series connected semiconductor switches are configured for high frequency switching of at least 1 kHz.

In some embodiments, each cell is a full-bridge or half-bridge cell.

In some embodiments, each cell comprises an inductor L connected in series with the secondary capacitive storage element C_2.

In some embodiments, the converter has a power rating of at least 100 MW, e.g. for use in a FACTS converter or medium voltage drive, or of at least 1 GW, e.g. for use in a HVDC converter.

In some embodiments, the converter has a voltage rating of at least 50 kV, e.g. for use in a FACTS converter or medium voltage drive, or of at least 300 kV, e.g. for use in a HVDC converter.

It is to be noted that any feature of any of the aspects may be applied to any other aspect, wherever appropriate. Likewise, any advantage of any of the aspects may apply to any of the other aspects. Other objectives, features and advantages of the enclosed embodiments will be apparent from the following detailed disclosure, from the attached dependent claims as well as from the drawings.

Generally, all terms used in the claims are to be interpreted according to their ordinary meaning in the technical field, unless explicitly defined otherwise herein. All references to "a/an/the element, apparatus, component, means, step, etc." are to be interpreted openly as referring to at least one instance of the element, apparatus, component, means, step, etc., unless explicitly stated otherwise. The steps of any method disclosed herein do not have to be performed in the exact order disclosed, unless explicitly stated. The use of “first”, “second” etc. for different features/components of the present

disclosure are only intended to distinguish the features/components from other similar features/components and not to impart any order or hierarchy to the features/components.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments will be described, by way of example, with reference to the accompanying drawings, in which:

Fig 1 illustrates a squared relationship between a capacitor's energy and voltage in a converter cell.

Fig 2 is a schematic circuit diagram of an embodiment of a full-bridge converter cell in accordance with the present invention.

Fig 3 is a schematic circuit diagram of an embodiment of a half-bridge converter cell in accordance with the present invention.

Fig 4 is a schematic circuit diagram of an embodiment of a converter in cascaded wye (Y) topology of full-bridge cells in accordance with the present invention.

Fig 5 is a schematic circuit diagram of an embodiment of an MMC topology with decoupling power fluctuation half-bridge cells in accordance with the present invention.

DETAILED DESCRIPTION

Embodiments will now be described more fully hereinafter with reference to the accompanying drawings, in which certain embodiments are shown. However, other embodiments in many different forms are possible within the scope of the present disclosure. Rather, the following embodiments are provided by way of example so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Like numbers refer to like elements throughout the description.

The capacitive storage elements discussed herein may e.g. be capacitors, but may alternatively be any other known capacitive storage element or a combination thereof.

Figure 2 illustrates an embodiment of a cell 1 for a multilevel converter. The cell 1 comprises a regular full-bridge unit 4, comprising two legs of series connected switches in parallel with a primary capacitive storage element C_1, and a sub-unit 2 in accordance with the present invention. The sub-unit 2 comprises a secondary capacitive storage element C_2 in parallel with the primary capacitive storage element C_1, as well as an additional (third) leg of series connected semiconductor switches 3. In the embodiment of figure 2, the additional leg of series connected semiconductor switches 3 comprises two (and only two) switches, a first switch 3a connected in series with the secondary capacitive storage element C_2 and a second switch 3b connected in parallel with the secondary capacitive storage element C_2. The switches 3 controls the current flow and voltages within the cell 1, especially between the primary and secondary capacitive storage elements. An inductor L may also be comprised in the sub-unit 2, connected in series with the secondary capacitor C_2, to effectively control the current flow between the primary and secondary capacitive storage elements.

Figure 3 illustrates another embodiment of a cell 1 for a multilevel converter. The cell 1 comprises a regular half-bridge unit 4, comprising one leg of series connected switches in parallel with a primary capacitive storage element C_1, and a sub-unit 2 in accordance with the present invention and as also discussed in relation to figure 2. The sub-unit 2 comprises a secondary capacitive storage element C_2 in parallel with the primary capacitive storage element C_1, as well as an additional (third) leg of series connected semiconductor switches 3. In the embodiment of figure 3, as also of figure 2, the additional leg of series connected semiconductor switches 3 comprises two (and only two) switches, a first switch 3a connected in series with the secondary capacitive storage element C_2 and a second switch 3b connected in parallel with the secondary capacitive storage element C_2. The switches 3 controls the current flow and voltages within the cell 1, especially between the

primary and secondary capacitive storage elements. An inductor L may also be comprised in the sub-unit 2 to effectively control the current flow between the primary and secondary capacitive storage elements.

Thus, the extra leg of switches 3 is responsible for controlling the amount of stored energy in the secondary capacitive storage element C_2. In order to achieve this control, the switches of the leg of the sub-unit 2 are configured for a much higher switching frequency than the fundamental frequency (which may be e.g. 50 Hz) which the other (regular full-bridge) switches of the cell are typically configured for. The higher switching frequency may e.g. be at least ten times the fundamental frequency, such as at least 500 Hz or 1 kHz.

With reference to figures 2 and 3, An advantage of the proposed cells 1 is to control current I_2 such that the secondary capacitor C_2 absorbs the majority of the first and second order harmonics (50 and 100 Hz energy variations in case of a fundamental frequency of 50 Hz) while the primary capacitor C_1 (only) performs a filtering function. In this sense, the extra switching leg of the sub-unit 2 can be thought of as performing a voltage boosting function. In this way, the voltage appearing at the terminals of the cell may always be (or be close to) the nominal DC value (or zero when bypassed), even when the voltage on the secondary capacitor C_2 varies between the nominal DC value and 0.

The switches 3 of the additional leg of the sub-unit 2 may need to be switched sufficiently fast to minimize the size of the inductance of the inductor L, to the range 20-40 μH. Otherwise, the total stored energy in the cell may only move from the primary capacitor C_1 to the inductor L. This may require switching frequencies of one or a few kHz or higher. These frequencies may require wide-bandgap devices to keep semiconductor losses at a reasonable level. Thus, in some embodiments of the present invention, the series connected semiconductor switches 3 each comprises a wide-bandgap semiconductor material, e.g. having a band gap of at least three electron volts (eV), such as silicon carbide (SiC), aluminium nitride (AlN), gallium nitride

(GaN) or boron nitride (BN), preferably silicon carbide. Silicon carbide is especially preferred since it has properties making it suitable for high switching frequencies with low losses, but any other wide-bandgap material may also be suitable.

Figure 4 illustrates an embodiment of a why connected converter 10 with full-bridge cells 1 similar to the full-bridge cells shown in figure 2, where each cell 1 comprises a sub-unit 2 as discussed in relation to figures 2 and 3.

The present invention utilizes an extra leg in each half or full bridge cell of the modular converters 10 for e.g. FACTS or HVDC applications to achieve any of the following benefits:

- Reduce cell capacitance by a factor of 2-3. With associated cost and volume savings.

- Possibility to maintain output cell voltage at nominal value throughout fundamental cycle. Meaning a possible 10-20% reduction in the number of cascaded cells 1 needed.

- Extra control loop for decoupling the power fluctuation.

- Significantly reduce protection requirements during cell bypass operation.

To provide these benefits, the semiconductor area within each cell 1 may be increased. With extra semiconductor area, the cells may also incur higher losses why wide bandgap semiconductor materials may be used in the additional leg of the sub-unit 2 to reduce these higher losses. The semiconductor area and conduction losses in the full- bridge version of the cell 1 may increase, which may be mitigated by the cell's ability to maintain nominal output voltage and thereby reduce the number of required cascaded cells.

Example 1

Simulations for an 11-level delta connected cascaded static synchronous compensator (StatCom) converter 10 have been performed. In this simulation the H-bridge cell StatCom appears as a purely capacitive load to the three phase distribution network. In the converter 10 the chain-link connected cells 1 are as depicted in figure 2.

The output voltage and current, as well as primary and secondary capacitor C_1 and C_2 voltages, from a phase leg with the cells 1 of figure 2 were compared with a phase leg with regular full-bridge cells (without the sub unit 2). From the magnitude of the ripple on the regular phase full-bridge voltages it could be seen that the full-bridge capacitors have been sized so that the ripple has a ±10% bounds, the cell capacitance used is 8 mF.

The total cell capacitance used in the phase leg with cells 1 of figure 2 (according to the invention) was 3.5 mF, i.e. $C_1+C_2 = 3.5$ mF. This means that the cell capacitance has been reduced by a factor of 2.3. Given that the peak voltage on the capacitance remains constant, this means that the total energy in the capacitors has also reduced by a factor of 2.3.

Even though the primary capacitors C_1 are only rated at 0.6 mF, the capacitor voltages are regulated between 2700 V and 2800 V throughout the fundamental cycle. The secondary capacitors C_2 absorb the energy variations such that their voltages vary between 2800 V and 1200 V, making a more effective use of the energy storage of the capacitors.

It could also be seen that as the duty cycle decreases the peak of current I_2 increases. This is due to the relationship between input and output currents in a DC-DC converter:

$$I_{in} = DI_{out}$$

where D is the duty cycle.

The peak value of I_2 may be reduced by controlling the secondary capacitors C_2 to absorb/supply the average value of absorbed/supplied cell energy over each 5 ms period, instead of controlling I_1 to be equal to I_2 at all times. Employing this strategy may result in more voltage variation on the primary capacitors C_1. So, a trade-off between peak current rating of the semiconductors 3 used in the additional leg of the sub-unit 2 and the size of the primary capacitors C_1 occurs. Note, however, that the reduction factor of total capacitance may remain in the range 2-3.

Example 2

In this example, the effectiveness of a half-bridge cell 1 in accordance with the present invention is studied when used in the MMC topology shown in figure 5 (with three phase legs, each having two arms) in which each half-bridge cell comprises the sub-unit 2 as discussed in relation to figures 2 and 3. The half-bridge cells 1 are as shown in figure 3, but reference numerals are only given for one of the cells 1 to simplify figure 5.

An MMC converter 10 with the parameters shown in Table 1 is setup in the MATLAB/Simulink environment. A hysteresis current control has been applied to control the inductor and current. The reference for the hysteresis current has been generated by the average current follows toward the DC link. This way, the fundamental current is redirected toward the secondary capacitors C_2.

Parameter	Value
DC voltage	12 kV
Number of cells per arm	6
Cell capacitance of the DC capacitor when the regular cell is used	6 mF
Cell capacitance of the primary capacitor C_1 when the cell 1 of figure 3 is used	1 mF
Cell capacitance of the secondary capacitor C_2 when the cell 1 of figure 3 is used	5 mF
Active power drawn from the converter 10	2.45 MW
Power factor	~1

Table 1: Simulation parameters of the MMC 10 with the cell 1 of figure 3, and compared with a regular half-bridge cell (without the sub-unit 2).

Simulation results showed an overvoltage of 150 V (7.5%) on each regular (also called conventional) cell when operating at the operation point mentioned in Table 1. Running the MMC 10 with the cell 1 of the present invention (also called new cell) at the same point of operation it was observed that the peak voltage on the primary cell capacitors C_1 is 2150 V (107.5%) and 1400 V on the secondary capacitors C_2. Only considering the peak voltage that each capacitor must withstand, the energy requirement of the MMC when the new cell and when conventional cell are used can be simplified as follows:

$$E_{conventional\ cell} = \frac{1}{2}cv^2 = \frac{1}{2} \times 6e-3 \times (2.15e3)^2 = 13867.5\ J$$

$$E_{new\ cell} = \frac{1}{2}c_1 v_1^2 + \frac{1}{2}c_2 v_2^2 = \frac{1}{2} \times 1e-3 \times (2.15e3)^2 + \frac{1}{2} \times 5e-3 \times (1.4e3)^2 = 7211.25\ J$$

It was observed that in an MMC 10 with the novel cell 1, the minimum required energy storage is about 50% of that of an MMC with the conventional cell. Therefore, the novel cell 1 may reduce the minimum energy storage requirement of various converters 10.

Example 3 – Cell Protection

Protection of a cell 1 is dependent on the total stored energy in the cell capacitor(s). If a semiconductor switch fails, the cell capacitor(s) need to be discharged and the cell bypassed. In the cell 1 of the present invention there is a smaller amount of energy in the primary capacitor C_1 since the capacitance is reduced by e.g. 90% of the typical full-bridge value of a regular cell. The peak energy in the secondary capacitor C_2 may also be reduced by at least 50% in comparison with the capacitance in a regular cell (without a sub-unit 2). Additionally, the inductor L limits the rate of discharge which reduces stresses on the semiconductor switches during an internal cell fault.

The present disclosure has mainly been described above with reference to a few embodiments. However, as is readily appreciated by a person skilled in the art, other embodiments than the ones disclosed above are equally possible within the scope of the present disclosure, as defined by the appended claims.

CLAIMS

1. A multilevel electrical converter (10) comprising a plurality of chain-linked cells (1);

wherein each cell comprises a primary capacitive storage element (C_1) and a secondary capacitive storage element (C_2), connected in parallel with the primary capacitive storage element;

wherein the secondary capacitive storage element is connected in the cell via at least first and second series connected semiconductor switches (3a, 3b) connected in parallel with the primary capacitive storage element;

wherein the first series connected semiconductor switch (3a) is connected in series with the secondary capacitive storage element and the second series connected semiconductor switch (3b) is connected in parallel with the secondary capacitive storage element;

wherein the series connected semiconductor switches are configured for high frequency switching of at least ten times the fundamental frequency of the converter.

2. The converter of claim 1, wherein the series connected semiconductor switches (3a, 3b) each comprises a wide-bandgap semiconductor material, e.g. having a band gap of at least three electron volts, such as silicon carbide, aluminium nitride, gallium nitride or boron nitride, preferably silicon carbide.

3. The converter of claim 1 or 2, wherein the series connected semiconductor switches (3a, 3b) are configured for high frequency switching of at least 1 kHz.

4. The converter of any preceding claim, wherein each cell is a full-bridge or half-bridge cell.

5. The converter of any preceding claim, wherein each cell comprises an inductor (L) connected in series with the secondary capacitive storage element (C_2).

6. The converter of any preceding claim, wherein the converter (10) has a power rating of at least 100 MW.

7. The converter of any preceding claim, wherein the converter (10) has a voltage rating of at least 50 kV.

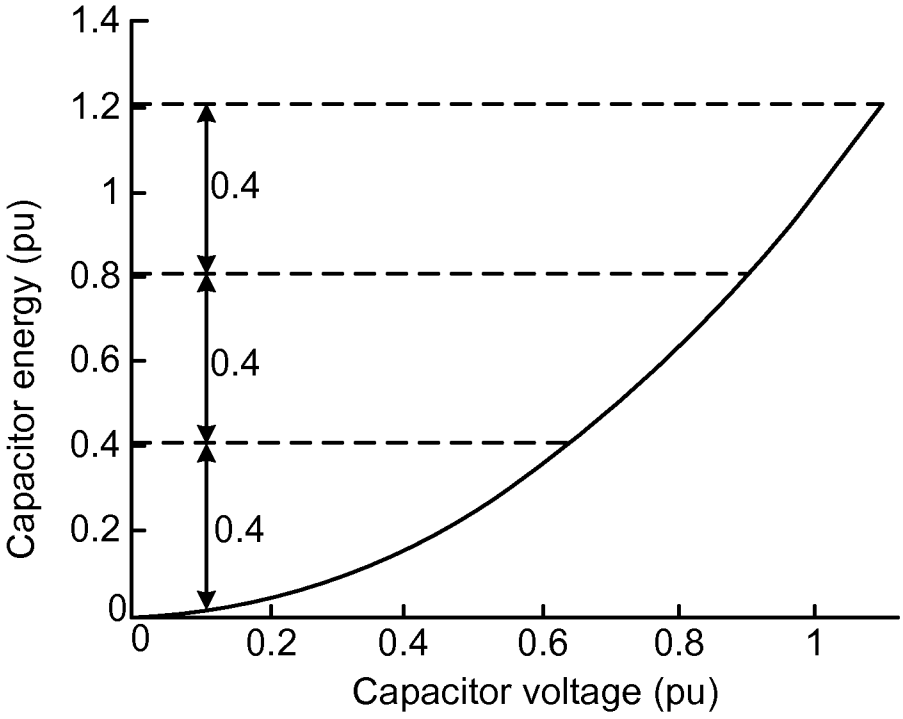
8. Use of a cell (1) in an electrical multilevel converter (10);

wherein the cell comprises a primary capacitive storage element (C_1) and a secondary capacitive storage element (C_2), connected in parallel with the primary capacitive storage element;

wherein the secondary capacitive storage element is connected in the cell via at least first and second series connected semiconductor switches (3a, 3b) connected in parallel with the primary capacitive storage element;

wherein the first series connected semiconductor switch (3a) is connected in series with the secondary capacitive storage element and the second series connected semiconductor switch (3b) is connected in parallel with the secondary capacitive storage element;

wherein the series connected semiconductor switches are operating at a switching frequency which is at least ten times the fundamental frequency of the converter.


1.4
1.2
1
0.8
0.6
0.4
0.2
0
0.4
0.4
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Capacitor energy (pu)
0
0.2
0.4
0.6
0.8
1
Capacitor voltage (pu)

Fig. 1

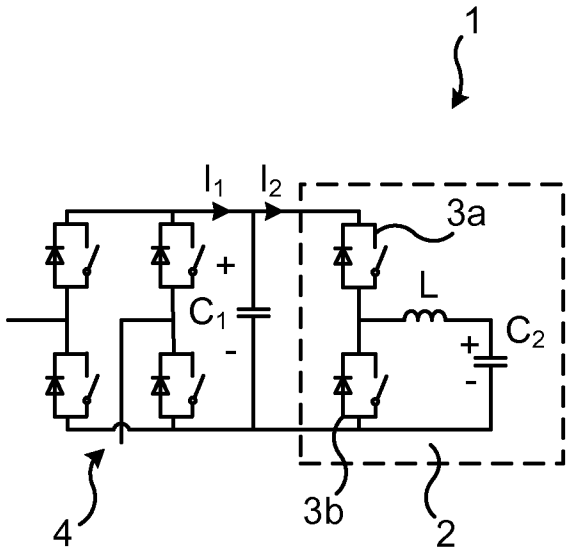
1
I1
I2
3a
+
C1
-
L
C2
+
-
4
3b
2

Fig. 2

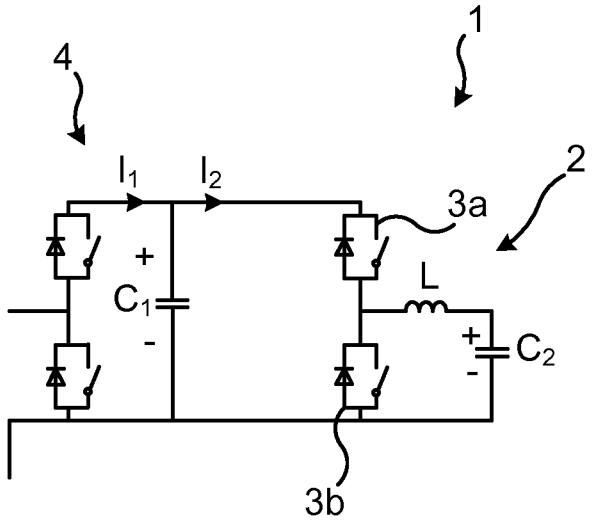

Fig. 3

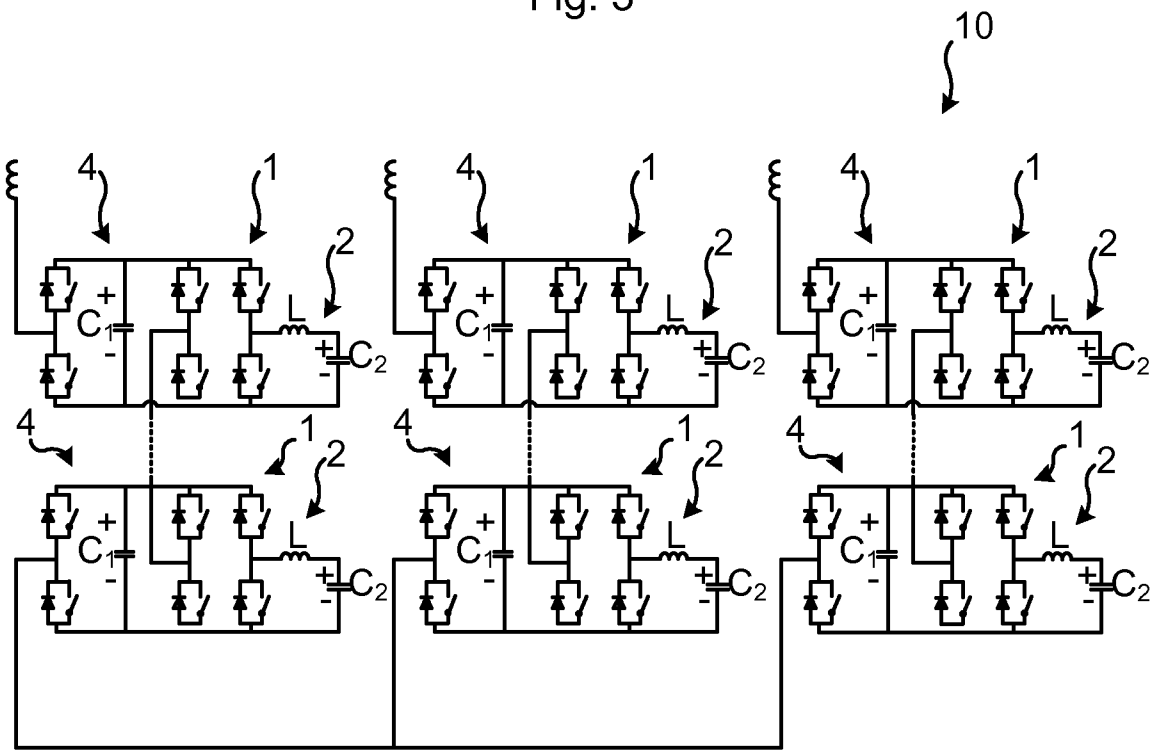

Fig. 4

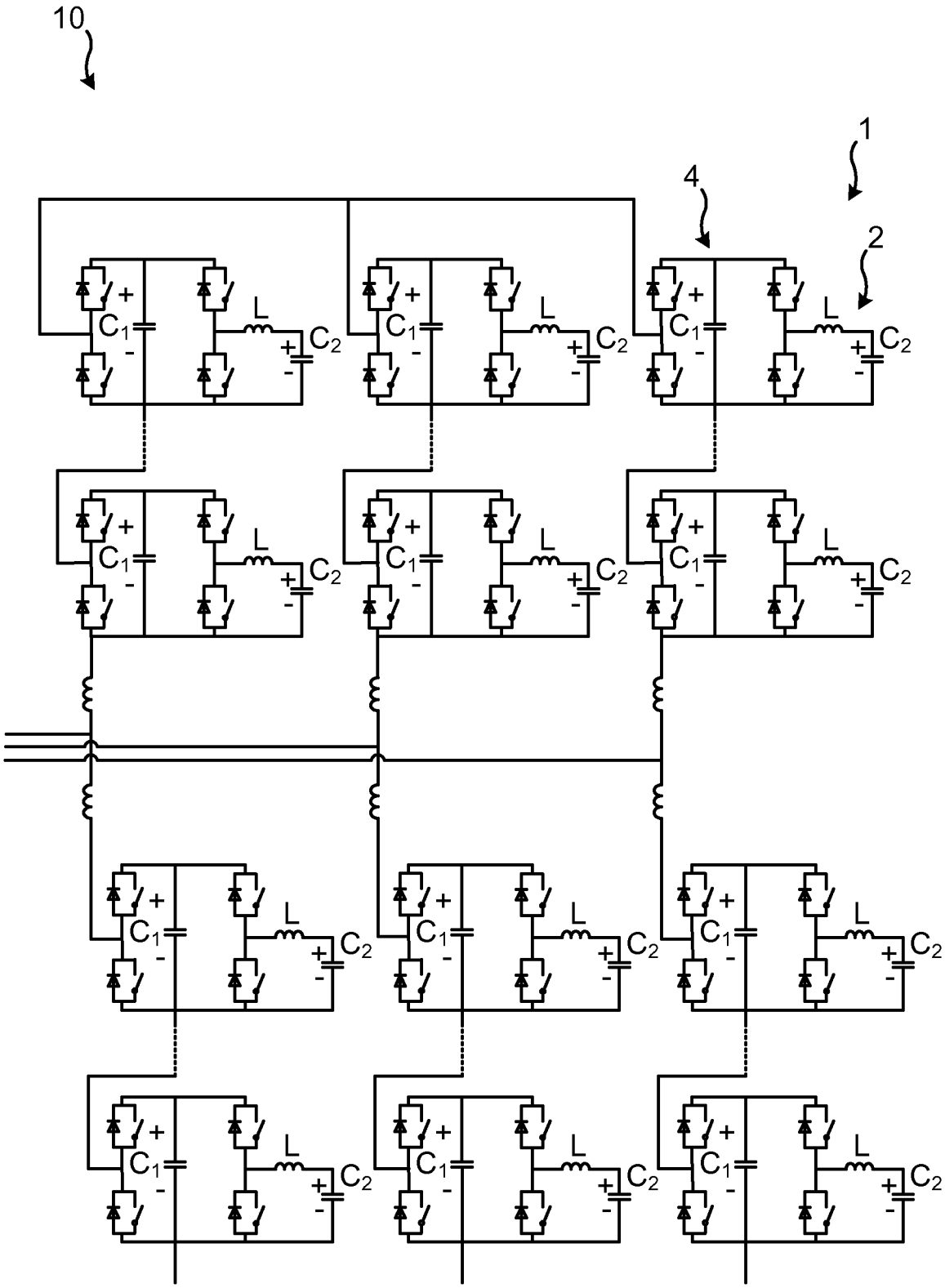

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/065144

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M7/483 H02M1/15
ADD. H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 525 483 A1 (INGETEAM TECHNOLOGY S A [ES]) 21 November 2012 (2012-11-21) figures 1, 2 paragraph [0020] - paragraph [0023] paragraph [0025] - paragraph [0029] -----	1-8
X	WO 2011/120679 A2 (UNIV HANNOVER [DE]; MERTENS AXEL [DE]; BARUSCHKA LENNART [DE]) 6 October 2011 (2011-10-06) page 9, line 1 - page 10, line 27 page 11, line 14 - page 12, line 25 figures 1, 2 -----	1-8
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2016	25/01/2016

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/065144

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