(19) **United States**
(12) **Patent Application Publication**
Itoi et al.
(10) **Pub. No.: US 2008/0203527 A1**
(43) **Pub. Date: Aug. 28, 2008**

(54) **SEMICONDUCTOR DEVICE HAVING GATE ELECTRODE CONNECTION TO WIRING LAYER**

(75) Inventors: **Kazuhisa Itoi**, Kohtoh-ku (JP); **Masakazu Sato**, Kohtoh-ku (JP); **Tatsuya Ito**, Kohtoh-ku (JP)

Correspondence Address:
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW, SUITE 700
WASHINGTON, DC 20036 (US)

(73) Assignee: **FUJIKURA LTD.**, Tokyo (JP)

(21) Appl. No.: **12/081,960**

(22) Filed: **Apr. 24, 2008**

Related U.S. Application Data

(63) Continuation of application No. 11/189,134, filed on Jul. 26, 2005.

(30) **Foreign Application Priority Data**

Jul. 29, 2004 (JP) 2004-221785
Oct. 18, 2004 (JP) 2004-302696

Publication Classification

(51) **Int. Cl.**
H01L 29/00 (2006.01)

(52) **U.S. Cl.** **257/531**; 257/E23.141

(57) **ABSTRACT**

A semiconductor device includes a semiconductor substrate having an electrode formed above a surface thereof; a first insulating resin layer that is provided over the semiconductor substrate and has a first opening defined at a position corresponding to the electrode; a first wiring layer that is provided on the first insulating resin layer and is connected to the electrode through the first opening; a second insulating resin layer provided over the first insulating resin layer and the first wiring layer, the second insulating resin layer having a second opening that is defined at a position different from the position of the first opening in a direction of the surface of the semiconductor substrate; and a second wiring layer that is provided on the second insulating resin layer and is connected to the first wiring layer through the second opening, wherein the second wiring layer includes an induction element, and a sum of a thickness of the first insulating resin layer and a thickness of the second insulating resin layer is not less than 5 μm and not more than 60 μm.

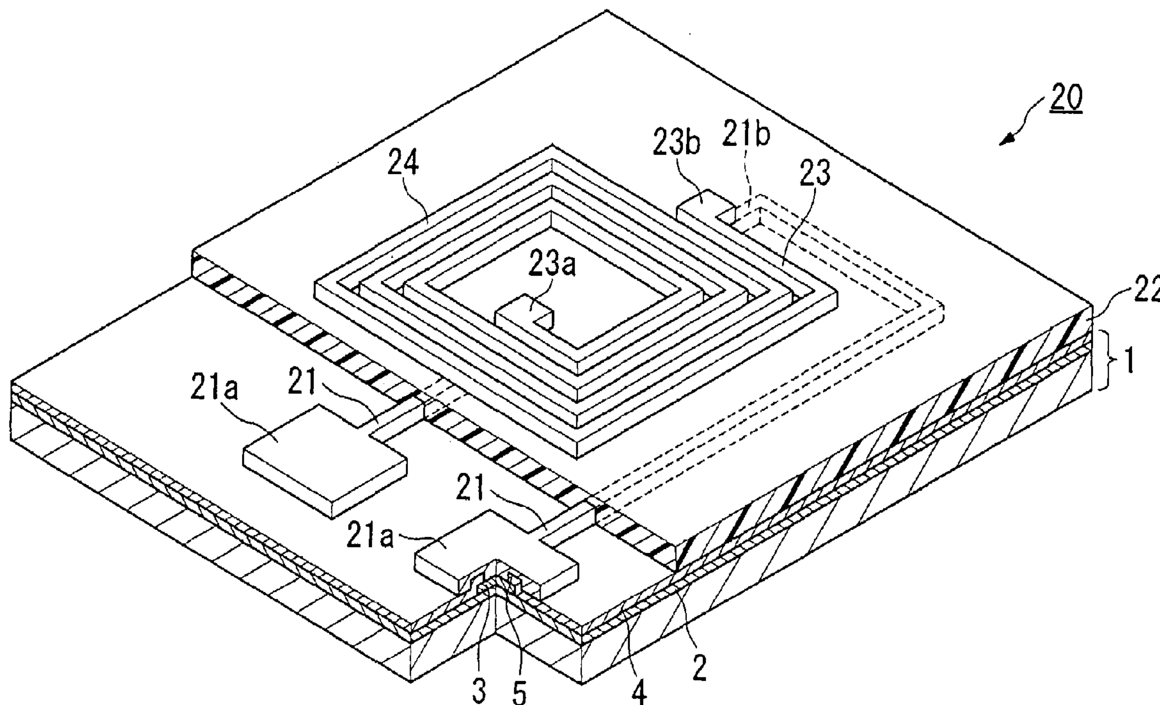
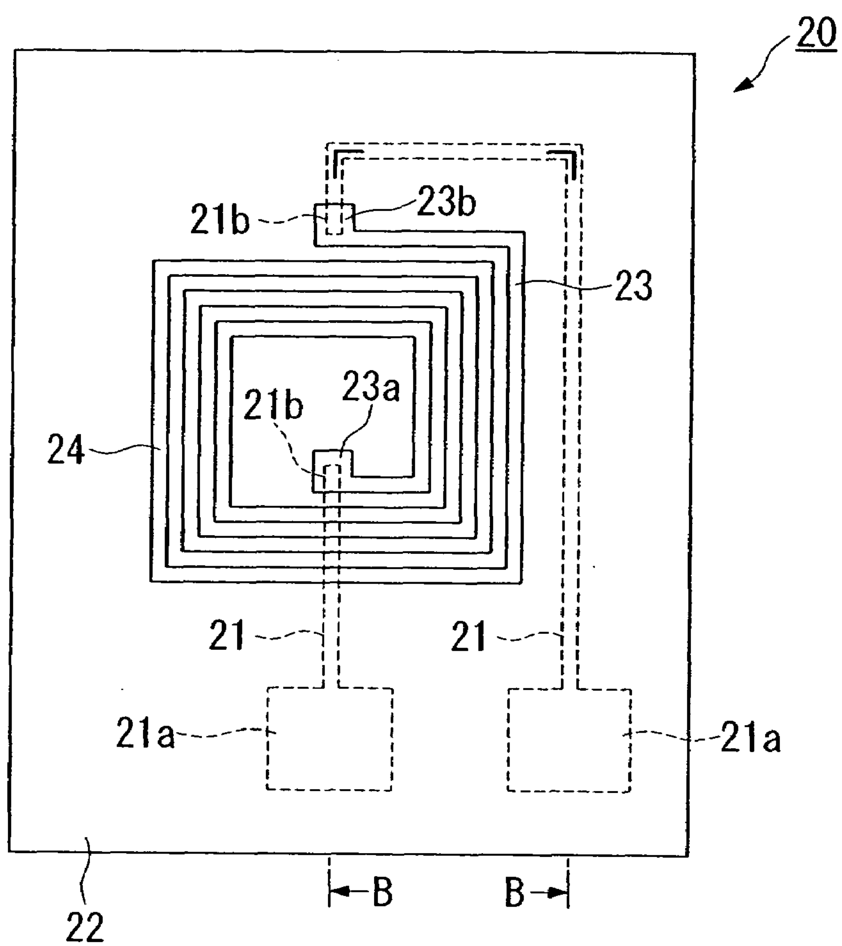


FIG. 1



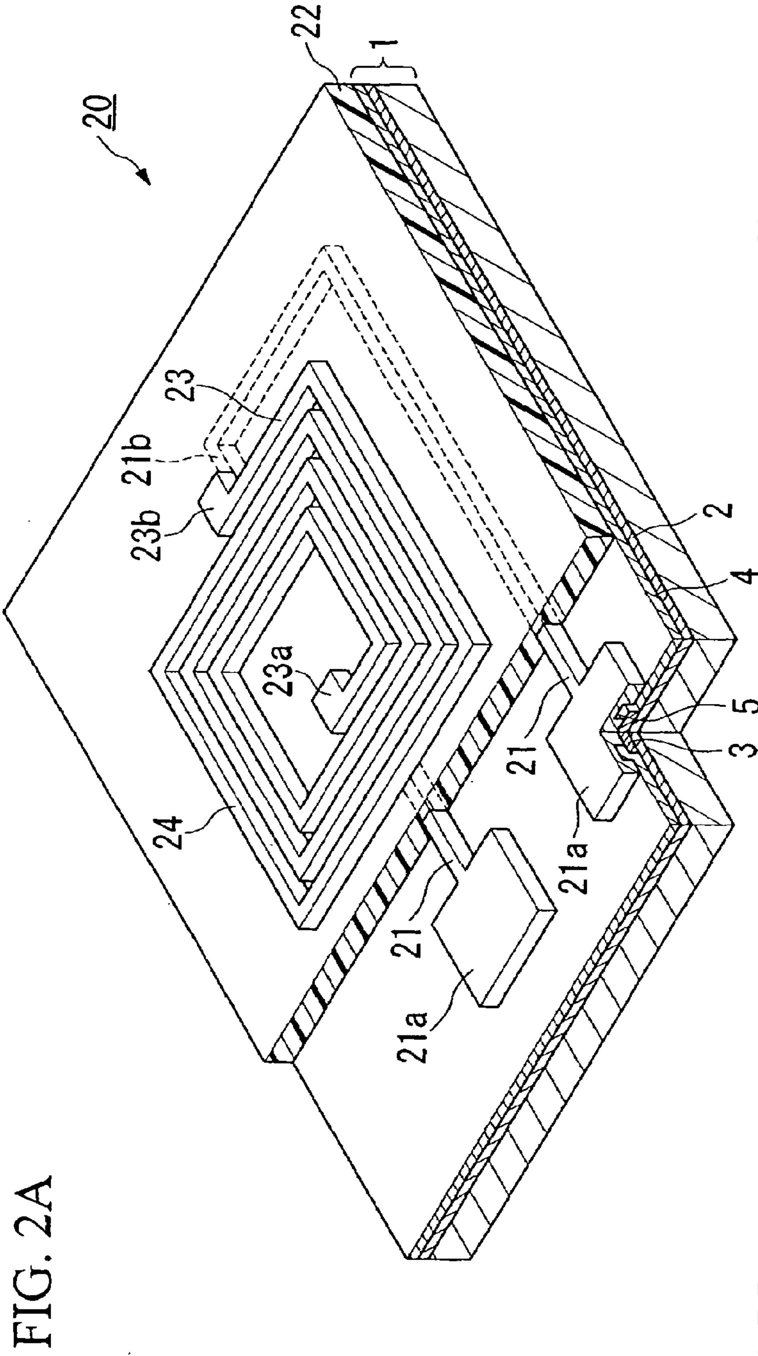


FIG. 2A

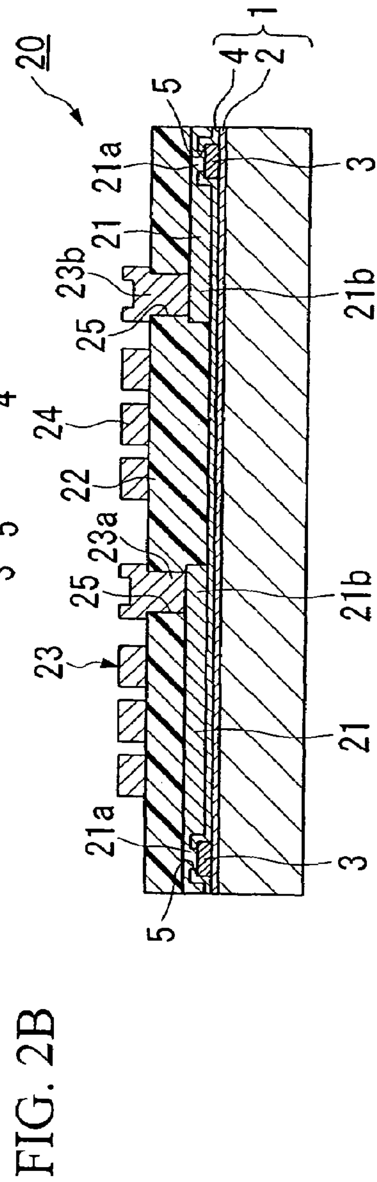


FIG. 2B

FIG. 3A

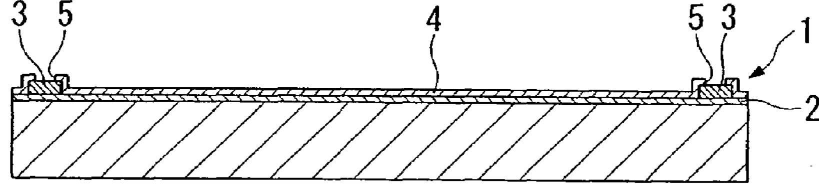


FIG. 3B

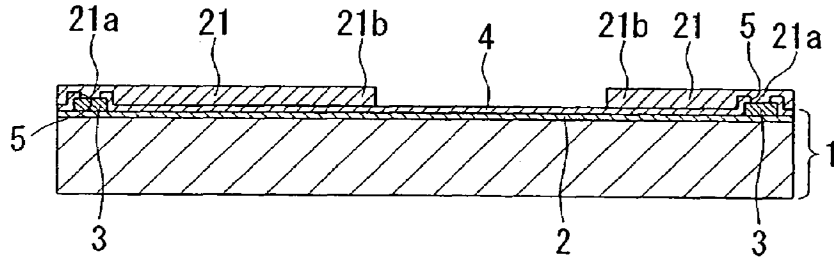


FIG. 3C

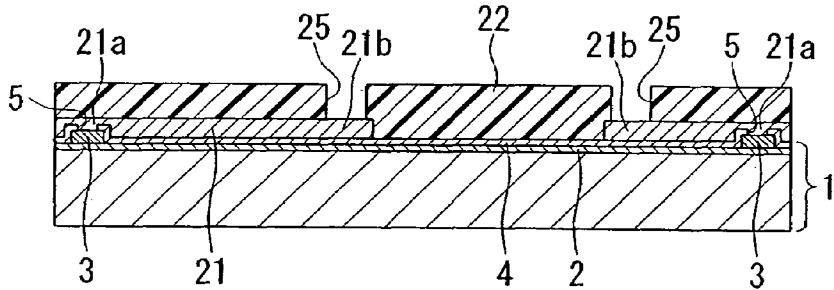


FIG. 3D

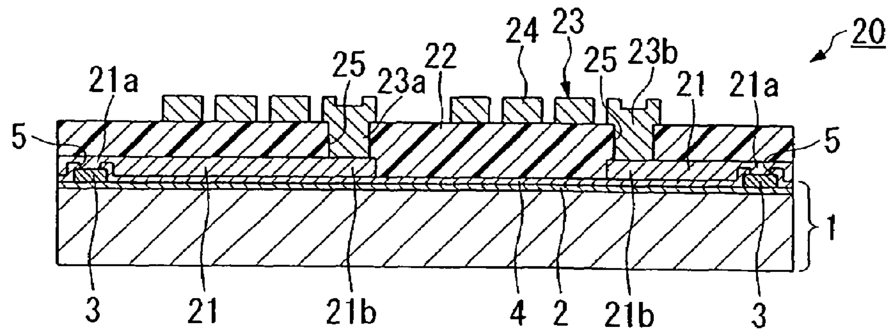


FIG. 4A

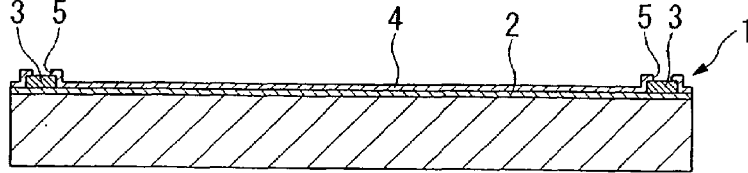


FIG. 4B

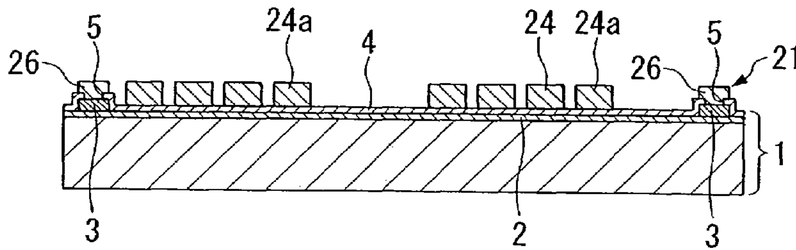


FIG. 4C

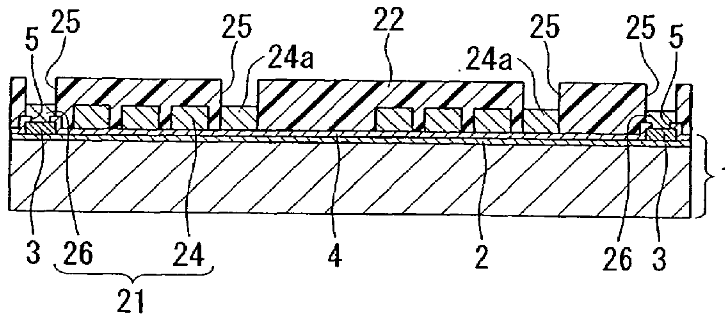


FIG. 4D

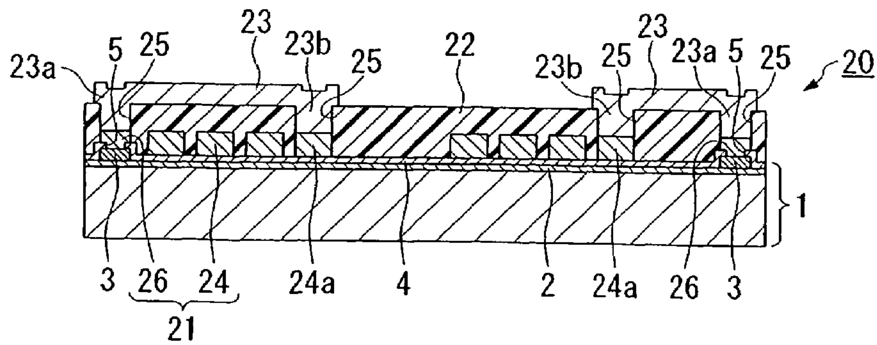


FIG. 5

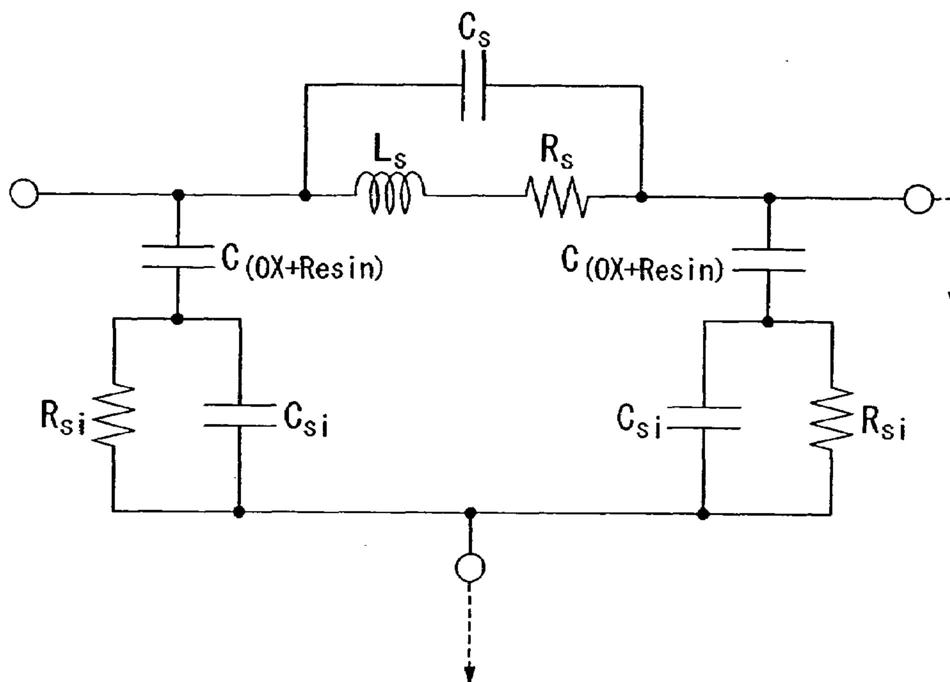
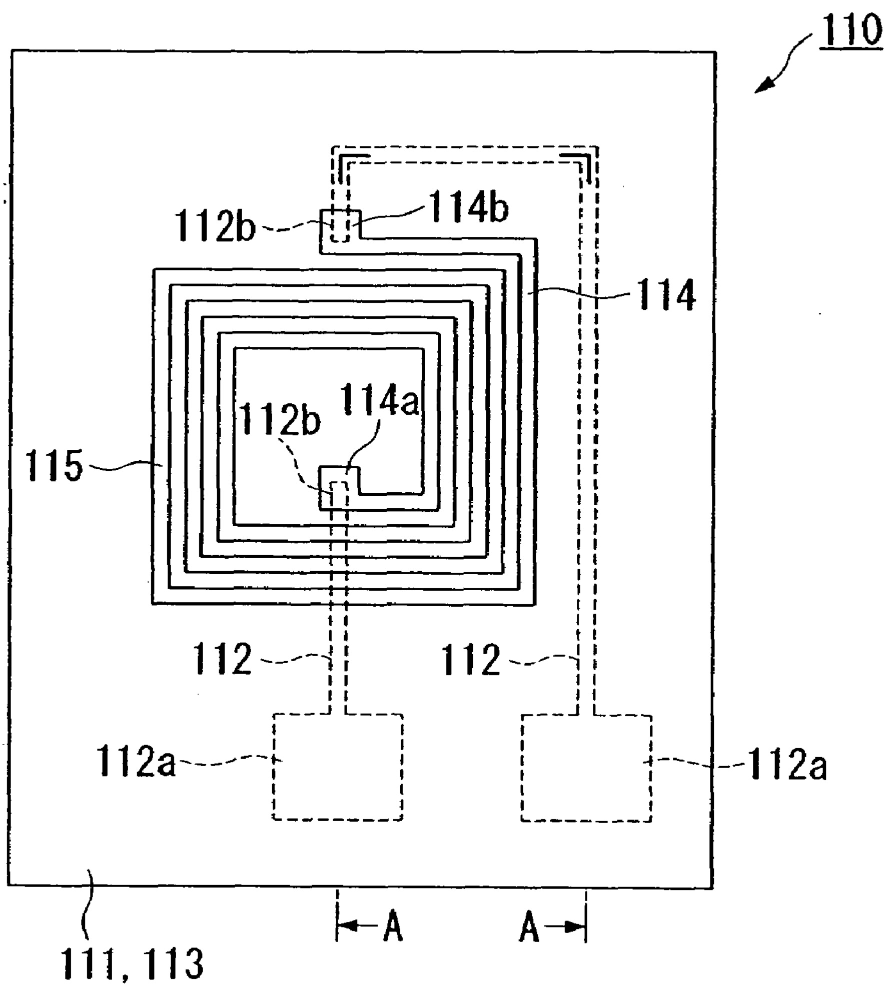


FIG. 6



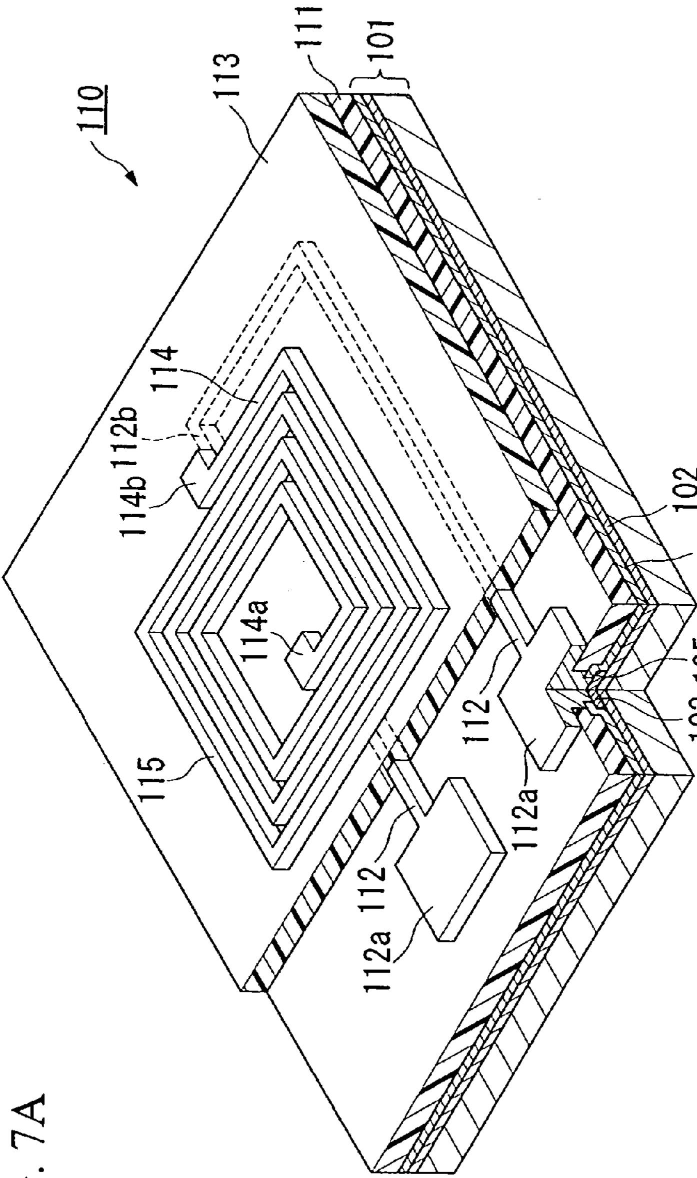


FIG. 7A

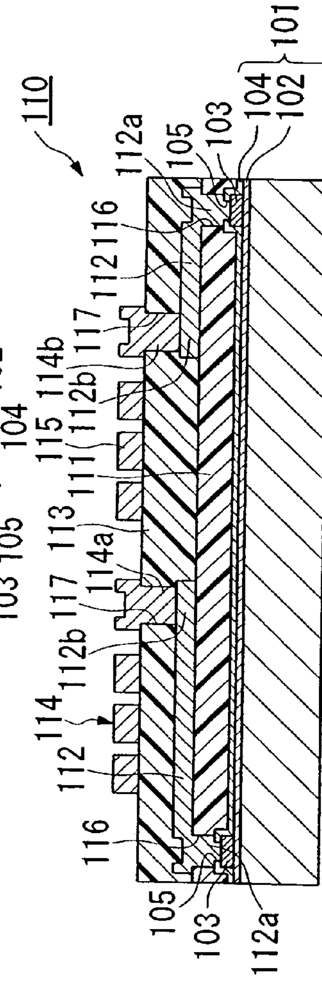


FIG. 7B

FIG. 8A

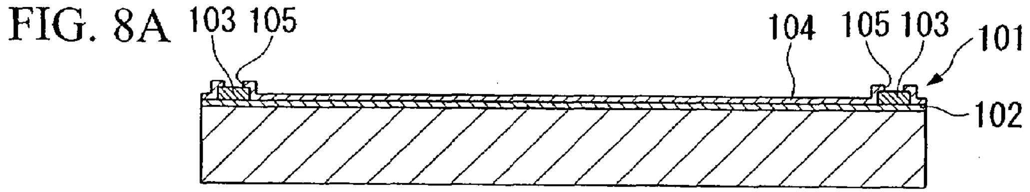


FIG. 8B

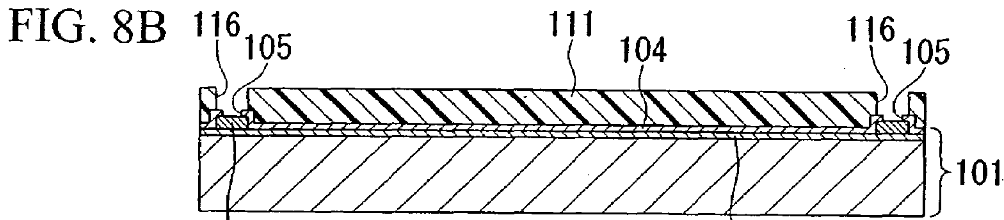


FIG. 8C

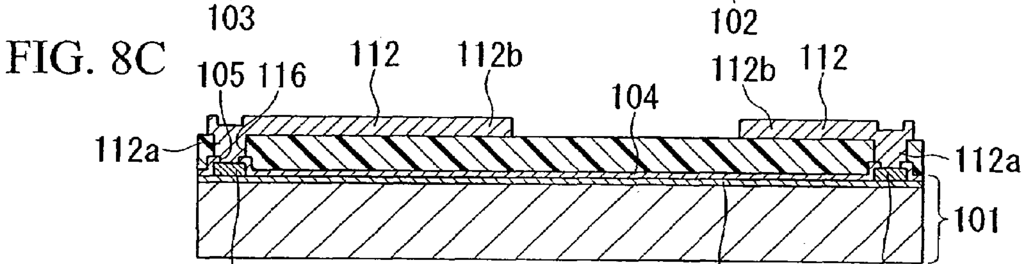


FIG. 8D

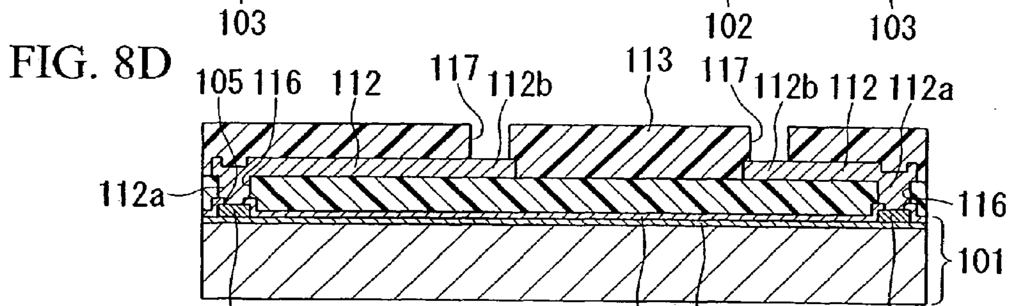


FIG. 8E

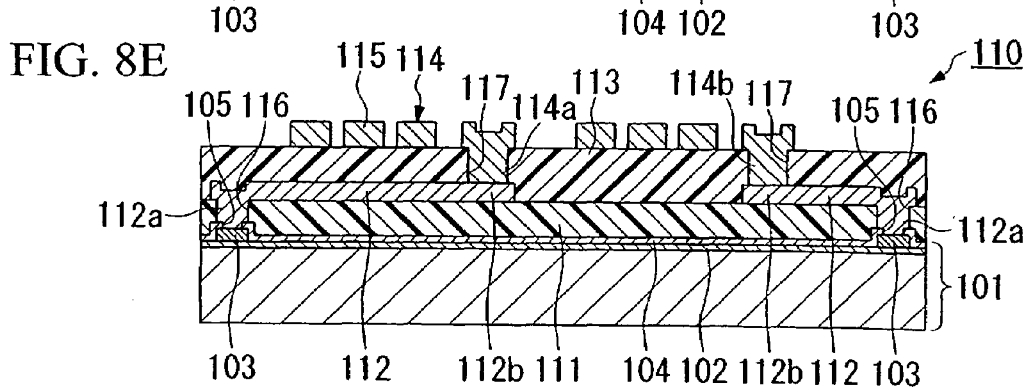


FIG. 9

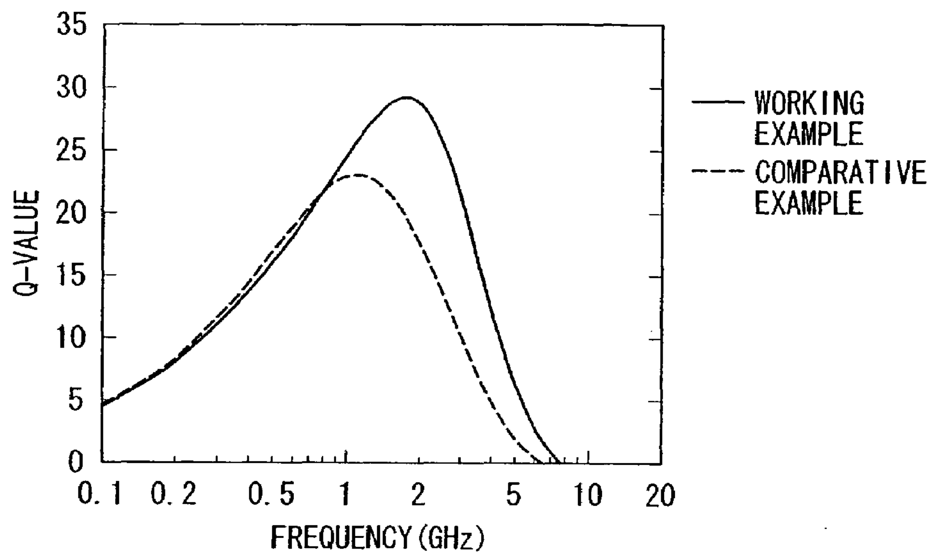


FIG. 10

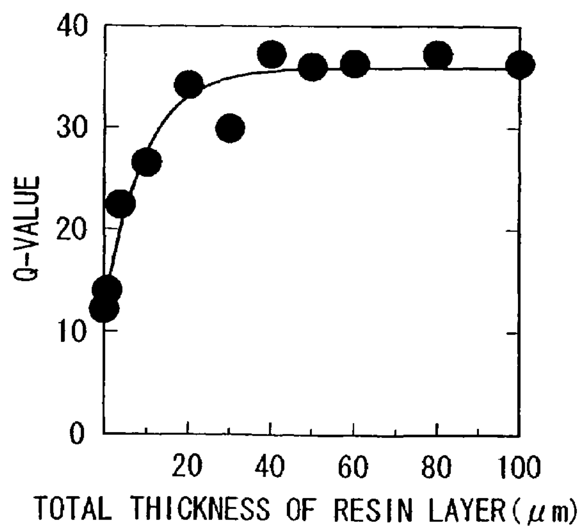


FIG. 11

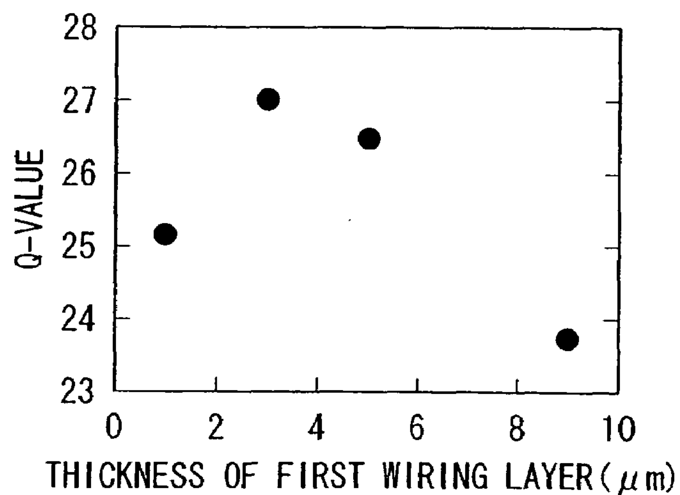
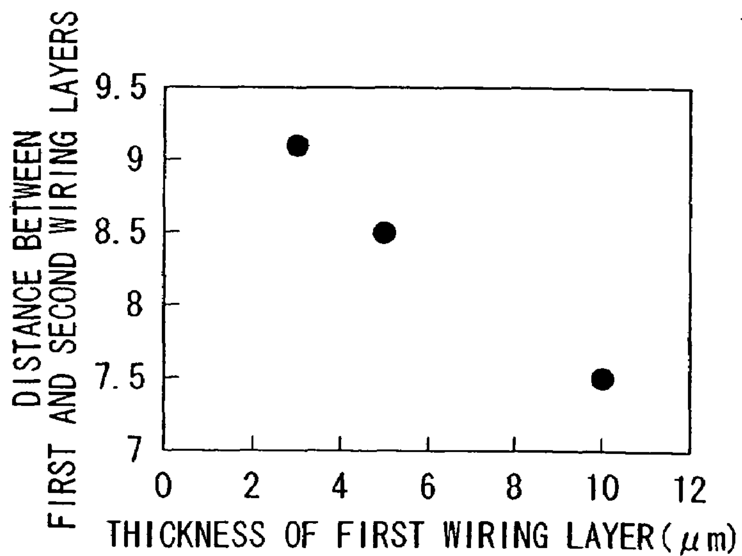


FIG. 12



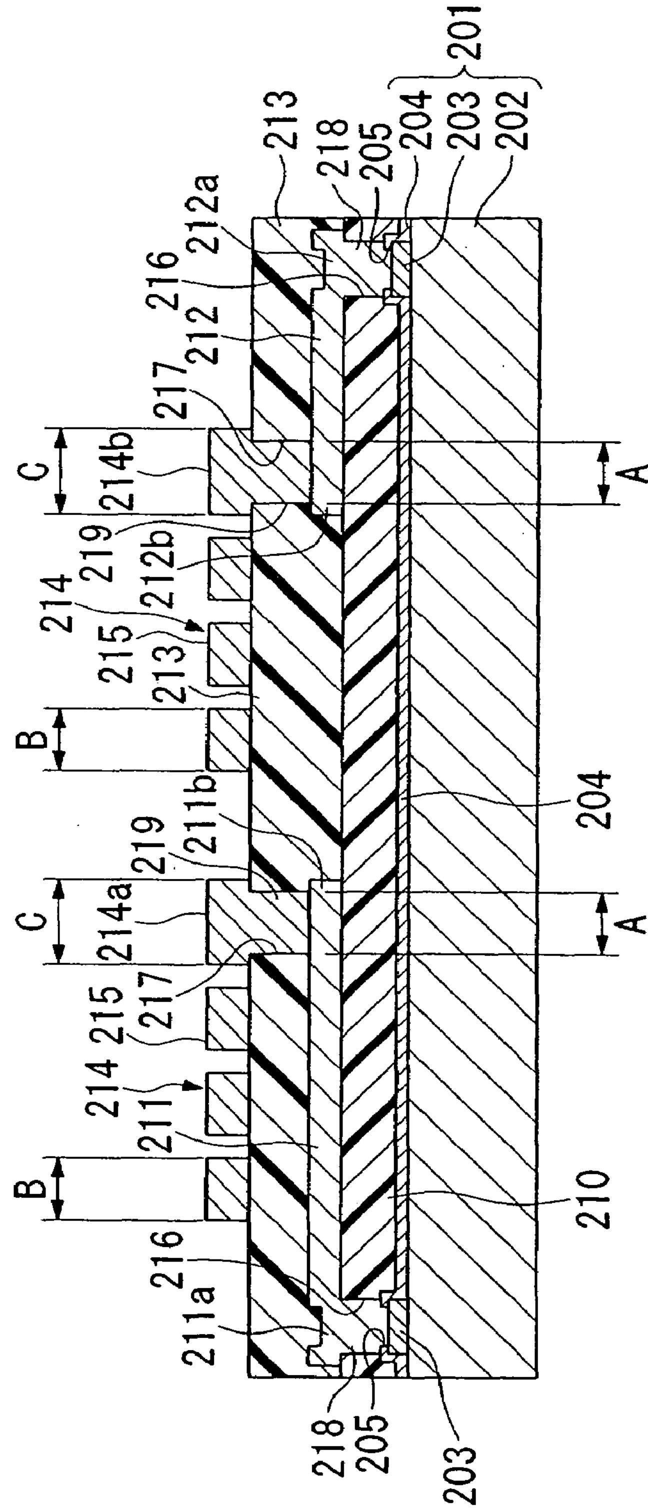


FIG. 13

FIG. 14

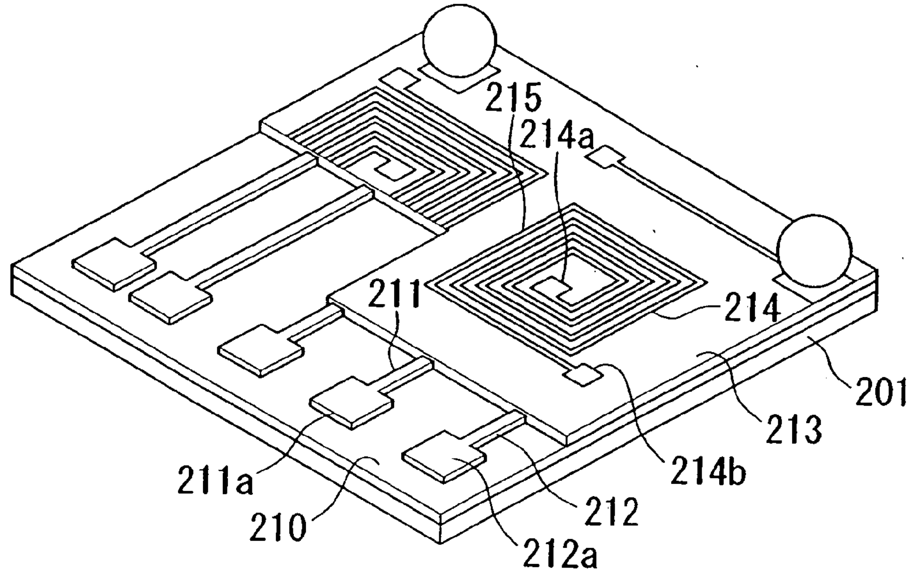


FIG. 15

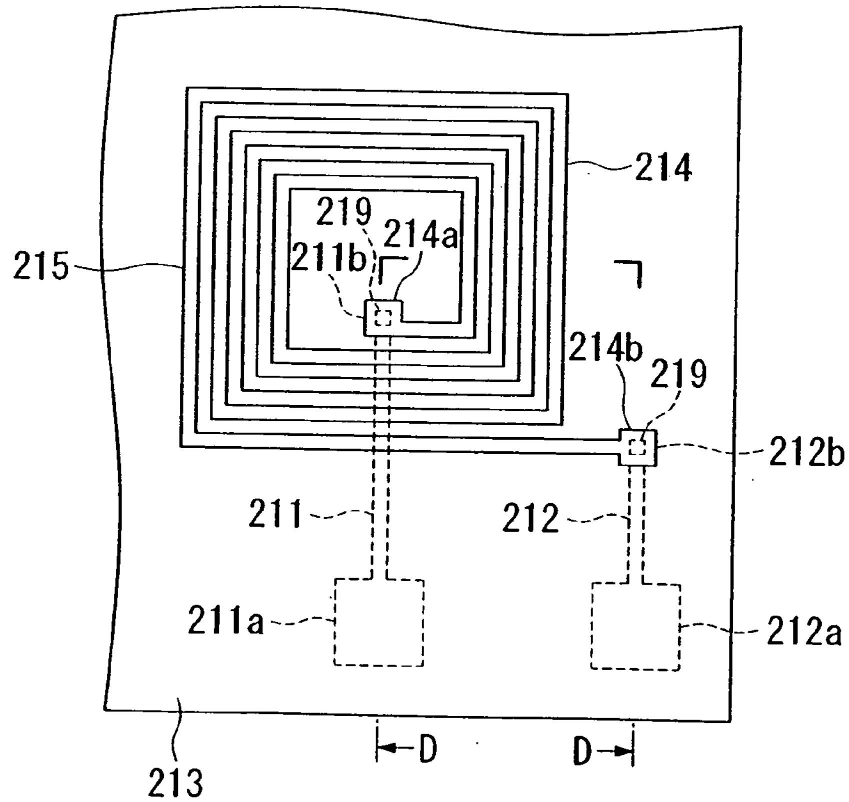


FIG. 16

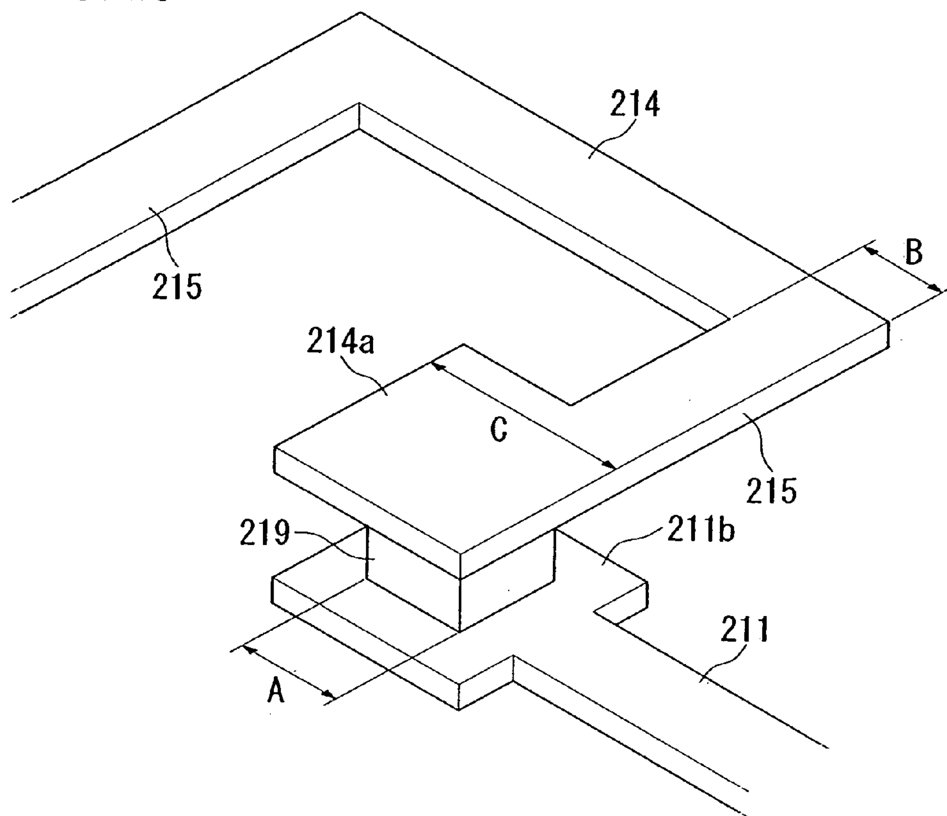


FIG. 17

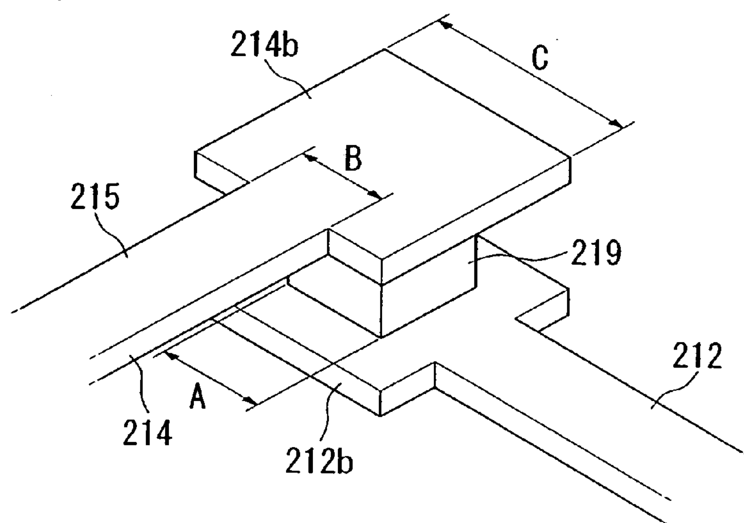


FIG. 18A

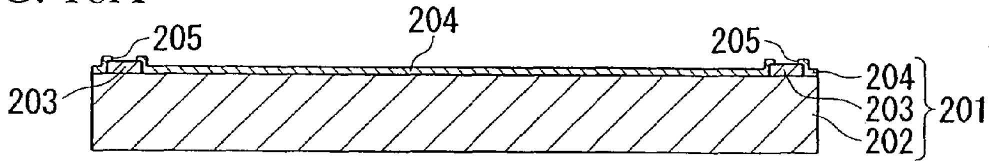


FIG. 18B

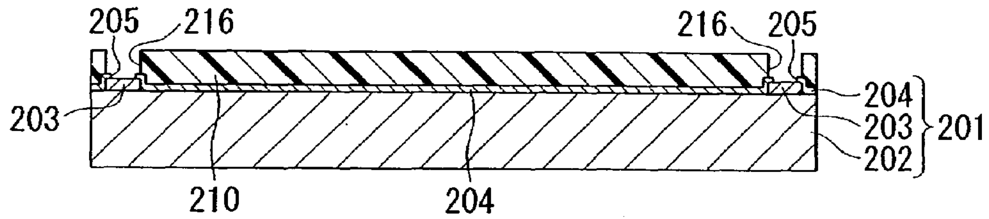


FIG. 18C

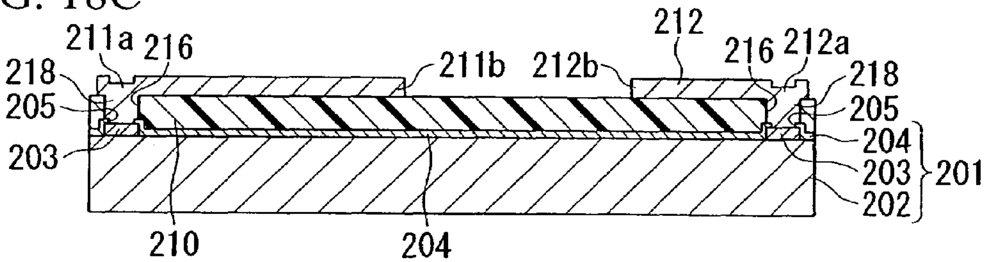


FIG. 18D

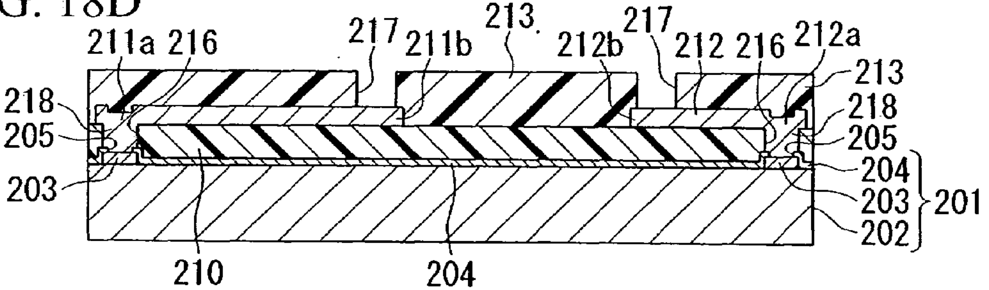


FIG. 18E

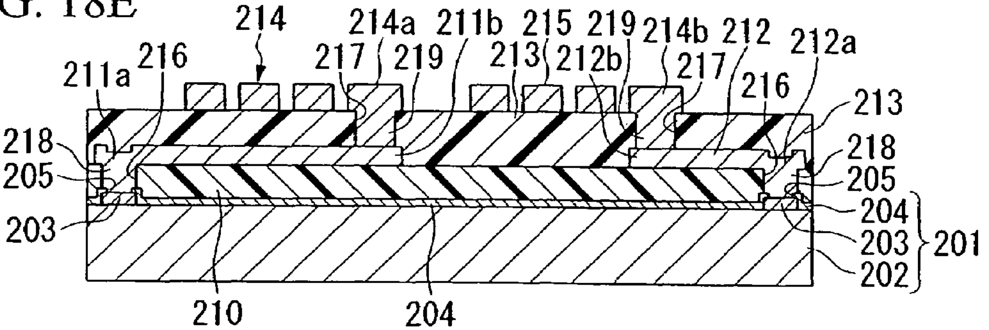


FIG. 19

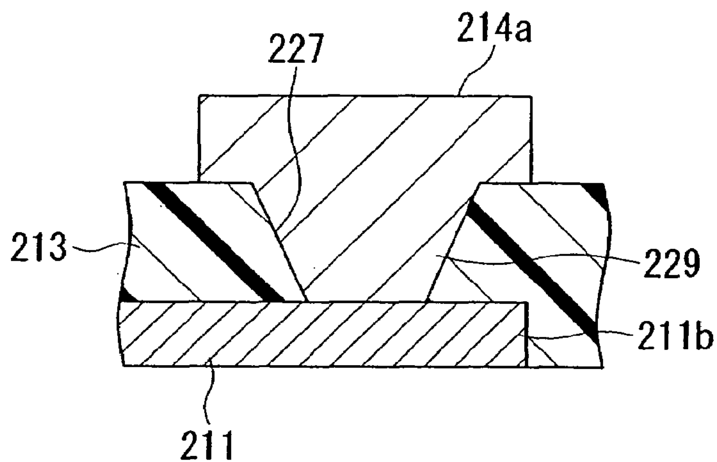


FIG. 20

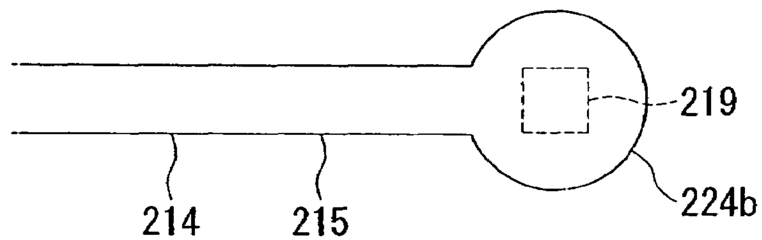


FIG. 21

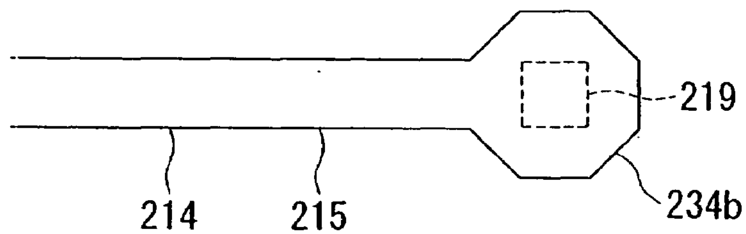
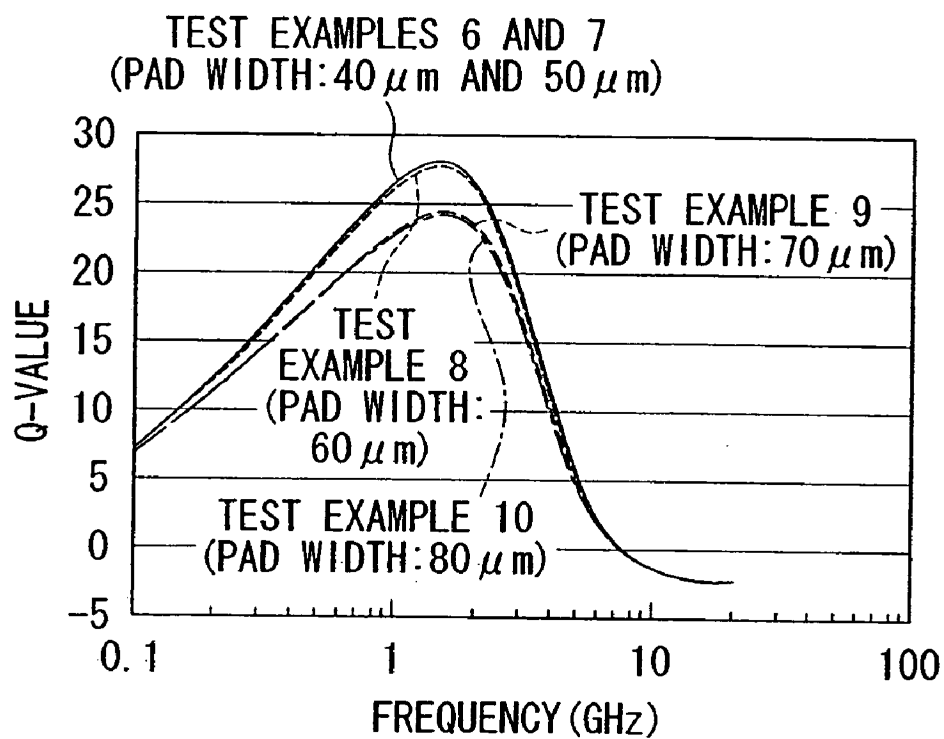


FIG. 22



SEMICONDUCTOR DEVICE HAVING GATE ELECTRODE CONNECTION TO WIRING LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of Ser. No. 11/189,134, filed Jul. 26, 2005, which is based on Japanese priority Application Nos. 2004-221785, filed Jul. 29, 2004, and Japanese Patent Application No. 2004-302696, filed Oct. 18, 2004, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device and a method for manufacturing the same in which formation of a semiconductor having a induction element formed above a semiconductor substrate, such as a silicon wafer is done together with packaging thereof.

[0004] 2. Description of Related Art

[0005] In recent years, in a fabrication of a high-frequency semiconductor element, an induction element, such as a spiral inductor, is formed on a semiconductor substrate for the purpose of ensuring impedance matching thereof or the like. In such a semiconductor element, however, a part of electromagnetic energy generated by the induction element is lost in the substrate or a wiring constructing the induction element due to parasitic capacitance between the wiring and the semiconductor substrate. This type of energy loss is disclosed in, for example, Japanese Unexamined Patent Application, First Publication No. 2003-86690.

[0006] One cause of this type of electromagnetic energy loss is a relatively close vertical distance between the wiring and the semiconductor substrate, which makes the influence of the parasitic capacitance significant. To eliminate such losses, one technique is proposed in which a thick resin layer is provided between the semiconductor substrate and the induction element so that loss of electromagnetic energy is prevented (see, for example, NIKKEI MICRODEVICES, March 2002, pp. 125-127).

[0007] FIGS. **1**, **2**A, and **2**B illustrate an example of a conventional semiconductor device having a spiral coil. FIG. **1** is a plan view, FIG. **2**A is a partially broken perspective view, and FIG. **2**B is a cross-sectional view taken along line B-B shown in FIG. **1**.

[0008] In a semiconductor device **20**, a semiconductor substrate **1** includes an integrated circuit (IC) **2** formed thereon, and electrodes **3** and a passivation film **4** (insulator film) of the integrated circuit **2** are provided above the surface of the semiconductor substrate **1**.

[0009] Furthermore, a lower wiring layer **21** that is connected to the electrodes **3** is formed on the passivation film **4** above the semiconductor substrate **1**, and an insulating resin layer **22** is formed over the semiconductor substrate **1** and the lower wiring layer **21**. Above the insulating resin layer **22**, an upper wiring layer **23** having a spiral coil **24** is provided as a dielectric element. The spiral coil **24** is connected to the electrodes **3** of the integrated circuit **2** via the lower wiring layer **21**.

[0010] FIGS. **3**A to **3**D are schematic cross-sectional views stepwise illustrating an exemplary method for manufacturing the semiconductor device shown in FIGS. **1**, **2**A, and **2**B.

[0011] First, as shown in FIG. **3**A, the semiconductor substrate **1** having the integrated circuit **2**, the electrodes **3**, and the passivation film **4** is provided. The semiconductor substrate **1** is, for example, a silicon wafer on which aluminum pads have been provided as the electrodes **3**, which are covered with the passivation film **4** made of SiN, SiO_2, or the like. In the passivation film **4**, openings **5** are defined in the positions corresponding to the electrodes **3**, and the electrodes **3** are exposed from the openings **5**. The passivation film **4** may be formed, for example, using any well-known method, such as the low-pressure chemical vapor deposition (LPCVD) technique, to a thickness of between 0.1 μm and 0.5 μm, for example.

[0012] Next, as shown in FIG. **3**B, the lower wiring layer **21** is formed on the passivation film **4** above the semiconductor substrate **1**. The lower wiring layer **21** is a redistribution layer (under path) that connects between the electrodes **3** and the spiral coil **24**, and first ends **21***a* thereof are connected to the electrodes **3**, and second ends **21***b* are connected to ends **23***a* and **23***b* of the upper wiring layer **23** that are provided above the lower wiring layer **21** (see FIG. **3**D). The material of the lower wiring layer **21** may be, aluminum or copper, for example, and the thickness thereof may be between 0.1 μm and 10 μm, for example. The lower wiring layer **21** may be formed using any well-known method, for example, sputtering, evaporation, plating, or the like.

[0013] Next, as shown in FIG. **3**C, the insulating resin layer **22** is formed over the passivation film **4** and the lower wiring layer **21** above the semiconductor substrate **1**. The insulating resin layer **22** may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be between 0.1 μm and 10 μm, for example. The insulating resin layer **22** may be formed using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like. In the insulating resin layer **22**, the openings **25** are defined in the positions corresponding to the second ends **21***b* of the lower wiring layer **21** (two openings are shown in FIGS. **3**A to **3**D). The openings **25** may be defined using a patterning technique or the like, by means of photolithography, for example.

[0014] Next, as shown in FIG. **3**D, the upper wiring layer **23** having the spiral coil **24** is formed on the insulating resin layer **22**. The ends **23***a* and **23***b* of the upper wiring layer **23** penetrates through the openings **25** defined in the insulating resin layer **22** and are connected to the second ends **21***b* of the lower wiring layer **21** through the openings **25**. The material of the upper wiring layer **23** may be, for example, copper, and the thickness thereof may be, for example, between 1 μm and 20 μm. The upper wiring layer **23** may be formed, for example, using any well-known technique, such as electroplating.

[0015] Although the spiral coil **24** is formed in the upper wiring layer **23** in the conventional example shown in FIGS. **3**A to **3**D, the spiral coil **24** may be formed on the lower wiring layer **21** as shown FIGS. **4**A to **4**D. Next, a procedure for manufacturing a semiconductor device in which the spiral coil **24** is formed in the lower wiring layer **21** will be explained with reference to FIGS. **4**A to **4**D.

[0016] First, as shown in FIG. **4**A, the semiconductor substrate **1** having the integrated circuit **2**, the electrodes **3**, and the passivation film **4** is provided. The description of the semiconductor substrate **1** shown in FIGS. **4**A to **4**D is omitted since it is similar to the semiconductor substrate **1** shown in FIG. **3**A.

[0017] Next, as shown in FIG. 4B, the lower wiring layer 21 is formed on the passivation film 4 above the semiconductor substrate 1. The lower wiring layer 21 includes an interconnecting conductive layer 26 connected to the electrodes 3 and the spiral coil 24. The spiral coil 24 is to be connected to the interconnecting conductive layer 26 and the electrodes 3 in a later stage.

[0018] The material of the lower wiring layer 21 may be, aluminum or copper, for example, and the thickness of thereof may be between 0.1 ||m and 10 ||m, for example. The lower wiring layer 21 may be formed using any well-known method, for example, sputtering, evaporation, plating, or the like.

[0019] Next, as shown in FIG. 4C, the insulating resin layer 22 is formed over the passivation film 4 and the lower wiring layer 21 above the semiconductor substrate 1. The insulating resin layer 22 may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be between 0.1 μm and 10 μm, for example. The insulating resin layer 22 may be formed using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like. In the insulating resin layer 22, the openings 25 are defined in the positions corresponding to the interconnecting conductive layer 26 and ends 24*a* of the spiral coil 24 (two openings are shown in FIGS. 4C and 4D). The openings 25 may be defined using a patterning technique or the like, by means of photolithography, for example.

[0020] Next, as shown FIG. 4D, the upper wiring layer 23 is formed on the insulating resin layer 22. The two ends 23*a* and 23*b* of the upper wiring layer 23 penetrate through the openings 25 defined in the insulating resin layer 22, and are connected to the interconnecting conductive layer 26 and the ends 24*a* of the spiral coil 24, respectively. In this manner, the spiral coil 24 is connected to the electrodes 3 via the upper wiring layer 23 (over path) and the interconnecting conductive layer 26.

[0021] The material of the upper wiring layer 23 may be, for example, copper, and the thickness thereof may be, for example, between 1 μm and 20 μm. The upper wiring layer 23 may be formed, for example, using any well-known technique, such as electroplating.

[0022] However, the conventional semiconductor device 20 as shown in FIGS. 3A to 3D and FIGS. 4A to 4D still have shortcomings as follows.

[0023] Referring to FIG. 5, an equivalent circuit of the conventional semiconductor device is shown. In FIG. 5, C_S is the capacitance of the spiral coil, R_S is the electrical resistance of the spiral coil, and Ls is the inductance of the spiral coil. $C_{(OX+Resin)}$ is the capacitance of the passivation film and the insulating resin layer, C_{Si} is the capacitance of the semiconductor substrate (silicon substrate), and R_{Si} is the electrical resistance of the semiconductor substrate (silicon substrate).

[0024] Provision of the spiral coil 24 on the upper wiring layer 23 as shown in FIGS. 3A to 3D suffers from the following shortcomings (1) and (2).

[0025] (1) Because the lower wiring layer 21 and the semiconductor substrate 1 are close, C_{Si} is increased due to parasitic capacitance, which results in energy loss.

[0026] (2) Because the lower wiring layer 21 and the upper wiring layer 23 (the spiral coil 24) are close, Cs is increased, causing energy loss.

[0027] Provision of the spiral coil 24 on the lower wiring layer 21 as shown in FIGS. 4A to 4D suffers from the following shortcomings (1) and (2).

[0028] (1) Because the lower wiring layer 24 and the semiconductor substrate 1 are close, R_{Si} is increased due to eddy current loss, which results in energy loss.

[0029] (2) Because the lower wiring layer 21 and the upper wiring layer 23 (the spiral coil 24) are close, Cs is increased, causing energy loss.

[0030] As described previously, in recent years, in a fabrication of a high-frequency semiconductor element, an induction element, such as a spiral inductor, is formed on a semiconductor substrate for the purpose of ensuring impedance matching thereof or the like (see, for example, Japanese Unexamined Patent Application, First Publication No. 2003-86690). Therefore, one technique is proposed in which a thick resin layer is provided between the semiconductor substrate and the induction element so that loss of electromagnetic energy is reduced.

[0031] In a conventional semiconductor device, however, a multi-layered wiring structure may be required. In such a case, impedance mismatching occurs at the junctions (contact holes) that connect an induction element and a wiring that are formed in the different layers, which may result in a decrease in the quality factor value (Q value).

SUMMARY OF THE INVENTION

[0032] The present invention was conceived in light of the above-described background, and one object thereof is to provide a low energy-loss and high performance semiconductor device having an induction element formed thereabove.

[0033] In order to solve the first aspect of the above problems is directed to a semiconductor device including: a semiconductor substrate having an electrode formed above a surface thereof; a first insulating resin layer that is provided over the semiconductor substrate and has a first opening defined at a position corresponding to the electrode; a first wiring layer that is provided on the first insulating resin layer and is connected to the electrode through the first opening; a second insulating resin layer provided over the first insulating resin layer and the first wiring layer, the second insulating resin layer having a second opening that is defined at a position different from the position of the first opening in a direction of the surface of the semiconductor substrate; and a second wiring layer that is provided on the second insulating resin layer and is connected to the first wiring layer through the second opening, wherein the second wiring layer includes an induction element, and a sum of a thickness of the first insulating resin layer and a thickness of the second insulating resin layer is not less than 5 μm and not more than 60 μm.

[0034] According to a second aspect of the present invention, in the above-described semiconductor device, a value obtained by dividing a thickness of the first wiring layer by a thickness of the second wiring layer may be between 0.3 and 10.5.

[0035] According to a third aspect of the present invention, the induction element may be a spiral coil.

[0036] Furthermore, a fourth aspect of the present invention is directed to a method for manufacturing a semiconductor device, including the steps of: forming a first insulating resin layer over a semiconductor substrate having an electrode provided thereabove; defining a first opening in the first insulating resin layer such that the electrode is exposed; forming, on the first insulating resin layer, a first wiring layer

connected to the electrode through the first opening; forming, over the first insulating resin layer and the first wiring layer, a second insulating resin layer; forming a second opening at a position different from a position of the first opening in a direction of the surface of the semiconductor substrate, a position of the second opening corresponding to a position of the first wiring layer; and forming, on the second insulating resin layer, a second wiring layer that is connected to the first wiring layer through the second opening and functions as an induction element, wherein a sum of a thickness of the first insulating resin layer and a thickness of the second insulating resin layer is not less than 5 μm and not more than 60 μm.

[0037] According to a fifth aspect of the present invention, in the above-described method for manufacturing semiconductor device, a value obtained by dividing a thickness of the first wiring layer by a thickness of the second wiring layer may be between 0.3 and 0.5.

[0038] According to the present invention, since the first insulating resin layer and the second insulating resin layer are provided between the induction element, such as a spiral coil, and the semiconductor substrate, the induction element and the semiconductor substrate are spaced apart with a sufficient distance by the two insulating resin layers. In this manner, energy loss, such as eddy current loss, can be reduced, and a semiconductor device having a dielectric element that exhibits a high Q value (quality factor) and excellent characteristics can be obtained.

[0039] Furthermore, the present invention was conceived in light of the above-described background, and another object thereof is to provide a semiconductor device having an induction element that exhibits a high Q value.

[0040] A sixth aspect of the present invention is directed to a semiconductor device including: a semiconductor substrate having an electrode formed above a surface thereof; a first insulating resin layer that is provided over the semiconductor substrate and has a first opening defined at a position corresponding to the electrode; a wiring layer that is formed above the first insulating resin layer and is connected to the electrode through the first opening; a second insulating resin layer that is formed over the first insulating resin layer and the first wiring layer in the position corresponding to the first wiring layer, the second insulating resin layer having a second opening; and a second wiring layer that is formed on the second insulating resin layer and has an induction element, wherein the second wiring layer is connected to the first wiring layer via a junction provided in the second opening, and a width of the junction is equal to or greater than a line width of the second wiring layer that constructs the induction element.

[0041] According to a seventh aspect of the present invention, in the above-described semiconductor device, a first contact pad and a second contact pad may be provided to the first wiring layer and the second wiring layer, respectively, the junction may be provided between the first contact pad of the first wiring layer and the second contact pad of the second wiring layer, and a difference between a width C of at least one of the first contact pad of the first wiring layer and the second contact pad of the second wiring layer and a width A of the junction (C−A) may be 30 μm or less.

[0042] According to an eighth aspect of the present invention, in the above-described semiconductor device, the induction element may be a spiral coil.

[0043] According to a ninth aspect of the present invention, in the above-described semiconductor device, the contact pad may have one of a substantially rectangular shape and a substantially circular shape.

[0044] According to the present invention, since the junction is formed so that the width thereof is same as or greater than that of the second wiring layer that constructs the induction element, the flow of current is not blocked at the junction and loss can be reduced. In particular, impedance mismatching within the induction element can be prevented at high frequencies.

[0045] Accordingly, a semiconductor device having an induction element with a high Q value (quality factor) can be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0046] FIG. **1** is a plan view illustrating an example of a conventional semiconductor device;

[0047] FIG. **2**A is a partially broken perspective view of an example of the conventional semiconductor device;

[0048] FIG. **2**B a cross-sectional view illustrating an example of the semiconductor device according to the present invention taken along line B-B in FIG. **1**;

[0049] FIGS. **3**A to **3**D are schematic cross-sectional views stepwise illustrating an example of a method for manufacturing the semiconductor device shown in FIG. **1**;

[0050] FIGS. **4**A to **4**D are schematic cross-sectional views illustrating an example of a method for manufacturing another example of a conventional stepwise semiconductor device;

[0051] FIG. **5** is a circuit diagram showing an equivalent circuit of the conventional semiconductor device;

[0052] FIG. **6** is a plan view illustrating one example of a semiconductor device according to the present invention;

[0053] FIG. **7**A is a partially broken perspective view illustrating one example of a semiconductor device according to the present invention;

[0054] FIG. **7**B is a cross-sectional view illustrating an example of the semiconductor device according to the present invention taken along line A-A in FIG. **6**;

[0055] FIGS. **8**A to **8**E are schematic cross-sectional views stepwise illustrating an example of a method for manufacturing the semiconductor device shown in FIG. **6**;

[0056] FIG. **9** is a graph illustrating an example of the relationship between frequency and the Q value for semiconductor devices having an induction element that is positioned in various locations;

[0057] FIG. **10** is a graph illustrating an example of the relationship between the sum of the layer thicknesses of the first insulating resin layer and the second insulating resin layer (total thickness of all resin layers) and the Q value;

[0058] FIG. **11** is a graph illustrating an example of the relationship between the thickness of the first wiring layer and the Q value of the semiconductor device;

[0059] FIG. **12** is a graph illustrating an example of the relationship between the thickness of the first wiring layer and the distance between the first wiring layer and the second wiring layer;

[0060] FIG. **13** is a figure showing an alternative example of a semiconductor device according to the present invention;

[0061] FIG. **14** is a partially broken perspective view of the semiconductor device shown in FIG. **13**;

[0062] FIG. **15** is a plan view illustrating a main portion of the semiconductor device shown in FIG. **13**;

[0063] FIG. **16** is a perspective view illustrating a main portion of the semiconductor device shown in FIG. **13**;

[0064] FIG. **17** is a perspective view illustrating a main portion of the semiconductor device shown in FIG. **13**;

[0065] FIGS. **18**A to **18**E are schematic cross-sectional views stepwise illustrating an example of a method for manufacturing the semiconductor device shown in FIG. **13**;

[0066] FIG. **19** is a cross-sectional view illustrating a variation of the second junction;

[0067] FIG. **20** is a plan view illustrating a variation of a contact pad;

[0068] FIG. **21** is a plan view illustrating another variation of a contact pad; and

[0069] FIG. **22** is a graph showing the results of the tests.

DETAILED DESCRIPTION OF THE INVENTION

[0070] Hereinafter, the present invention will be described based on preferable embodiment with reference to the drawings.

[0071] FIG. **6** and FIGS. **7**A and **7**B show an example of the semiconductor device according to the present invention. FIG. **6** is a plan view, FIG. **7**A is a partially broken perspective view, and FIG. **7**B is a cross-sectional view taken along line A-A shown in FIG. **6**.

[0072] In a semiconductor device **110**, a semiconductor substrate **101** has an integrated circuit (IC) **102** formed thereabove, and electrodes **103** and a passivation film **104** of the integrated circuit **102** are provided above the surface of the semiconductor substrate **101**.

[0073] This semiconductor device **110** further includes a first insulating resin layer **111** provided on the passivation film **104** of the semiconductor substrate **101**, a first wiring layer **112** formed on the first insulating resin layer **111**, a second insulating resin layer **113** formed over the first insulating resin layer **111** and the first wiring layer **112**, and a second wiring layer **114** formed on the second insulating resin layer **113**.

[0074] The semiconductor substrate **101** is, for example, a silicon wafer above which aluminum pads are provided as the electrodes **103**, on which a passivation film **104**, such as SiN or SiO_2 (a passivated insulator film) is formed. Openings **105** are defined in the passivation film **104** in the positions corresponding to electrodes **103**, and the electrodes **103** are exposed from the openings **105**. The passivation film **104** may be formed, for example, using any well-known method, such as the LPCVD technique, and the film thickness thereof is between 0.1 μm and 0.5 μm, for example.

[0075] In this embodiment, the electrodes **103** that connect the wiring layer having a spiral coil **115** to the integrated circuit **102** are provided in two positions on the surface of the semiconductor substrate **101**.

[0076] According to the present invention, the semiconductor substrate may be a semiconductor wafer, such as a silicon wafer, or may be a semiconductor chip that is obtained by dicing a semiconductor wafer to the size of a chip. In the case where the semiconductor substrate is a semiconductor chip, a plurality of semiconductor chips can be obtained by forming groups of various semiconductor elements, ICs, or induction elements on a semiconductor wafer, and then dicing the semiconductor wafer to the size of the chip.

[0077] Although a portion of the semiconductor device with one induction element formed on the semiconductor substrate is shown in FIG. **6** and FIGS. **7**A and **7**B, it should be noted that the present invention is applicable to form a plurality of induction elements on a semiconductor substrate, such as semiconductor wafer. It should also be noted that various structures are additionally provided, such as a sealing layer for sealing the second wiring layer **114**, output terminals to outside elements, such as bumps, or the like, to the semiconductor device according to the present invention, although such additional structures are not shown in the figures.

[0078] The first insulating resin layer **111** has first openings **116** defined in the position corresponding to each of the electrodes **103**. The first insulating resin layer **111** may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be, for example, between 1 μm and 30 μm.

[0079] The first insulating resin layer **111** may be formed using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like. Furthermore, the first opening **116** may be defined using a patterning technique or the like, by means of photolithography, for example.

[0080] The second insulating resin layer **113** has second openings **117** that are defined in the positions different from the positions of the first opening **116** in the direction of the surface of the semiconductor substrate **101**. The second openings **117** are defined in the positions corresponding to ends **114***a* and **114***b* of the second wiring layer **114**.

[0081] The first wiring layer **112** is a redistribution layer that connects between the electrodes **103** and the spiral coil **115**. First ends **112***a* of the first wiring layer **112** penetrate through the first insulating resin layer **111** through the first opening **116**, and are connected to the electrodes **103**. Furthermore, second ends **112***b* of the first wiring layer **112** extend so as to align to the second openings **117**.

[0082] The material of the first wiring layer **112** may be, for example, copper, and the thickness thereof may be, for example, between 1 μm and 20 m. This ensures excellent conductivity. The first wiring layer **112** may be formed using, for example, a plating technique, such as copper electroplating or the like, sputtering, evaporation, or combination of any two or more of these methods.

[0083] The second wiring layer **114** includes the spiral coil **115** as a dielectric element. The ends **114***a* and **114***b* of the second wiring layer **114** penetrate through the second insulating resin layer **113** through the second opening **117**, and are connected to the respective second end **112***b* of the first wiring layer **112**.

[0084] The material of the second wiring layer **114** may be, for example, copper, and the thickness thereof may be, for example, between 1 μm and 20 μm. This ensures excellent conductivity. The second wiring layer **114** may be formed using, for example, a plating technique, such as copper electroplating or the like, sputtering, evaporation, or combination of any two or more of these methods.

[0085] A sealing layer (not shown) may be provided on the second insulating resin layer **113** and the second wiring layer **114** according to requirements, covering at least the second wiring layer **114**.

[0086] The sealing layer may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be between 10 μm and 150 μm, for example. Openings for connecting to terminals of outside elements may be defined in the sealing layer.

[0087] Furthermore, in the semiconductor device **110** of this embodiment, the sum of the layer thickness of the first insulating resin layer **111** and the layer thickness of the sec-

ond insulating resin layer **113** is not less than 5 μm and not more than 60 μm. By this, a semiconductor device having a dielectric element that exhibits a high Q value and excellent characteristics can be obtained, as described later.

[0088] In the semiconductor device of this embodiment, the layer thickness of the first wiring layer **112** is preferably smaller than the layer thickness of the second wiring layer **114**. In particular, a value obtained by dividing the layer thickness of the first wiring layer **112** by the layer thickness of the second wiring layer **114** is preferably between 0.3 and 0.5.

[0089] Furthermore, the thickness of the first wiring layer **112** is preferably smaller than the thickness of the second insulating resin layer **113**.

[0090] Next, a method for manufacturing the semiconductor device shown in FIG. **6** and FIGS. **7**A and **7**B will be explained.

[0091] FIGS. **8**A to **8**E are schematic cross-sectional views stepwise illustrating an example of a method for manufacturing the above-described semiconductor device. The cross-sectional views in FIGS. **8**A to **8**E are taken along line A-A shown in FIG. **6**.

[0092] First, as shown in FIG. **8**A, the semiconductor substrate **101** having the integrated circuit **102**, the electrodes **103**, and the passivation film **104** is provided.

[0093] As described above, the semiconductor substrate **101** is a semiconductor wafer having the electrodes **103** and the passivation film **104** formed above the surface threreof, and the openings **105** are defined in the passivation film **104** in the positions corresponding to electrodes **103**.

[0094] Next, as shown in FIG. **8**B, the first insulating resin layer **111** having the first openings **116** is formed on the passivation film **104** of the semiconductor substrate **101**.

[0095] The first insulating resin layer **111** may be formed, for example, by forming a film made of one or more of the above-described resins using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like, over the entire surface of the passivation film **104** (first insulating resin layer formation step), and then defining the first opening **116** using a patterning technique or the like, by means of photolithography, for example, in the positions corresponding to the electrodes **103** (first opening formation step).

[0096] Next, as shown in FIG. **8**C, the first wiring layer **112** is formed on the first insulating resin layer **111** (first wiring layer formation step). The particular method for forming the first wiring layer **112** in a predetermined position is not particularly limited, and the method disclosed in PCT International Application Publication No. WO00/077844 may be employed, for example.

[0097] Here, an example of a preferable method for forming the first wiring layer **112** will be explained.

[0098] First, a thin seed layer (not shown) for electroplating, which is to be carried out later, is formed by means of a sputtering technique or the like, over the entire surface of the first insulating resin layer **111** or selected regions thereof. The seed layer is, for example, a stacked body including a copper layer and a chromium (Cr) layer formed by means of sputtering, or a stacked body including a copper layer and a titanium (Ti) layer. Furthermore, the seed layer may be a electroless copper plating layer, or a thin metal layer formed using evaporation, a coating method, chemical vapor deposition (CVD), or the like, or a any combination of the above-described metal layer formation techniques.

[0099] Next, a resist layer (not shown) for electroplating is formed on the seed layer. Openings are defined in the resist layer in regions in which the first wiring layer **112** is to be formed, and the seed layer is exposed from the openings. The resist layer may be formed, for example, by laminating a film resist, spin coating a liquid resist, or by any other suitable method.

[0100] Then, the first wiring layer **112** is formed on the seed layer using the resist layer as a mask by means electroplating or the like. After forming the first wiring layer **112** in desired regions, unnecessary portions of the resist layer and the seed layer are removed by etching them so that the first insulating resin layer **111** is exposed except the regions where the first wiring layer **112** is formed (see FIG. **8**C).

[0101] Next, as shown in FIG. **8**D, the second insulating resin layer **113** is formed over the first insulating resin layer **111** and the first wiring layer **112**.

[0102] The second insulating resin layer **113** may be formed, for example, by forming a film made of one or more of the above-described resins over the entire surface of the first insulating resin layer **111** and the first wiring layer **112** using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like (second insulating resin layer formation step), and then defining the second opening **117** using a patterning technique or the like, by means of photolithography, for example, in the positions corresponding to the second ends **112***b* of the first wiring layer **112** (second opening formation step).

[0103] Next, as shown in FIG. **8**E, the second wiring layer **114** having the spiral coil **115** is formed on the second insulating resin layer **113** (second wiring layer formation step). The particular method for providing the second wiring layer **114** in the predetermined region is similar to the method for providing the first wiring layer **112**, and thus detailed description thereof will be omitted.

[0104] In the case where the sealing layer is provided above the second wiring layer **114**, the sealing layer may be formed, for example, by patterning a photosensitive resin, such as a photosensitive polyimide resin, using photolithography to define openings in predetermined positions. It should be noted that the particular method for forming the sealing layer is not limited to this method, and various techniques may be used.

[0105] After forming the sealing layer, a semiconductor chip in which the induction element and the like are packaged can be obtained by dicing the semiconductor wafer having various structures, such as the induction element, thereon to a predetermined size.

[0106] Next, the operation and the effects of the semiconductor device of this embodiment will be explained.

[0107] Since the first resin layer and the second resin layer are interposed between the semiconductor substrate and the dielectric element, the dielectric element and the semiconductor substrate are spaced apart with a sufficient distance. As a result, the resistance of the semiconductor substrate is decreased (R_{Si} shown in FIG. **5**), whereby reducing eddy current loss. Furthermore, the first wiring layer positioned close to the semiconductor substrate is an interconnection wiring connecting between the electrodes and the dielectric element, and the dielectric element is provided in the second wiring layer distant from the semiconductor substrate. Thus, since the dielectric element and the semiconductor substrate

are spaced apart with a sufficient distance, the eddy current loss due to magnetic flux generated by the dielectric element can be reduced.

[0108] Furthermore, the first insulating resin layer and the second insulating resin layer are interposed between the semiconductor substrate and the dielectric element, and the sum of the thicknesses of these insulating resin layers is set to no less than 5 μm and not more than 60 μm. By this, preferable semiconductor devices having various advantages, such as greater increase in the Q value, smaller size, and reduced manufacturing cost, can be obtained. If the sum of the thicknesses of the two insulating resin layers is less than 5 μm, the improvement in the Q value is smaller, which is not desirable. Furthermore, the sum of the thicknesses of the two insulating resin layers of greater than 60 μm is not disadvantageous in terms of the manufacturing cost or manufacturing conditions since further increase in the Q value is not expected (see FIG. **10**). In order to use the device as a dielectric element, the Q value is preferably 20 or higher.

[0109] In the semiconductor device of this embodiment, the inductor is made of the first wiring layer and the second wiring layer, among which the first wiring layer is an under path that connects between the electrodes on the semiconductor substrate and the dielectric element (coil) and the second wiring layer has the dielectric element (coil).

[0110] In this structure, the resistance of the second wiring layer becomes dominant in the resistance (R_S) of the inductor.

[0111] Furthermore, when the thicknesses of the first insulating resin layer and the second insulating resin layer are the same, if the thickness of the second insulating resin layer is too small, the distance between the first wiring layer and the second wiring layer is reduced. As a result, the effect of the energy loss becomes significant due to increased capacitance (C_S) of the inductor. This is because the second insulating resin layer (see FIGS. **7**A and **7**B) have two different portions: one directly formed on the first insulating resin layer and the other formed on the first wiring layer. If the first wiring layer is too thick, a resin may flow from the first wiring layer during formation of the second insulating resin layer and the thickness of the resin on the first wiring layer tends to become smaller than desired.

[0112] If the thickness of the first wiring layer is too small, the electrical resistance is reduced due to the reduction in the cross-sectional area of the first wiring layer, which is not desirable.

[0113] By maintaining a value obtained by dividing the layer thickness of the first wiring layer by the layer thickness of the second wiring layer to no less than 0.3 and not more than 0.5, the influence of increased capacitance (C_S) is reduced and a semiconductor device having further excellent characteristics can be realized.

EXAMPLES

[0114] Semiconductor devices were manufactured, and the characteristics thereof were evaluated. Silicon substrates were used as semiconductor substrates. The first insulating resin layer and the second insulating resin layer were formed from a polyimide resin. The first wiring layer were provided between the first insulating resin layer and the second insulating resin layer, and the second wiring layer was provided on the second insulating resin layer. The dielectric element was formed as a 3.5-turn spiral coil. Copper (Cu) was used as the material of the first second wiring layer and second wiring layer.

Position of Induction Element

[0115] As a working example of the present invention, semiconductor devices having a first wiring layer positioned close to a semiconductor substrate as an interconnection wiring (under path), and a second wiring layer distant from the semiconductor substrate as a dielectric element were manufactured. As a comparative example, semiconductor devices having a first wiring layer positioned close to the semiconductor substrate as a dielectric element, and a second wiring layer distant from the semiconductor substrate as an interconnection wiring (over path) were manufactured. For these semiconductor devices, the relationship between frequency and Q value was evaluated.

[0116] The semiconductor elements of the working example and the semiconductor elements of the comparative example were manufactured under the same conditions, such as the thicknesses of the insulating resin layers, of the working examples, except for the positions of the induction element as described above.

[0117] In FIG. **9**, the solid line shows the Q values of the semiconductor elements of the working example in which the dielectric element was provided in the second wiring layer. Furthermore, the dashed line shows the Q values of the semiconductor elements of the comparative example in which the dielectric element was provided in the first wiring layer.

[0118] The results of FIG. **9** indicate that an inductor having a high Q value can be realized by disposing the dielectric element distant from the semiconductor substrate when two wiring layers are provided.

Thicknesses of Insulating Resin Layers

[0119] As shown in Table 1, a plurality of semiconductor devices were manufactured while varying the sum of the layer thicknesses of the first insulating resin layer and the second insulating resin layer, and the Q values of these semiconductor devices at a frequency of 2 GHz were measured.

[0120] In these semiconductor devices, the first wiring layer positioned close to the semiconductor substrate is an interconnection wiring (under path), and the second wiring layer distant from the semiconductor substrate is a dielectric element.

[0121] The relationship between the sum of the layer thicknesses of the first insulating resin layer and the second insulating resin layer (total thickness of all resin layers) and the Q value is shown in FIG. **10** and Table 1. These results indicate that a Q value of 20 or higher was obtained when the sum of the layer thicknesses of the first insulating resin layer and the second insulating resin layer was no less than 5 μm and not more than 60 μm. In this case, the effect of enhancing the Q value is favorable whereas the total thickness of the insulating resin layers is prevented from being unnecessarily increased.

TABLE 1

Sum of Thicknesses of First and Second Insulating Resin Layers (μm)	Q Value (at 2 GHz)
1	12.2
2	14.2
5	22.4

TABLE 1-continued

Sum of Thicknesses of First and Second Insulating Resin Layers (μm)	Q Value (at 2 GHz)
10	26.5
20	34.0
30	29.8
40	37.1
50	36.0
60	36.3
80	37.1
100	36.1

Thickness of Conductive Layer

[0122] A plurality of semiconductor devices were manufactured while varying the thickness of the first wiring layer when fixing the thickness of the second wiring layer to 10 μm.

[0123] In these semiconductor devices, the first wiring layer positioned close to the semiconductor substrate is an interconnection wiring (under path), and the second wiring layer distant from the semiconductor substrate is a dielectric element.

[0124] FIG. **11** shows the measured Q values of the semiconductor devices in which the thickness of the first wiring layer is 1 μm, 3 μm, 5 μm, or 9 μm, and the thickness of the second wiring layer is 10 μm at a frequency of 2 GHz. In this measurement, the thickness of the first insulating resin layer was 10 μm, and the thickness of the second insulating resin layer was 10 μm.

[0125] The results of FIG. **11** indicate that a semiconductor device having an even higher Q value can be realized when a value obtained by dividing the thickness of the first wiring layer by the thickness of the second wiring layer is between 0.3 and 0.5.

[0126] FIG. **12** shows measured distances between the first wiring layer and the second wiring layer of semiconductor devices in which the thickness of the second insulating resin layer (the thickness right above the first insulating resin layer) was 10 μm and the thickness of the first wiring layer was 3 μm, 5 μm, or 10 μm. Upon the measurement shown in FIG. **12**, the thickness of the first insulating resin layer was 10 μm, and the thickness of the second wiring layer was 10 μm.

[0127] As indicated by the graph in FIG. **12**, as the ratio of the thickness of the first wiring layer to the thickness of the second insulating resin layer decreases, the distance between the first wiring layer and the second wiring layer increases. This indicates that an excellent semiconductor device having a high Q value is obtained as the ratio of the thickness of the first wiring layer to the thickness of the second insulating resin layer decreases.

[0128] Hereafter, alternative embodiments of the present invention will be described with reference to the drawings.

[0129] FIGS. **13** to **17** illustrate an alternative embodiment of the semiconductor device according to the present invention. FIG. **13** is a cross-sectional view, FIG. **14** is a partially broken perspective view, FIG. **15** is a plan view of a main portion, and FIG. **16** and FIG. **17** are perspective views of the main portion. FIG. **13** is a cross-sectional view taken along line D-D shown in FIG. **15**.

[0130] As shown in FIG. **13**, this semiconductor device includes a semiconductor substrate **201**, a first insulating resin layer **210** provided over the semiconductor substrate **201**, first wiring layers **211** and **212** provided on the first insulating resin layer **210**, a second insulating resin layer **213** provided over the first insulating resin layer **210** and the first wiring layers **211** and **212**, and a second wiring layer **214** provided on the second insulating resin layer **213**.

[0131] The semiconductor substrate **201** is a base material **202**, such as a silicon wafer, above which electrodes **203** of an integrated circuit (not shown) and a passivation film **204** are formed.

[0132] The electrodes **203** may be formed of aluminum, copper, or the like.

[0133] The passivation film **204** is a passivated insulator film, and may be made of SiN, SiO_2, or the like.

[0134] In the passivation film **204**, openings **205** are defined in the positions corresponding to the electrodes **203**, and the electrodes **203** are exposed from the openings **205**.

[0135] The passivation film **204** may be formed, for example, using any well-known method, such as the LPCVD technique, and the film thickness thereof is between 0.1 μm and 0.5 μm, for example.

[0136] According to the present invention, the semiconductor substrate may be a semiconductor wafer, such as a silicon wafer, or may be a semiconductor chip. Semiconductor chips can be obtained by forming groups of various semiconductor elements, ICs, or induction elements on a semiconductor wafer, and then dicing the semiconductor wafer to the size of a chip.

[0137] The first insulating resin layer **210** has first openings **216** defined so as to open in the position corresponding to each of the electrodes **203**.

[0138] The first insulating resin layer **210** may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be, for example, between 1 μm and 30 μm.

[0139] The second insulating resin layer **213** has openings **217** defined in the position corresponding to the two ends of the second wiring layer **214**.

[0140] The second insulating resin layer **213** may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like.

[0141] Since the first wiring layers **211** and **212** and the second wiring layer **214** are spaced apart with a sufficient distance by setting the thickness of the second insulating resin layer **213** to 10 μm or greater, it is possible to reduce energy loss and increase the Q value. The thickness of the second insulating resin layer **213** is preferably between 10 μm and 20 μm.

[0142] The insulating resin layers **210** and **213** may be formed using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like. The openings **216** and **217** may be defined using a patterning technique or the like, by means of photolithography, for example.

[0143] The first wiring layers **211** and **212** (first conductive layer) are redistribution layers connecting between the electrodes **203** and the second wiring layer **214**. First ends **211***a* and **212***a* of the first wiring layers **211** and **212** are connected to the electrodes **203** via first junctions **218** formed in the first openings **216**.

[0144] As shown in FIGS. **13**, **16**, and **17**, contact pads **211***b* and **212***b* having an substantially rectangular plate shape are provided on the first wiring layers **211** and **212**.

[0145] The contact pads **211***b* and **212***b* are provided in the positions corresponding to the second openings **217**, and are

formed so that the length and the width thereof are greater than the width of the first wiring layers **211** and **212**.

[0146] The material of the first wiring layers **211** and **212** may be, for example, aluminum or copper, and the thickness thereof may be, for example, between 1 μm and 20 μm. The first wiring layer **211** and **212** may be formed using any well-known method, or example, sputtering, evaporation, plating, or the like.

[0147] As shown in FIGS. **13** to **15**, the second wiring layer **214** (second conductive layer) includes a spiral coil **215** as an induction element.

[0148] The material of the second wiring layer **214** may be, for example, copper, and the thickness thereof may be, for example, between 1 μm and 20 μm. The second wiring layer **214** may be formed using, for example, plating technique, such as copper electroplating or the like, sputtering, evaporation, or the like.

[0149] Contact pads **214***a* and **214***b* in an substantially rectangular plate shape are provided to the two ends of the second wiring layer **214**.

[0150] The contact pads **214***a* and **214***b* are provided in the positions corresponding to the second openings **217**, and are formed so that the length and the width thereof is greater than the width of the second wiring layers **214**.

[0151] The contact pads **214***a* and **214***b* are connected to the contact pads **21** lb and **212***b* of the first wiring layers **211** and **212** via second junctions **219** defined in the second openings **217**, respectively.

[0152] The aspect ratio, i.e., the ratio of the minimum width and the length (the thickness of the second insulating resin layer **213**) (width/length) of the second openings **217** is too small, a metal material is not completely filled in the second openings **217** upon defining the second junctions **219**, resulting in malformation of the second junctions **219**. For the above reason, the aspect ratio is preferably 1 or greater.

[0153] The second junctions **219** are defined along the walls of the second openings **217**.

[0154] In the example shown in the figures, the second junctions **219** has a prism shape having a rectangular cross-section, and the four sides thereof are parallel to each of the edges of the contact pad **214***a*, **214***b*, **211***b*, or **212***b*.

[0155] The second junctions **219** are preferably provided substantially at the center of the contact pad **214***a*, **214***b*, **211***b*, or **212***b*.

[0156] The width of the second junctions **219** (width A shown in FIGS. **13**, **16**, and **17**) is set to be the same as or greater than the line width of the second wiring layer **214** that constructs the spiral coil **215** (width B shown in FIGS. **13**, **16**, and **17** the spiral coil **215**).

[0157] By setting the width of the second junctions **219** to fall within the above-described range, impedance mismatching within the spiral coil **215** can be prevented and a high Q value can be achieved.

[0158] The difference between the width of the second junctions **219** and the line width of the second wiring layer **214** that constructs the spiral coil **215** (A–B) is preferably set to 10 μor smaller.

[0159] The difference between the width of the contact pads **214***a*, **214***b*, **211***b*, and **212***b* (shown in FIGS. **13**, **16**, and **17** width C) and the width of the second junctions **219** (shown in FIGS. **13**, **16**, and **17** width A) (C–A) is preferably 30 μm or smaller. By setting the difference between the widths to fall within the above-described range, a high Q value can be achieved.

[0160] The above-described difference between the widths is preferably 10 μm or greater so that connection failure can be prevented even when the second junctions **219** are formed misaligned.

[0161] The ratio of the contact pads **214***a*, **214***b*, **211***b*, and **212***b* C to the width of the second junctions **219** A (C/A) is preferably 2 or less. By setting the ratio (C/A) to fall within this range, a high Q value can be achieved.

[0162] The ratio (C/A) is preferably or 1.33 or greater because connection failure can be prevented even when the second junctions **219** are formed misaligned.

[0163] The difference between the area of the contact pad **214***a*, **214***b*, **211***b*, or **212***b* and the cross-sectional area of the second junctions **219** is preferably 2700 μm^2 or less. By setting the difference in the areas to fall within the above range, a high Q value can be achieved.

[0164] The above difference in the areas is preferably 700 μm^2 or greater so that connection failure can be prevented even when the second junctions **219** are formed misaligned.

[0165] The ratio the area of the contact pad **214***a*, **214***b*, **211***b*, or **212***b* to the cross-sectional area of the second junctions **219** is preferably 4 or less. By setting the difference in the areas to fall within the above range, a high Q value can be achieved.

[0166] The above area ratio is preferably 1.78 or greater so that connection failure can be prevented even when the second junctions **219** are formed misaligned.

[0167] The difference in widths, the width ratio, the difference in areas, and the area ratio of the contact pad **214***a*, **214***b*, **211***b*, or **212***b* and the second junctions **219** are preferably satisfied for all of the contact pads **214***a*, **214***b*, **211***b*, and **212***b*. However, the above advantageous effects are achieved even when above-described conditions are met for any one of the contact pads to which the second junctions **219** are connected.

[0168] It should be noted that the width of the second wiring layer **214** constructing the spiral coil **215** as used herein refers to an average width of the spiral coil **215**.

[0169] Furthermore, the widths of the contact pads **214***a*, **214***b*, **211***b*, and **212***b* and the second junctions **219** as used herein refer to a maximum width.

[0170] A sealing layer (not shown) may be provided above the second insulating resin layer **213** and the second wiring layer **214** covering at least the second wiring layer **214**, according to requirements.

[0171] The sealing layer may be made of, for example, a polyimide resin, an epoxy resin, a silicone resin, or the like, and the thickness thereof may be between 5 μm and 20 μm, for example. Openings (not shown) for connecting to terminals of outside elements may be defined in the sealing layer.

[0172] Next, a method for manufacturing the semiconductor device mentioned above will be described.

[0173] FIGS. **18**A to **18**E are schematic cross-sectional views illustrating an example of a method for manufacturing the above-described semiconductor device. FIGS. **18**A to **18**E are cross-sectional views taken along line D-D shown in FIG. **15**.

[0174] Next, as shown in FIGS. **18**A and **18**B, the first insulating resin layer **210** having the first openings **216** is formed on the passivation film **204** of the semiconductor substrate **201**.

[0175] The first insulating resin layer **210** may be formed, for example, using the following methods.

[0176] The second insulating resin layer **210** may be formed, for example, by forming a film made of one or more of the above-described resins over the entire surface of the passivation film **204** using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like (first insulating resin layer formation step).

[0177] Next, the first openings **216** may be defined using a patterning technique or the like, by means of photolithography, for example, in the positions corresponding to the electrodes **203** (first opening formation step).

[0178] As shown in FIG. **18**C, the first wiring layers **211** and **212** are formed on the first insulating resin layer **210** (first wiring layer formation step).

[0179] The first wiring layers **211** and **212** may be formed, for example, using the following methods.

[0180] A seed layer is formed on the first insulating resin layer **210** using a sputtering technique or the like. The seed layer is, for example, a stacked body including a copper layer and a chromium (Cr) layer, or a stacked body including a copper layer and a titanium (Ti) layer.

[0181] Next, a resist layer (not shown) for electroplating is formed on the seed layer. The resist layer is formed on regions other than where the first wiring layers **211** and **212** are to be provided.

[0182] The first wiring layers **211** and **212** made of copper, for example, are formed on the seed layer using electroplating or the like, and the first junctions **218** are formed in the first openings **216**. After forming the first wiring layers **211** and **212** and the first junctions **218**, unnecessary portions of the resist layer and the seed layer are removed by etching them.

[0183] As shown in FIG. **18**D, the second insulating resin layer **213** is formed over the first insulating resin layer **210** and the first wiring layers **211** and **212**.

[0184] The second insulating resin layer **213** may be formed, for example, using the following methods.

[0185] A film made of one or more of the above-described resins is formed using any well-known method, for example, the spin coating method, the printing method, the lamination method, or the like, over the entire surface of the first insulating resin layer **210** and the first wiring layers **211** and **212** (second insulating resin layer formation step).

[0186] Next, the second openings **217** are defined using a patterning technique or the like, by means of photolithography, for example, in positions corresponding to the contact pads **211***b* and **212***b* of the first wiring layers **211** and **212** (second opening formation step).

[0187] As shown in FIG. **18**E, the second wiring layer **214** having the spiral coil **215** is formed on the second insulating resin layer **213** (second wiring layer formation step).

[0188] The second wiring layer **214** may be formed using the same method as the method for forming the first wiring layers **211** and **212**.

[0189] In other words, a seed layer and a resist layer is formed above the second insulating resin layer **213**. Then, the second wiring layer **214** made of copper or the like is formed on the seed layer using electroplating or the like, as well as forming the second junctions **219** in the second openings **217**.

[0190] In the case where the sealing layer is provided above the second wiring layer **214**, sealing layer may be formed, for example, by patterning a photosensitive resin, such as a photosensitive polyimide resin, using photolithography to form the sealing layer in predetermined positions.

[0191] Next, the operation and the effects of the semiconductor device of this embodiment will be explained.

(1) By setting the width of the second junctions **219** A to be the same as or greater than the line width B of the second wiring layer **214** (the spiral coil **215**), the flow of current is not blocked by the second junctions **219**. Thus, loss can be maintained to a low level. In particular, impedance mismatching within the spiral coil **215** can be prevented at high frequencies.

[0192] Accordingly, a semiconductor device having a spiral coil **215** that exhibits a high Q value (quality factor) can be obtained.

(2) By setting the difference between the width of the contact pads **214***a*, **214***b*, **211***b*, and **212***b* and the width of the second junctions **219** (C−A) to 30 μm or less, the Q value of the spiral coil **215** can be further enhanced.

[0193] The reason why a high Q value is obtained by setting the above-described difference between the widths (C−A) to the above-described range is believed that variations in current distribution can be reduced when current flows in a contact pad.

(3) Since the contact pad **214***a*, **214***b*, **211***b*, or **212***b* is shaped in a substantially rectangular shape, connection failure between the second junctions **219** and the contact pads **214***a*, **214***b*, **211***b*, and **212***b* rarely occurs even when the second junctions **219** are formed misaligned.

[0194] Although the second junctions **219** have a substantially constant width in the direction of the depth in the semiconductor device shown in FIG. **13**, the present invention is not limited to such an embodiment.

[0195] The semiconductor device shown in FIG. **19** is different from the semiconductor device shown in FIG. **13** in that the width of a second junction **229** gradually decreases with an increase in the distance from the surface.

[0196] The second junction **229** may be easily formed by defining a second opening **227** so that the width thereof is decreased with an increase in the distance from the surface.

[0197] In semiconductor device having the second junction **229**, a metal material is evenly distributed to fill within the second opening **227** with no void when the second junction **229** is formed using electroplating or the like.

[0198] Accordingly, malformation of the second junction **229** can be prevented.

[0199] FIGS. **20** and **21** illustrate other embodiments of contact pads.

[0200] A contact pad **224***b* shown in FIG. **20** has a substantially circular shape in plan view, which is different from the rectangular-shaped contact pads **214***a*, **214***b*, **211***b*, and **212***b* shown in FIGS. **14** to **17**.

[0201] A contact pad **234***b* shown in FIG. **21** has a polygonal shape in plan view, which is different from the contact pads **214***a*, **214***b*, **211***b*, and **212***b*.

[0202] The contact pad **234***b* preferably has a polygonal shape having five (pentagon) or more sides. In the example shown in FIG. **21**, the pad has an octagonal shape.

[0203] In the semiconductor device having the contact pads **224***b* and **234***b*, the Q value of the spiral coil **215** can be further enhanced. In particular, the semiconductor device having the substantially circular-shaped contact pad **224***b* exhibits a high Q value.

[0204] The reason why a high Q value is achieved is believed that variations in current distribution can be reduced when current flows in a contact pad.

EXAMPLES

Test Example 2-1 to 2-5

[0205] As shown in FIG. **13**, semiconductor devices including the semiconductor substrate **201** that was a silicon substrate, the first insulating resin layer **210** made of a polyimide resin, the first wiring layers **211** and **212** made of copper, the second insulating resin layer **213** made of a polyimide resin, and the second wiring layer **214** made of copper were manufactured.

[0206] The thicknesses of the first insulating resin layer and the second insulating resin layer **210** and **213** were 10 μm.

[0207] The widths of the first wiring layers **211** and **212** were 30 μm.

[0208] The spiral coil **215** had 3.5 turns, and the line width thereof was 30 μm.

[0209] The second junctions **219** were formed in a square shape in cross-section and the width thereof was set to the values shown in Table 2.

[0210] The contact pads **214***a*, **214***b*, **211***b*, and **212***b* were formed in a square shape, and the width thereof was set to 50 μm.

[0211] The Q value of the spiral coil **215** was measured at a frequency of 2 GHz. The results are listed in Table 1.

TABLE 2

	Width of Second Junction (μm)	Width of Spiral Coil (μm)	Q Value (at 2 GHz)
Test Example 2-1	20	30	25.5
Test Example 2-2	25	30	25.8
Test Example 2-3	30	30	27.0
Test Example 2-4	35	30	27.4
Test Example 2-5	40	30	28.0

[0212] The results in Table 2 indicates that high Q values were achieved by setting the width of the second junctions **219** to be equal to or larger than the width of the spiral coil **215**.

Test Example 2-6 to 2-10

[0213] The semiconductor devices shown in FIG. **13** were manufactured.

[0214] The second junctions **219** were formed in a square shape in cross-section and the width thereof was set to 30 μm.

[0215] The contact pads **214***a*, **214***b*, **211***b*, and **212***b* were formed in a square shape in cross-section and the widths thereof were set to 40 μm, 50 μm, 60 μm, 70 μm, or 80 μm. Other conditions were the same as those of Test Example 2-1.

[0216] The Q value of the spiral coil **215** was measured at frequencies between 0.1 GHz and 20 GHz. The results are shown in FIG. **22**.

[0217] The results in FIG. **22** indicate that higher Q values were achieved when the width of the contact pads **214***a*, **214***b*, **211***b*, and **212***b* were between 40 μm and 60 μm compared to when the width were between 70 μm and 80 μm.

[0218] Since the width of the contact pads was 30 μm, favorable results were achieved when the difference between the width of the contact pads and the width of the second junctions were 30 μm or less.

[0219] The present invention is applicable to various semiconductor device having an induction element, such as, for example, a semiconductor device for non-contact type IC tag in which the induction element functions as an antenna coil.

[0220] While preferred embodiments of the invention have been described and illustrated above, it should be understood that these are examples of the invention and are not to be considered as limiting. Additions, omissions, substitutions, and other modifications can be made without departing from the spirit or scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description, and is only limited by the scope of the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having an electrode formed above a surface thereof;

a first insulating resin layer that is provided over the semiconductor substrate and has a first opening defined at a position corresponding to the electrode;

a first wiring layer that is provided on the first insulating resin layer and is connected to the electrode through the first opening;

a second insulating resin layer provided over the first insulating resin layer and the first wiring layer, the second insulating resin layer having a second opening that is defined at a position different from the position of the first opening in a direction of the surface of the semiconductor substrate; and

a second wiring layer that is provided on the second insulating resin layer and is connected to the first wiring layer through the second opening,

wherein the second wiring layer comprises an induction element, and a sum of a thickness of the first insulating resin layer and a thickness of the second insulating resin layer is not less than 5 μm and not more than 60 μm.

2. The semiconductor device according to claim **1**, wherein a value obtained by dividing a thickness of the first wiring layer by a thickness of the second wiring layer is between 0.3 and 0.5.

3. The semiconductor device according to claim **1**, wherein the induction element is a spiral coil.

4. The semiconductor device according to claim **2**, wherein the induction element is a spiral coil.

5. The semiconductor device according to claim **1**, wherein the first insulating resin layer and the second insulating resin layer are made of a polyimide resin, an epoxy resin, or a silicone resin.

6. The semiconductor device according to claim **1**, further comprising a passivation film which is provided on the surface of the semiconductor substrate and has an opening defined at a position corresponding to the electrode,

wherein the first insulatig resin layer is formed on the passivation film, and

wherein the thickness of the first insulating resin layer is not less than the 1 μm and not more than 30 μm.

7. A semiconductor device comprising:

a semiconductor substrate having an electrode formed above a surface thereof;

a first insulating resin layer that is provided over the semiconductor substrate and has a first opening defined at a position corresponding to the electrode;

a wiring layer that is formed above the first insulating resin layer and is connected to the electrode through the first opening;

a second insulating resin layer that is formed over the first insulating resin layer and the first wiring layer in the position corresponding to the first wiring layer, the second insulating resin layer having a second opening; and

a second wiring layer that is formed on the second insulating resin layer and has an induction element,

wherein the second wiring layer is connected to the first wiring layer via a junction provided in the second opening, and

a width of the junction is equal to or greater than a line width of the second wiring layer that constructs the induction element.

8. The semiconductor device according to claim **7**, wherein the induction element is a spiral coil.

9. The semiconductor device according to claim **7**, wherein the first insulating resin layer and the second insulating resin layer are made of a polyimide resin, an epoxy resin, or a silicone resin.

* * * * *