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[54] **DIGITAL SYSTEM FOR CONTROLLING TRAFFIC SIGNALS**

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[21] Appl. No.: **226,919**

[52] **U.S. Cl.** **340/40**

[51] **Int. Cl.** **G08g 1/07**

[58] **Field of Search** 340/35, 40

[56] **References Cited**

UNITED STATES PATENTS

3,675,196	7/1972	Molloy et al.	340/40
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2,050,039	8/1936	Campbell et al.	340/40

Primary Examiner—William C. Cooper
Attorney—Jack M. Wiseman

[57] **ABSTRACT**

System for controlling traffic signals in which a local controller is located at each controlled intersection, respectively, to control the operation of a traffic signal at its associated intersection. A central controller is connected to the local controllers for the transmission of signals thereto. The central controller is programmed to provide output data which activate the local controllers. The data includes two digital words. One digital word selects the local controller to be activated and the other digital word selects the phase to which the selected local controller is to be advanced. The selected local controllers are operated by the central controller for controlling the traffic lights at their associated intersections. Each local controller includes a set of timers for controlling intervals that are program invariants. The local controllers will continue to operate in a fixed time mode in the absence of an overriding signal for the local controllers. When a local controller is activated by the central controller to advance to a designated light phase, the local controller will advance to the appropriate vehicle clearance interval and to time-out this interval independently before advancing the intersection lights to the phase designated by the central controller.

2 Claims, 11 Drawing Figures

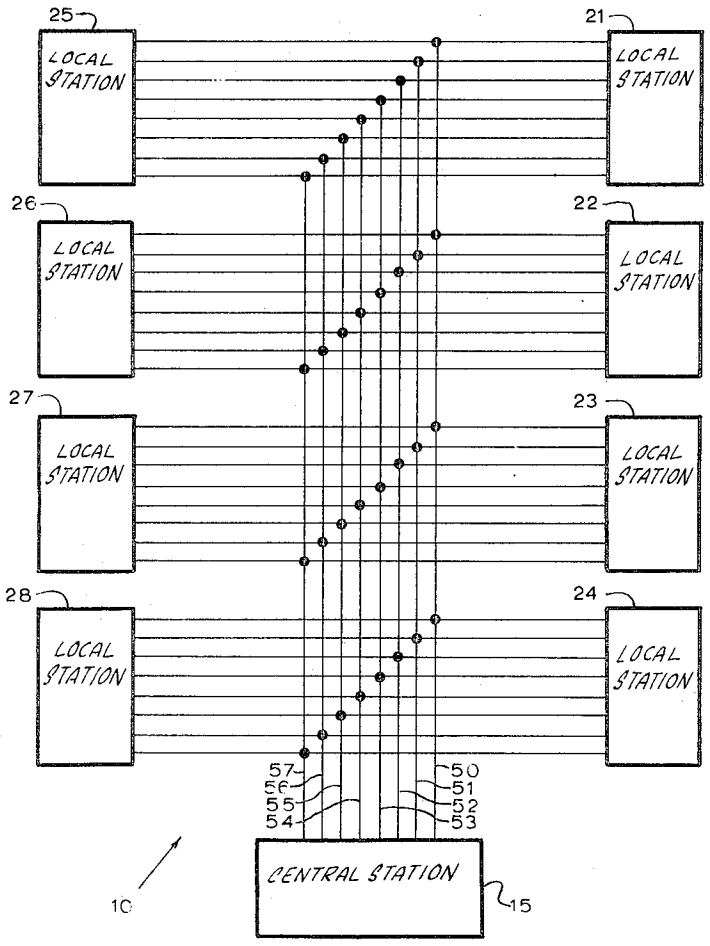


FIGURE 1

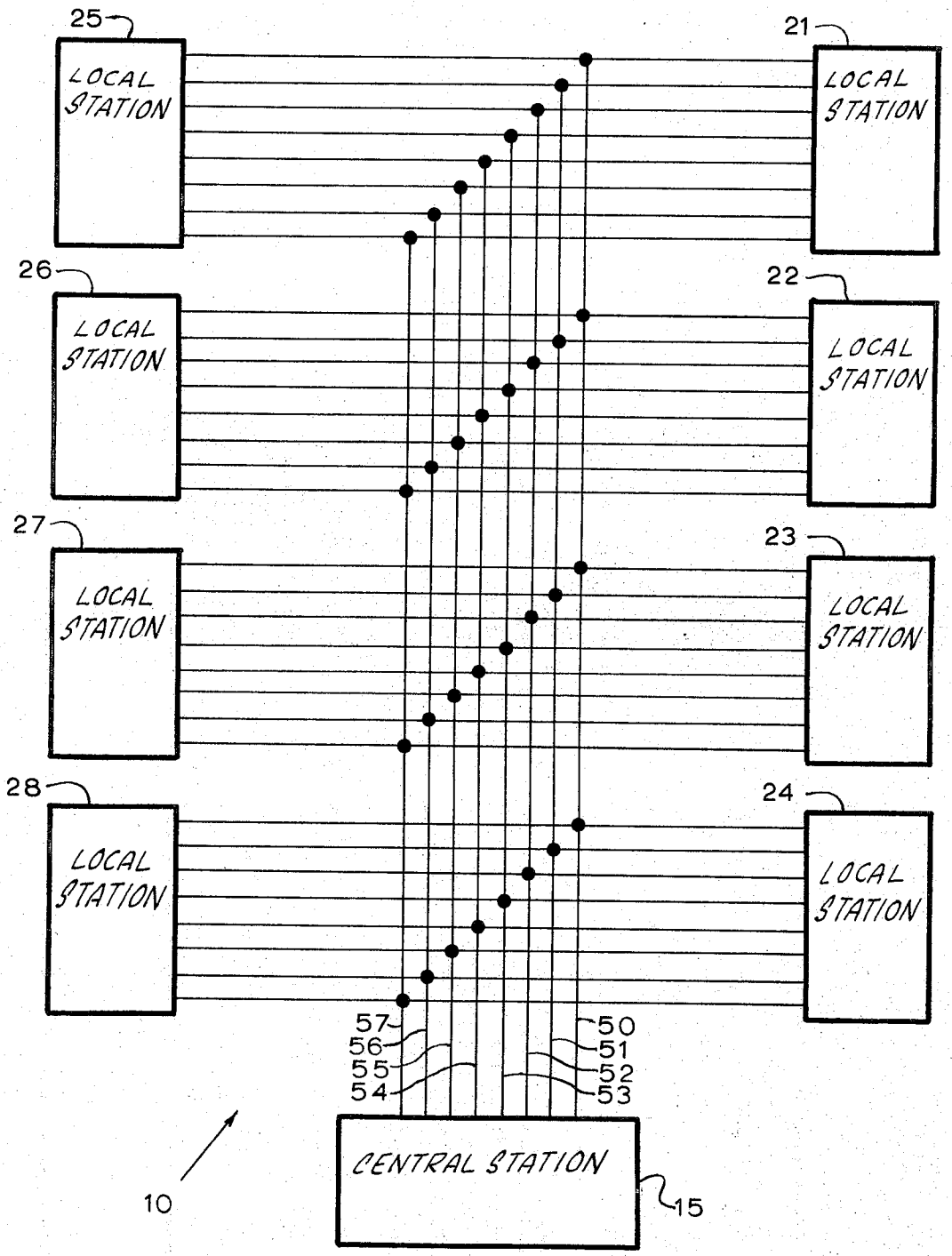

25
LOCAL STATION
21
LOCAL STATION
26
LOCAL STATION
22
LOCAL STATION
27
LOCAL STATION
23
LOCAL STATION
28
LOCAL STATION
24
LOCAL STATION
57
56
55
54
50
51
52
53
CENTRAL STATION
15
10

FIGURE 3d

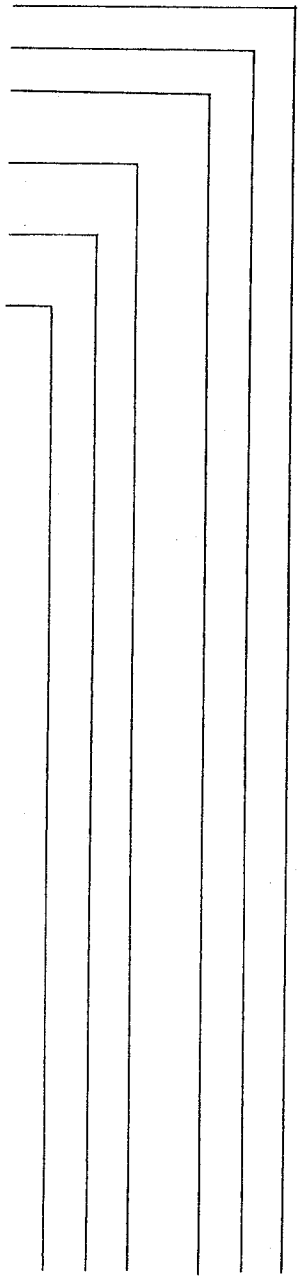


FIGURE 2

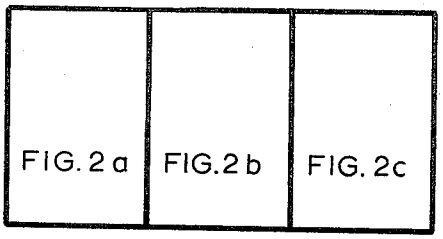


FIGURE 3

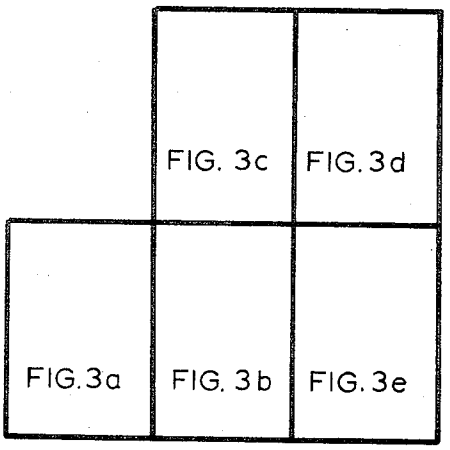


FIGURE 2a

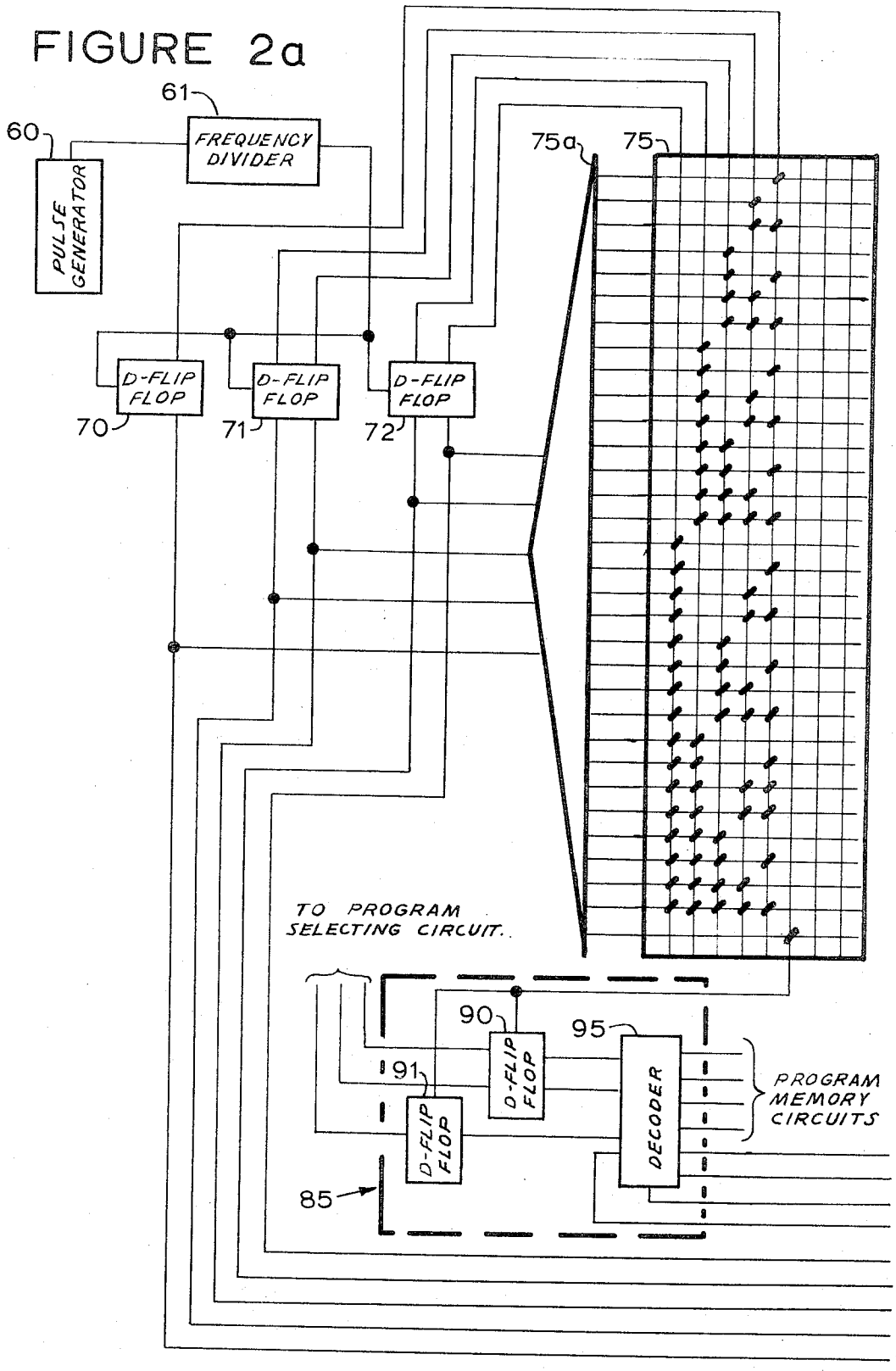

61
60
FREQUENCY DIVIDER
PULSE GENERATOR
75a
75
D-FLIP FLOP
D-FLIP FLOP
D-FLIP FLOP
70
71
72
TO PROGRAM SELECTING CIRCUIT.
90
95
91
D-FLIP FLOP
D-FLIP FLOP
DECODER
PROGRAM MEMORY CIRCUITS
85

FIGURE 2b

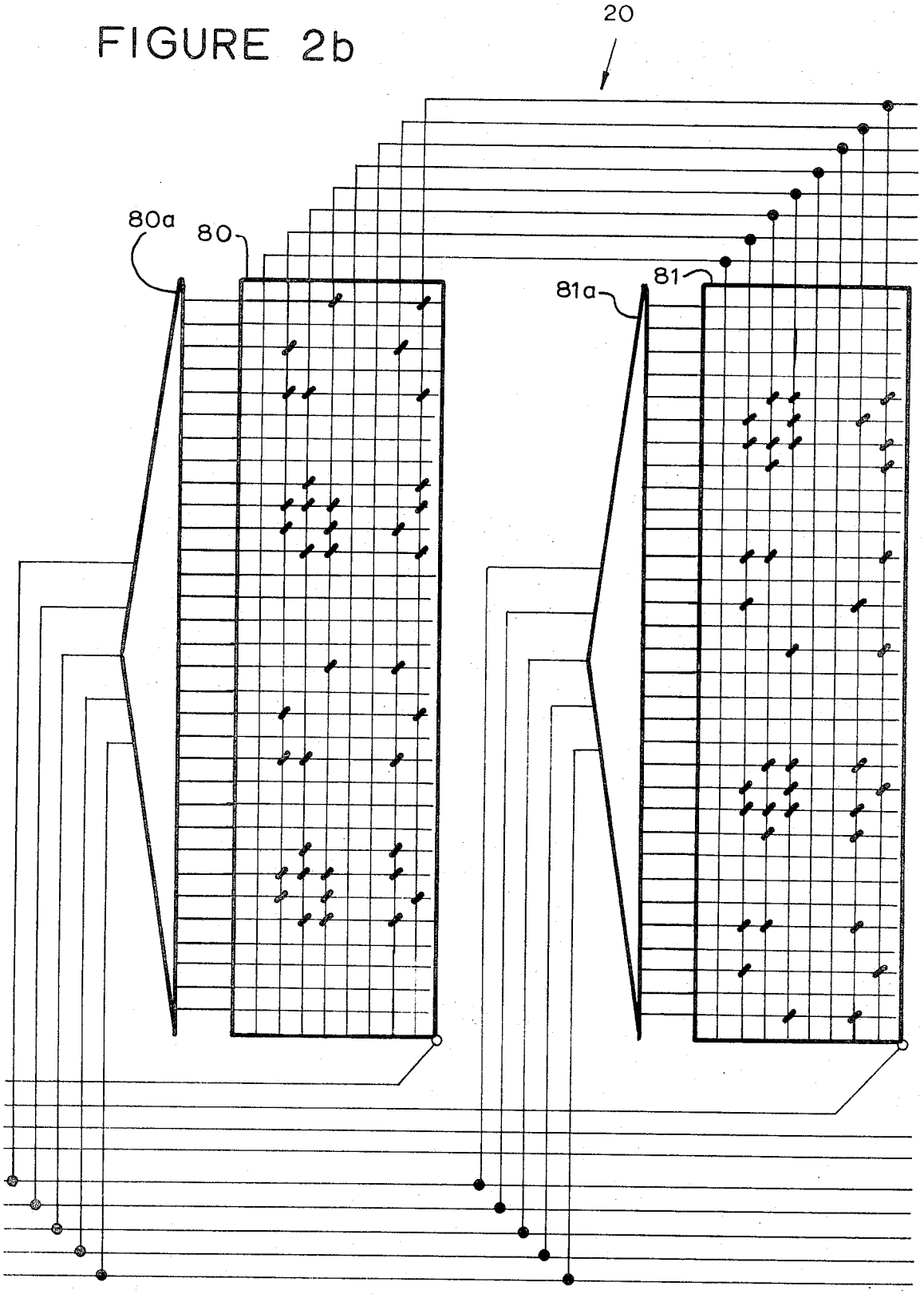


FIGURE 2c

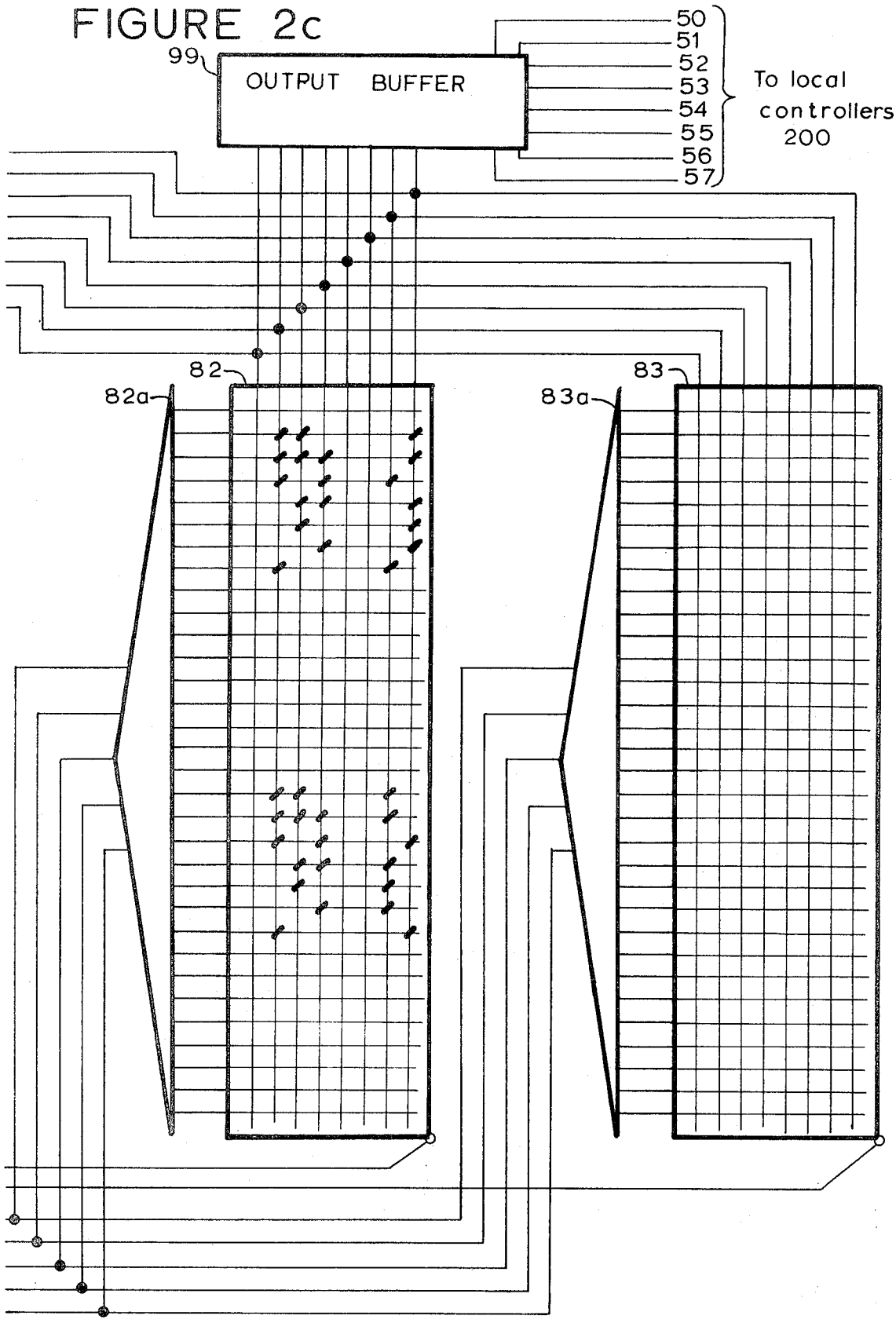

99
OUTPUT BUFFER
50
51
52
53
54
55
56
57
To local controllers 200
82
82a
83
83a

FIGURE 3a

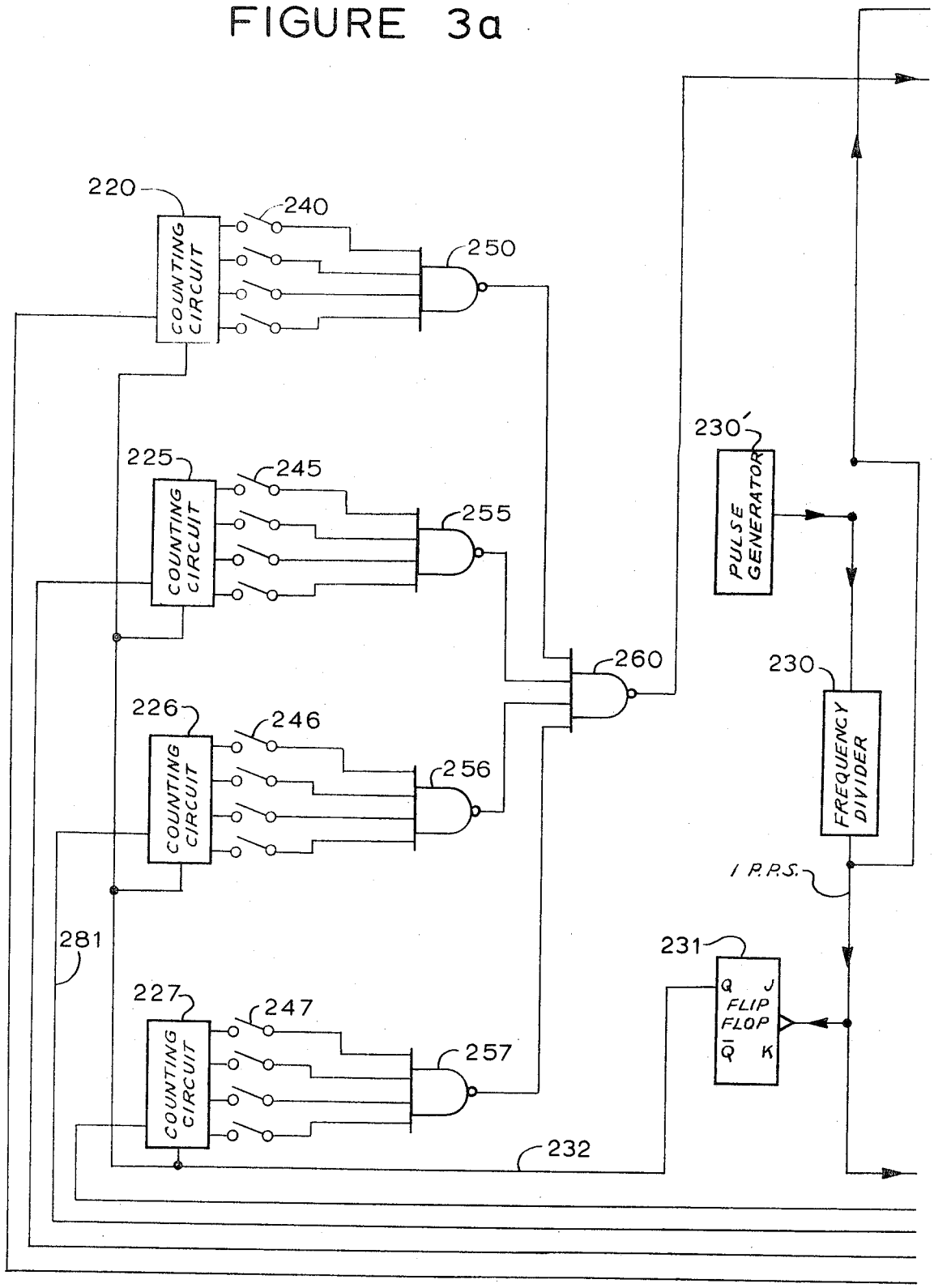

220
240
250
COUNTING CIRCUIT
225
245
255
COUNTING CIRCUIT
226
246
256
COUNTING CIRCUIT
227
247
257
COUNTING CIRCUIT
260
230'
PULSE GENERATOR
230
FREQUENCY DIVIDER
1 P.P.S.
231
Q J
FLIP FLOP
Q̄ K
281
232

FIGURE 3b

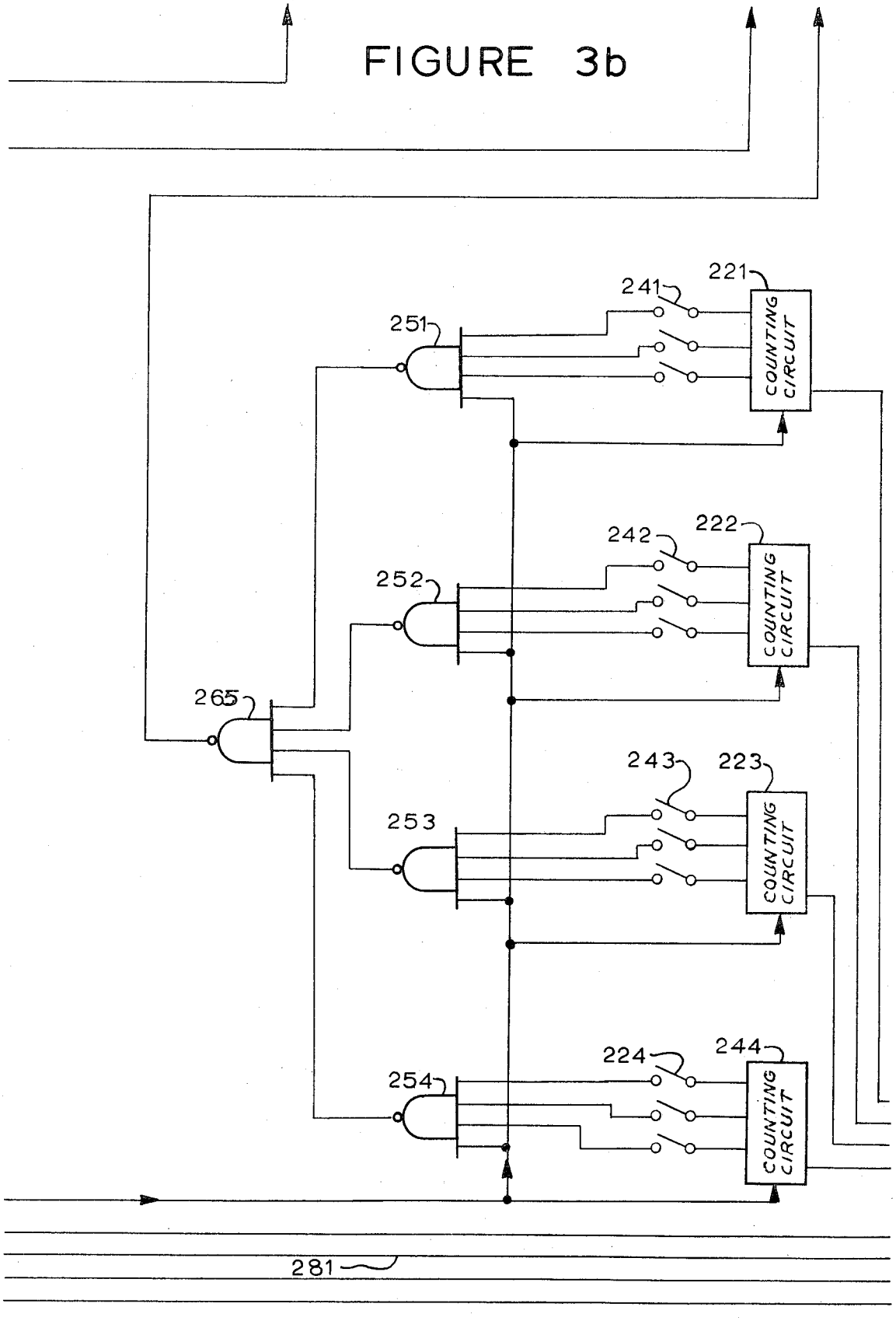

221
241
251
COUNTING CIRCUIT
222
242
252
COUNTING CIRCUIT
265
243
223
253
COUNTING CIRCUIT
224
244
254
COUNTING CIRCUIT
281

FIGURE 3c

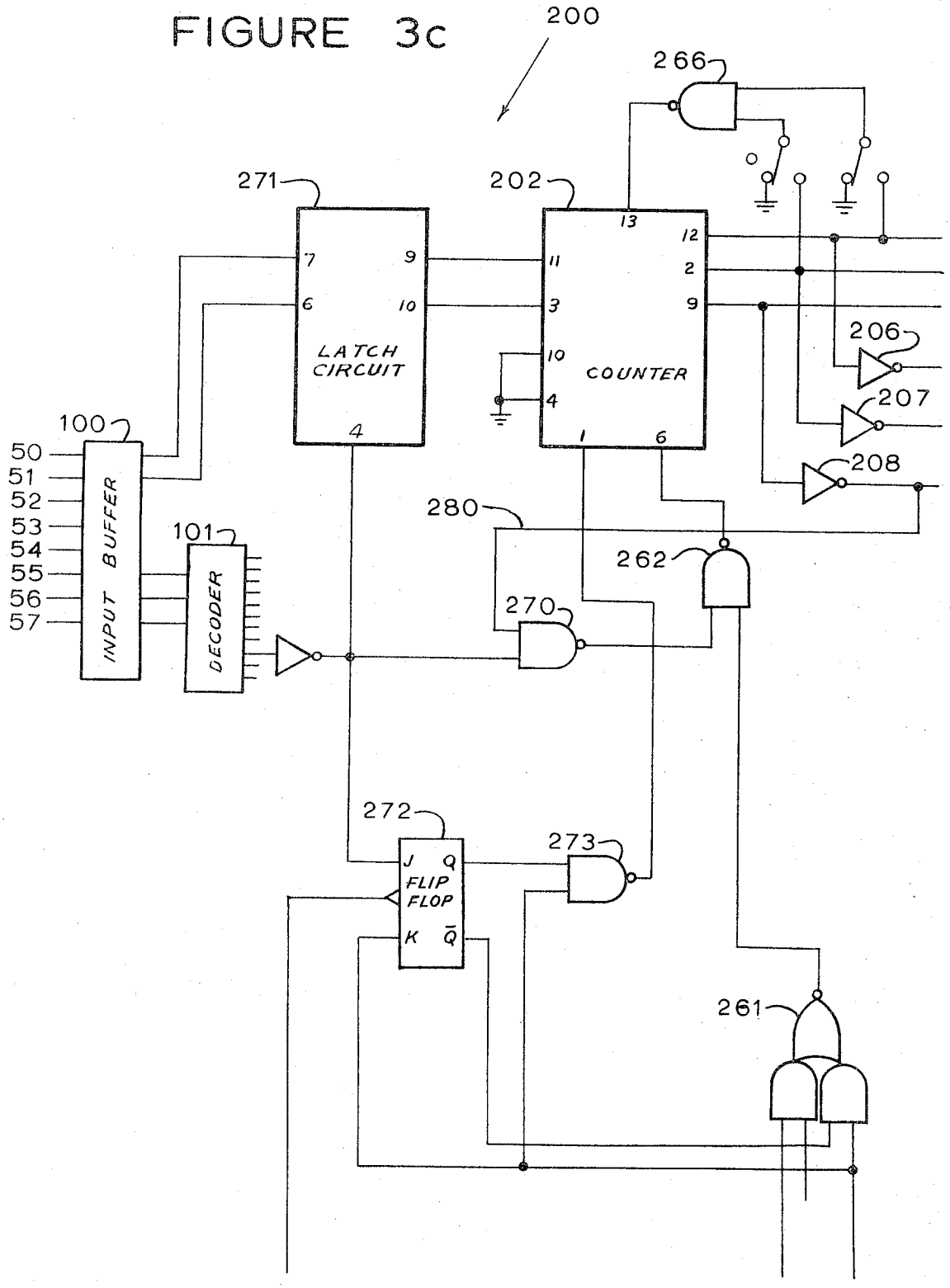
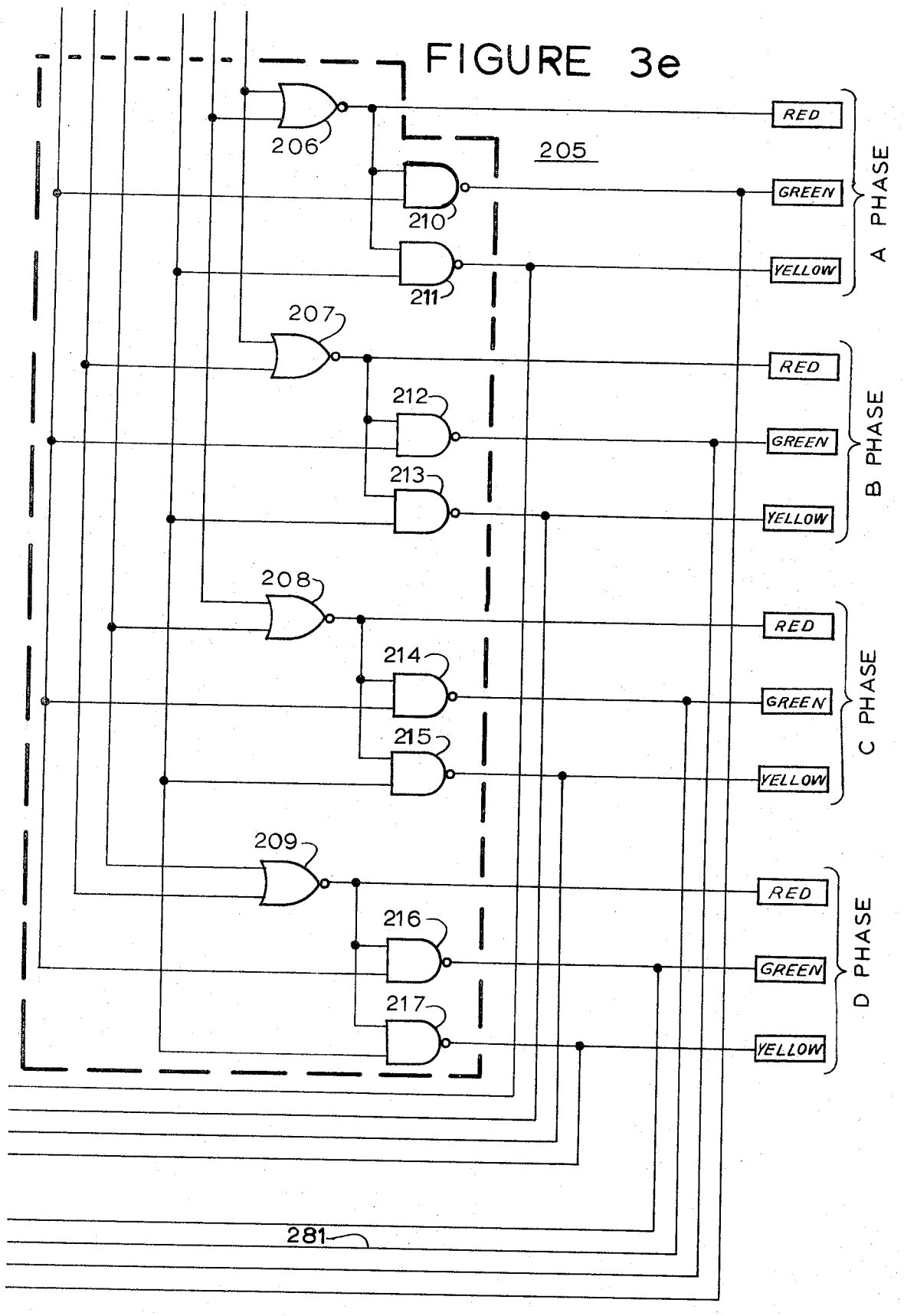

200
266
271
202
LATCH CIRCUIT
COUNTER
206
207
208
100
INPUT BUFFER
50
51
52
53
54
55
56
57
101
DECODER
280
262
270
272
FLIP FLOP
J Q
K $\bar{Q}$
273
261

FIGURE 3e


205
206
207
208
209
210
211
212
213
214
215
216
217
RED
GREEN
YELLOW
A PHASE
B PHASE
C PHASE
D PHASE
281

DIGITAL SYSTEM FOR CONTROLLING TRAFFIC SIGNALS

BACKGROUND OF THE INVENTION

The present invention relates in general to apparatus for controlling traffic signal, and more particularly to apparatus for controlling the phase of a plurality of traffic signals.

Heretofore, each controlled intersection was individually controlled by its individual local controller. Each local controller had its own timing arrangement. Also, a central digital computer operated a plurality of local controllers. To coordinate a series of spaced intersections along a thoroughfare or a series of spaced intersections within a prescribed area, an operator would manually adjust each local controller indivudually or would operate all the local controllers by a central digital computer. However, such systems were not capable of skipping phases and regardless of computer output each local controller must follow the predetermined sequence.

An article of interest is "Contemporary Concepts of Microprogramming and Emulation" by Robert F. Rosin appearing in "Computer Surveys," Vol. 1, No. 4, December 1969, and a book entitled "Microprogramming" by Husson. Also of interest is a report by Stanford Research Institute dated October 1971 entitled "Chicago CBD Traffic Control System." Multi Sonics Development Corporation of Alamo, Calif. has manufactured and sold Model FR-200 On-Line Master Computer for traffic control, and FR-100 Traffic Controllers. Gulf-Western Industries at Davenport, Iowa has manufactured and sold MC 20 Lines Controllers for digital coordination or pretimed control.

SUMMARY OF THE INVENTION

A system for controlling the operation of a plurality of traffic lights in which a central controller transmits signals to local controllers for selecting one or more local controllers for activation and for preselecting a phase at which the selected local controllers would operate their associated traffic lights.

A feature of the present invention is that the selected local controllers can skip or omit any phase upon command from the central controller. In the absence of a command from the central controller the local controllers, respectively, will operate at preset fixed times modes.

By virtue of the present invention, traffic signals along a thoroughfare or within a preselected area can be automatically coordinated from a central station to effect an optimum flow of traffic through continuous movement of vehicles at an optimum velocity at greatly reduced circuit complexities.

Another feature of the present invention is that the central controller is programmed with a plurality of predetermined programs. Data transmitted by the central controller to the local controllers comprises a series of signals to select one or more of the local controllers to be activated and also comprises a series of signals to select the phase at which the selected local controllers advance to operate their respective associated traffic lights. A local controller may be activated by the central controller and the local controller may be locally controlled for a preselected fixed time operation.

DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a system for controlling traffic signals embodying the present invention.

FIGS. *2a–2c* when placed in the manner shown in FIG. **2** is a schematic diagram of the central controller employed in the system shown in FIG. **1.**

FIGS. *3a–3e* when placed in the member shown in FIG. **3** is a schematic diagram of a local controller employed in the system shown in FIG. **1.**

DESCRIPTION OF THE PREFERRED EMBODIMENTS

General Description

Illustrated in FIG. **1** is a system **10** for controlling traffic signals embodying the present invention. The system **10** comprises a central station **15,** which includes a central controller **20** (FIGS. *2a–2c*), and a plurality of local stations **21–28.** EAch of the local stations **21–28** include a local controller **200** and intersection traffic lights. In FIGS. *3a–3e* is illustrated the local controller **200.** All local controllers **200** include like parts and operate in a similar manner. Suitable conductors **50–57** carry signals from the central controller **20.** Each local station **21–28** includes suitable terminals for connection to the conductors **50–57** for receiving signals transmitted from the central controller **20.** While signals are shown to be transmitted in parallel, it is apparent that the transmission may be effected by serial means. This would entail the addition of appropriate converters.

The central controller **20** is programmed with preselected data stores in semiconductor devices. An operator or computer selects one of the programs by selecting a memory device and thereby transmits data representing information stored in the selected memory devices over the conductors **50–57.** The data contained in the selected memory device has two words. The first word activates selected local stations **21–28** and the second word operates the local controllers of the selected local stations for advancing the associated traffic signals to a designated phase.

CENTRAL CONTROLLER CIRCUITS

As shown in FIGS. *2a–2c*, the central traffic controller **20** comprises a conventional timer or time pulse generator **60** that produces 60Hz clock pulses. The clock pulses are fed to a conventional pulse frequency divider circuit **61.** In the exemplary embodiment, the output frequency of the clock pulses for the divider circuit **61** is such that the leading edge of a clock pulse occurs every 2 seconds and a traffic control cycle occurs every 64 seconds.

The output of the clock pulse divider circuit **61** provides clock signals for three edge-triggered D-type flip-flop circuits or bistable binary devices **70–72.** The flip-flop circuits **70-72** incorporate therein two binary circuits in each package anc can be implemented by the Texas Instruments SN 7474. The logic data applied to the input side thereof is transferred to its output side upon the positive going transition or leading edge of the clock signal.

The flip-flop circuits **70–72** produce logic levels which are fed into a sequence memory circuit **75** through a memory decoder **75a** and also to eight program memory circuits, only four of which are shown, namely: program memory circuits **80–83.** The trans-

mission to the respective program memory circuits **80–83** are through their associated memory decoders **80***a*–**83***a*. It is to be observed that the program memory circuits **80–83** are connected in parallel to the output of the flip-flop circuits **70–72** as is the sequence memory circuit **75.** Therefore, the output of the flip-flop circuits **70–72** are transmitted simultaneously to the sequence memory circuit **75** and all of the program memory circuits, such as **80–83.**

The sequence memory circuit **75** is programmed to function as a counter. However, the program may be varied so that the count may be in a numerical sequence as in the Wilkes principle. The sequence memory circuit **75** is conventional and is similar to the 8223 FROM device produced by Signetics Corp. of Sunnyvale, Calif.

The output of the sequence memory circuit **75** provides the address of the next word in the sequence. In addition thereto, the sixth bit of the output of the sequence memory circuit **75** provides a clock input to a program select circuit **85.** More specifically, the clock input transfers the logic levels on the input of D-type flip-flop circuits **90** and **91** in the manner previously described for the flip-flop circuits **70–72.** This action inhibits a change in program until the end of a cycle. The input signals for the flip-flop circuits **90** and **91** may be from any suitable source such as a time clock.

The program selecting apparatus will preset or precondition the flip-flop circuits **90** and **91** for a prescribed program operation. At the end of each cycle, which is when the last word of the sequence memory circuit **75** is being addressed, the sequence memory circuit **75** emits an output signal to change the state of the flip-flop circuits **90** and **91.** Connected to the output of the flip-flop circuits **90** and **91** is a conventional **4** to **16** decoder circuit **95.**

The output of the decoder **95** includes, in the exemplary embodiment, eight output terminals. The program memory circuits, such as program memory circuits **80–83** are connected respectively to the output terminals of the decoder **95** and the program memory circuits are respectively enabled or disabled by the signals appearing on the associated output terminal on the decoder circuit **95.** Thus, for each given program selection only one of the program memory circuits will be operated through the program selector circuit **85.** More specifically, for each different program selection a different program memory circuit will be operated. Only one program memory circuit is operated during a given selected program. The decoder **95** is conventional and is procuced by Signetics Corp. of Sunnyvale, Calif. as device No. 74,154 or 74,141. The flip-flops **90** and **91** with the decoder **95** serve to inhibit the changing of a program in the middle of a cycle and would tend to reduce operation changes from false signals.

The program memory circuits, such as program memory circuits **80-83,** receive simultaneously the output logic from the flip-flop circuits **70-72.** Only one of the program memory circuits will be enabled by the program selector circuit **85** to operate during a given program cycle.

Each of the program memory circuits **80-83** is individually programmed with a preselected code of eight bit words. The first four bits select the local controller or controllers of the controller stations **21–28** to be addressed. The next four bits select the phase at which the selected local controller or controllers will operate in order to activate the associated traffic displays or lights.

The program memory circuits are similar to devices **8223** FROM produced by Signetics Corp. of Sunnyvale, Calif. The output terminals of the program memory circuits **80–83** are connected in the OR configuration to an output buffer **99.** Hence, the only data that is presented to the output buffer **99** is the word being addressed in the enabled memory circuit of the memory circuits **80–83.** The output buffer **99** may be any suitable signal conditioning device which changes the output signals to render the same compatible with the signal transmission facilities. In the exemplary embodiment, the output signals from the buffer **99** are transmitted in parallel over the conductors **50–57.** When a serial converter is employed for series transmission the number of conductors may be reduced.

From the foregoing, it is to be observed that the output of the sequence memory decoder **75***a* is gated through the flip-flop circuits **70–72.** The output of the flip-flop circuits **70–72** is transmitted to the input of the sequence memory decoder **75***a* and to the input sides of the program memory circuits **80–83.** The logic levels produced by selected program memory circuit are transmitted to the output buffer **99,** which then transmits the code pulses over the conductors **50–57** to the local controllers **200.** At the end of each cycle, the sequence memory circuit **75** operates the flip-flop circuits **90** and **91** of the program select circuit **85.**

LOCAL CONTROLLER

Illustrated in FIGS. **3***a*–**3***e* is a local controller **200** which produces clock pulses of an adjustable constant frequency transmitted from a clock pulse generator **230'**. A presettable binary counter circuit **202** has clock pulses applied to its pulse terminal **6** which controls the logic on its output terminals **12, 2** and **9.** The counter circuit **202** is an integrated circuit manufactured by Texas Instruments as SN 74,197.

Connected to the output of the counter circuit **202** is a decoder circuit **205** which includes NOR gate circuits **206–209,** NAND gate circuits **210–217.** The gates **206–217** of the decoder circuit **205** will selectively have an output 1 potential or a zero potential. When the output potential of a given gate is 0 or low, its associated lamp is illuminated. When the output potential of a given gate is 1 or high, its associated lamp is extinguished. For example, if the output at pins **12, 2** and **9** of the counter circuit **202** were all low (000), then the output potentials for the gate circuits **207–209** are low, and the associated red lamps will be illuminated. Also, the output potential of the gate circuit **206** is high, or at a 1 potential, and the red lamp connected to its output is extinguished. At this time, the output of the gates **211, 213, 215** and **217** will be high to extinguish the yellow lamps associated therewith. The gate circuit **210** will be low to illuminate the green lamp associated therewith. The traffic lights are well-known and are conventionally operated in a well-known manner through the associated gate circuits **206–217.** The traffic lights or displays with the operating circuits thereof are designated red, yellow and green for the respective phases A-D. The NAND gates **210–217** are manufactured by Signetics or Texas Instruments as SN 7400 integrated circuits.

With the output of the NAND gate **210** at zero potential, the input terminal of the counter circuit **220** is at

low potential and the input terminal of counter circuits **221–227** are high. Therefore, the counters **221–227** are reset to zero and held in that condition. The counters are conventional counters of the type manufactured by Signetics or Texas Instruments as SN7493. With the input terminal thereof at zero potential the counter **220** is enabled for counting. The frequency divider **230,** which has a frequency of one pulse per second, is connected to a JK flip-flop circuit **231.** The clock pulse output from the JK flip-flop **231** is transmitted simultaneously to the counters **220** and **225–227** over a conductor **232.** Each time the counter **220** receives a clock pulse from the JK flip-flop circuit **231,** which is once every **2** seconds, the output thereof is advanced by one binary digit. The counters **225–227** are not enabled at this time to count. The JK flip-flop is manufactured by Signetics or Texas Instruments as a SN 7473 integrated circuit.

Connected to the output circuits of the binary counters **220** and **225–227** are switching networks, **240** and **245–247** and connected to the other side of the switching networks **240** and **245–247** are NAND gate circuits **250** and **255–257.** The NAND gate circuits **250** and **255–257** are manufactured by Signetics or Texas Instruments as SN **7420** integrated circuits. It is apparent to one skilled in the art that "pull up" resistors at the input of the NAND gates **250–257** may be required.

When the counter **220** has advanced to a binary output 15 (1111), 32 seconds has elapsed. At this time, the NAND gate **250** will have a zero potential on its output, assuming that all switches are closed. This action causes the output of a NAND gate circuit **260** to go high or to a 1 potential. Prior to the NAND gate **250** having a zero potential at its output, all the input circuits to the NAND gate **260** were high, and also all the input circuits except for the terminal **9** of an AND-OR-INVERT gate **261** were low. The time required for the input of the NAND gate **250** to reach the 1111 state can be varied by the switching network **240.** The NAND gate **260** is manufactured by Texas Instruments as SN 7430 integrated circuit and the AND-OR-INVERT gate **261** is also manufactured by Texas Instruments as a SN 7451 integrated circuit.

When the output potential for the NAND gate **260** goes high, the output of the AND-OR-INVERT **261** goes to zero potential. Initially, the input to a NAND gate **262** is high. With the output of the AND-OR-INVERT gate **261** low, the output of the NAND gate **262** goes to a 1 potential. The counter **202** does not count until the clock input at the terminal **6** goes low. This occurs when the input to the NAND gate **250** advances to something other than 1111.

When the output from the counter **220** goes from a **1111** output to a **0000** output, the NAND gate **250** will have a 1 potential on its output. The output potential of the NAND gate **260** will go low. When the output potential of the NAND gate **260** goes low, the AND-OR-INVERT gate **261** has a 2 potential on its outpout terminal. As a consequence thereof, the output of the NAND gate **262** goes low and the potential applied to the clock terminal of the counter circuit **202** goes low. Thereupon, the output of the counter circuit **202** advances from a 000 output to a 001 output on the output terminals **12, 2** and **9** thereof.

When the counter circuit **202** advances to the **001** output potential, the gate **211** of the decoder **205** goes low to illuminate the yellow lamp of the A phase cycle, and the outputs of the gates **206** and **210** of the decoder **205** are high so that the A phase green and the A phase red lamps are off. The outputs of the gates **207-209** are low to illuminate the red lamps of the B, C and D phases.

With the output of the gate **211** of the decoder **205** low, the terminal **2** of the counter **221** is low. Thereupon the counter **221** is enabled for counting and the counters **222–224** will be held at 0000 output potential state. The clock generator **230'** through the frequency divider **230** supplies the clock pulses to operate the counter **221** for a counting cycle. In the counters **221–224** only three bits are used so that each counter can count up to binary **7.** The clock pulses transmitted by the clock pulse generator **230** are fed to the NAND gates **251–254.**

When the input to the NAND gate **251** reaches **111,** the output of the NAND gate **265** goes high. The high output potential of the NAND gate **265** changes the state of the AND-OR-INVERT gate **261** to turn on the NAND gate **262.** This action transmits a pulse to the input terminal **6** of the counter circuit **202** to advance the counter **202** to **010** potential output on its terminals **12, 2** and **9.**

The purpose of switching networks **240–247** is to adjust the green light duration for the various phases. The opening of a switch presents a high potential to the associated NAND gate circuit. When the counter output is low, the opening of the switch causes the associated NAND gate circuit to operate as if the counter output is 1 although it may actually be zero.

The foregoing steps are continued for all of the four phases of operation. Should it be desired to use the local controller **200** as a two or three phase unit, then the input signal to a NAND gate **266** will be connected to the output of the counter circuit **202.** In the two phase operation, one of the inputs to the NAND gate circuit **266** would be opened and the other input would be connected to terminal **12** of counter circuit **202.**

The A phase green lamp will be illuminated when the potential output from the counter circuit **202** to the decoder **205** is 000. The A phase yellow lamp will be illuminated when the potential output from the counter circuit **202** to the decoder **205** is 001. The B phase green lamp will be illuminated when the potential output from the counter circuit **202** to the decoder **25** is 010 and the B phase yellow lamp will be illuminated when the potential output from the counter circuit **202** to the decoder **205** is 011.

At the end of the B phase yellow time sequence, the potential applied to the input of the decoder circuit **205** from the output of the counter circuit **202** is 100. At this time, the input terminals of the NAND gate **266** are at a high potential. The output of the NAND gate **266** goes low to clear the counter **202** and reset the output potential thereof to 000. The clearing and resetting takes less than a microsecond. In a three phase operation, the input of the NAND gate **266** is connected to the output terminals **12** and **2** of the counter circuit **202.**

Should the central controller **20** (FIGS. **2***a*–**2***c*) transmit signals to the local controller **200** over conductors **50–57** to override the fixed time pulses of the frequency divider **230,** then the local controller **200** can be operated to advance to a preselected phase. The output of the central controller **20** will include a code for addressing the intersection and for selecting the

phase. For example, A phase would be encoded with **00**, B phase with an **01**, C phase with a **10** and D phase **11**.

The local controller **200** includes an input buffer **100** with level changing and signal squaring devices connected to the conductors **50–57**. The output of the buffer **100** is connected to a latch circuit **271** and the decoder **101**. The output of the decoder **101** provides input for a NAND gate circuit **270** and the J input to a JK flip-flop circuit **272**. The latch circuit **271** may be of the type manufactured by Texas Instruments as SN 7475 and the JK flip-flop circuit **272** may be of the type manufactured by Texas Instruments as SN 7473. The output of the NAND gate **270** is connected to the NAND gate circuit **262** and the output of the NAND gate circuit **273** is connected to the counter circuit **202**. The logic transmitted from the central controller **20** to the latch circuit **271** are the phase bits of the transmitted code and the logic transmitted to the JK flip-flop **272** from the central controller **20** through the decoder **101** is dependent upon the address output bits for the intersection of the transmitted code pulses.

Assuming that the local controller is illuminating the A phase green lamp and is to be advanced to the C phase green lamp. Under these circumstances, the potential on the input terminal **6** of the latch **271** is low. The latch **271** has the data or potential applied to the input transferred to its output when the clock input to terminal **4** thereof is at a high or 1 potential.

The input buffer **100** provides a **10** to the terminals **7** and **6** of the latch **271** and the output of the inverter would go high. This would transfer data on the input of the latch **271** to the output thereof at the pins **9** and **10**. At this time, the flip-flop **272** is set and input of the NAND gate **270** goes high.

When the data was transferred to the output of the latch **271**, such data was transmitted to the input side of the counter circuit **202**. When the output of the NAND gate **273** is low so that the potential applied to the load terminal **1** of the counter circuit **202** is low, the input data applied to the terminals **11, 3** and **10** of the counter **202** are transferred to the output terminals **12, 2** and **9** of the counter **202**. The output of the counter **202** at that time is **100**.

The pulse from the central controller **20** that had set the latch **271** also applies a high potential to the J input of the JK flip-flop **272**. The truth table for the JK flip-flop **272** is as described in the Signetics or Texas Instruments data sheet or catalogues.

Applied to the JK flip-flop are clock or timing pulses from the frequency divider **230**. At the falling edge of the clock pulse applied to the JK flip-flop **272**, the flip-flop **272** is set with the Q high and the $\overline{Q}$ low.

If the controller **200** is in a yellow state, the input to the NAND gate **270** from the output of the inverter **208** is low. Consequently, the counter **202** cannot be advanced while the local controller is in the yellow state except when advanced by one of the counters **241-244**. Should the controller **200** be in a green state, the input to the NAND gate **270** from the inverter **208** is high permitting the logic from the decoder **101** to activate the NAND gate **262**.

When the NAND gate **270** output is low, the potential input of the NAND gate **262** is low. Although the input on the other terminal of the NAND gate **262** is high, the output of the NAND gate **262** will go high. With the potential applied to the clock terminal **6** of the counter **202** high, the counter circuit **202** advances the count thereof by 1 at the falling edge of the clock pulse. The falling edge occurs when the potential applied to the input terminal of the latch circuit **271** from the central controller **20** through the buffer **100** and the decoder **101** is zero. At this time, the output of the counter **202** is advanced to a 001 from a 000 and the state advances from an A phase green to an A phase yellow. The counter circuit **221** now is enabled by the NAND gate **211** and starts to count from the pulses transmitted from the clock pulse generator **230**. Thus, the counting by the counter circuit **221** is independent of the code transmission by the central controller **20**.

At the termination of the prescribed counting pulses of the yellow phase time period, the output of the NAND gate **251** is low and the output of the NAND gate **265** is high. This action applies a high potential to the input terminal of the AND-OR-INVERT gate **261**, the input terminal of the NAND gate **273**, and K input terminal of the JK flip-flop circuit **272**. The state of the AND-OR-INVERT gate **261** is not changed because of the AND condition with the $\overline{Q}$ output of the JK flip-flop circuit **272**, which is connected to the input terminal of the AND-OR-INVERT gate **261**. The $\overline{Q}$ output of the JK flip-flop circuit **272** is low at this time. However, the Q output of the JK flip-flip circuit **272** applies a potential to the input terminal of the NAND gate **273** to cause the output of the NAND gate **273** to be at a low potential. This action causes a low potential to be applied to the count/load terminal **1** of the counter circuit **202**, thereby pre-loading the counter circuit **202** with the data applied to the input terminals **11, 3** and **10** of the counter circuit **202**. Now, the counter outpout is **100** or a C phase green.

The output of the NAND gate **265** is also applied to K input of the JK flip-flop **272** so that the $\overline{Q}$ output terminal thereof is at a high potential and the Q output terminal is at a low potential. When the clock input from the pulse generator **230** goes low the local controller is in C phase green and the counter circuit **226** is counting. When the local controller is in C phase green, the output of the NAND gate **214** is at a low potential. The potential is applied to a conductor **281** and thereby to the input terminal of the counter **226** to enable the counter circuit **266** to count. Counting pulses are transmitted from the clock pulse generator **230** through the JK flip-flop circuit **231** to the clock input terminal of the counter **226**.

I claim:

1. A traffic control system comprising:

a. a central control unit, said central control unit comprising means for transmitting respectively a plurality of selectable programs;

b. a plurality of local control units;

c. a plurality of traffic control displays connected to each of said local control units, said traffic control displays being operatively controlled by the local control unit connected thereto,

d. data of the selected program transmitted by said central control unit to said local control units selecting at least one of said local control units to be operated;

e. each of said local control units comprising timing means to provide signals for controlling the operation of the traffic control displays connected to the local control unit; and

f. means in said central control unit for providing data to said selected local control unit to dominate the operation of the selected local control over the signals provided within the selected local control unit for controlling the operation of traffic control displays connected to the selected local control unit.

2. A traffic control system as claimed in claim 1 wherein said selected control unit comprises circuit means for disabling the timing means thereof in controlling the operation of the traffic control displays connected thereto in response to said central control unit providing therefor a signal for controlling the operation of the traffic control displays connected thereto.

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