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(54) **METHOD AND APPARATUS FOR INDEPENDENT READOUT AND RESET OF PIXELS WITHIN A CMOS IMAGE SENSOR**

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(57) **ABSTRACT**

A method of increasing the flexibility of the read out and reset functions of a CMOS image sensor is disclosed. This architecture allows new and unique modes of operation. These include the ability to read out and reset the pixels within a row simultaneously, for maximum exposure time, and the ability to reset a selected pixel or a selected group of pixels independently, without resetting any other pixels within the array, allowing the exposure time to be different than the frame time. Also allowing integration time to be unique for every pixel I the array

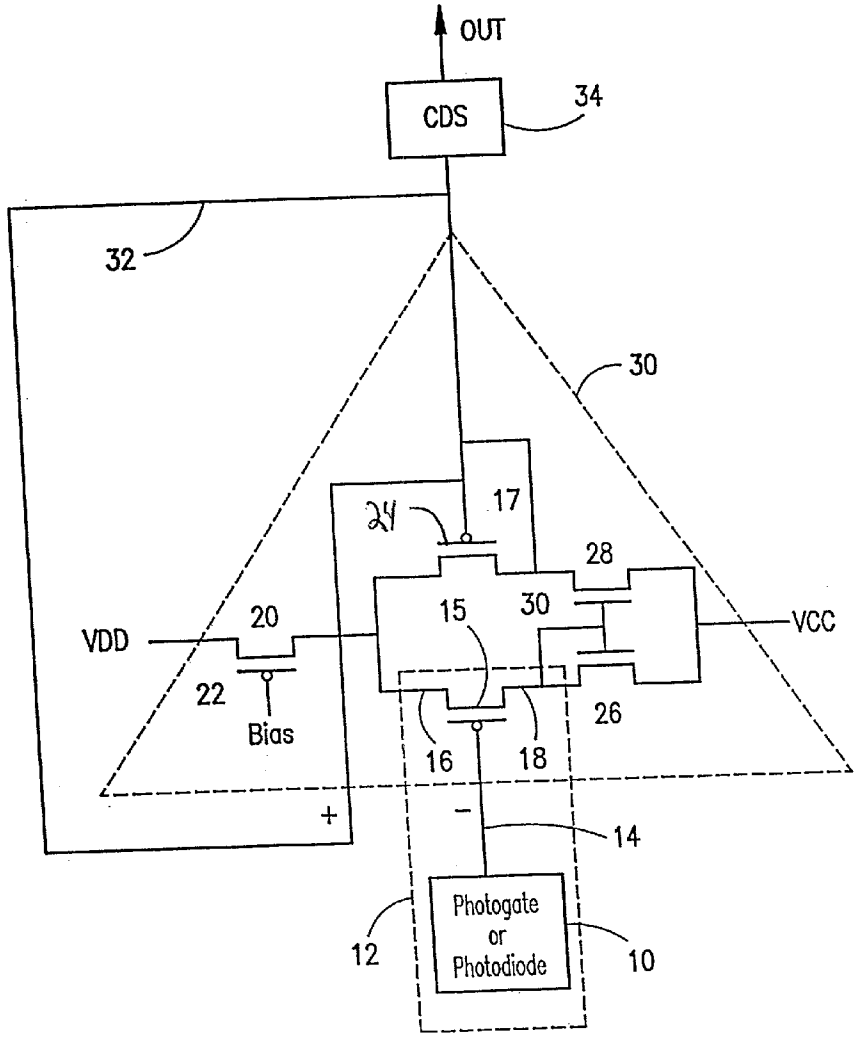
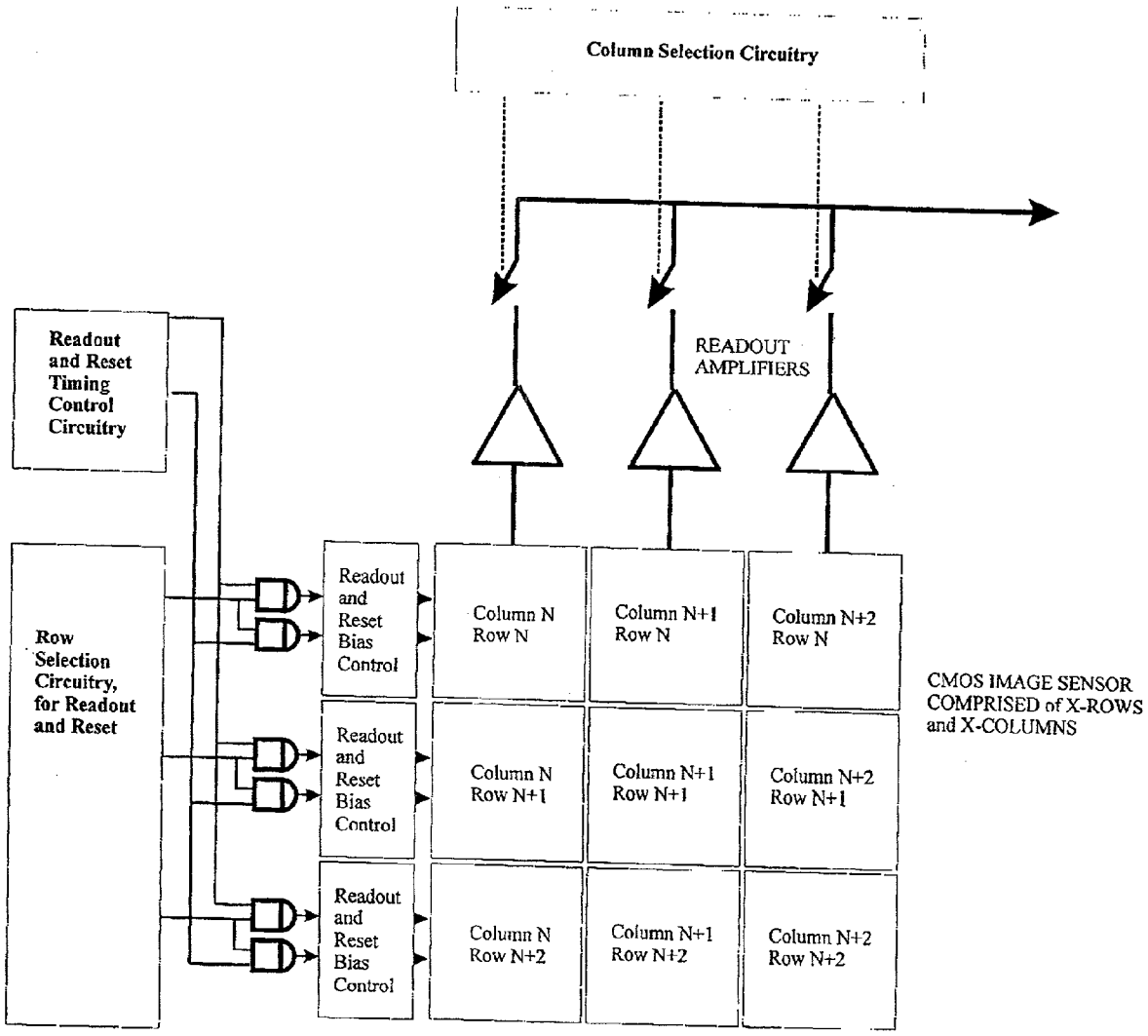


Figure 1, Fixed Readout and Reset



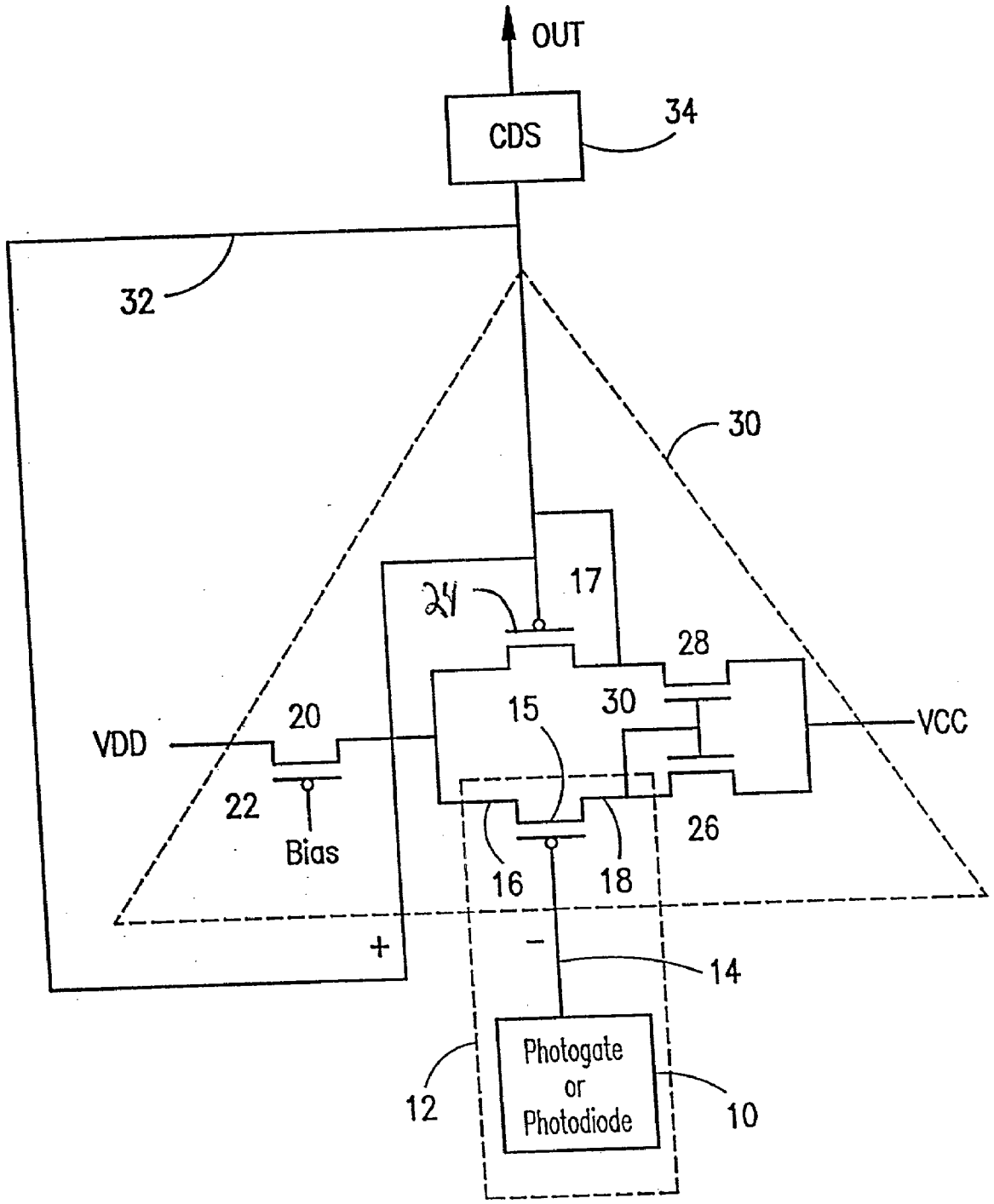

OUT
CDS
34
32
30
24
17
28
15
30
VDD
20
VCC
22
Bias
26
16
18
+
−
14
Photogate
or
Photodiode
12
10

FIG. 2

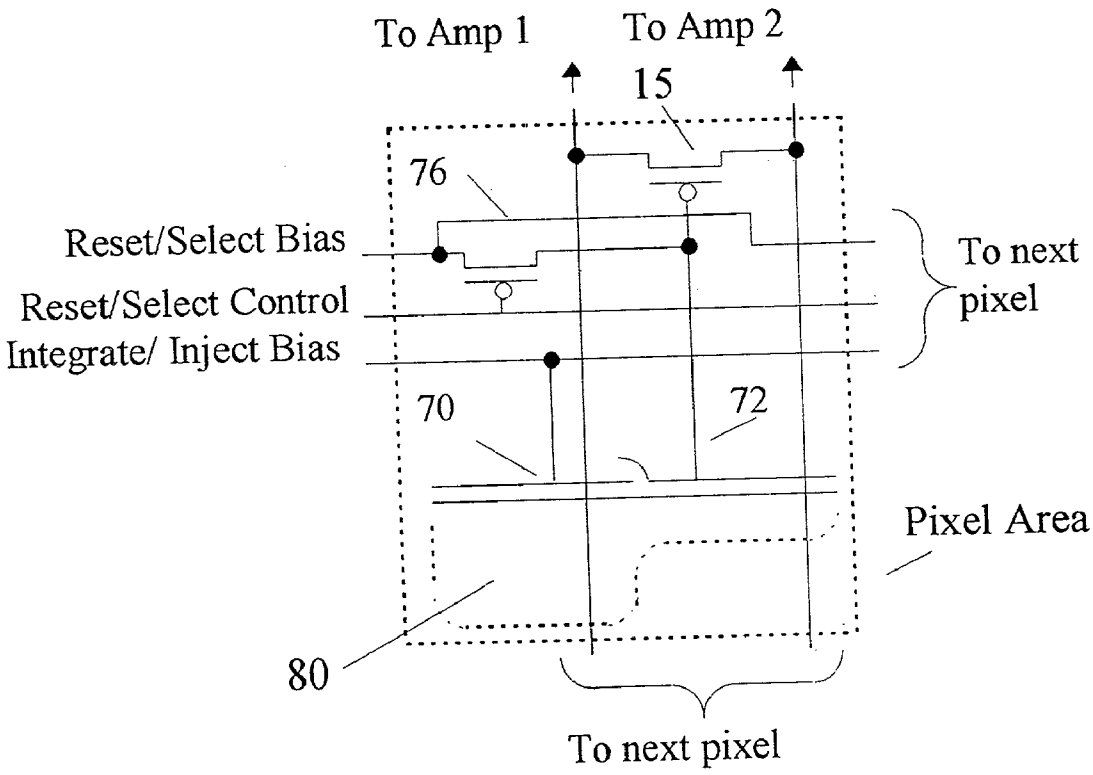

To Amp 1
To Amp 2
15
76
Reset/Select Bias
Reset/Select Control
Integrate/ Inject Bias
To next pixel
70
72
Pixel Area
80
To next pixel

Figure 3

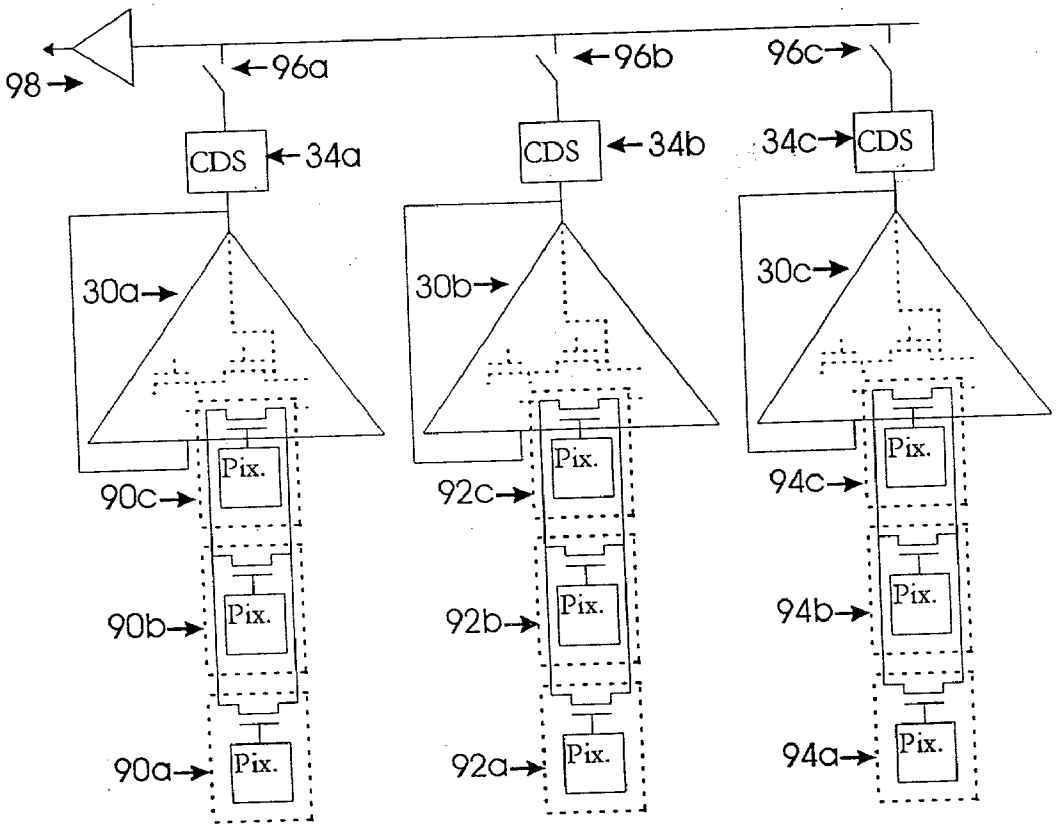

98
96a
96b
96c
CDS
34a
CDS
34b
34c
CDS
30a
30b
30c
Pix.
90c
90b
90a
92c
92b
92a
94c
94b
94a

Figure 4

Independent Readout and Reset

Figure 5

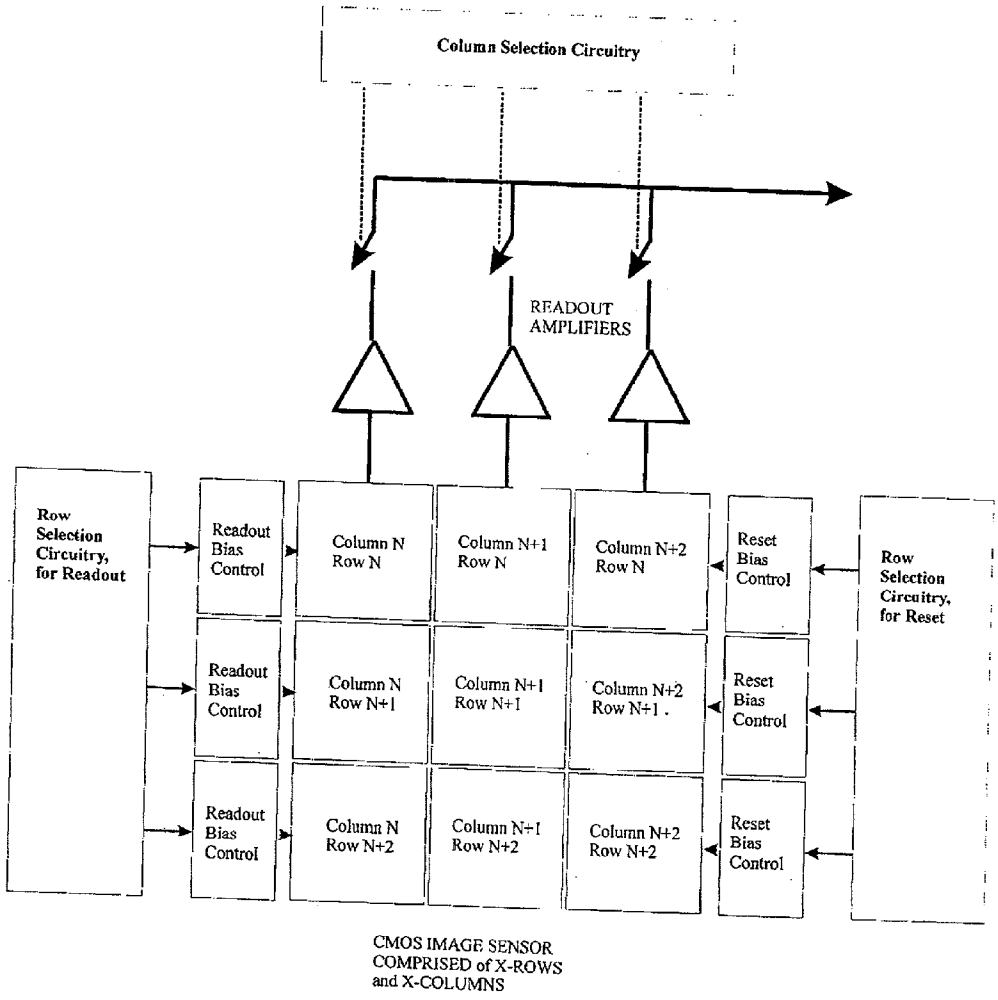
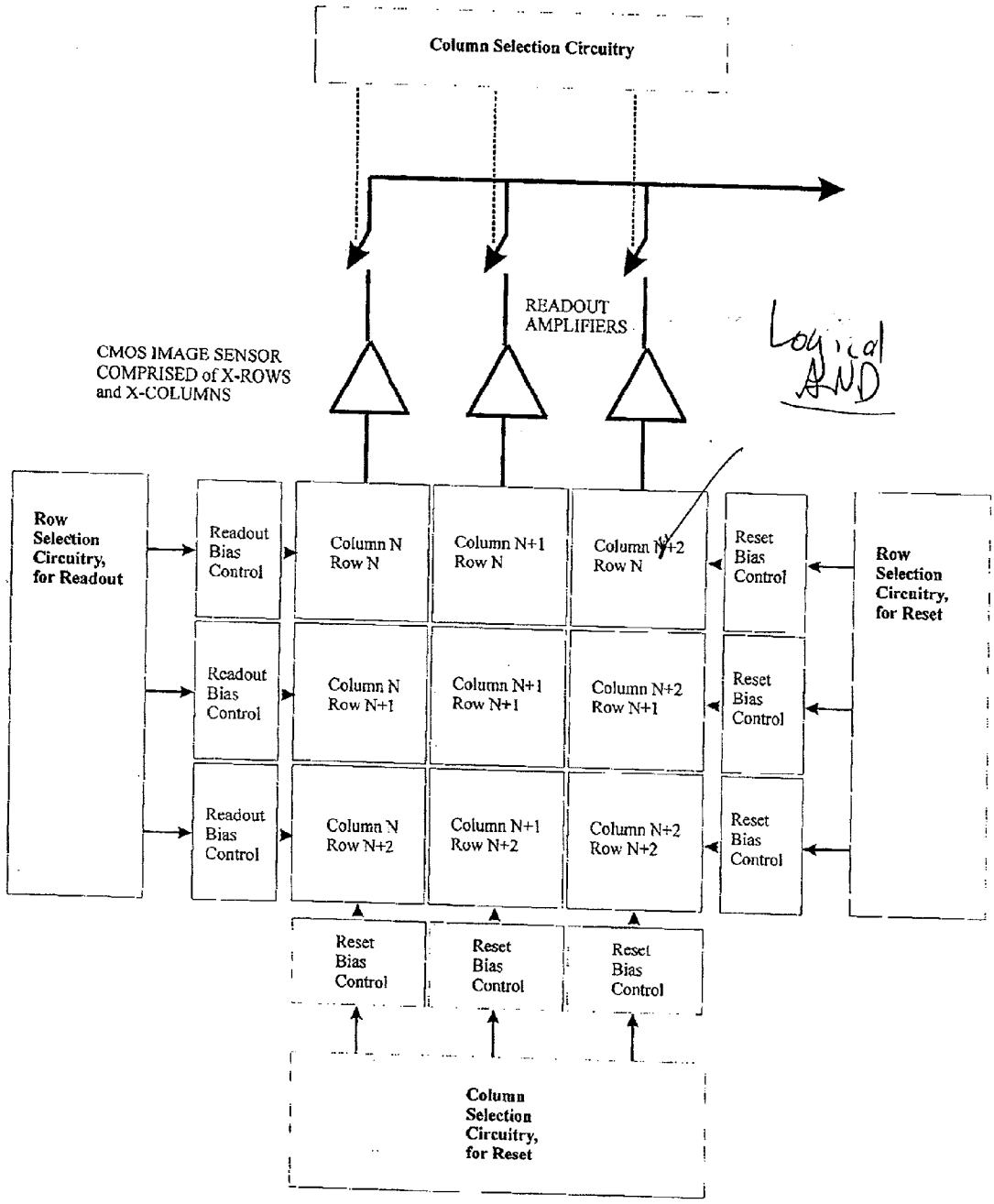


Figure 6

Independent Readout and Reset with Row and Column Selection



Independent Readout and Reset with Row and Column Selection

Figure 7

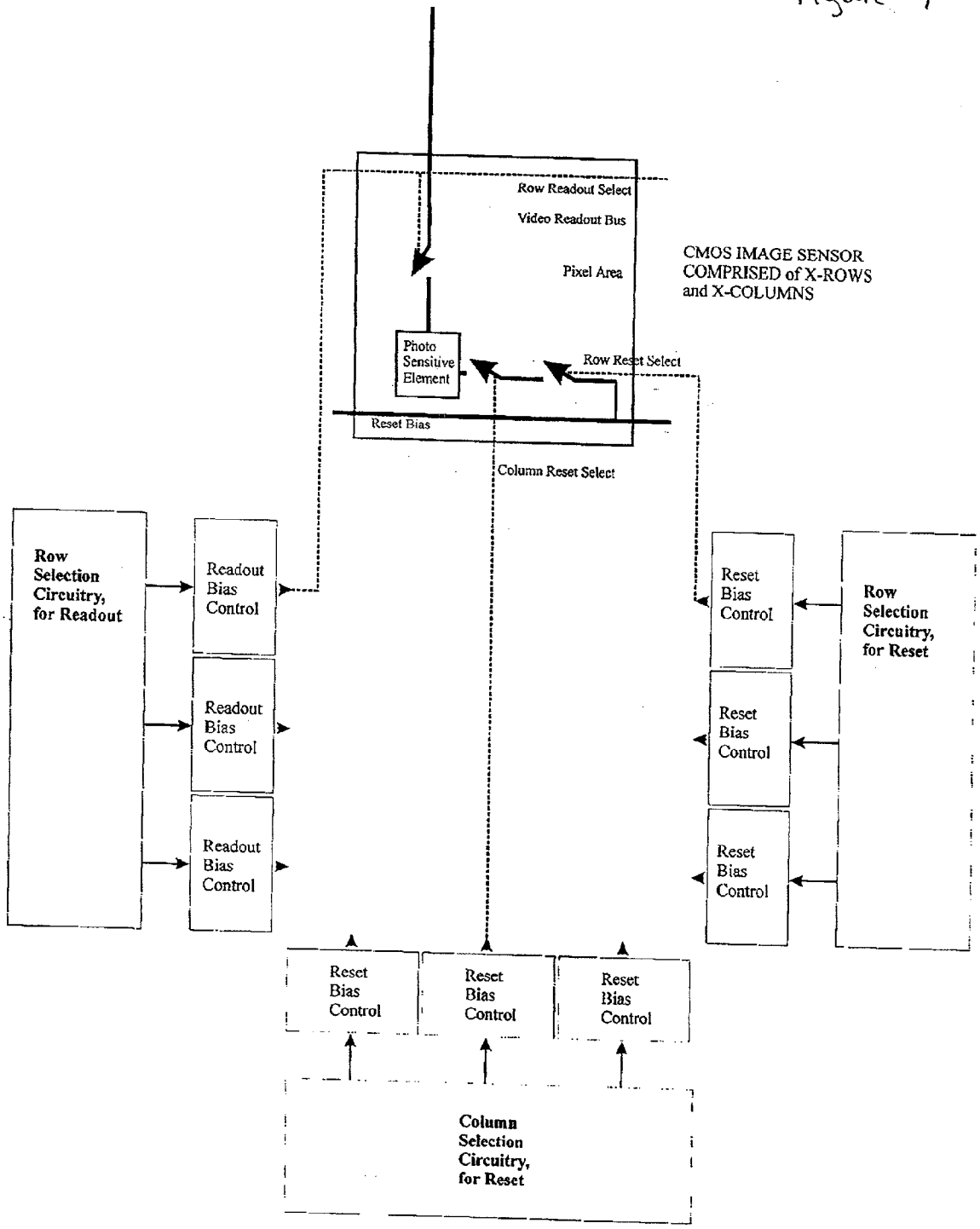
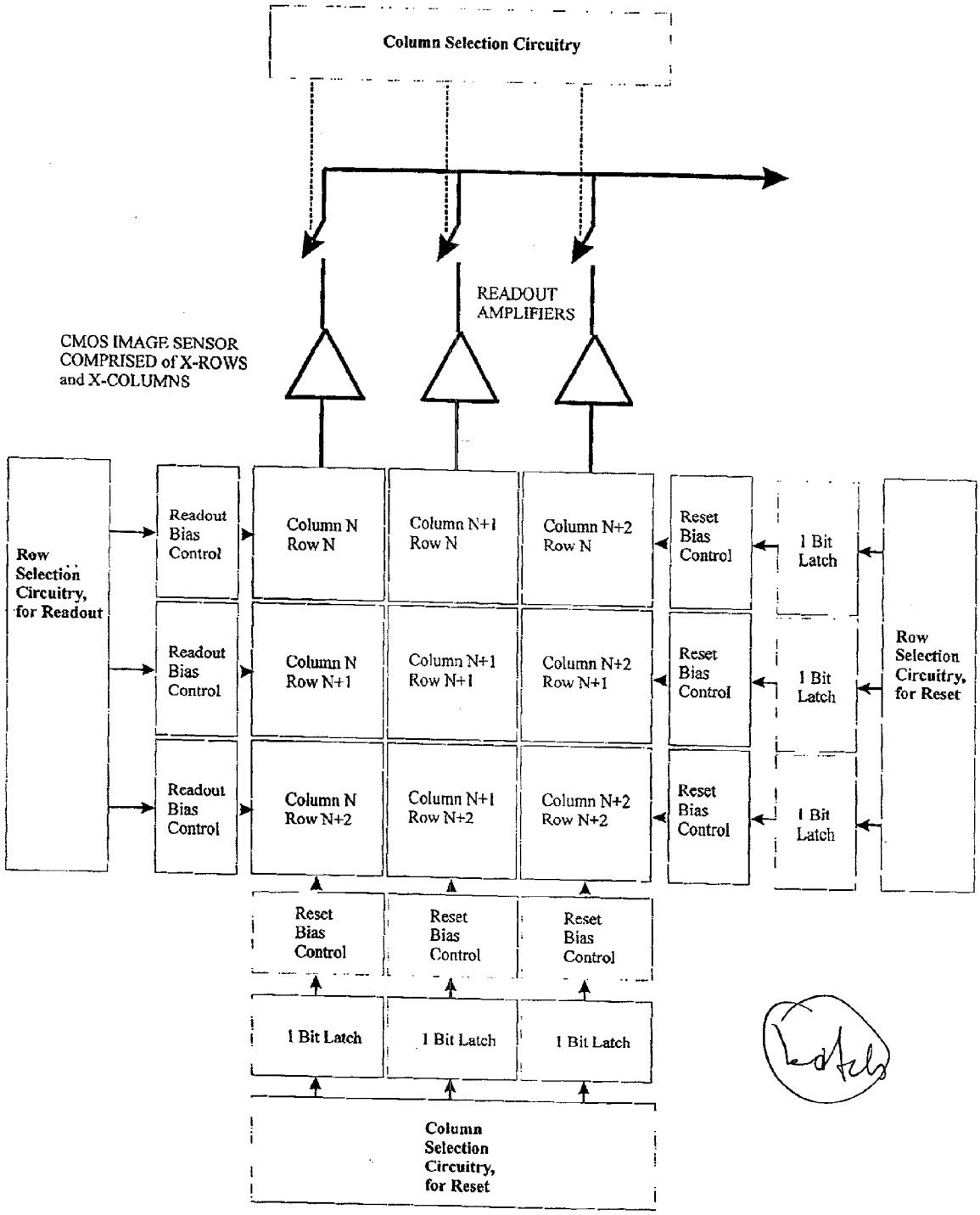


Figure 8

, Independent Readout and Reset with Row and Column Selection and Latch



METHOD AND APPARATUS FOR INDEPENDENT READOUT AND RESET OF PIXELS WITHIN A CMOS IMAGE SENSOR

[0001] This application is a Continuation-in-Part of U.S. patent application Ser. No. 09/039,835 filed on Mar. 16, 1998 naming Matthew A. Pace and Jeffrey J. Zarnowski as inventors.

FIELD OF THE INVENTION

[0002] This invention relates generally to controlling the exposure time for elements of a scene. More specifically, it allows one to control the exposure time of any pixel or group of pixels within a scene, independent of readout time (frame-rate), therefore extending the dynamic range to accommodate a given scene.

BACKGROUND OF THE INVENTION

[0003] Prior to the current invention, it was not possible to have independent control of the readout and reset functions of a CMOS imager pixel. In prior art imagers, selection circuitry was connected to the rows of a pixel array for selecting a row to be readout or reset. That row was then either readout or reset by control circuitry connected to it. The problem with these prior art imagers was that it was not possible to independently select one row for readout and a second row for reset. Only one selection circuit was connected to each row. Once a row was selected, that row could be readout or reset, but no other row could be reset while the first row was being read. After the pixels in the selected row were readout, the pixels within that row were reset, or placed in the exposure state. This mode of operation fixes the exposure time to the readout rate (frame rate).

[0004] In a scene that contained both well-illuminated and poorly illuminated portions, it was necessary to compromise readout time (frame rate) to achieve sufficient signal in the poorly illuminated portions, while attempting not to over expose the portions that were well illuminated.

[0005] Because of the independent row read nature and random address capability inherent to the active column sensor, this invention is possible.

SUMMARY OF THE INVENTION

[0006] This invention allows readout rate (and exposure time) to be optimized to the portion of the scene that is poorly illuminated, achieving good signal level, AND control the exposure time of the portion of the scene that is well illuminated at the same time. This achieves maximization of the intra-scene illumination levels unavailable before now.

[0007] This is accomplished through the addition of a second selection circuit. Now, a row for readout may be selected simultaneously with a row for reset and both readout and reset may occur. The further addition of another selection circuit allows a column of elements to be chosen for additional readout or reset. The additional selection circuit enables one to select individual pixels for readout and reset.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **FIG. 1** is prior art CMOS Imager, with fixed readout and reset control.

[0009] **FIG. 2** is an active column sensor in accordance with this invention;

[0010] **FIG. 3** is an implementation of a pixel in accordance with the invention;

[0011] **FIG. 4** is a schematic illustration of a matrix of pixels connected to incorporate a full operational amplifier per pixel forming an active column sensor.

[0012] **FIG. 5** is the invention that enables independent readout and reset control.

[0013] **FIG. 6** shows additional selection circuitry on the column.

[0014] **FIG. 7** shows typical pixel implementation.

[0015] **FIG. 8** shows that by adding latches, an entire group or sub-array can be addressed simultaneously.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0016] **FIG. 1** illustrates a typical prior art CMOS imager, utilizing a fixed read out and reset control in which a given row is selected, and its pixels are read out. After the pixels in the selected row are readout, the pixels within that row are reset, and then immediately placed in the exposure state. This mode of operation fixes the exposure time to the readout rate (frame rate).

[0017] **FIG. 2** is a schematic diagram of a pixel **12** in accordance with the present invention in which the threshold variations from pixel to pixel of the prior art are eliminated. All pixels **12** in a row or column are read out in parallel and for simplicity only one is shown. Pixel **12**, which can consist of any photosensitive device **10**, is coupled to a FET **15** to isolate the pixel from the readout circuitry. The FET **15** is one FET of a differential input pair of an operational amplifier **30** that includes FET **24**. For simplicity, in **FIG. 2** the amplifier circuit **30** is configured as a positive feedback unity gain amplifier. A feedback path **32** connects the output of amplifier **30** to input **17**, which in this case is the gate of FET **24**. The amplifier **30** can be configured to have gain, a full differential input, or any operational amplifier configuration as the application required. The fixed gain of amplifier **30** eliminates the gain variability of the prior art. The output of the unity gain amplifier is connected to a Correlated Double Sampler (CDS) that is utilized to eliminate any fixed pattern noise in the video.

[0018] A current source **20** comprising a FET **22** has its source connected to a power source VDD and its drain connected to the sources of differential input FETs **15** and **24**.

[0019] The drains of input FETs **15** and **24** are connected to a current mirror formed from FETs **26** and **28**. The gates of FETs **26** and **28** are connected together and to the source **18** of input FET **15**. The sources of FETs **26** and **28** are connected to a negative power source, VCC.

[0020] The source **30** of FET **24** is the output of the differential pair and is connected to CDS **34**.

[0021] The input FET **15** could be either an N channel or P channel FET as the application requires. The pixel #**80** could be either a photogate or a photodiode.

[0022] **FIG. 3** is a detailed schematic of pixel **12** of the active column sensor shown in **FIG. 2**. In this implementation a photogate **76** is utilized. FET **76** controls the selection and reset of sense node #**72**. This active column sensor pixel eliminates the separate selection/access FET **58** of prior art. All biasing and controls signals are supplied from the periphery of the pixel array.

[0023] The pixel can be operated in the following manner. An N type substrate is used and the substrate is biased the most positive potential, e.g. 5.0 volts. The photogate #**70**, preferably a layer of polysilicon, is biased to an integrate level (e.g.. 0.0 volts). The region **80** under the photogate #**70** is depleted and as light strikes the immediate area, it will collect (integrate) photon generated carriers. Photogate **72** is biased to 5.0 volts and will not collect photon-generated carriers during the integration because it is biased to the same potential as the substrate. Selecting FET **76** with the reset/Select Control signal biases Photogate **72**. In this configuration FET **76** is a P channel FET that is selected by a negative signal relative to the substrate, for example 0.0 volts. During integration FET **76** is selected, the photogate is biased by the reset/select bias that preferably is at 5.0 volts. After a predetermined integration time period the pixel is read.

[0024] Reading the pixel is preferably accomplished in the following manner. The reset/select control is changed to 2.5 volts, causing the region beneath photogate #**72** to be depleted, and the background level is read. Setting the reset/select control to 5.0 volts turns off Reset/select FET **76**. Photogate **70** has its potential removed, and in this example 5.00 volts. Reading the signal will occur as the collected photon generated charge transfers from the region beneath photogate **70** to the region beneath photogate **72**. The transferred photon generated charge modulates the gate of input FET **15**, according to the amount of collected.

[0025] Fixed Pattern Noise (FPN) can be eliminated from the video information by utilizing CDS circuit **34**. The first sample applied to the CDS circuit is the background level. The signal information is then applied to the CDS. The difference of the two signals provides for a fixed pattern noise free signal.

[0026] **FIG. 4** is a schematic diagram of an array of pixels in accordance with this invention. A plurality of pixels **90***a*, **90***b*, and **90***c*, form a first column of the array, and similar columns **92***a-c* and **94***a-c* complete the array. Within each column, the pixels are connected with their output FETs in parallel, the combination forming the first one of the differential input pair of operational amplifier **30**. In all other respects, amplifiers **30***a*, **30***b* and **30***c* are identical to **FIG. 2**. Each amplifier **30** is connected to CDS **34***a*, **34***b*, and **34***c* respectively. The outputs of CDS **34***a, b, c* are connected through column select switches **96***a*, **96***b*, and **96***c*, the common terminals of which are connected to output buffer **98** which can be a source follower, or a more complex signal conditioner as required by the specific application.

[0027] **FIG. 5** illustrates a further embodiment of the claimed invention. In this embodiment the reset portion of the circuitry is separated from the readout circuitry. It is joined with its own independent row selection method. This allows any given row to be reset and placed into the exposure state while any other row is being readout. The readout and reset functions can now be performed independently.

[0028] **FIG. 6** illustrates a further improvement for the invention. In this embodiment, selection circuitry is placed along both the columns and the rows. A type of logic gate commonly known as an "AND" gate is located within the pixel. The AND gate is simply two switches connected in series within the pixel. One switch is connected to and triggered by the row selection circuitry, and the other switch is connected to and triggered by the column selection circuitry. Only when both switches are triggered can the pixel be reset or readout. This configuration enables one to readout or reset any given pixel independently.

[0029] **FIG. 8** demonstrates that by adding additional circuitry to latch the selected addresses, a group or "sub-array" can be reset and put into the exposure state simultaneously, causing all the pixels comprising that sub-array to have the identical exposure time.

[0030] While the invention has been described in connection with preferred embodiments, it is not intended to limit the scope of the invention to the particular forms set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

What is claimed:

1. An imager comprising:

(a) a plurality of photosensitive elements, each element having a readout selection switch connected to a readout terminal, and a first reset selection switch connected to a reset terminal, separate from the readout terminal;

(b) an addressable selection circuit connected to the reset terminal;

(c) a separately addressable readout circuit connected to the readout terminal, so that a first photosensitive element can be selected for readout and a second photosensitive element can be selected for reset simultaneously.

2. The imager of claim 1, further comprising a second reset selection switch in series circuit relationship with the first reset selection switch, and a second, separately addressable circuit connected to the second reset switch.

3. The imager of claim 1, further comprising a second readout selection switch in series circuit relationship with the first readout selection switch, and a second, separately addressable circuit connected to the second readout switch.

4. The imager of claim 1, further comprising a latch circuit for storing address information.

5. The imager of claim 1, further comprising a plurality of unitary, differential-input, amplifiers, each amplifier having a plurality of first input transistors, one first input transistor located at each element within the periphery.

6. The imager of claim 5, where the plurality of photosensitive elements are located within a periphery.

7. The imager of claim 6, where each amplifier further comprises a second input transistor located outside the periphery of the array and connected to the first input transistors so as to create a feedback loop.

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