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(54) Title: CRYSTALLINE-THIN-FILM PHOTOVOLTAIC STRUCTURES AND METHODS FOR FORMING THE SAME

(57) Abstract: Methods for forming semiconductor devices include providing a textured template, forming a buffer layer over the textured template, forming a substrate layer over the buffer layer, removing the textured template, thereby exposing a surface of the buffer layer, and forming a semiconductor layer over the exposed surface of the buffer layer. In various embodiments, semiconductor structures include a substantially untextured substrate layer, a textured buffer layer disposed over the substrate layer, and a semiconductor layer disposed over the textured buffer layer.

CRYSTALLINE THIN-FILM PHOTOVOLTAIC STRUCTURES AND METHODS FOR FORMING THE SAME

Cross-Reference to Related Application

[0001] This application claims priority to and the benefit of, and incorporates herein by reference in its entirety, U.S. Provisional Patent Application No. 60/984,796, which was filed on November 2, 2007.

Technical Field

[0002] In various embodiments, the present invention relates to photovoltaic structures and devices, and in particular to thin-film photovoltaics.

Background

[0003] Both the alternative-energy and flat-panel display markets have a need for high-quality, flexible substrates on which to produce highly crystalline semiconductor thin films.

[0004] The current solar cell (i.e., photovoltaic) market relies on technology that has been essentially unchanged for decades. Over 90% of the market is served by crystalline silicon (Si), either single-crystal or polycrystalline, with average conversion efficiencies of 12 – 20%. The costs of crystalline Si devices are high due to high-cost production methods and high demand for the raw materials in competition with the semiconductor electronics industry. Si devices must also be quite thick to achieve these efficiencies, consuming significant quantities of material. The remaining 10% of the market is served largely by thin-film structures based on amorphous Si, CdTe, or copper-indium-gallium-selenide ("CIGS") that are cheaper to produce but have energy conversion efficiencies below 10%. Amorphous Si efficiencies also degrade with time.

[0005] Higher conversion efficiencies, over 30%, have been demonstrated for thin film multi-junction devices based on III-V semiconductors such as GaAs. However, their production costs are very high since these devices are most advantageously grown on single-crystal germanium (Ge) or GaAs wafers costing over $10,000 per square meter.

[0006] Emerging low-cost photovoltaic technologies include ribbon-grown Si, polymeric/organic films, and nanotechnology-based approaches. None of these new solutions fully addresses the market needs for increased production volume, increased efficiency, and lower cost per watt generated.

[0007] A useful substrate for the growth of high efficiency semiconductor films (e.g., III-V semiconductor films) preferably enables the growth of low-defect films (similar to those formed on single-crystal wafers) but at much lower cost and with higher area. Flexibility is a useful attribute. The substrate is also preferably chemically compatible with both the semiconductor material and with the semiconductor process environment. These demanding attributes restrict the number of materials that may effectively be used for this application.

[0008] The ability to produce polycrystalline metals with crystallographic orientation (e.g., "biaxial texture") approaching single-crystal quality in pure metals has been known since the 1940's. Practical applications of such texture control have included the production of aluminum sheet with textures that enhance the production of cans. Most commercial uses of sheet materials avoid texture, however, because the properties of sheet materials are more isotropic in its absence.

[0009] Face-centered cubic (fcc) metals, some body-centered cubic (bcc) metals, and some alloys based on fcc metals may be useful as substrate materials, as they may be biaxially textured using well-known rolling-deformation and annealing processes. A well-known texture in fcc metals and alloys is the "cube texture," in which the c-axis of each of the substrate grains is substantially perpendicular to the substrate surface, and the a-axes align primarily along a length direction. Under controlled rolling and annealing processes, these deformation-textured metals may possess biaxial texture approaching that of single crystals.

[0010] Nickel (Ni) is one fcc metal that may be made into thin foils with a well-defined cube texture using a rolling and annealing process. Prior work has shown that oxide intermediate layers may be deposited on a biaxially textured Ni surface using conditions under which nickel oxide is not stable, but where the intermediate layer (for example, CeO_2 or Y_2O_3) is stable, allowing the oxide to inherit the texture of the underlying Ni foil, i.e., form epitaxially thereon. The high-purity Ni required to achieve good biaxial texture is expensive and Ni is mechanically weak following the typical annealing heat treatment used to form the cube texture.

[0011] For these reasons, Ni alloys and other alloys have been developed to make stronger, non-magnetic biaxially textured foils. These alloys often contain alloying elements such as tungsten (W), molybdenum (Mo), vanadium (V), or chromium (Cr) in small controlled amounts. Relatively pure copper (Cu) may also be processed to produce a high-quality cube texture. Commercial grades of Cu with relatively low oxygen content and relatively low content of substitutional and interstitial elements have been of particular utility. In addition, prior work has shown that a wide range of Ni-Cu alloys may also be processed to produce high-quality cube textures.

[0012] Epitaxial films of other materials such as metals, oxides and nitrides can be grown on the biaxially textured foil. As used herein, "epitaxial" means that the crystallographic orientation of the deposited film is derived from and directly related to the crystallographic orientation of the underlying template.

[0013] Unfortunately, the existing deformation-textured foil approach is frequently not commercially viable for the deposition of semiconducting films necessary for high-performance optical and photovoltaic devices, e.g., Si, Ge, GaAs, InP, and related alloys and compounds. One promising approach utilizing Cu or Cu-Ni alloy textured foils is described in U.S. Patent Application Publication No. 2007/0044832A1, the entire disclosure of which is incorporated by reference herein. However, such foils may be incompatible with conventional semiconductor processes. Both Cu and Ni form arsenide and silicide phases when exposed to As- or Si-containing gases at typical processing temperatures above approximately 350 °C. The formation of these phases causes a significant increase in volume, embrittles the foils, and renders the foils largely unusable for subsequent processing and for most applications.

[0014] Thus, while considerable progress has been made in the use of biaxially textured foils for superconductor applications, there is a need for processes and structures for non-superconductor materials and applications such as optical devices, optoelectronic devices, and photovoltaics.

Summary

[0015] The foregoing limitations of conventional thin-film photovoltaic platforms and fabrication processes are herein addressed by removing a highly textured template layer after a buffer layer has "inherited" a texture therefrom but before the formation of semiconductor layers. The template layer is thereby utilized to create a texture suitable for the subsequent fabrication of high-quality semiconductor materials and devices, but is removed before exposure to processes tending to embrittle the template layer.

[0016] In one aspect, embodiments of the invention feature a method for forming a semiconductor device. The method includes providing a textured template, forming a buffer layer over the textured template, forming a substrate layer over the buffer layer, removing the textured template (thereby exposing a surface of the buffer layer), and forming a semiconductor layer over the exposed surface of the buffer layer. During formation of the buffer layer, the buffer layer may inherit the texture of the textured template (such that the texture is revealed on the exposed surface). A sacrificial layer, which may include or consist essentially of Pd, may be formed over the textured template prior to forming the buffer layer. During formation of the sacrificial layer, the sacrificial layer may inherit the texture of the textured template. The sacrificial layer may be removed during removal of the textured template.

[0017] The method may include forming an insulator layer over the buffer layer prior to forming the substrate layer. The insulator layer may include or consist essentially of an oxide, and/or may be amorphous. A diffusion barrier, which may be substantially free of the texture of the textured template, may be formed over the buffer layer prior to forming the substrate layer. The diffusion barrier may include or consist essentially of a metal or metal alloy such as W or Re, and/or may include or consist essentially of an oxide or a nitride. The diffusion barrier may include or consist essentially of W.

[0018] The substrate layer may include or consist essentially of at least one of W, Mo, a metal alloy, a ceramic, or a glass. The substrate layer may include or consist essentially of a material substantially impervious to the formation of As-containing phases and/or Si-containing phases at a temperature greater than approximately 350 °C. The substrate layer may be substantially free of the texture of the textured template. The semiconductor layer may include or consist essentially of at least one of Si, Ge, or InGaAs. The coefficient of thermal

expansion of the substrate layer may substantially match the coefficient of thermal expansion of the semiconductor layer. The buffer layer may include or consist essentially of at least one of Cr, an oxide, or a nitride. The textured template may include or consist essentially of at least one of Cu, Ni, or a Cu-Ni alloy.

[0019] The semiconductor layer may include or consist essentially of at least one of a p-n junction or a p-i-n junction, and a semiconductor device may be formed on the semiconductor layer. The semiconductor device may include or consist essentially of at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, InGaAs, or alloys or mixtures thereof. The semiconductor device may include at least one of a photovoltaic cell, a light-emitting diode, or a laser. The substrate layer may function as a back contact for the semiconductor device.

[0020] In another aspect, embodiments of the invention feature a semiconductor structure including a substantially untextured substrate layer, a textured buffer layer disposed over the substrate layer, and a semiconductor layer disposed over the textured buffer layer. The grain size of the textured buffer layer and/or the semiconductor layer may be greater than approximately 25 μm. The textured buffer layer may include or consist essentially of a metal or a metal alloy, e.g., Cr. The textured buffer layer may include or consist essentially of at least one of an oxide or a nitride.

[0021] The structure may include a diffusion barrier disposed between the substrate layer and the textured buffer layer. The diffusion barrier may include or consist essentially of a metal or a metal alloy, e.g., at least one of W or Re. The diffusion barrier may include or consist essentially of at least one of an oxide or a nitride.

[0022] The structure may include an insulator layer disposed between the substrate layer and the textured buffer layer. The insulator layer may include or consist essentially of an oxide, and may be amorphous. The substrate layer may include or consist essentially of at least one of W, Mo, a metal alloy, a ceramic, or a glass. The coefficient of thermal expansion of the substrate layer may substantially match the coefficient of thermal expansion of the semiconductor layer.

[0023] The structure may include a semiconductor device disposed over the semiconductor layer. The semiconductor device may include or consist essentially of at least one of a photovoltaic cell, a light-emitting diode, or a laser. The semiconductor device may include or

consist essentially of at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, InGaAs, or alloys or mixtures thereof.

[0024] In yet another aspect, embodiments of the invention feature a semiconductor device including a substantially untextured flexible substrate layer and a plurality of textured semiconductor junctions disposed over the substrate layer. The device may include a textured buffer layer and/or an insulator layer disposed between the substrate layer and the plurality of semiconductor junctions. The plurality of semiconductor junctions may form a photovoltaic cell having an energy conversion efficiency greater than approximately 15%, or even greater than approximately 20%. The grain size of each of the semiconductor junctions may be larger than approximately 25 μm.

[0025] In another aspect, embodiments of the invention feature a structure including a textured template that itself includes or consists essentially of a first metal (or metal alloy); a buffer layer, disposed over the textured template, that includes or consists essentially of a second metal (or metal alloy) different from the first metal (or metal alloy); and a substantially untextured substrate layer, disposed over the buffer layer, that includes or consists essentially of at least one of a ceramic, a glass, or a third metal (or metal alloy) different from both the first and second metals (or metal alloys). The texture of the buffer layer may substantially match the texture of the textured template. The substrate layer may include or consist essentially of a material substantially impervious to formation of As-containing phases and/or Si-containing phases at a temperature greater than approximately 350 °C. The textured template may include or consist essentially of a material that forms As-containing phases and/or Si-containing phases at a temperature greater than approximately 350 °C.

[0026] The structure may include a substantially untextured diffusion barrier disposed between the buffer layer and the substrate layer. The diffusion layer may include or consist essentially of at least one of an oxide, a nitride, or a fourth metal (or metal alloy) different from the first, second, and third metals (or metal alloys). The structure may include a textured sacrificial layer including or consisting essentially of a fifth metal (or metal alloy) different from the first, second, third, and fourth metals (or metal alloys), e.g., Pd, disposed between the textured template and the buffer layer.

[0027] These and other objects, along with advantages and features of the present invention herein disclosed, will become more apparent through reference to the following description, the accompanying drawings, and the claims. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and may exist in various combinations and permutations.

Brief Description of the Drawings

[0028] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

Fig. 1A is a schematic cross-sectional diagram of an exemplary structure formed on a textured template in accordance with various embodiments of the invention;

Fig. 1B is a schematic diagram of the structure of Fig. 1A after removal of the textured template; and

Figs. 2-4 are schematic diagrams of the structure of Fig. 1B after further deposition and processing in accordance with various embodiments of the invention.

Detailed Description

[0029] Templates suitable for use in embodiments of the present invention include crystallographically oriented material layers that are chemically compatible and are lattice-matched with known and anticipated semiconductor materials, in particular with compound semiconductors (e.g., III-V semiconductor materials). "Lattice-matched," as used herein, refers to layers or materials having relative lattice spacings that allow the epitaxial growth of one layer (e.g., a buffer) on the other (e.g., a template) with a controlled texture and an acceptable level of defects to enable the subsequent integration of high-quality semiconductor materials and/or high-efficiency semiconductor devices. For metallic films, lattice-matching may be within an approximately 10% relative difference in lattice spacing, preferably within approximately 5%, and more preferably within approximately 2%. The lattice spacing may refer to the material's unit-cell lattice constant as it is commonly defined in the art, or to another interatomic spacing that can be defined in reference to the lattice constant. For

instance, the lattice constant of a material may be lattice-matched to the lattice spacing defined by the diagonal of a face of a cubic crystal (which is approximately equal to 1.414 times the lattice constant). Furthermore, a material having a lattice constant (or other lattice spacing) that is approximately an integral multiple (again, within approximately 10%, approximately 5%, or approximately 2%) of that of another material may also be considered to be "lattice matched." For example, a material having a lattice spacing approximately twice that of a second material will achieve approximate lattice registry with every other atom of the second material. The necessary degree of matching may depend on the type of material under consideration. For example, a high-quality semiconductor layer may require closer lattice-matching to an underlying layer than a metal layer deposited on another metal layer. Non-limiting examples of lattice-matching include Cr and palladium (Pd), which are matched to within approximately 8%, as well as the cube-face diagonal of Cr and one-half the cube-face diagonal of Ge, which are matched to within approximately 3%.

[0030] "Chemically compatible," as used herein, means that a material is not reactive with a semiconductor process environment and preferably is not reactive with and does not react with (at least at the processing temperatures contemplated herein) or contaminate a semiconductor material integrated thereon. Further, even if a reaction does occur, a chemically compatible material should not react with a semiconductor to the extent that it degrades the quality or performance of the semiconductor. As one non-limiting example of chemical compatibility, Ge and Cr may react to form a GeCr compound, but this compound is stable and does not affect the performance of either the Ge or other semiconductors formed atop the Ge.

[0031] As used herein, "texture" refers to a defined crystallographic orientation that extends throughout the thickness of a layer of material, as opposed to mere topology of a surface that does not extend through an entire thickness. As used herein, "biaxial" refers to crystal grains in the substrate or film in close alignment with both a direction perpendicular to the surface of the film and a direction in the plane of the film. Biaxial texturing allows for the production of a low volume of point and line defects in a semiconducting film, and minimizes the carrier-trapping effects of high-angle grain boundaries. This enables very high current densities in these films at typical device operating conditions. "Untextured," as utilized herein refers to materials that lack texture (as defined above), e.g., materials having randomly oriented crystal grains or that are amorphous.

[0032] Referring to Fig. 1A, a textured template 100 is provided by, e.g., deformation rolling and annealing processes known in the art. Textured template 100 may be in the form of a thin foil, and may have a thickness between approximately 10 micrometers (μm) and approximately 100 μm, e.g., approximately 25 μm. A surface of textured template 100 may be polished, e.g., to mirror smoothness. Textured template 100 may include or consist essentially of a metal or a metal alloy, e.g., Cu, Ni, a Cu alloy, and/or a Ni alloy. Textured template 100 has a defined texture, e.g., a biaxial texture such as a cube texture. Preferably the textured template 100 will exhibit, upon measurement by x-ray diffraction pole figure analysis, a full-width-half-maximum (FWHM) texture spread less than approximately 10 degrees, and preferably less than approximately 5 degrees. In some embodiments, textured template 100 has a grain size greater than approximately 25 μm, preferably greater than approximately 50 μm, and even more preferably greater than approximately 100 μm. Textured template 100 may not be chemically compatible with semiconductor materials such as Ge, Si, and III-V semiconductors at typical processing temperatures above approximately 350 °C. In certain embodiments, textured template 100 includes or consists essentially of a material that forms As-containing phases and/or Si-containing phases at temperatures greater than approximately 350 °C upon exposure to precursors or other materials containing As and/or Si.

[0033] Optionally, a sacrificial layer 110 is formed over textured template 100. Sacrificial layer 110 may include or consist essentially of a metal or a metal alloy, e.g., Pd, platinum (Pt), aluminum (Al), or silver (Ag), or may include or consist essentially of an element or compound enabling improved lattice matching between textured template 100 and buffer layer 120 (described below), e.g., a material having a lattice spacing therebetween. Sacrificial layer 110 may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, metallorganic deposition, or by electrochemical means such as electroplating (with or without electrodes). During formation, sacrificial layer 110 "inherits" the texture of textured template 100, i.e., forms with such atomic registry as to replicate the texture through its thickness. The "inheritance" of an underlying texture may provide superior texture through a thickness of a layer when compared to, e.g., a layer formed via ion-beam assisted deposition on a substantially untextured substrate (while small-range texturing and small grains (i.e., less than 1 μm in size) may develop in such layers, they will generally lack consistent texturing through their entire thicknesses). Formation of sacrificial layer 110 may be performed without ion-beam assistance. During

subsequent processing of textured template 100, sacrificial layer 110 may substantially react with or diffuse into textured template 100. Sacrificial layer may have a thickness of, e.g., less than approximately 200 nm, e.g., less than approximately 100 nm, or even less than approximately 50 nm.

[0034] A buffer layer 120 is formed over textured template 100 and optional sacrificial layer 110. Buffer layer 120 may include or consist essentially of a metal or a metal alloy, e.g., Cr, or may include or consist essentially of a nitride or an oxide. Such an oxide may be a compound consisting essentially of oxygen and at least one non-metallic element, e.g., Si. Buffer layer 120 may have a thickness of, e.g., between approximately 100 nm and approximately 500 nm, e.g., approximately 200 nm. Buffer layer 120 may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, metallorganic deposition, or by electrochemical means such as electroplating (with or without electrodes). During formation, buffer layer 120 inherits the texture of textured template 100. Buffer layer 120 may be provided without ion-beam assistance. In some embodiments, multiple buffer layers 120 may be formed over textured template 100.

[0035] An optional diffusion barrier 130 is formed over buffer layer 120. Diffusion barrier 130 may be formed substantially non-epitaxially and thus be substantially lacking the texture of buffer layer 120 and textured template 100. Diffusion barrier 130 may include or consist essentially of a metal or a metal alloy, e.g., W or rhenium (Re), or may include or consist essentially of a nitride or an oxide, e.g., a compound consisting essentially of oxygen and at least one non-metallic element such as Si. Diffusion barrier 130 prevents substantially all interdiffusion or reaction between substrate layer 140 and semiconductor materials and devices formed over buffer layer 120 (as further described below).

[0036] In addition to or instead of diffusion barrier 130, an insulator layer (not shown), e.g., a dielectric or other electrical insulator, may be formed over buffer layer 120. The insulator layer may be amorphous, and may include or consist essentially of an oxide, e.g., a compound consisting essentially of oxygen and at least one non-metallic element such as Si. In an embodiment, the insulator layer may include or consist essentially of a nitride or aluminum oxide. The insulator layer may be formed by deposition, e.g., evaporation, sputtering, chemical vapor deposition, atomic layer deposition, or molecular beam epitaxy, and

may be formed without ion-beam assistance. The insulator layer may provide electrical insulation between substrate layer 140 and subsequently formed semiconductor materials and devices (as further described below).

[0037] A substrate layer 140 is formed over buffer layer 120 and optional diffusion barrier 130 (and/or the insulator layer, if present). Substrate layer 140 provides structural support to semiconductor materials and devices formed over buffer layer 120 after removal of textured template 100 (as further described below), and is preferably chemically compatible with semiconductor materials such as Ge, Si, and III-V semiconductors at typical processing temperatures above approximately 350 °C. In a preferred embodiment, substrate layer 140 includes or consists essentially of a material substantially impervious to formation of As-containing phases and/or Si-containing phases at temperatures greater than approximately 350 °C. Substrate layer 140 may be formed substantially non-epitaxially and thus be substantially lacking the texture of buffer layer 120 and textured template 100. Therefore, substrate layer 140 may be formed by any method known in the art, e.g., vacuum deposition, chemical vapor deposition, heat lamination, electrodeposition, slurry coating, metallorganic deposition, or lamination. In the case of lamination, the laminating agent such as, for example, a braze alloy or adhesive, should also be chemically compatible and thermally stable with any subsequent semiconductor processes. In an embodiment, substrate layer 140 is formed by electron-beam evaporation at a temperature greater than approximately 900 °C. Substrate layer 140 may include or consist essentially of a composite, a ceramic (e.g., alumina and/or zirconia), a glass, a metal alloy, or a metal, e.g., W, Mo, and/or Al. In an embodiment, substrate layer 140 includes or consists essentially of a metal coated with a thicker ceramic material for additional structural support. In various embodiments, substrate layer 140 is flexible and thus capable of being manipulated into non-planar configurations. Substrate layer 140 may be substantially electrically conductive, enabling it to function as a contact, e.g., a back contact, for a subsequently formed semiconductor device. Substrate layer 140 may have a thickness of, e.g., between approximately 1 μm and approximately 0.5 mm.

[0038] Referring to Fig. 1B, textured template 100 (and optional sacrificial layer 110, if present) is removed, exposing surface 150 of buffer layer 120. Textured template 100 may be removed by a selective process and/or with end-point monitoring. As utilized herein, a selective process will remove substantially all of textured template 100 without adversely

affecting surface 150, thereby rendering surface 150 suitable for the subsequent formation of semiconductor materials and/or devices thereon. Suitable selective processes may include, e.g., chemical etching (with, e.g., an acid such as nitric acid), electrochemical etching, plasma etching, ion-beam bombardment, laser ablation, melting, and reverse-bias sputtering. Suitable end-point monitoring methods may include, e.g., surface reflectance, residual-gas analysis, optical-absorption spectroscopy, and other methods known in the art to be capable of detecting the substantially complete removal of textured template 100. Optionally, the exposed surfaces of substrate layer 140 may be protected from damage or removal by a protective layer (not shown) during removal of textured template 100. The texture of buffer layer 120 (inherited from textured template 100), and thus, surface 150, remains substantially unchanged after removal of textured template 100.

[0039] Referring to Fig. 2, at least one semiconductor layer 200 is formed over surface 150 of buffer layer 120. Buffer layer 120 and semiconductor layer 200 are preferably lattice-matched and chemically compatible. Semiconductor layer 200 may include or consist essentially of at least one group IV element or compound (e.g., Si, Ge, or SiGe), or a III-V compound (e.g., a compound including a combination of Al, Ga, In, As, P, and/or N), and may be doped (i.e., include n-type and/or p-type dopants). In a preferred embodiment, semiconductor layer 200 includes or consists essentially of at least one of Si, Ge, or InGaAs. Semiconductor layer 200 may inherit the texture of buffer layer 120 and may be substantially crystallographically oriented; the orientation may be, e.g., (100), (110), or (111). Semiconductor layer 200 may be formed by deposition, e.g., chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, liquid phase epitaxy, or physical vapor deposition, at a deposition temperature between approximately 25 °C and approximately 700 °C. The thickness of semiconductor layer 200 may be between approximately 100 nm and approximately 5 μm, e.g., approximately 2 μm. In an embodiment, semiconductor layer 200 is doped to form a p-n junction and/or a p-i-n junction therein. Such a junction may function as part of a subsequently fabricated semiconductor device (as described further below). Semiconductor layer 200 may include or consist essentially of at least one homojunction or of at least one heterojunction (incorporating multiple semiconductor materials, e.g., forming a quantum well of one material "sandwiched" between layers of another material).

[0040] In a preferred embodiment, coefficients of thermal expansion of semiconductor layer 200 (and/or subsequently formed semiconductor materials and devices) and substrate layer 140 are substantially matched, thus enabling the fabrication of semiconductor materials and devices substantially free of deleterious residual stresses and/or cracks. According to various embodiments of the invention, substantially matched coefficients of thermal expansion have a relative difference of less than approximately 20%, preferably less than approximately 10-15%, and even more preferably less than approximately 5%. For example, a coefficient of thermal expansion of Mo is approximately 4.8×10^{-6} /°C, matched to within approximately 15% of that of Ge or GaAs (approximately 5.7×10^{-6} /°C).

[0041] Referring to Fig. 3, in various embodiments of the invention, a semiconductor device 300 is formed over semiconductor layer 200. Semiconductor device 300 may include or consist essentially of a photovoltaic cell (see also, e.g., Fig. 4), a light-emitting diode, a laser, or a display. Semiconductor device 300 may include or consist essentially of a III-V compound (e.g., a compound including a combination of Al, Ga, In, As, P, and/or N), and may be doped (i.e., include n-type and/or p-type dopants). In an embodiment, semiconductor device 300 includes or consists essentially of at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, or InGaAs. Semiconductor device 300 may be doped to form at least one p-n junction and/or p-i-n junction. In Fig. 3, boundary 310 represents the approximate boundary between p- and n-type doped regions in a p-n junction or the intrinsic region in a p-i-n junction. Semiconductor device 300 may be lattice-matched to semiconductor layer 200, and may have a texture substantially equal to that of semiconductor layer 200. Semiconductor device 300 may include or consist essentially of at least one homojunction or of at least one heterojunction.

[0042] Fig. 4 illustrates a multijunction photovoltaic cell 400 formed over semiconductor layer 200. Cell 400 includes a plurality of p-n or p-i-n junctions; three such junctions 410, 420, 430 are depicted in Fig. 4. Each of the junctions may have a different bandgap; thus, each junction may absorb light of a different wavelength, increasing the overall efficiency of cell 400. The intrinsic layer in a p-i-n junction may decrease dark current of cell 400 (or a junction therein) by substantially preventing the formation of current leakage paths from the p-type doped layer to the n-type doped layer (or vice versa) along grain boundaries in one or more of the layers. One or more of the semiconductor materials in cell 400 may be substantially

lattice-matched to semiconductor layer 200, and semiconductor layer 200 may include a p-n or p-i-n junction (and thus form an active portion of the device, as mentioned above). A top contact 440, which may include or consist essentially of, e.g., a metal or a transparent conductor (such as indium tin oxide), may be formed to enable electrical contact to cell 400. Substrate layer 140 may function as a back contact to cell 400. In structures containing an optional insulator layer over substrate layer 140, the insulator layer may provide isolation between multiple semiconductor devices 300 and/or cells 400 formed over a common substrate layer 140. Cell 400 (and/or other semiconductor devices 300) may exhibit energy conversion efficiencies greater than approximately 15%, greater than approximately 20%, or even greater than approximately 30% under one-sun terrestrial illumination conditions. The devices may exhibit greater than 80% of the energy conversion efficiencies of substantially similar devices fabricated over single-crystal semiconductor substrates.

[0043] The layer and/or device fabrication processes described herein may be practiced in a conventional batch or single-wafer process or by a roll-to-roll continuous or stepwise manufacturing method. The resulting devices may have surface areas greater than approximately 115 cm^2. Roll-to-roll processes may take place in a continuous system in which each step of the process is performed, or in a series of systems, each of which performing one or more of the steps in the process. A roll-to-roll process (or processes) may include or consist essentially of deposition of sacrificial layer 110, buffer layer 120, diffusion layer 130, and one or more semiconductor layers 200. A roll-to-roll process may also include the removal of textured template 100. Moreover, devices and materials utilized in accordance with embodiments of the present invention may be substantially non-superconducting.

[0044] The terms and expressions employed herein are used as terms and expressions of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described or portions thereof. In addition, having described certain embodiments of the invention, it will be apparent to those of ordinary skill in the art that other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. Accordingly, the described embodiments are to be considered in all respects as only illustrative and not restrictive.

[0045] What is claimed is:

1. A method for forming a semiconductor device, the method comprising:
providing a textured template;
forming a buffer layer over the textured template;
forming a substrate layer over the buffer layer;
removing the textured template, thereby exposing a surface of the buffer layer; and
forming a semiconductor layer over the exposed surface of the buffer layer.

2. The method of claim 1, wherein, during formation of the buffer layer, the buffer layer inherits the texture of the textured template.

3. The method of claim 2, wherein the texture appears on the exposed surface of the buffer layer.

4. The method of claim 1, further comprising forming a sacrificial layer over the textured template prior to forming the buffer layer.

5. The method of claim 4, wherein, during formation of the sacrificial layer, the sacrificial layer inherits the texture of the textured template.

6. The method of claim 4, further comprising removing the sacrificial layer during removal of the textured template.

7. The method of claim 4, wherein the sacrificial layer comprises Pd.

8. The method of claim 1, further comprising forming an insulator layer over the buffer layer prior to forming the substrate layer.

9. The method of claim 8, wherein the insulator layer comprises an oxide.

10. The method of claim 1, further comprising forming a diffusion barrier over the buffer layer prior to forming the substrate layer.

11. The method of claim 10, wherein the diffusion barrier is substantially free of the texture of the textured template.

12. The method of claim 10, wherein the diffusion barrier comprises at least one of W, Re, an oxide, or a nitride.

13. The method of claim 12, wherein the diffusion barrier comprises W.

14. The method of claim 1, wherein the substrate layer comprises at least one of W, Mo, a metal alloy, a ceramic, or a glass.

15. The method of claim 1, wherein the substrate layer comprises a material substantially impervious to formation of at least one of As-containing phases or Si-containing phases at a temperature greater than approximately 350 °C.

16. The method of claim 1, wherein the substrate layer is substantially free of the texture of the textured template.

17. The method of claim 1, wherein the semiconductor layer comprises at least one of Si, Ge, or InGaAs.

18. The method of claim 1, wherein a coefficient of thermal expansion of the substrate layer substantially matches a coefficient of thermal expansion of the semiconductor layer.

19. The method of claim 1, wherein the buffer layer comprises at least one of Cr, an oxide, or a nitride.

20. The method of claim 1, wherein the textured template comprises at least one of Cu, Ni, or a Cu-Ni alloy.

21. The method of claim 1, wherein the semiconductor layer comprises at least one of a p-n junction or a p-i-n junction.

22. The method of claim 1, further comprising forming a semiconductor device on the semiconductor layer.

23. The method of claim 22, wherein the semiconductor device comprises at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, or InGaAs.

24. The method of claim 22, wherein the semiconductor device comprises at least one of a photovoltaic cell, a light-emitting diode, or a laser.

25. The method of claim 22, wherein the substrate layer functions as a back contact for the semiconductor device.

26. A semiconductor structure comprising:
a substantially untextured substrate layer;
a textured buffer layer disposed over the substrate layer; and
a semiconductor layer disposed over the textured buffer layer.

27. The semiconductor structure of claim 26, wherein a grain size of the textured buffer layer is greater than approximately 25 μm.

28. The semiconductor structure of claim 26, wherein the textured buffer layer comprises a metal or a metal alloy.

29. The semiconductor structure of claim 28, wherein the textured buffer layer comprises Cr.

30. The semiconductor structure of claim 26, wherein the textured buffer layer comprises at least one of an oxide or a nitride.

31. The semiconductor structure of claim 26, further comprising a diffusion barrier disposed between the substrate layer and the textured buffer layer.

32. The semiconductor structure of claim 31, wherein the diffusion barrier comprises a metal or a metal alloy.

33. The semiconductor structure of claim 32, wherein the diffusion barrier comprises at least one of W or Re.

34. The semiconductor structure of claim 31, wherein the diffusion barrier comprises at least one of an oxide or a nitride.

35. The semiconductor structure of claim 26, further comprising an insulator layer disposed between the substrate layer and the textured buffer layer.

36. The semiconductor structure of claim 35, wherein the insulator layer comprises an oxide.

37. The semiconductor structure of claim 26, wherein the substrate layer comprises at least one of W, Mo, a metal alloy, a ceramic, or a glass.

38. The semiconductor structure of claim 26, wherein a coefficient of thermal expansion of the substrate layer substantially matches a coefficient of thermal expansion of the semiconductor layer.

39. The semiconductor structure of claim 26, further comprising a semiconductor device disposed over the semiconductor layer.

40. The semiconductor structure of claim 39, wherein the semiconductor device comprises at least one of a photovoltaic cell, a light-emitting diode, or a laser.

41. The semiconductor structure of claim 39, wherein the semiconductor device comprises at least one of GaAs, AlGaAs, InGaP, InGaAsN, InGaAsP, InP, AlInAs, or InGaAs.

42. A semiconductor device comprising:

a substantially untextured flexible substrate layer; and

a plurality of textured semiconductor junctions disposed over the substrate layer.

43. The semiconductor device of claim 42, further comprising a textured buffer layer disposed between the substrate layer and the plurality of semiconductor junctions.

44. The semiconductor device of claim 42, further comprising an insulator layer disposed between the substrate layer and the plurality of semiconductor junctions.

45. The semiconductor device of claim 42, wherein the plurality of semiconductor junctions form a photovoltaic cell having an energy conversion efficiency greater than approximately 15%.

46. The semiconductor device of claim 42, wherein a grain size of each of the semiconductor junctions is greater than approximately 25 μm.

47. A structure comprising:

a textured template comprising a first metal;

a buffer layer disposed over the textured template, the buffer layer comprising a second metal different from the first metal; and

a substantially untextured substrate layer disposed over the buffer layer, the substrate layer comprising at least one of a ceramic, a glass, or a third metal different from both the first and second metals.

48. The structure of claim 47, wherein a texture of the buffer layer substantially matches the texture of the textured template.

49. The structure of claim 47, wherein the substrate layer comprises a material substantially impervious to formation of at least one of As-containing phases or Si-containing phases at a temperature greater than approximately 350 °C, and the textured template comprises a material that forms at least one of As-containing phases or Si-containing phases at a temperature greater than approximately 350 °C.

50. The structure of claim 47, further comprising a substantially untextured diffusion barrier disposed between the buffer layer and the substrate layer, the diffusion layer comprising at least one of an oxide, a nitride, or a fourth metal different from the first, second, and third metals.

51. The structure of claim 47, further comprising a textured sacrificial layer comprising Pd disposed between the textured template and the buffer layer.

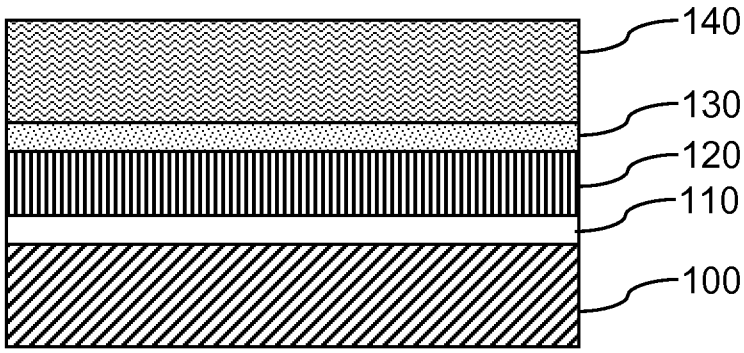


Fig. 1A

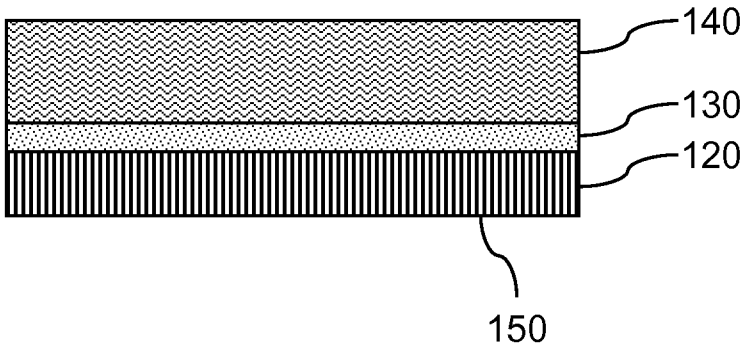


Fig. 1B

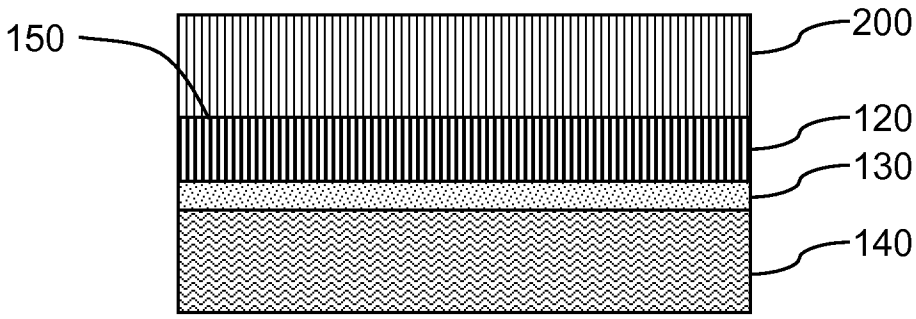


Fig. 2

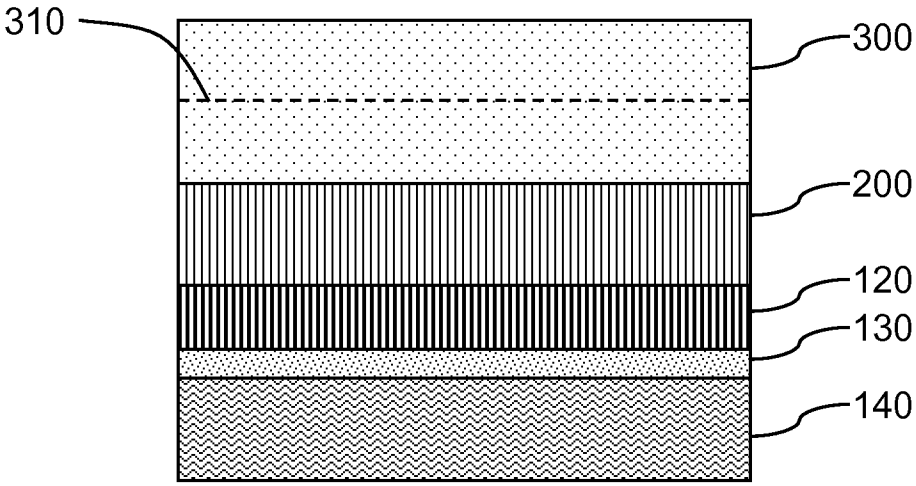


Fig. 3

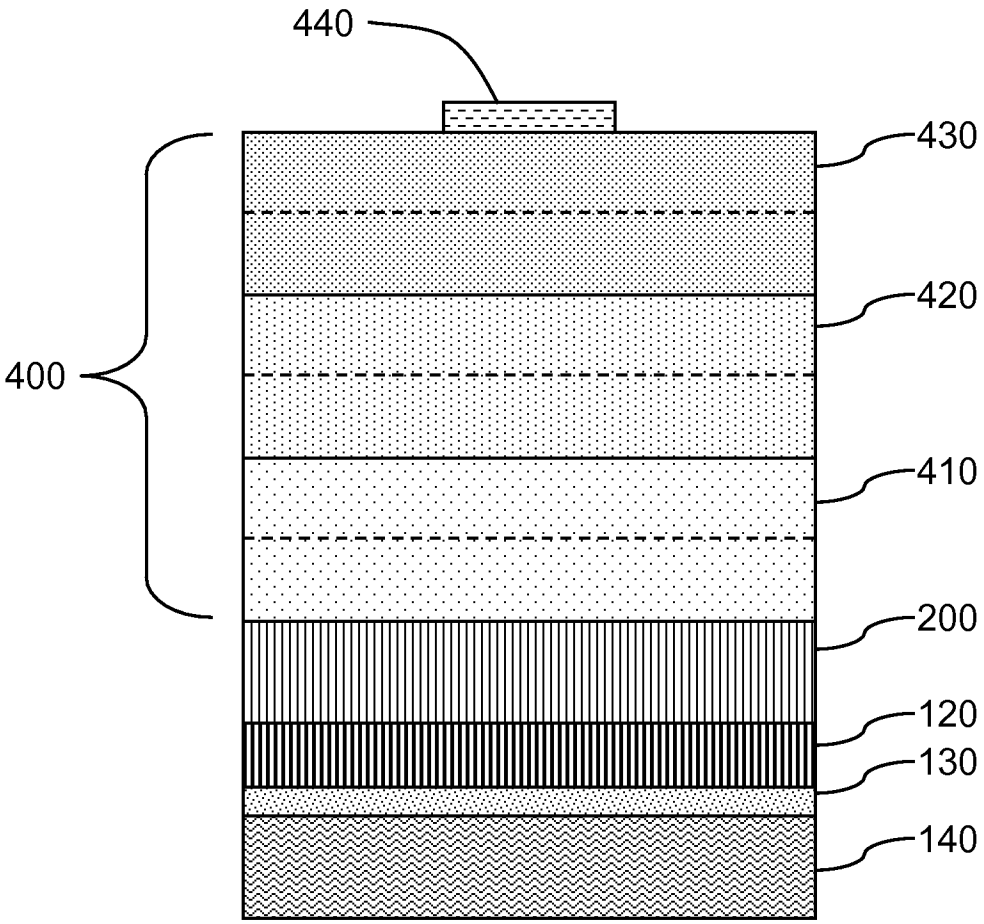


Fig. 4