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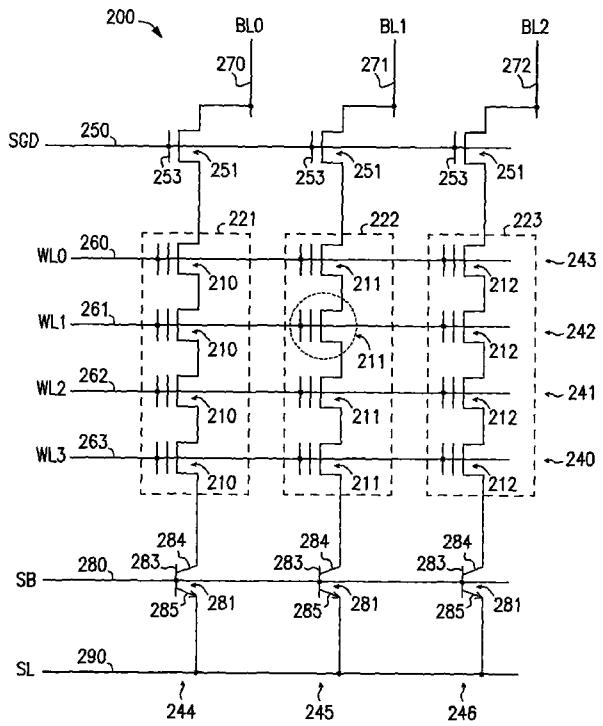
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(54) Title: APPARATUS AND METHODS INCLUDING A BIPOLAR JUNCTION TRANSISTOR COUPLED TO A STRING OF MEMORY CELLS

FIG. 2



(57) Abstract: Some embodiments include apparatus and methods having a string of memory cells, a conductive line and a bipolar junction transistor configured to selectively couple the string of memory cells to the conductive line. Other embodiments including additional apparatus and methods are described.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 16/02; G11C 7/00; G11C 16/04; G11C 16/10; G11C 11/413; G11C 16/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: bipolar junction transistor, memory cell, string, select, conductive line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 05371703 A (MIYAMOTO; JUNICHI) 06 December 1994 See abstract; page 4, line 56 - page 5, line 19; figure3.	1-32
A	US 2008-0144371 A1 (YEH CHIH-CHIEH et al.) 19 June 2008 See abstract; paragraphs [0049],[0050]; figures 1,3,7.	1-32
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A	JP 05-012880 A (NEC CORP.) 22 January 1993 See paragraphs [0001],[0010]; figure 1; claim 1.	1-32

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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