

(51) International Patent Classification:
G11C 13/00 (2006.01)(21) International Application Number:
PCT/US2015/030370(22) International Filing Date:
12 May 2015 (12.05.2015)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

- with international search report (Art. 21(3))

(54) Title: NON-VOLATILE RESISTANCE MEMORY DEVICES INCLUDING A VOLATILE SELECTOR

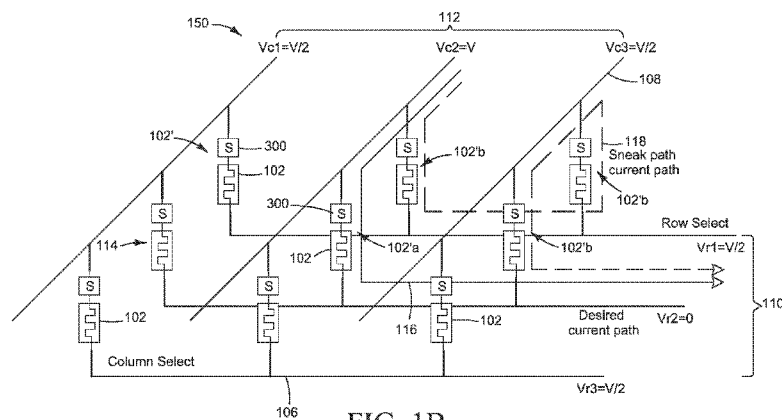


FIG. 1B

(57) **Abstract:** A nonvolatile memory cell includes a volatile selector electrically coupled in series with a nonvolatile memory device. The nonvolatile memory device includes a switching oxide or switching nitride sandwiched between a first bottom electrode and a first top electrode. The volatile selector includes a selector oxide matrix sandwiched between a second bottom electrode and a second top electrode. The selector oxide matrix may be composed of either copper oxide, silicon dioxide, or a mixture of copper oxide and silicon dioxide. One or both of the second bottom electrode and the second top electrode may be composed of silver. A memory array including a plurality of the nonvolatile memory cells is also disclosed, as is a method for manufacturing the array.

NON-VOLATILE RESISTANCE MEMORY DEVICES INCLUDING A VOLATILE SELECTOR

BACKGROUND

[0001] Non-volatile memory is computer memory that can store information even when not powered. Types of non-volatile memory may include resistive RAM (random access memory) (RRAM or ReRAM), phase change RAM (PCRAM), conductive bridge RAM (CBRAM), ferroelectric RAM (F-RAM), etc.

[0002] Resistance memory elements, such as resistive RAM, or ReRAM, can be programmed to different resistance states by applying programming energy. After programming, the state of the resistive memory elements can be read and remains stable over a specified time period. Large arrays of resistive memory elements can be used to create a variety of resistive memory devices, including non-volatile solid state memory, programmable logic, signal processing, control systems, pattern recognition devices, and other applications. Examples of resistive memory devices include valence change memory and electrochemical metallization memory, both of which involve ionic motion during electrical switching and belong to the category of memristors.

[0003] Memristors are devices that can be programmed to different resistive states by applying a programming energy, for example, a voltage or current pulse. This energy generates a combination of electric field and thermal effects

that can modulate the conductivity of both non-volatile switch and non-linear select functions in a memristive element. After programming, the state of the memristor can be read and remains stable over a specified time period.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A-1B depict, in perspective, a memristor crossbar and a selector-memristor crossbar, respectively, according to an example.

[0005] FIG. 2 depicts a half V scheme with selector, according to an example.

[0006] FIG. 3 is a cross-sectional view, depicting a device structure for a selector, according to an example.

[0007] FIG. 4 is a cross-sectional view, depicting another device structure, according to an example.

[0008] FIGS. 5A-5D, in cross-sectional view, depict a process for fabricating the device structure of FIG. 4, according to an example.

[0009] FIG. 6, in cross-sectional view, illustrates a nonvolatile memory cell that may include a volatile selector electrically coupled in series with a non-volatile resistance memory device, according to an example.

[0010] FIG. 7 depicts a method of manufacturing a memory array with nonvolatile resistance memory devices and volatile selectors, according to an example.

[0011] FIGS. 8A-8B show the I-V results for a selector having a Cu_2O selector oxide matrix sandwiched between a TiN bottom electrode and an Ag-containing top electrode, according to an example.

DETAILED DESCRIPTION

[0012] Memristors are nano-scale devices that may be used as a component in a wide range of electronic circuits, such as memories, switches, radio frequency circuits, and logic circuits and systems. In a memory structure, a crossbar array of memristor devices may be used. When used as a basis for memories, memristors may be used to store bits of information, 1 or 0. When used as a logic circuit, a memristor may be employed as configuration bits and switches in a logic circuit that resembles a Field Programmable Gate Array, or may be the basis for a wired-logic Programmable Logic Array. It is also possible to use memristors capable of multi-state or analog behavior for these and other applications. While specific examples to memristors are provided herein, it is appreciated that many other types of non-volatile memory may beneficially employ the teachings herein. Examples of such other types of non-volatile memory may include resistive RAM (random access memory) (RRAM or ReRAM), phase change RAM (PCRAM), conductive bridge RAM (CBRAM), ferroelectric RAM (F-RAM), etc.

[0013] The resistance of a memristor may be changed by applying a voltage across or a current through the memristor. Generally, at least one channel may be formed that is capable of being switched between two states—one in which the channel forms an electrically conductive path (“ON”) and one in which the channel forms a less conductive path (“OFF”). In some cases, conducting channels may be formed by metal ions and/or oxygen vacancies. Some memristors exhibit bipolar switching, where applying a voltage of one polarity may switch the state of the memristor and where applying a voltage of the opposite polarity may switch back to the original state. Alternatively, memristors may exhibit unipolar switching, where switching is performed, for example, by applying different voltages of the same polarity.

[0014] Using memristors in crossbar arrays may lead to read and/or write failure due to sneak currents passing through the cells that are not selected, for

example, cells on the same row or column as a targeted cell. Failure may arise when there is insufficient current through the targeted memristor due to current sneaking through untargeted neighboring cells. As a result, effort has been spent on minimizing sneak currents. Using a transistor with each memristor has been proposed to isolate each cell and overcome the sneak current. However, using a transistor with each memristor in a crossbar array limits array density and increases cost, which may impact the commercialization of memristor devices.

[0015] When used as a switch, the memristor may either be in a low resistance (ON) or high resistance (OFF) state in a crosspoint memory. During the last few years, researchers have made great progress in finding ways to make the switching function of these memristors behave efficiently. For example, tantalum oxide (TaO_x)-based memristors have been demonstrated to have superior endurance over other nano-scale devices capable of electronic switching. In lab settings, tantalum oxide-based memristors are capable of over 10 billion switching cycles.

[0016] A memristor may use a switching material, such as TiO_x , HfO_x or TaO_x , sandwiched between two electrodes. Memristive behavior is achieved by the movement of ionic species (e.g., oxygen ions or vacancies) within the switching material to create localized changes in conductivity via modulation of a conductive filament between two electrodes, which results in a low resistance "ON" state, a high resistance "OFF" state, or intermediate states. Initially, when the memristor is first fabricated, the entire switching material may be nonconductive. As such, a forming process may be required to form the conductive channel in the switching material between the two electrodes. A known forming process, often called "electroforming", includes applying a sufficiently high (threshold) voltage across the electrodes for a sufficient length of time to cause a nucleation and formation of a localized conductive channel (or active region) in the switching material. The threshold voltage and the length of time required for the forming process may depend upon the type of material used for the

switching material, the first electrode, and the second electrode, and the device geometry.

[0017] Metal or semiconductor oxides may be employed in memristive devices; examples include either transition metal oxides, such as tantalum oxide, titanium oxide, yttrium oxide, hafnium oxide, niobium oxide, zirconium oxide, or other like oxides, or non-transition metal oxides, such as aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include transition metal nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride.

[0018] TaO_x and HfO_x based memristors have demonstrated the most promising results. However, both of these oxide systems have a linear current-voltage relation in the ON state, which is not desired due to the sneak path current issue, described above. For applications in high density crossbar arrays, a nonlinear selector may be in series with each memristor to form a 1S1R (one selector - one resistor) structure. A bipolar nonlinear selector to suppress the sneak current in the crossbar array has been fabricated using a simple metal-oxide-metal structure realized by the Schottky emission over the metal/oxide barriers or other method. Many materials can be used for the oxide (e.g., VO_2 , TiO_2 , NbO_2 , etc.). The metal for the bottom electrode and the top electrode can be TiN, TaN, etc. For illustration example, both TaN/ NbO_2 /TaN and TaN/TaO/TaN have shown good performance.

[0019] However for practical applications, the selectors presently under development may not be able to meet the requirement for both high nonlinearity (>1000), low leakage current (less than 1 nA at below threshold voltage), and high current density requirement at above threshold voltage (on the order of 10^6 A/cm²). As used herein, "high nonlinearity" is based on a comparison of the current density level at two different voltages, here, V and V/2. The ratio of the two current densities should be at least 10^3 to be considered nonlinear. In some cases, the ratio may approach or even exceed 10^6 for improved nonlinearity.

[0020] Herein, a new type of selector is described, which can satisfy both requirements of high nonlinearity and be able to conduct current at a level of a few tens of μA for a nano device size such as $30\text{ nm} \times 30\text{ nm}$, or have a current density of at least 10^6 A/cm^2 . The new selector may enable the final production of memristors for large crossbar applications.

[0021] In accordance with the teachings herein, a volatile, nonlinear selector may be made with a matrix oxide (e.g., Cu_2O or SiO_2 or a Cu_2O - SiO_2 mixture) and at least one of two electrodes based on a cation metal, such as Ag. By "volatile", in reference to memory, is meant computer memory that requires power to maintain the stored information; it retains its contents while powered on but when the power is interrupted, the stored data is immediately lost or decays with time, which is characterized by a relaxation time. By "fast-diffusing" is meant that the rate of diffusion should be faster than the rate of diffusion of oxygen vacancies in a memristor oxide (or nitrogen vacancies in a memristor nitride). Specifically, interstitial diffusion is much faster than substitutional diffusion. Fast diffusion is a relative term which can be originated from diffusion of impurities in Si. There are two main lattice point defects: interstitial and substitutional. Interstitial diffusion has a lower activation energy, and a higher jump frequency (neighboring interstitial sites are always vacant). Substitutional diffusion has a higher activation energy, and a lower jump frequency (neighboring substitutional site may not be vacant). Cu, Ag, and Au are some examples of fast diffusers.

[0022] In some examples, fast ions, e.g., silver, and the matrix oxide (Cu_2O or SiO_2 or Cu_2O - SiO_2 mixture) may have phase equilibrium and no mutual solubility. This can be seen from the phase diagrams involved (not shown). For example, from an inspection of the ternary phase diagrams Ag-Cu-O (and Ag-Si-O, and Cu-Si-O), Ag- CuO_x is seen to be in equilibrium (co-exist without chemical reaction or atomic interaction). No mutual solubility means Ag will not be dissolved in CuO_x and CuO_x will not be dissolved in Ag (i.e., not form a solid solution). This can be due to the heat of mixing being positive.

[0023] The selector may be configured in series with a nonvolatile element, such as a memristor. The term “in series” means that the components are electrically connected along a single path so that the same current flows through all of the components. While the components may be in series, they may or may not be in direct contact with one another, and the order of the components may vary.

[0024] In an example, the nonvolatile element may be linear, or, if non-linear, then only slightly. The selector formed with the materials mentioned (fast-diffusing cation metal particles) evidences high nonlinearity and volatile characterizations. The terms “linear” and “non-linear” refer to the nature of the current-voltage (I-V) curve; that is, whether the curve is linear or non-linear, respectively. As used in the present specification and in the appended claims, the term “nonlinear” may refer to a property of the selector or memristor wherein a change in voltage applied across the selector or memristor results in a disproportionate change in current flowing through the selector or memristor, respectively.

[0025] The sneak-path issue is inherent for crossbar architectures, regardless of the memory element employed. FIG. 1A depicts a crossbar 100 containing a plurality of memory elements 102. Each memory element 102 may include a switching oxide sandwiched between a bottom electrode and a top electrode (not visible in FIG. 1, but depicted in FIG. 4). Each memory element 102 is sandwiched between a bottom electrically conducting trace 106 and a top electrically conducting trace 108. The crossbar 100 is made of a lower layer 110 of electrically conducting traces formed by a plurality of bottom conducting traces 106 and an upper layer 112 of electrically conducting traces formed by a plurality of top conducting traces 108, with the memory element 102 at each crosspoint 114 formed by a bottom trace 106 and a top trace 108. The bottom conductive traces 106 may be referred to as row, or bit, lines, while the top conductive traces 108 may be referred to as column, or word, lines. However, it is immaterial whether the row (bit) lines are above or below the column (word) lines.

[0026] FIG. 1A depicts the situation that while trying to read the high resistive element 102a, a current sneak path exists due to three low resistive elements 102b. The thin line 116 with arrow head shows the desired current path. The dashed line 118 with arrow head shows a sneak path current path.

[0027] The solution, illustrated in FIG. 1B, may be to increase the nonlinearity or asymmetry of the I-V characteristic of the memristor elements 102, which may ensure that the memristor, or other nonlinear memory device, can be used in large crossbar arrays 150. Increasing the nonlinearity of the memristor cells 102 may result in reduction or even elimination of the sneak path current path 118. As noted above, a nonlinear, nonvolatile memristor cell 102' may include a selector 300 (discussed below in connection with FIG. 3) and a memristor element 102. The selector 300 may be nonlinear and volatile; the memristor 102 may be linear and nonvolatile. While these are the ideal states of the selector 300 and memristor 102, respectively, it is understood that there may be slight variations from the ideal state. In any event, the net intent is to provide a memory cell 102' that is both nonlinear and nonvolatile.

[0028] The selector 300 may be used to mitigate the sneak path current issue by suppressing the total current passing through the non-selected devices in the array at the given voltage. Nonlinearity may depend on the operating voltage range, which in turn depends on the materials used and structure of the device stack (memristor plus selector). For memristors having a certain operating voltage, there may be a need to tune the threshold of selector 300, such as by adjusting the species, film thickness, concentration, etc., as described in greater detail below.

[0029] The concept for a selector associated with the popular reading scheme is shown in FIG. 2. The selected high resistance cell is denoted 102'a and the cells having low resistance are denoted 102'b. The low resistance cells 102'b are in the same row or column as the selected cell 102'a. It is the low resistance cells 102'b that may support sneak path currents. V is the applied voltage, V/2 is half voltage, and G is ground.

[0030] The selector 300, shown in FIG. 3, may include a bottom electrode 302, a top electrode 304, and a selector oxide matrix 306 disposed between the two electrodes. The bottom electrode 302 and top electrode 304 may be symmetrical or asymmetrical. If symmetrical, both electrodes 302 and 304 may be made of the same metal, here, silver (Ag). If asymmetrical, one of the two electrodes 302, 304 may be silver and the other of the two electrodes may be, but not limited to, aluminum (Al), platinum (Pt), tungsten (W), gold (Au), titanium (Ti), ruthenium dioxide (RuO_2), titanium nitride (TiN), tungsten nitride (WN_2), tantalum (Ta), hafnium nitride (HfN), niobium nitride (NbN), tantalum nitride (Ta₂N₅), and the like. The thickness of the electrodes 302, 304 may be in the range of 0.3 to 20 nm. In some examples, the minimum thickness may be 0.6 nm.

[0031] The selector oxide matrix 306 may be copper oxide or silicon dioxide or a mixture of copper oxide and silicon dioxide. In particular, the copper oxide may be Cu_2O . The mixture of Cu_2O and SiO_2 may be a two-phase mixture. The thickness of the dielectric layer 310 may range from about 3 to 100 nm. Other dielectric oxides that may be used in place of (or in conjunction with) SiO_2 to lower leakage current may include Cr_2O_3 , HfO_2 , MoO_3 , NiO , Ta_2O_5 , V_2O_5 , Y_2O_3 , and ZrO_2 , for example. The dielectric oxide, if used, may be a good insulator (to lower leakage current) and be in equilibrium with Ag and Cu_2O (not reactive with either).

[0032] FIG. 4 is a cross-sectional view of an example selector 300', showing a particular implementation useful in a commercial device. FIGS. 5A-5D, described in greater detail below, illustrate a process for manufacturing the selector shown in FIG. 4.

[0033] A tungsten (W) layer 402 may be formed on a substrate (not shown). The W layer 402 may provide electrical conductivity. Examples of other electrically conductive layers that may be used in place of (or in conjunction with) may include Al, Cu, Ni, Mo, Pd, Pt, Ta, Ti, Ag, and Au and their alloys. The

electrically conductive layer 402 may be about 100 to 500 nm thick. In an example, the conductive layer 402 may be about 300 nm thick.

[0034] A layer 404 of silicon nitride (Si_3N_4) may be formed on the tungsten layer 402. The Si_3N_4 layer 404 may be about 5 to 30 nm thick. In an example, the Si_3N_4 layer 404 may be about 15 nm thick.

[0035] A layer 406 of silicon dioxide (SiO_2) may be formed on the silicon nitride layer 404. The SiO_2 layer 406 may be about 50 to 300 nm thick. In an example, the SiO_2 layer 406 may be about 100 nm thick.

[0036] A via may be formed and filled with a plug of titanium nitride (TiN) 302. The TiN plug 302 may form the bottom electrode for the selector 300'. The thin Si_3N_4 is to provide some etch selectivity for W. The thick SiO_2 is the bulk dielectric. Using TiN as the bottom electrode 302 may provide an asymmetric or unipolar selector 300'. Alternatively, the bottom electrode 302 can be Ag for a symmetric or bipolar selector 300'. Other electrically conducting materials, such as Pt, may be used to form an asymmetric selector 300'.

[0037] The selector oxide matrix 306 is formed on the SiO_2 layer 406 and in physical and electrical communication with the TiN plug 302. The thickness of the selector oxide matrix 306 may be in the range of 2 to 50 nm. In an example, the thickness of the selector oxide matrix 306 may be about 15 nm.

[0038] The selector oxide matrix 306 may be Cu_2O , a two-phase mixture of Cu_2O and SiO_2 , or SiO_2 . The selector oxide matrix 306 may act as a dielectric matrix in which a volatile conducting bridge can form under an electric field. As used herein, the term "volatile conducting bridge" may be described by the following. The conductive bridge can be divided between ionic and electronic conduction. Ionic transport is involved to form a conductive path (or bridge, or channel, or filament) from one electrode through the dielectric film to the other electrode under an applied electric field. Once a conductive path is formed, electronic conduction can occur from one electrode to the other electrode under an applied electric field. The conductive bridge being volatile means it will decay or dissolve when the applied voltage is decreased or removed.

[0039] While in some examples, the selector oxide matrix 306 may be Cu_2O , it has been found that the addition of a more insulating oxide (more insulating than Cu_2O), such as SiO_2 , to the Cu_2O may further reduce leakage current. Since Cu_2O and SiO_2 are in equilibrium, then the dielectric film composition can be optimized within the entire composition range. For example, a system may be defined in which equilibrium exists between $\text{Ag-Cu}_2\text{O}$, Ag-SiO_2 , and $\text{Cu}_2\text{O-SiO}_2$.

[0040] Equilibrium, which can include chemical equilibrium, mechanical equilibrium, and thermal equilibrium, may be an important and essential property for materials to function properly and with long term stability. For example, chemical equilibrium means equal chemical potentials between its components such that no chemical reactions will occur to form new components that can be undesirable or detrimental. Further increasing the SiO_2 portion in the ($\text{Cu}_2\text{O-SiO}_2$) matrix may reduce leakage current even more.

[0041] The top electrode 304, which contacts the selector oxide matrix 306, may be made of a metal. The top electrode may be composed of three layers 304a-304c. Layer 304a may be silver. Where the selector oxide matrix 306 is Cu_2O , then the Ag-Cu-O ternary phase diagram may be considered. The ternary phase diagram may be constructed from Ag-Cu , Ag-O , and Cu-O binaries, and from the thermodynamic properties of Ag_2O , Cu_2O , and CuO . From these considerations, the following points may be noted:

Ag is in equilibrium with Cu;

Ag is in equilibrium with Cu_2O , and CuO , or in equilibrium with CuO_x , where $x = 0.5$ or 1 ;

Ag and CuO_x show no mutual solubility;

Cu_2O (bandgap approximately 2.1 eV) is more resistive than CuO (bandgap approximately 1.2 eV);

Ag responds fast under voltage so that Cu_2O does not switch; and

An Ag electrode can be used as a source and sink for Ag ions.

[0042] The silver layer 304a may have a thickness of about 1 to 30 nm. In an example, the thickness may be about 10 nm. The top electrode 304 may further include additional metal layers 304b and 304c. Metal layer 304b may be platinum (Pt), for example, and metal layer 304c may be chromium (Cr), for example. Pt layer 304b may have a thickness in the range of 5 to 50 nm. In an example, Pt layer 304b may have a thickness of about 10 nm. Cr layer 304c may have a thickness in the range of 5 to 50 nm. In an example, Cr layer 304c may have a thickness of about 20 nm. The Pt layer 304b may be used for electric conductivity, while the Cr layer 304c may be used as a self-aligned etch mask, if desired. The Pt layer 304b may be replaced with CMOS-compatible metals or a conductive oxide, such as RuO₂, or a conductive nitride, such as TiN. The Cr layer 304c can be omitted if no bit etch is used (to remove an oxide film not covered by electrode 304).

[0043] FIGS. 5A-5D depict an example process for forming the example selector 300' depicted in FIG. 4.

[0044] In FIG. 5A, a nano-via device platform is formed, with TiN as the bottom electrode 302, in which the diameter of via 502 is about 30 nm. The bottom metal contact 402, e.g., W, is for electric connection to the bottom electrode of the selector 300' structure. The bottom metal contact 402 may in turn be supported by a dielectric substrate, such as SiO₂ (not shown). The W layer 402 may be formed by sputter deposition. The Si₃N₄ layer 404 and the SiO₂ layer 406 may be successively formed on the W layer 402. Formation of these two dielectric layers 404, 406 may be done by CVD (chemical vapor deposition). The via 502 may be formed by lithography to define an opening that extends through both the dielectric layers 404, 406, down to and exposing the W layer 402. The TiN plug 302 may be formed by ALD (atomic layer deposition) or CVD (chemical vapor deposition) to fill the via 502. If necessary, CMP (chemical-mechanical polishing), or other suitable process, may be used to planarize the top surfaces of the SiO₂ layer 406 and the TiN plug 302.

[0045] In FIG. 5B, the Cu₂O layer 306 may be blanket sputtered from a Cu₂O target to a thickness of about 20 nm, covering both the SiO₂ layer 406 and the TiN plug 302.

[0046] In FIG. 5C, the top electrode 304 may be formed by e-beam evaporation, in succession, of Ag, Pt, and Cr, using a shadow mask. In an example, the Ag layer 304a may be formed to a thickness of about 5 nm, the Pt layer 304b may be formed to a thickness of about 20 nm, and the Cr layer 304c may be formed to a thickness of about 10 nm.

[0047] In FIG. 5D, the selector oxide matrix layer 306 may be laterally reduced by, for example, an ion etch to isolate it and form individual selectors. The top Cr layer 304c may be used as the etch mask.

[0048] Although the resulting selector 300' is asymmetrical, it offers the advantage that nano-size devices can be readily made and tested on the existing TiN nano-via platform. On the other hand, the device stack is not symmetric and the device I-V curves accordingly are not symmetric.

[0049] As indicated above and as shown in FIG. 6, an example nonvolatile memory cell 102' may include the volatile selector 300 electrically coupled in series with the nonvolatile resistance memory device, such as memristor 102. The nonvolatile resistance memory device 102 may include a switching layer 606 composed of an oxide or nitride sandwiched between a first bottom electrode 602 and a first top electrode 604. The volatile selector 300 may include the selector oxide matrix 306 sandwiched between a second bottom electrode 302 and a second top electrode 304. In a crossbar configuration (FIG. 1, 150), each memory cell 102' may be disposed at the intersection 114 formed by one of the bottom conducting traces 106 and one of the top conducting traces 108.

[0050] The electrodes 602, 604 for the memristor 102 may include aluminum (Al), platinum (Pt), tungsten (W), gold (Au), titanium (Ti), ruthenium dioxide (RuO₂), titanium nitride (TiN), tungsten nitride (WN₂), tantalum (Ta), hafnium ni-

tride (HfN), niobium nitride (NbN), tantalum nitride (TaN), and the like. The thickness of the electrodes 602, 604 may be in the same range as for electrodes 302, 304.

[0051] The teachings herein may be employed with an crossbar that is fabricated with resistance memory devices, or resistance random access memory devices, denoted RRAM or ReRAM, such as phase change RAM (PCRAM), spin transfer torque RAM (STTRAM), conductive bridge RAM (CBRAM), and others. In some examples, the nonvolatile resistance memory device 102' may be a memristor.

[0052] In some examples, the nonvolatile memory cell 102' may include an optional interface layer 608 sandwiched between the first top electrode 604 of the nonvolatile resistance memory element 102 and the second bottom electrode 302 of the selector 300. The interface layer 608 may serve as a buffer layer to separate the memristor and selector so that they do not chemically and/or physically interfere with each other. The interface layer 608 may be a good electrical conductor over the temperature range from room temperature (approximately 20° to 26°C) to 85°C and a good diffusion barrier. In some examples, the interface layer 608 may be a metal, such as tantalum or tungsten. The choice of a material for the interface layer may depend on layers below and above it. Additional non-limiting examples of the interface layer 608 may include TiN, Ti₄O₇, TaN, NbN, Ru, and W. The interface layer 608 is optional, in that it may be omitted, since the nonvolatile memory cell 102' may operate fine without it. Alternatively, it may be used for an improved device 102', but accepting the costs associated with providing the extra layer.

[0053] A memory array, or crossbar, 150 (in FIG. 1B) having nonvolatile resistance memory devices may include a set 110 of electrically conducting row traces 106 intersecting a set 112 of electrically conducting column traces 108 to form intersections 114, with a memory cell 102' disposed at each intersection between one of the row lines and one of the column lines. As shown in FIG. 6, the memory cell 102' may be a combination of a volatile selector 300 electrically

coupled in series with the nonvolatile resistance memory device 102, as described above. The first bottom electrode 602 may be electrically coupled to a row trace 106 or to a column trace 108 and wherein the second top electrode 304 may be electrically coupled to the other of the row trace 106 or the column trace 108. In some examples, one or both of the first bottom electrode 602 and the second top electrode 304 may be omitted, and the switching oxide 606 and selector oxide matrix 306 layers may be coupled directly to the electrically conducting row trace 106 and the electrically conducting column trace 108, respectively.

[0054] A method of manufacturing a memory array with nonvolatile resistance memory devices and selectors is depicted in FIG. 7. The method 700 includes providing 705 a set 110 of electrically conducting row traces 106. The electrically conducting row traces 106 may be formed by any of a number of processes, including electroplating, sputtering, evaporation, ALD (atomic layer deposition), co-deposition, chemical vapor deposition, IBAD (ion beam assisted deposition), oxidation of pre-deposited materials, or any other film deposition technology.

[0055] The method 700 further includes providing 710 memory cells 102' disposed at a plurality of locations along the set 110 of row traces 106. The memory cell 102' may include the nonvolatile resistance memory device 102 electrically coupled in series with the volatile selector 300 or 300', as described above.

[0056] Taking FIG. 6 as an example, deposition of the metal layers 602, 604, 302, and 304 may be performed by such processes as electroplating, sputtering, evaporation, ALD (atomic layer deposition), co-deposition, chemical vapor deposition, IBAD (ion beam assisted deposition), oxidation of pre-deposited materials, or any other film deposition technology. The switching oxide layer 606, the optional interface layer 608, and the selector oxide matrix 306 may be formed by e-beam deposition, sputter deposition, atomic layer deposition (ALD), and the like. The layers 602, 606, 604, 608 (if used), 302, 306, and 304 may be

deposited sequentially. It will be appreciated that in FIG. 6, the selector 300 is shown on "top" and the memristor 102 is shown on the "bottom" of the device 102'. However, in some examples, the memristor 102 may be on "top" and the selector 300 on the "bottom".

[0057] The method 700 concludes with providing 715 a set 112 of electrically conducting column traces 108 to contact the memory cells 102' at unique intersections 114. The electrically conducting column traces 112 may be formed by any of a number of processes, including electroplating, sputtering, evaporation, ALD (atomic layer deposition), co-deposition, chemical vapor deposition, IBAD (ion beam assisted deposition), oxidation of pre-deposited materials, or any other film deposition technology. The process used may be the same as or different than the process used to form the electrically conducting row traces 110. The order of the steps of method 700 may be reversed, so that the column traces 108 are formed first and the row traces 106 are formed last.

[0058] In some examples, the new selector 300, 300' may have a nonlinearity of $>10^6$ with large current density. The higher the current ratio (nonlinearity), the larger the potential crossbar size. For example, a nonlinearity of $>10^6$ may allow a crossbar array of 1000 rows by 1000 columns, or 10^6 memristors to populate the 10^6 crosspoints. On the other hand, a nonlinearity on the order of 10^3 could lead to a smaller array.

[0059] FIGS. 8A-8B show the I-V results using the Cu_2O selector oxide matrix 306 with TiN bottom electrode 302 and Ag-containing top electrode 304. In an example of the device 300', the selector oxide matrix 306 was a 20 nm thick layer composed of Cu_2O . The bottom electrode 302 was a layer of TiN, which supported the selector oxide matrix 306. The top electrode was a three-layer element of silver 304a (5 nm), covered with a layer of platinum 304b (20 nm) and chromium 304c (10 nm). The Cu_2O layer 306 was sputtered from a Cu_2O target. The device size was 30 nm in diameter, which was the size the TiN via.

[0060] As shown in FIG. 8A, under a positive voltage bias (+V DC sweep), the selector showed volatile switching. Without subscribing to any particular theory, it appears that Ag ions were being driven from the top electrode (silver layer 304a), to form the volatile conducting bridge (VCB) through the Cu₂O selector oxide matrix 306.

[0061] As shown in FIG. 8B, under a DC sweep from +V to -V, the device exhibited an asymmetrical I-V curve, such that at +V polarity, a volatile switch was created, as also shown in FIG. 8A. However, at -V polarity, no switch was created. To obtain symmetrical VCB switching, both bottom electrode 302 and top electrode 304 would be the same, such as an Ag source/sink. On the other hand, an asymmetrical selector may find use in a unipolar memristor.

[0062] The selector disclosed herein may achieve both high current in a low resistance state and high nonlinear selection functions. The selector may return to the high resistance state when the voltage is below its holding voltage (the voltage to hold selector in the ON state).

[0063] It is appreciated that, in the foregoing description, numerous specific details are set forth to provide a thorough understanding of the examples. However, it is appreciated that the examples may be practiced without limitation to these specific details. In other instances, well-known methods and structures may not be described in detail to avoid unnecessarily obscuring the description of the examples. Also, the examples may be used in combination with each other.

[0064] While a limited number of examples have been disclosed, it should be understood that there are numerous modifications and variations therefrom. Similar or equal elements in the Figures may be indicated using the same numeral.

[0065] It is be noted that, as used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise.

CLAIMS

What is claimed is:

1. A nonvolatile memory cell, including:

a volatile selector electrically coupled in series with a nonvolatile resistance memory device, the nonvolatile resistance memory device comprising a switching oxide or switching nitride sandwiched between a first bottom electrode and a first top electrode and the volatile selector comprising a selector oxide matrix sandwiched between a second bottom electrode and a second top electrode,

wherein the selector oxide matrix comprises copper oxide, silicon dioxide, or a mixture of copper oxide and silicon dioxide, and

wherein one or both of the second bottom electrode and the second top electrode comprises silver.

2. The nonvolatile memory cell of claim 1, wherein the non-volatile resistance memory device is a memristor.

3. The nonvolatile memory cell of claim 1, further including an interface layer sandwiched between the first top electrode of the nonvolatile resistance memory element and the second bottom electrode of the selector, the interface layer acting as a diffusion barrier while being electrically conducting.

4. The nonvolatile memory cell of claim 3, wherein the interface layer comprises a material selected from the group consisting of TiN, Ti₄O₇, TaN, Ta, NbN, Ru, and W.

5. The nonvolatile memory cell of claim 1, wherein the second bottom electrode comprises TiN, Ag, or Pt and the second top electrode comprises Ag.

6. The nonvolatile memory cell of claim 1, wherein the selector oxide matrix comprises a mixture of Cu_2O and SiO_2 as $(\text{Cu}_2\text{O})_x(\text{SiO}_2)_{1-x}$ in a composition range of $x=0$ to $x=1$.

7. A memory array with nonvolatile memory cells, the memory array including:

- a set of electrically conducting row lines intersecting a set of electrically conducting column lines to form intersections; and

- each nonvolatile memory cell disposed at each intersection between one of the row lines and one of the column lines;

- wherein the memory cell comprises a nonvolatile resistance memory device electrically coupled in series with a volatile selector, the nonvolatile resistance memory device comprising a switching oxide or switching nitride sandwiched between a first bottom electrode and a first top electrode and the volatile selector comprising a selector oxide matrix sandwiched between a second bottom electrode and a second top electrode,

- wherein the selector oxide matrix comprises copper oxide, silicon dioxide, or a mixture of copper oxide and silicon dioxide,

- wherein one or both of the second bottom electrode and the second top electrode comprises silver, and

- wherein the first bottom electrode is electrically coupled to a row trace or to a column trace and wherein the second top electrode is electrically coupled to the other of the row trace or the column trace.

8. The memory array of claim 7, wherein the non-volatile memory device is a memristor.

9. The memory array of claim 7, further including an interface layer sandwiched between the first top electrode of the nonvolatile resistance memory element and the second bottom electrode of the selector.

10. The memory array of claim 9, wherein the interface layer comprises a material selected from the group consisting of TiN, Ti_4O_7 , TaN, Ta, NbN, Ru, and W.

11. The memory array of claim 7, wherein the selector oxide matrix comprises a mixture of Cu_2O and SiO_2 as $(\text{Cu}_2\text{O})_x(\text{SiO}_2)_{1-x}$ in a composition range of $x=0$ to $x=1$.

12. A method of manufacturing a memory array with nonvolatile memory cells, the method including:

providing a set of electrically conducting row traces;

providing a memory cell disposed at a plurality of locations along each of the row traces, wherein each memory cell comprises a nonvolatile memory device electrically coupled in series with a volatile selector having a selector oxide matrix, the nonvolatile resistance memory device comprising a switching oxide or switching nitride sandwiched between a first bottom electrode and a first top electrode and the volatile selector comprising the selector oxide matrix sandwiched between a second bottom electrode and a second top electrode; and

providing a set of electrically conducting column traces to contact the memory cells at unique intersections,

wherein each nonvolatile memory device comprises a switching oxide or switching nitride sandwiched between a first bottom electrode and a first top electrode and the volatile selector comprises a selector oxide matrix sandwiched between a second bottom electrode and a second top electrode,

wherein the selector oxide matrix comprises copper oxide, silicon dioxide, or a mixture of copper oxide and silicon dioxide,

wherein one or both of the second bottom electrode and the second top electrode comprises silver, and

wherein the first bottom electrode of each memory device is electrically coupled to a given row trace or to a given column trace and wherein the

second top electrode of each selector is electrically coupled to the other of the row trace or the column trace.

13. The method of claim 12, wherein the second bottom electrode comprises TiN, Ag, or Pt and the second top electrode comprises Ag.

14. The method of claim 13, wherein the selector oxide matrix is formed from a mixture of Cu_2O and SiO_2 in a ratio of $\text{Cu}_2\text{O}:\text{SiO}_2$ as $(\text{Cu}_2\text{O})_x(\text{SiO}_2)_{1-x}$ in a composition range of $x=0$ to $x=1$.

15. The method of claim 12, further including providing an interface layer sandwiched between the first top electrode of the nonvolatile memory element and the second bottom electrode of the selector.

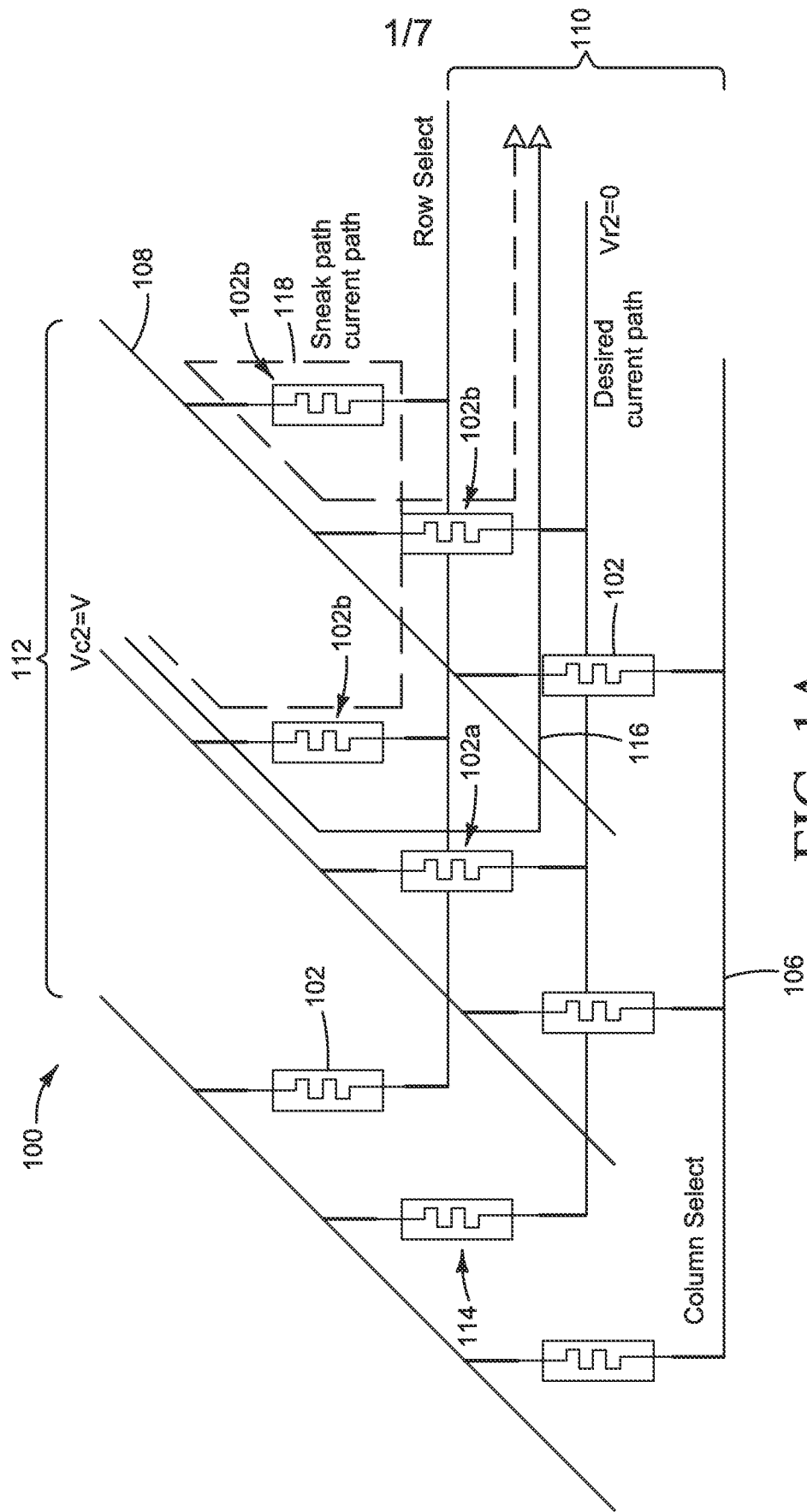


FIG. 1A

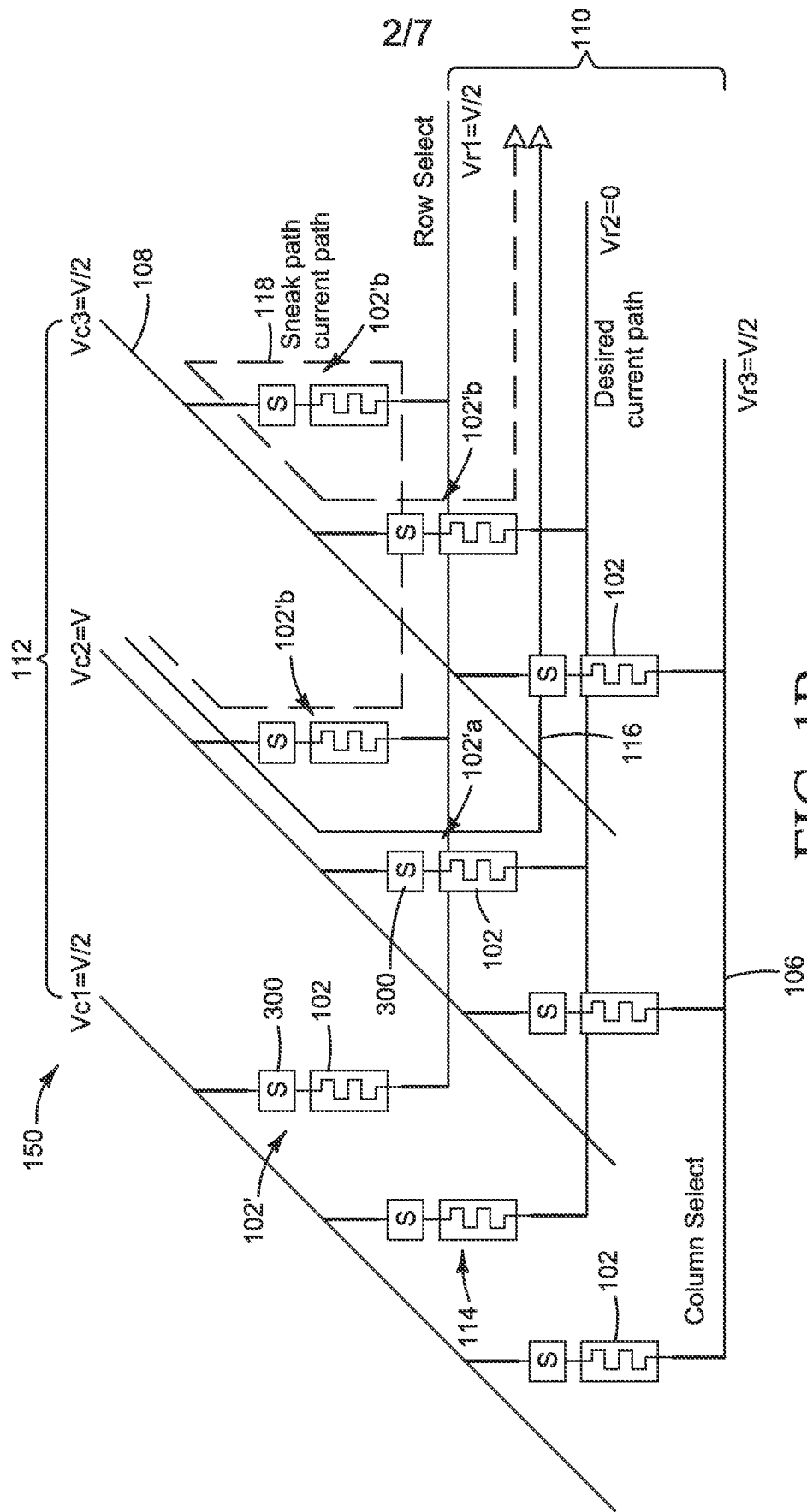


FIG. 1B

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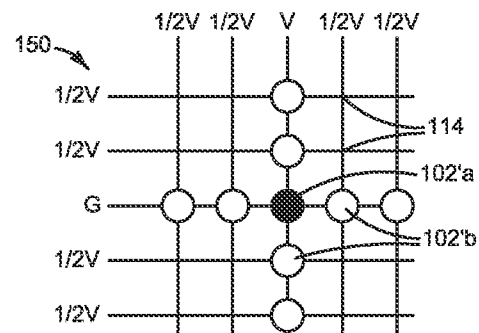


FIG. 2

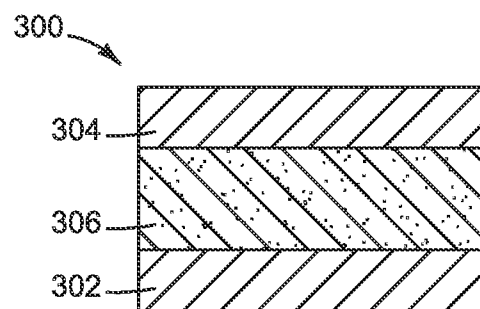


FIG. 3

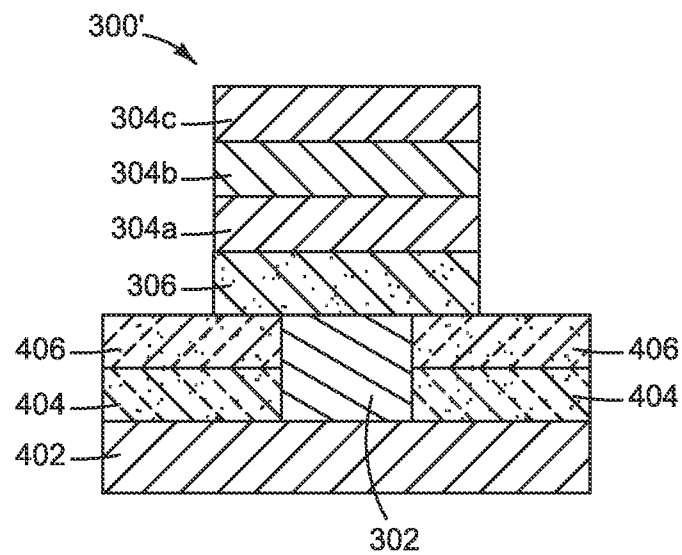


FIG. 4

FIG. 5A

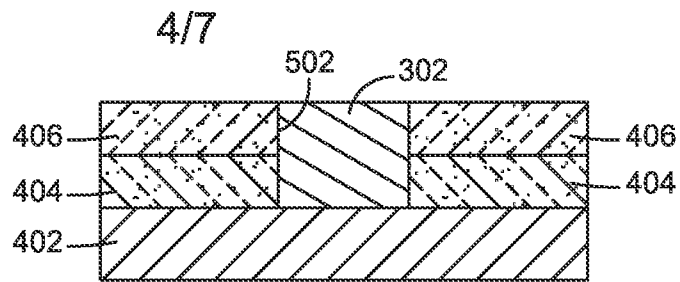


FIG. 5B

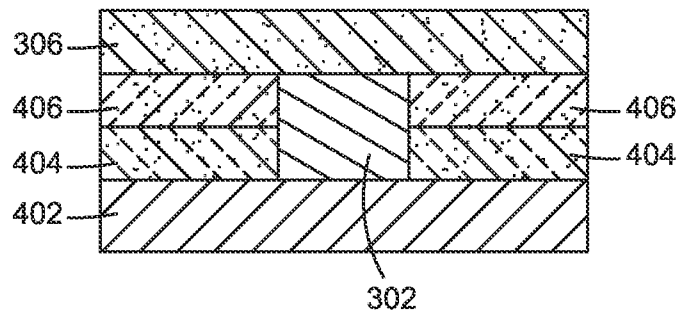


FIG. 5C

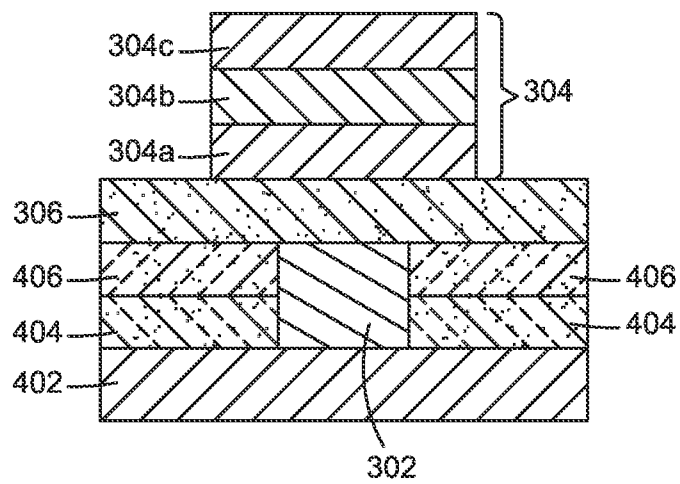
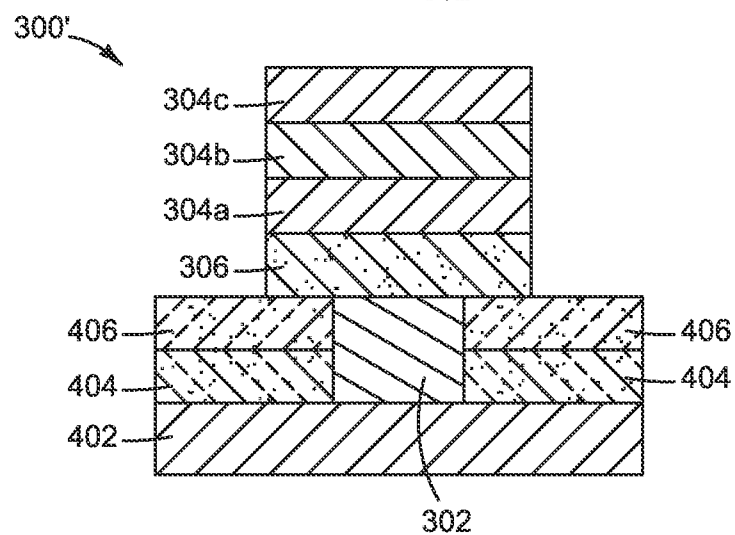


FIG. 5D



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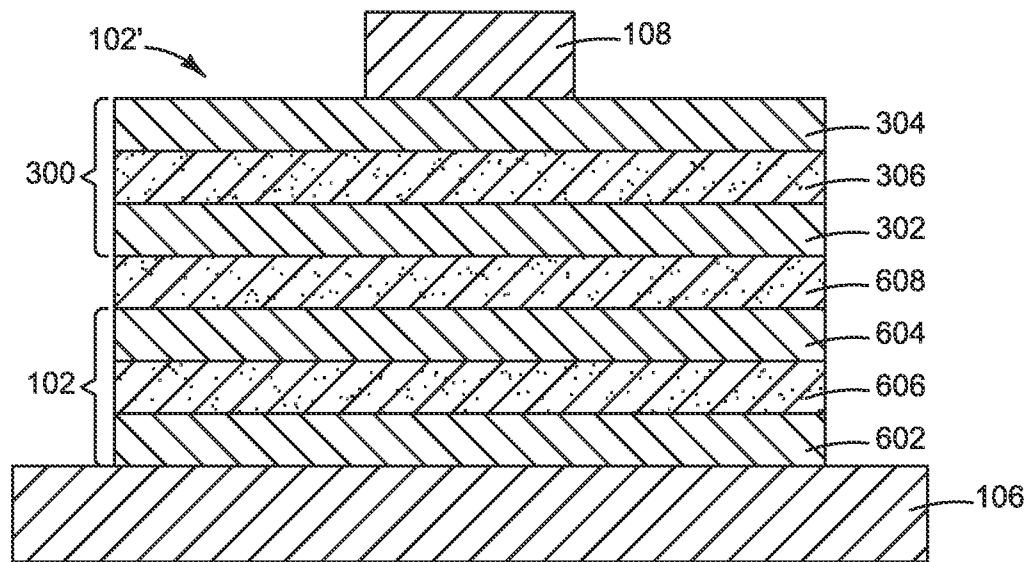


FIG. 6

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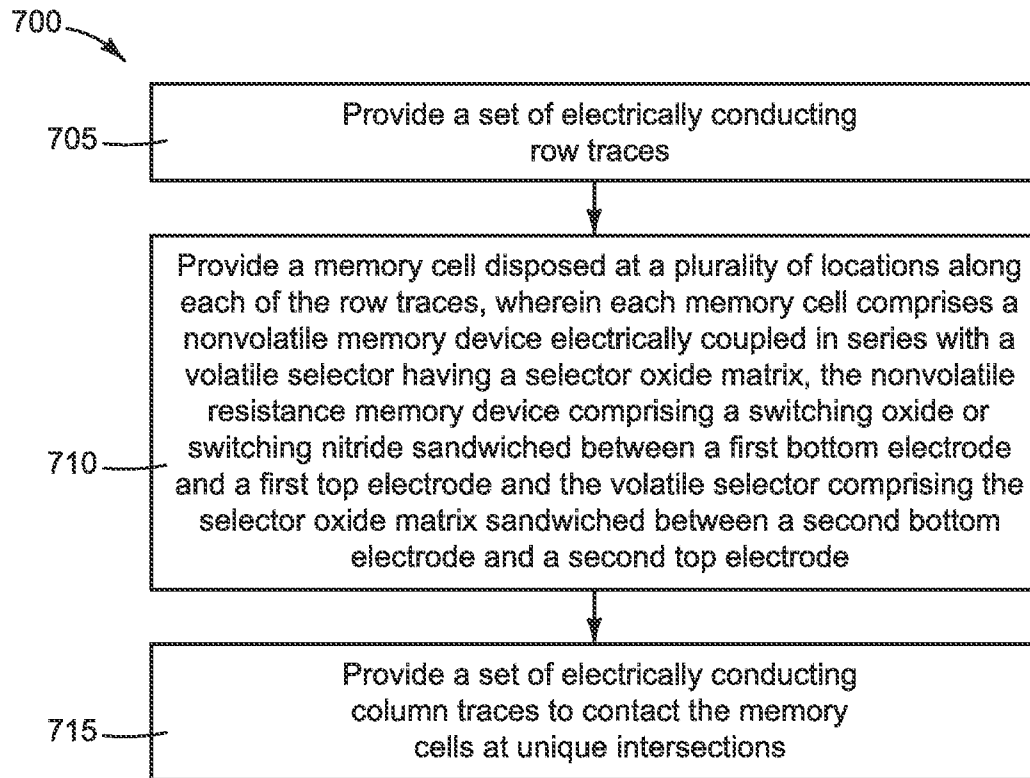


FIG. 7

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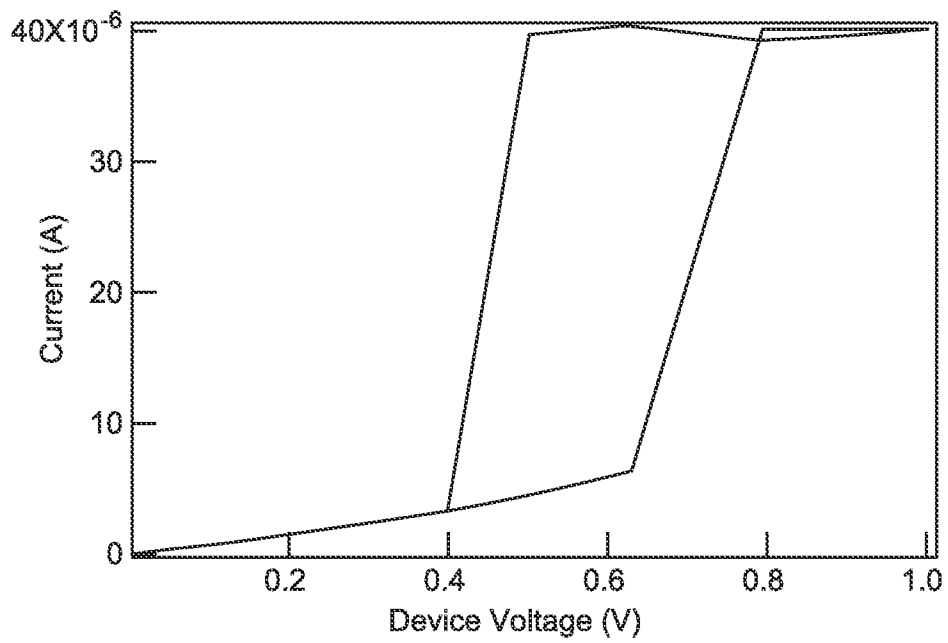


FIG. 8A

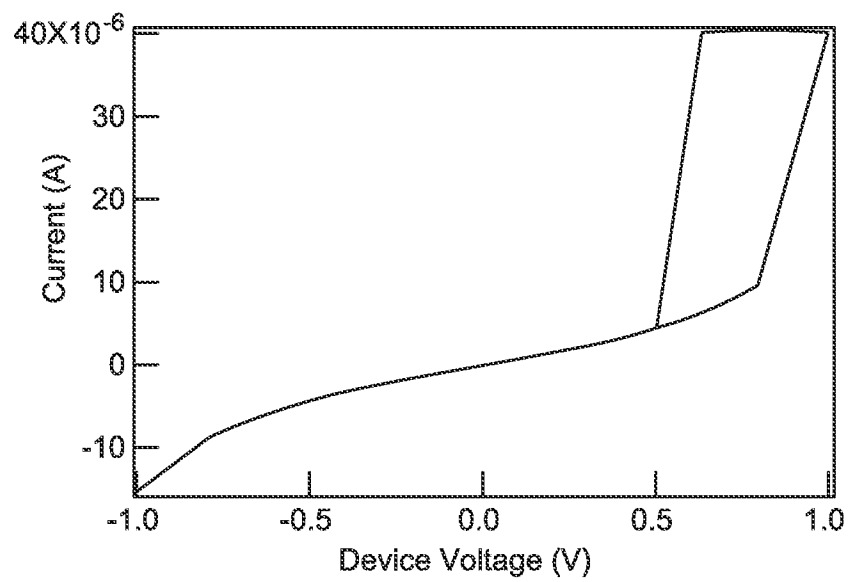


FIG. 8B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/030370**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G11C 13/00; H01L 29/92; G11C 11/34; G11C 16/04; G11C 11/21; H01L 21/02; G11C 19/08Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: volatile, selector, nonvolatile, resistance, memory, electrode, oxide, silicon, dioxide, copper, silver, memristor**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0135925 A1 (ROY E. SCHEUERLEIN) 30 May 2013 See paragraphs [0004], [0017], [0032], [0038]-[0039], [0085]; and figures 3-4b, 8-9.	1-5, 7-10, 12-13, 15
A		6, 11, 14
Y	US 2014-0169062 A1 (MANKOO LEE et al.) 19 June 2014 See paragraph [0059]; and figure 1A.	1-5, 7-10, 12-13, 15
A	US 2011-0204474 A1 (FRANZ KREUPL et al.) 25 August 2011 See paragraphs [0045]-[0046]; and figure 3A.	1-15
A	US 2006-0126395 A1 (SHIH-HUNG CHEN et al.) 15 June 2006 See paragraphs [0036]-[0039]; and figure 2.	1-15
A	US 2004-0170040 A1 (DARRELL RINERSON et al.) 02 September 2004 See paragraphs [0039]-[0048]; and figure 2.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 February 2016 (23.02.2016)

Date of mailing of the international search report

24 February 2016 (24.02.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/030370

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