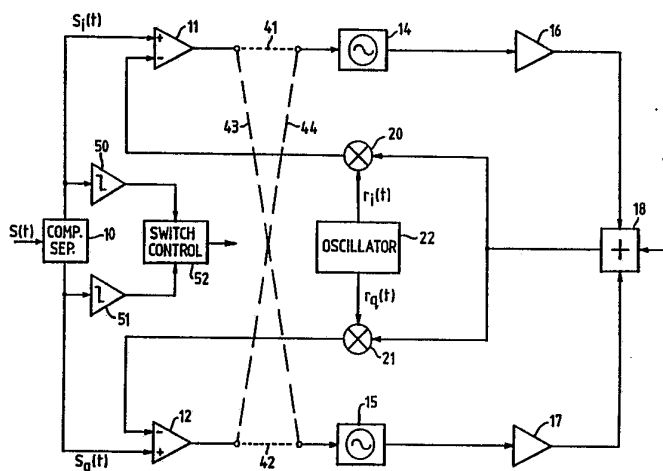




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H03C 1/06, H03D 3/24 H03F 1/32, H03L 7/07	A1	(11) International Publication Number: WO 93/23921 (43) International Publication Date: 25 November 1993 (25.11.93)
(21) International Application Number: PCT/GB93/00954 (22) International Filing Date: 10 May 1993 (10.05.93) (30) Priority data: 9209982.9 8 May 1992 (08.05.92) GB (71) Applicant (for all designated States except US): UNIVERSITY OF BRISTOL [GB/GB]; Senate House, Tyndall Avenue, Bristol BS8 1TH (GB). (72) Inventors; and (75) Inventors/Applicants (for US only) : BATEMAN, Andrew [GB/GB]; Roseacre, Crowe Hill, Limpley Stoke, Bath BA3 6HX (GB). CHAN, Kam, Yuen [GB/GB]; 16 Pembroke Road, Clifton, Bristol BS8 3AX (GB).		(74) Agent: DAVIS, Norman, Norbridge; Patents Department, British Technology Group Limited, 101 Newington Causeway, London SE1 6BU (GB). (81) Designated States: CA, JP, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: METHOD AND APPARATUS FOR AMPLIFYING, MODULATING AND DEMODULATING

**(57) Abstract**

A highly efficient linear amplifier and/or modulator and demodulator comprising first and second feedback loops is provided. Each loop processes a component of the input signal and the component signals are recombined at, for example, a summing junction (18). The feedback signals for each loop are dependent upon the output signal and are in phase quadrature. The input signal is separated into I and Q signals, which are also in phase quadrature, by a component separator (10).

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METHOD AND APPARATUS FOR AMPLIFYING,MODULATING AND DEMODULATING

The present invention relates to method and circuits for processing components of an input signal to provide a highly efficient linear amplifier and/or modulator or a demodulator.

A LINC amplifier has been proposed (see D.C. Cox, "Linear Amplification Using Non-Linear Components", IEEE Transactions on Communications, Vol. COM-22, 1974, pages 1942 to 1945) in which a modulating signal is split into two phase modulated components with constant envelopes which can be amplified separately using highly non-linear but power efficient amplifiers. Combining the two output signals yields the desired linearly amplified signal. With a LINC amplifier the potential for dc to RF conversion efficiency can approach 100%, assuming ideal matching amplifiers. However, in practical LINC amplifiers, the suppression of broadband phase modulation relies on a very tight tolerance on the gain and phase match between the two paths. A gain error of 0.01 dB and a phase error of 0.1° give a component suppression of only 54 dB. Such a tolerance is impossible to achieve in an open loop system where much greater gain and phase variations can occur with changes in operating frequency, output power and temperature, and the ageing of components.

It is an object of this invention to provide a linear amplifier/modulator which does not suffer significantly from these problems.

From GB 2073516 an arrangement for amplifying a previously modulated carrier signal using two phase locked loops is already known and in which phase feedback and phase comparators are used. In one embodiment the feedback signals are taken from a point before the final summing circuit. In practice the summing circuit will be imperfect and any phase errors introduced by the summing circuit will degrade the performance of the system. The input signal is at or near the same frequency as the output signal and where the output is to be at radio frequencies (RF) implementation

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of the summing circuits 14 and 15 is, in practice, complicated. Such an arrangement could not receive a baseband signal and incorporate modulation of that signal within the phase locked loops.

In a second embodiment of GB 2073516, the feedback signal is
5 taken from a point after the final summing circuit. However comparisons with the input signal are made in terms of the amplitude and phase and, when the input is at RF, such a system requires accurate RF envelope detection and subtraction and a wide dynamic range RF phase detector. Such devices are difficult to
10 construct.

From US 5105168 an arrangement for a vector locked loop for modulation of an input signal is already known. US 5105168 incorporates a mixer in the feedback path so that comparisons may be made at or near the input signal frequency, which may be a
15 baseband signal with an output signal at RF. However the realisation of envelope detectors for such an arrangement presents problems as they require subsequent filtering of the carrier components, which introduces an unacceptable amount of time delay. Additional significant time delays are introduced by the phase
20 detector which is required to generate the difference component and the filter which is required to remove the sum component.

It is another object of the invention to provide an amplifier/modulator which may use the Cartesian components of an input signal. The advantage of the a Cartesian signal is that a
25 representation of the signal can be produced with a low sampling rate, especially when derived by a digital signal processor (DSP).

It is a further object of the invention to provide an amplifier/modulator which incorporates modulation, amplification and summation within a feedback loop, so that there is compensation
30 for any deficiencies in the system.

According to one aspect of the invention there is provided apparatus for processing components of an input signal to provide a processed output signal, comprising

first and second feedback control loops for generating

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respective components for use in generating a processed output signal and ensuring that the components are correctly in phase for this purpose,

each loop comprising means for generating a loop output signal
5 having a frequency or phase which is variable in response to a control signal, and which forms one of the components of the processed output signal, or from which one such component is derived, and a comparator for generating the control signal, and

means for combining the loop output signals in deriving a
10 resultant signal, and

means for providing first and second feedback signals, dependent on the resultant signal and in phase quadrature with one another,

the feedback signals being applied to one input of the
15 comparators of the first and second loops, respectively, and another input of each comparator being coupled to receive a reference signal.

According to a second aspect of the invention there is provided a method of processing the components of an input signal
20 to provide a processed output signal by using first and second feedback control loops to generate respective components used in generating the processed output signal and ensuring that the components are correct in phase for this purpose, comprising

generating a loop output signal for each loop having a
25 frequency which is variable in response to a respective control signal and which forms one of the components of the processed output signal, or from which one such component is derived,

combining the loop output signals in deriving a resultant signal,

30 generating feedback signals from the resultant signal, one for each loop, and

comparing each feedback signal with a respective reference signal to provide the respective control signals.

Processing carried out by the invention may, for example, be

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modulation and/or amplification, or demodulation.

The feedback signals may be provided by mixing the said resultant signal with respective quadrature signals from an oscillator.

5 Where modulation is to be carried out, the Cartesian components of the input signals may be applied as the reference signals and the said resultant signal is the modulated output signal in which a signal at the frequency of the oscillator is modulated by the input signal, that is frequency translation of the
10 input signal to the frequency of the oscillator occurs.

For amplification, each loop contains an amplifier to amplify the loop output signals before they are combined, and if any amplification without modulation is required, then the oscillator output frequency is set to zero.

15 To achieve demodulation the loop output signals are combined with a modulated signal in such a way that frequency translated signals derived from the resultant signal indicate any frequency or phase deviations of the loop output signals from respective components of the modulated signal. Also a zero magnitude signal
20 is applied as the respective reference signals, for example by grounding one input terminal of each comparator, and the loop output signals are demodulated using the respective quadrature components of the oscillator output signals to provide components of the output signal which can then be combined in a known way to
25 derive a signal representative of the modulation of the modulated signal.

One of the main advantages of the circuit is that it allows components of an output signal, or a signal from which such components can be derived, to be generated and combined within a
30 control loop so that problems of errors in combination are significantly reduced.

Other advantages which may be achieved include maximising the efficiency of the modulator/amplifier particularly when used in a transmitter, the ability to construct circuits according to the

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invention with readily available, low cost, low tolerance components, and minimising or eliminating the use of complex digital signal processing.

The demodulator also allows a variable strength input signal, such as might be received by a radio system, to be converted to two phase modulated components of constant amplitude which are easier to process.

It is believed that the input and/or output signals may be represented by other component systems than Cartesian components. For example polar components or non-rectangular components may possibly be used.

Embodiments of the invention will now be described by reference to the following drawings, in which:-

Figure 1 is a block diagram of an amplifier/modulator embodying the invention,

Figure 2 is a block diagram of a demodulator embodying the invention, and

Figure 3 is a diagram showing regions of stability for Figure 1,

Figure 4 is a block diagram of another amplifier/modulator embodying the invention,

Figure 5 is a block diagram of a third amplifier/modulator embodying the invention,

Figure 6 is a block diagram of an amplifier embodying the invention

In Figure 1, an input signal $s(t)$ having for example amplitude or phase variations, or both, is separated by a known component separator 10 into two component signals which vary in amplitude and phase but are in phase quadrature. These two components, $s_i(t)$ and $s_q(t)$ are the Cartesian components (I and Q) of the input signal and each component signal is passed to one of two feedback loops. As an alternative the input signal may be supplied in the form of separate I and Q signals. The first element in each loop is a comparator (11 and 12) and each component signal is passed to the

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inverting input of the comparator. The output signal of this comparator is passed, in this example, by way of connections 41 and 42 (which can be selected from connections 41 to 44 as is described below) to control the frequency of a voltage controlled oscillator (VCO) (14 and 15), and the resulting output signal is amplified by an a non-linear radio-frequency amplifier (16 and 17). The output signals from the amplifiers are combined, by a summing circuit 18 to produce, as is explained below, a frequency translated amplified version of the input signal $s(t)$, at the frequency of the oscillator 22.

Feedback control is created for each loop by taking the output of the summing circuit 18, demodulating that signal with a signal $r_i(t)$ and $r_q(t)$ at a mixer (20 and 21) and passing the resulting feedback signal to the non-inverting input of the comparator of that loop. The signals $r_i(t)$ and $r_q(t)$ supplied to each mixer are the quadrature Cartesian components of a signal $r(t)$ from an oscillator 22, and the frequency difference between the modulated signal at the output of the summing circuit 18 and the input to the component separator 10 equals the frequency of the oscillator 22.

In operation, the output of the mixer 20, for example, is compared by the comparator 11 with the signal $s_i(t)$ and any difference, assuming the direct connections 41 and 42 are made, controls the frequencies generated by the VCO 14 so that its output signal is such that when summed with the output of the VCO 15 and demodulated by the mixer 20, it forms a replica of $s_i(t)$. In a similar way the output signal of the VCO 15 when summed with the output of the VCO 14 and demodulated by the mixer 21 is a replica of $s_q(t)$. Thus when the output signals of the VCOs 14 and 15 are combined by the summing circuit 18 they provide a signal at the reference frequency which is a frequency translated amplified version of $s(t)$, assuming that the demodulation processes are exact (perfect gain and phase matching) and that the loop gain is infinite giving feedback control loops with error signals of zero.

Since the amplitudes of the outputs of the VCOs are inherently

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constant the amplifiers 16 and 17 can be non-linear, for example Class C, so that high efficiency amplification and modulation can be achieved. By providing feedback control the frequency and phase of each signal from the VCOs 14 and 15 is controlled to ensure that
5 gain and amplitude matching is as required in combining these signals as components of the required output signal from the summing circuit 18. Deviations in gain as well as phase are corrected by phase variations in the signals combined caused by the action of feedback.

10 Where only modulation is required the amplifiers 16 and 17 can be omitted or of unity gain. Where only amplification is required, without frequency translation, then the frequency of the oscillator 22 is set to zero. For example the oscillator 22 and the mixers 20 and 21 may be omitted when the signals from the
15 summing circuit 18 to the comparators 11 and 12 are arranged to be in phase quadrature, with the comparator 12 receiving a signal with a 90° phase shift, as described below in relation to Figure 6.

The modulator of Figure 1 can be viewed as a combination of two analogue phase locked loops and a basic understanding of the
20 factors affecting system performance can be drawn from conventional phase locked loop theory. Loop gain will in practice be limited by stability of the feedback process, and loop capture range will dictate the ultimate modulation bandwidth.

Figure 3 is a diagram in which a vector 45 represents the sine
25 signal $r_q(t)$ from the oscillator 22 and a vector 46 represents the cosine signal $r_i(t)$. It can be shown mathematically that, if the connections 41 and 42 are as shown in Figure 1 without any signal inversion, the stable region of lock for the combined loop system covers the semi-circle 49. This in effect limits the application
30 of the modulator to formats such as full carrier amplitude modulation and amplitude shift keying.

A limited performance in one quadrant does not provide a universal modulator and stable operation in all four quadrants can be achieved if the sign of the feedback components is controlled as

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a function of the sign of the signals $s_i(t)$ and $s_q(t)$.

In order to determine the sign of $s_i(t)$ and $s_q(t)$, the two outputs of the component separator 10 are coupled to comparators 50 and 51, respectively, with each comparator providing a logic 1 for a positive input and a logic 0 for a negative input. These logic signals are applied to a switch control circuit 53 which controls the connections 41 to 43 and whether inversion is to occur within these connections. Such connections may be provided by known circuits. A number of connection schemes are suitable for four-quadrant stable operation and one is given in the following table, by way of example, where a primed connection designation, for example 41', indicates signal inversion and designations without primes indicate no inversion.

	$s_i(t)$	$s_q(t)$	To VCO 14	To VCO 15
15	1	1	44	43'
	1	0	41	42
	0	1	41'	42'
20	0	0	44'	43

It may be shown, mathematically, that the stable region of lock for the combined loop system covers more than quadrant 48 and extends further to include the area up to line 48a.

Figure 2 shows a demodulator according to the invention, in which an input signal to be demodulated is received by a summing circuit 25 from a source in this example illustrated by an antenna 26 but which could be any modulated signal source. When VCOs 27 and 28 are operating at exactly the frequencies and phases of components of the input signal, the input signal is cancelled in the summing circuit 25. At other times a small error signal reaches demodulators 32 and 33 where Cartesian components of the error signal are generated using quadrature reference signals $r_i(t)$

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and $r_q(t)$ from an oscillator 34 at the frequency which carries the modulation to be detected (that is the carrier frequency). These Cartesian components, which should be zero when perfect cancellation occurs in the summing circuit 25, are compared with a
5 zero magnitude signal in comparators 35 and 36 obtained by grounding the non-inverting inputs of these comparators, and the outputs obtained control the frequencies of the VCOs 27 and 28. As a result the output frequencies of these VCOs are replicas of the components of the input signal to the demodulator and are down
10 converted by demodulators 37 and 38 using the respective quadrature outputs of the oscillator 34 to provide demodulated components of the modulation of the carrier signal. These components can be combined in a known way to provide a frequency translated replica of a radio-frequency input signal at the antenna 26.

15 Problems of stability also arise with the demodulation circuit and can be overcome by the use of the same switched connections as those of Figure 1 controlled by the signs of the outputs of the demodulators 32 and 33.

Amplifiers 29 and 30 are shown in Figure 2 at the outputs of
20 the VCOs 27 and 28 and are useful in correcting levels. To this end the gain of these amplifiers may be greater or less than unity, and in some circumstances they may not be required.

Figures 4 and 5 show embodiments of the invention which maintain stability in all four quadrants. The input signal is
25 confined to the quadrant where the amplifier/modulator is stable and the necessary phase shift is added back to the output signal.

In figure 4 an input signal $Ae^{j\alpha}$, having for example amplitude or phase variations, or both, is separated by a known component separator 61 in a manner as described in relation to figure 1.
30 Alternatively the input signal may be supplied as separate I and Q signals, $\cos\alpha$ and $\sin\alpha$. Each component signal is passed to a phase shifter 62 which shifts the phase of each signal by a factor β , which is the difference in phase between the input and the output signals. The absolute value of each phase shifted input component

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signal is taken by the 'rectifier' circuits 63 and 64, leaving a signal containing mainly amplitude information. This ensures that each component signal is kept in a region for which the combined system is stable, as illustrated by quadrant 48 of figure 3 and described above. The output signals of the rectifiers are passed to the inverting inputs of the comparators 65, 66 in the latter after inversion. The output signal of the comparator controls the frequency of a VCO 67, 68 via switchable connections 69, 70, 71 and 72. The resulting output signal may be amplified by a non-linear RF amplifier 73, 74. As before these amplifiers may be omitted or of unity gain where only modulation is required. The outputs of the two amplifiers are combined by summing circuit 75 to produce a frequency translated amplified version of the input signal.

Feedback control is provided for each loop in a similar manner to that used in the embodiment illustrated by figure 1, by demodulating the output of the summing circuit 75, $Be^{j(\beta+\omega t)}$ with quadrature signals $\cos(\omega t)$, $\sin(\omega t)$ produced by the oscillator 76 at the mixers 77, 78. The phase of each input component is added back into the feedback loop by shifting the demodulated component of the output signal with the phase of the component of the input signal at a phase shifter 79; thus the signal from the mixer 77, 78 are shifted in phase by a factor $\beta-\alpha$. The feedback loop is completed by passing the resulting signal to the non-inverting input of the comparator. The frequency difference between the output signal and the input signal is that of the frequency of the oscillator 76.

Figure 5 is a simplified version of the amplifier/modulator shown in figure 4. An input signal $Ae^{j\alpha}$, of the type described in relation to figure 4 is separated by a known component separator 85 in a manner as described in relation to figure 1. The absolute value of the input signal, ie the amplitude information, is selected by a 'rectifier' circuit 86 and this value is passed into the non-inverting input of a comparator 88. The phase component of each signal is selected by circuit 87 which limits each component signal to unity, with phase information. The non-inverting input

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of a comparator 89 is grounded and thus the output of the comparator mirrors the input of the non-inverting input. The output signal of the comparator 88, 89 controls the frequency of a VCO 90. 91 via switchable connections 92, 93, 94 and 95. The
5 resulting output signal may be amplified by a non-linear RF amplifier 96, 97. As before these amplifiers may be omitted or of unit gain where only modulation is required. The outputs of the two amplifiers are combined by summing circuit 98 to produce a frequency translated amplified version of the input signal at the
10 frequency of the oscillator 99.

Feedback control is provided for each loop in a similar manner so that used in the embodiment illustrated by figure 4, by demodulating the output of the summing circuit 98, $Be^{j(\beta+\omega t)}$ with quadrature signals $\cos(\omega t)$, $\sin(\omega t)$ produced by the oscillator 99
15 at mixers 100, 101. The phase of each input component is added back into each feedback loop by shifting the demodulated component of the output signal with the phase of each component of the input signal at a phase shifter 102. The feedback loop is completed by passing the resulting signal to the non-inverting input of the
20 comparator. The frequency difference between the output signal and the input signal is that of the frequency of the oscillator 98.

Although the input to the loops is constrained to be within the stable region of the system, VCO switching may be required to reduce impulse noise generated by the VCO. When the envelope of
25 the input signal crosses zero (hereafter 'zero crossing') the phase of the input signal changes by 180° and this can be illustrated by plotting a vector of the input signal onto figure 3. When the envelope crosses zero the vector will cross from one quadrant to the diagonally opposite quadrant and will pass through the origin.
30 The output of the VCOs, when summed at the summing junction, produces a similar signal to that of the input and thus when the input phase changes by 180° the output will also change by 180° . Since the output is created by summing the output of the two VCOs, it can be shown that the output of each VCO needs to change by 180°

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as well. The VOCs introduce a finite delay into the system and also generate an impulse noise. Figures 4 and 5 include a phase detector 105 and a differentiator 106 which in combination produce a signal when the phase changes by 180° . The output of the differentiator is coupled to the non-inverting input of a comparator 107, the inverting input of which is coupled to a reference signal. When the output of the differentiator crosses a threshold, which is that of the reference signal, the input to the VOCs are switched by the switching connections, (69, 70, 71 and 72 in figure 4 and 92, 93, 94 and 95 in figure 5).

The embodiment illustrated in figure 1 will also generate impulse noise when zero crossing occurs. For clarity the phase detector, differentiator, comparator and further switchable connections have been omitted. Alternatively the switch controls may take into account zero crossing and switch accordingly.

If the system is to amplify without modulation (if the oscillator is set near to or at zero) an alternative arrangement is needed to create suitable phase quadrature feedback signals. Figure 6 is an illustration of a modified version of the embodiment of the circuit shown in figure 1, which works substantially as described above. Similar arrangements may be applied to the embodiments illustrated in figures 4 and 5. An input signal of the type described in relation to figure 1 is separated by a component separator, as described above. The component signals are passed to the inverting input of the comparator 111, 112, the output of which is connected via switchable connections (as described in relation to figure 1) to a VCO 113, 114. The VCO generates at its output two signals I and Q, which are in phase quadrature with each other. The Q signal of each VCO (113, 114) is summed by summing circuit 115. One output of the summing junction forms the feedback loop and is passed to the non-inverting input of the comparator 112. The I signal of each VCO (113, 114) is summed by summing circuit 116. One output of the summing junction forms the feedback loop and is passed to the non-inverting input of the comparator

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111. The other outputs of the summing junctions 115, 116 are passed to amplifiers 117 and 118 and the amplified signals are summed by summing junction 119. Switch control for the VCOs may be provided in the same manner as described in relation to figure 1 and zero crossing switching may also be applied if desired.

Some alternative arrangements relating to figure 6 will now be mentioned. In the first, the amplifiers 117 and 118, and the summing junction 119 are omitted, respective substitute amplifiers are connected in the I signal paths between the VCOs 113 and 114, and the summing junction 116, and the output signal is taken from the summing junction 116. The substitute amplifiers may instead be in corresponding positions in the Q signal paths. In both cases an attenuator or a further amplifier is required to ensure that the two feedback signals are at corresponding levels at the comparators 111 and 112. Substitute amplifiers may be used in both I and Q paths at the VCO outputs. Such arrangements have the advantage that the substitute amplifiers are included in the feedback loop before summation to provide the output signal. The amplifiers 117 and 118 and/or the summing junction 119 may be used in addition to the substitute amplifiers in any of the substitute amplifier arrangements.

It will be realised that the invention can be put into operation in many other ways than those specifically described. For example the VCOs may be any form of frequency generator having an output signal which can be controlled using a control signal, for example some forms of unstable amplifier or direct digital synthesizers.

The switching matrices of figures 1, 4, 5 and 6 may in some situations be replaced by permanent connections which give a stable arrangement and prevent impulse noise on zero crossing.

Since Cartesian components of an input signal, and some alternative kinds of components, are phase modulated, the invention can handle any other types of modulation in addition to those mentioned.

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CLAIMS

1. Apparatus for processing components of an input signal to provide a processed output signal, comprising
first and second feedback control loops for generating
5 respective components for use in generating a processed output signal and ensuring that the components are correctly in phase for this purpose,
each loop comprising means for generating a loop output signal having a frequency or phase which is variable in response to a
10 control signal, and which forms one of the components of the processed output signal, or from which one such component is derived, and a comparator for generating the control signal, and
means for combining the loop output signals in deriving a resultant signal, and
15 means for providing first and second feedback signals, dependent on the resultant signal and in phase quadrature with one another,
the feedback signals being applied to one input of the comparators of the first and second loops, respectively, and
20 another input of each comparator being coupled to receive a reference signal.
2. Apparatus according to Claim 1 wherein the means for providing the feedback signals includes
an oscillator having quadrature output signals, and
25 first and second mixers, one for each loop, for generating the first and second feedback signals, the mixers both being coupled to receive the said resultant signal as one input, and to receive respective quadrature output signals from the oscillator as another input.
- 30 3. Apparatus according to Claim 1 or 2 including an amplifier for each loop connected between the means for generating the loop output signal for that loop and a respective input of the combining means.
4. Apparatus according to Claim 2 or Claim 3, insofar as

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dependent on Claim 2, arranged as a modulator including

first and second input terminals for the application of first and second Cartesian components of an input signal connected as the reference signals for the comparators of the first and second loops, respectively, and

an output terminal of the combining means,

whereby a modulated signal appears at the said output terminal which is the input signal frequency translated by the oscillator frequency.

5. Apparatus according to Claim 4 including a component separator for receiving a modulated input signal and deriving Cartesian components thereof for application to the said first and second input terminals.

6. Apparatus according to Claim 3 or Claim 4 or 5 insofar as dependent on Claim 3 for amplifying a signal, wherein the oscillator output frequency is zero.

7. Apparatus according to Claim 1 arranged as an amplifier wherein the means for providing the feedback signals comprises means for deriving quadrature-phase signals from the said resultant signal as the first and second feedback signals.

8. Apparatus according to Claim 2 or 3 arranged as a demodulator wherein

the combining means has first, second and third input terminals and an output terminal and is so constructed that if components nominally equal to the components of a signal to be processed are applied at the first and second input terminals, respectively, and the signal to be processed is applied at the third input terminal the said resultant signal appears at the output terminal and is indicative by its respective components of any frequency or phase deviations of the components applied to the first and second input terminals,

means are provided for applying a zero magnitude signal as the said amplitude-reference signal to the comparators of both loops, and

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a further mixer is provided for each loop for demodulating the loop output signal to derive one of the components of the said processed output signal representative of modulation carried by a signal applied to the third input terminal of the combining means.

- 5 9. Apparatus according to Claim 8 including means for combining the outputs of the further mixers to derive a signal representative of modulation carried by a signal applied to the third input terminal of the combining means.
- 10 10. Apparatus according to any preceding claim including control means for controlling respective connections within and/or between components for the two feedback control loops both in respect of determining the said connections and also whether the said connections include signal inversion, the control means operating in accordance with signal characteristics to ensure that stable operation occurs.
- 15 11. Apparatus according to Claim 9 wherein the signal characteristics are the signs of one input signal of each comparator, and the respective connections are connections between the comparators and the means for generating loop output signals.
- 20 12. Apparatus according to any preceding claim wherein the reference signals are Cartesian components of the input signals, including phase control means for controlling the phases of the reference signals to ensure stable operation of the apparatus.
- 25 13. Apparatus according to claim 12 wherein the phase control means comprises a first phase shifter for subtracting the phase of the resultant signal from that of both the reference signals before application to the comparators, and a second phase shifter for subtracting the phase of the input signal from that of both the first and second feedback signals before application to the comparators.
- 30 14. Apparatus according to claim 13 including rectifying means for taking the modulus of each output of the first phase shifter before application to the comparators.
- 35 15. Apparatus according to claim 12 wherein the phase control means comprises

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means for providing a signal representative of the amplitude of the reference signals as one reference signal means for providing a constant signal as to other reference signal,

5 a phase shifter for shifting the phases of the first and second feedback signals controlled by first and second phase control signals, respectively, and

means for providing signals representative of the phases of the reference signals as the first and second phase control signals.

16. Apparatus for processing components of an input signal to provide a processed output signal, comprising

10 first and second feedback control loops for generating respective components for use in generating a processed output signal and ensuring that the components are correctly in phase for this purpose,

15 each loop comprising means for generating a loop output signal having a frequency or phase which is variable in response to a control signal, and which forms one of the components of the processed output signal, or from which one such component is derived, and a comparator for generating the control signal, and

20 means for combining the loop output signals in deriving a resultant signal, and

means for providing first and second feedback signals, representative of the resultant signal,

25 the feedback signals being applied to one input of the comparators of the first and second loops, respectively, and another input of each comparator being coupled to receive a reference signal,

detection means for detecting zero crossings in the input signal or the envelope thereof, and

30 noise-reduction switching means for changing over the means for generating the loop output signals between loops when a said zero crossing occurs as indicated by the detector means.

17. Apparatus according to any of claims 1 to 15 including detection means for detecting zero crossings in the input signal or

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the envelope thereof, and

noise-reduction switching means for changing over the means for generating the loop output signals between loops when a said zero crossing occurs as indicated by the detector means.

- 5 18. Apparatus according to claim 1 wherein the reference signals are Cartesian components of an input signal wherein each means for generating a loop output signal generates Cartesian components of the loop output signal, and the apparatus includes

10 first and second means for combining corresponding Cartesian components from the said means for generating, respectively, to provide the first and second feedback signals, and third combining means for combining the output of the first and second combining means to provide the resultant signal.

- 15 19. Apparatus according to claim 18 including first and second amplifiers connected between the first combining means and the third combining means, and the second combining means and the second combining means, respectively.

- 20 20. A method of processing the components of an input signal to provide a processed output signal by using first and second feedback control loops to generate respective components used in generating the processed output signal and ensuring that the components are correct in phase for this purpose, comprising

25 generating a loop output signal for each loop having a frequency which is variable in response to a respective control signal and which forms one of the components of the processed output signal, or from which one such component is derived,

combining the loop output signals in deriving a resultant signal,

30 generating feedback signals from the resultant signal, one for each loop, and

comparing each feedback signal with a respective reference signal to provide the respective control signals.

21. A method according to Claim 20 wherein generating the feedback signals includes mixing the resultant signal with

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respective quadrature signals to provide the feedback signals.

22. A modulation method according to Claim 20 or 21 wherein
the components of the input signal are Cartesian components,
the Cartesian components are used as the respective reference
5 signals, and

the said resultant signal forms the processed output signal.

23. A method according to Claim 20 including amplifying the loop
output signals before combining them.

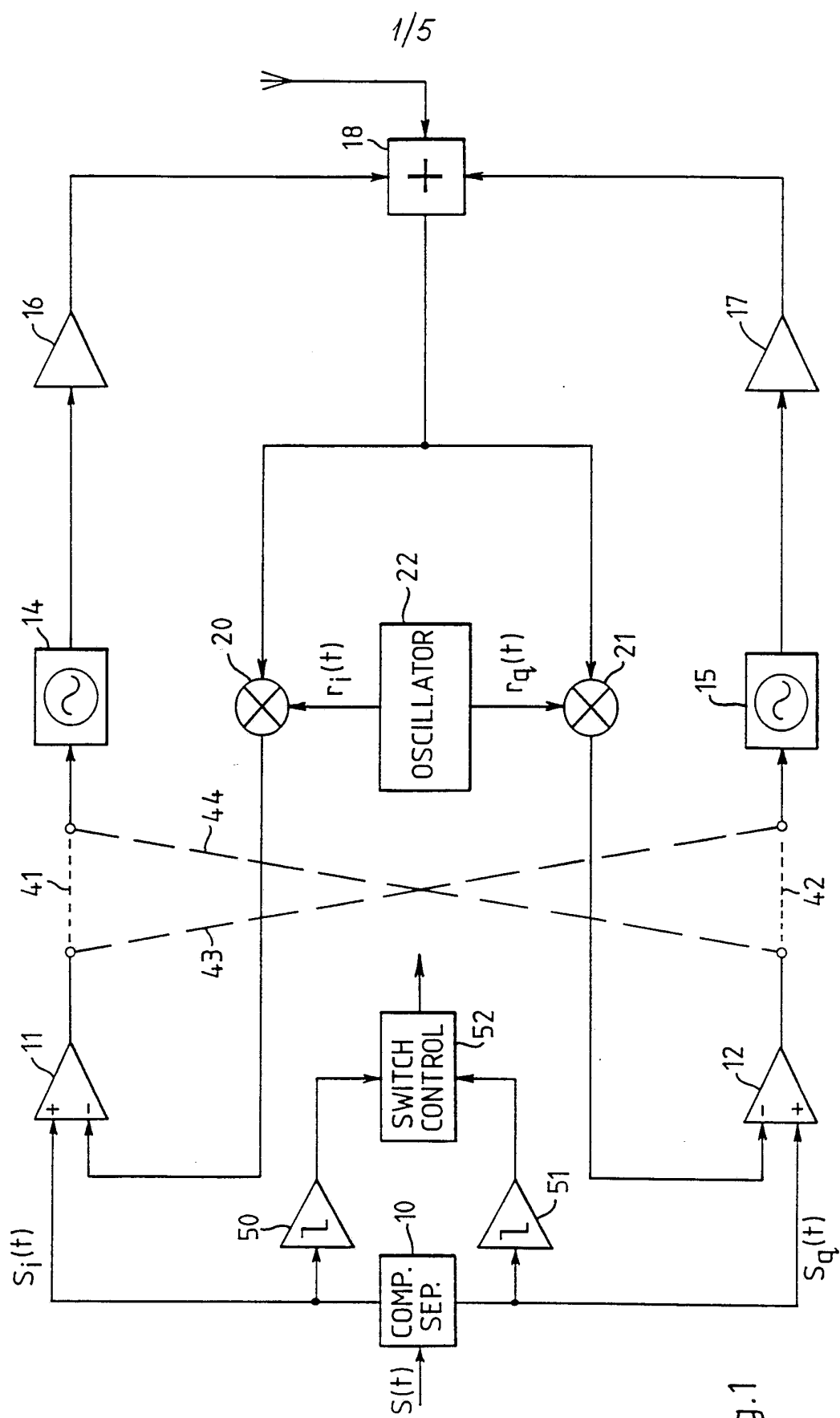
24. A demodulator method according to Claim 21 comprising
10 combining the loop output signals with a modulated signal in
such a way that the feedback signals derived from the resultant
signal indicate any frequency or phase deviations of the loop
output signals from respective components of the modulated signal,
applying a zero magnitude signal as the respective reference
15 signals, and

demodulating each loop output signal using a respective one of
the quadrature phase signals to provide the components of the
processed output signal.

25. An amplifying method according to Claim 20 wherein quadrature
20 phase versions of the said resultant signal form the feedback
signals.

26. Apparatus for processing Cartesian components of an input
signal to provide a processed output signal substantially as
hereinbefore described with reference to Figure 1 or Figure 2 of
25 the accompanying drawings.

27. A method of processing Cartesian components of an input
signal to provide a processed output signal substantially as
hereinbefore described with reference to Figure 1 or Figure 2 of
the accompanying
30 drawings.



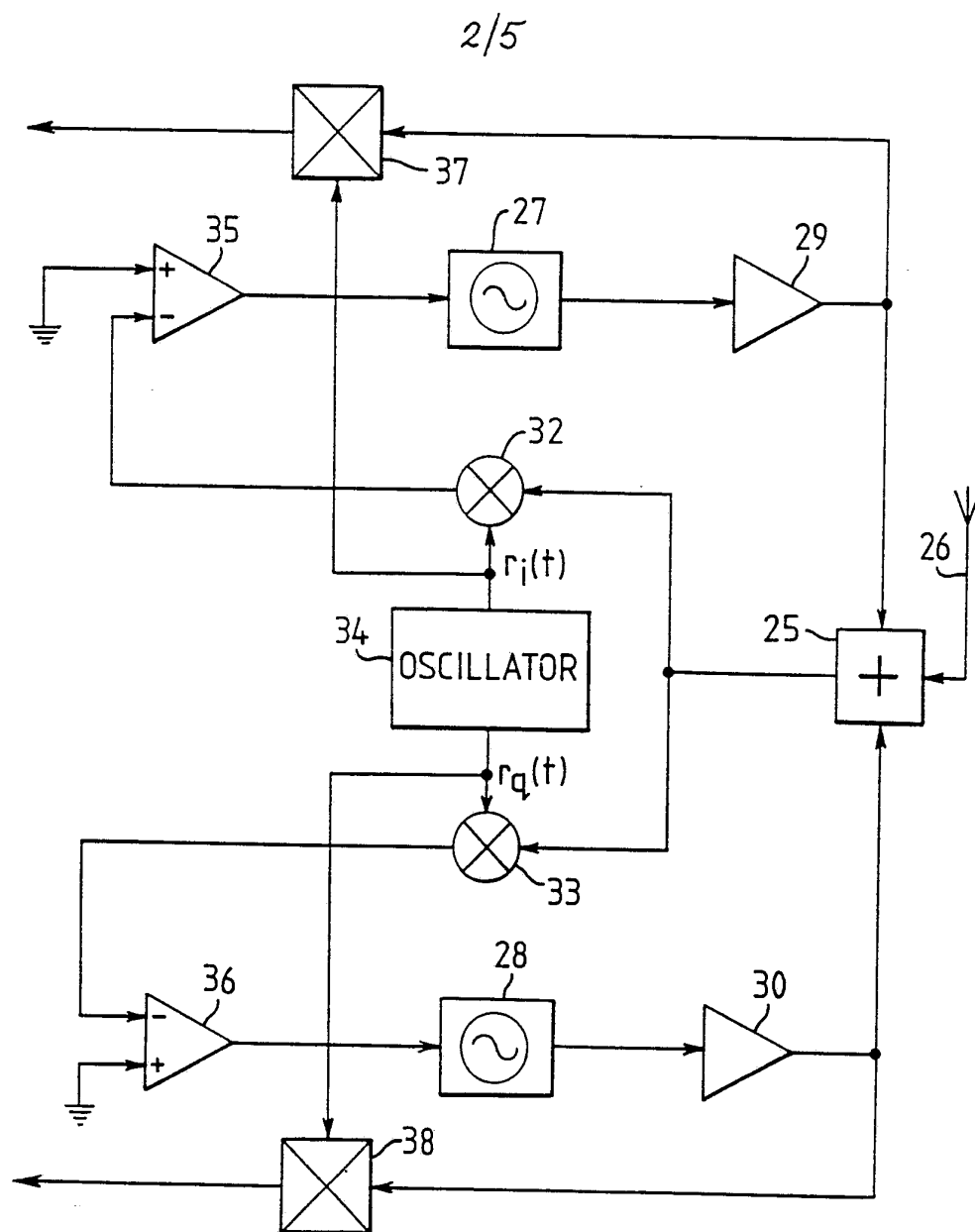


Fig. 2

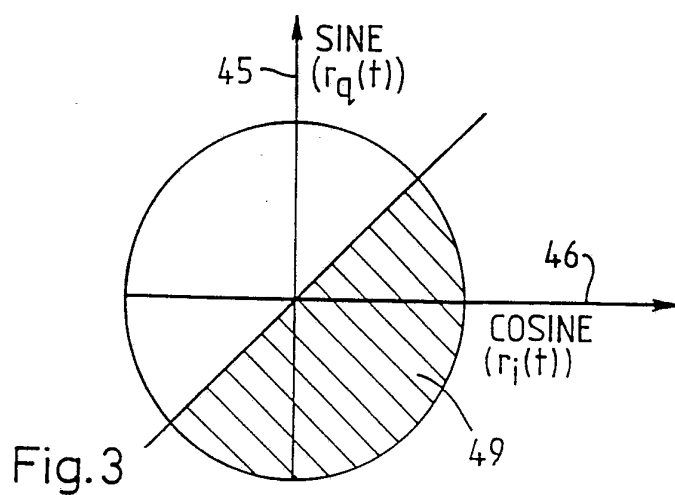


Fig. 3

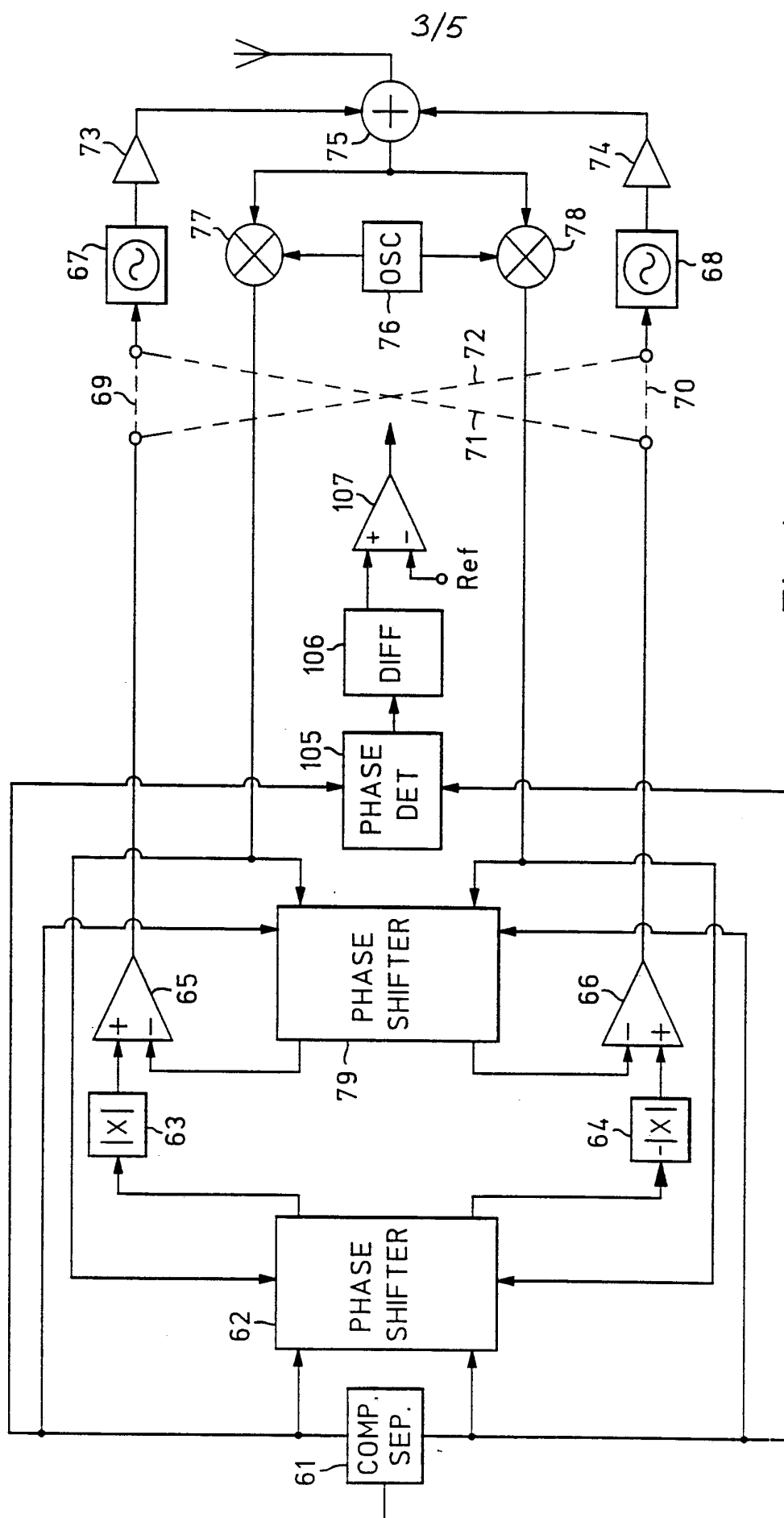


Fig.4

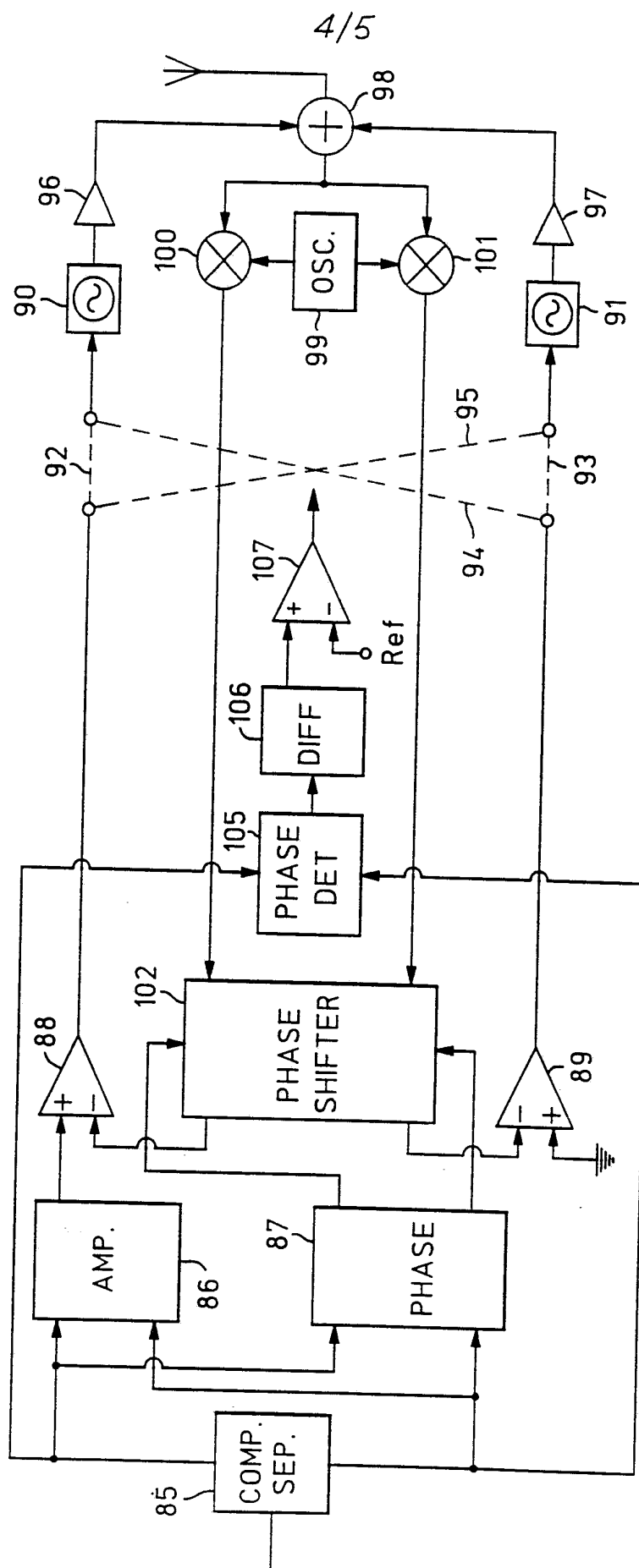


Fig. 5

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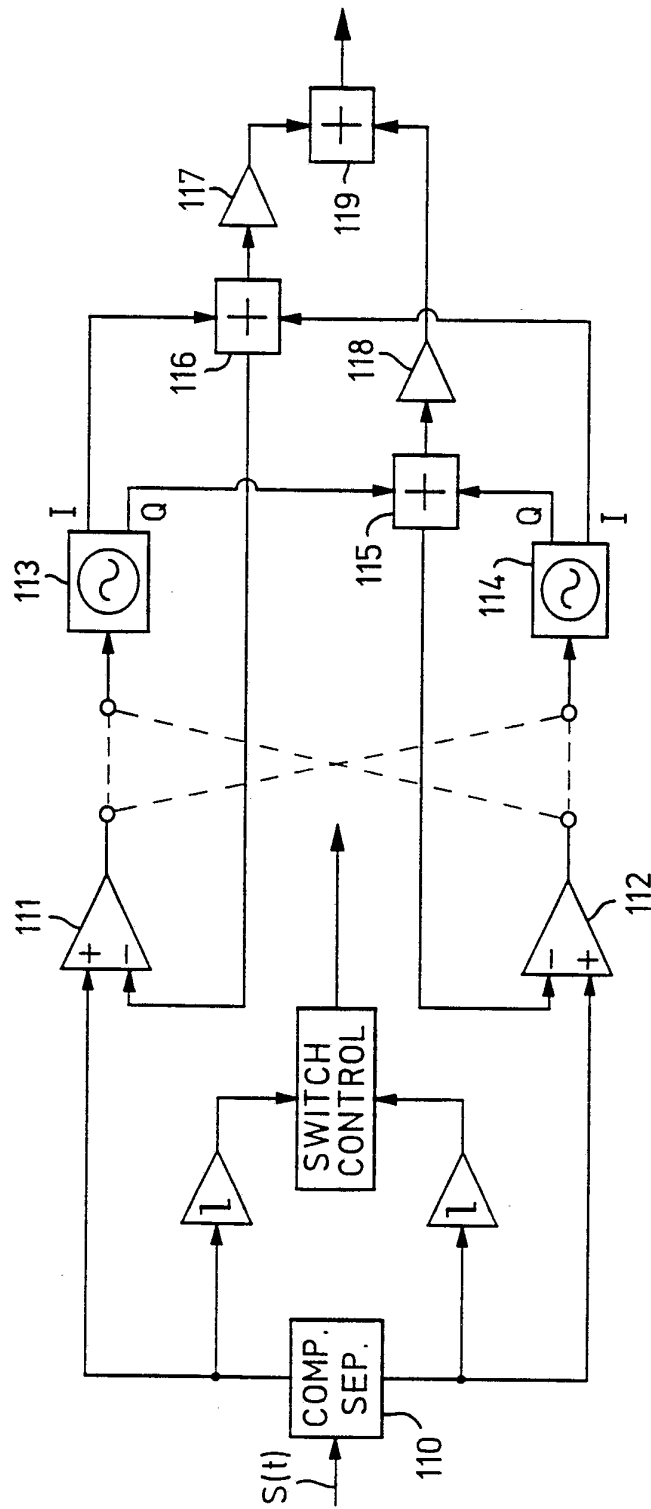


Fig. 6

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 93/00954

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
Int.Cl. 5 H03C1/06;	H03D3/24;	H03F1/32; H03L7/07
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
Int.Cl. 5	H03C ; H03D ; H03F ; H03L	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
A	US,A,5 105 168 (DASILVA) 14 April 1992 cited in the application see the whole document ---	1,3,12, 16,20,23
A	GB,A,2 073 516 (N.V. PHILIPS GLOEILAMPENFABRIEKEN) 14 October 1981 cited in the application see page 3, line 71 - page 4, line 96; figures 3A,3B ---	1,3,16, 20,23
A	US,A,3 953 805 (COUVILLON) 27 April 1976 see column 2, line 50 - column 3, line 10; figure 1 -----	1,16,20
¹⁰ Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
21 JULY 1993		30.07.93
International Searching Authority		Signature of Authorized Officer
EUROPEAN PATENT OFFICE		PEETERS M.M.G.

**ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.**

GB 9300954
SA 73687

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
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21/07/93

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		DE-A, C 3111729	18-03-82
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		JP-C- 1484712	14-03-89
		JP-A- 56152335	25-11-81
		JP-B- 63031131	22-06-88
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US-A-3953805	27-04-76	None	