Title: FIBRE CHANNEL TRANSPARENT SWITCH FOR MIXED SWITCH FABRICS

Abstract: A method and a Fibre Channel switch element are provided that allows communication between a host system and a target device attached to a proprietary switch fabric in a network. The Fibre Channel switch element includes a first port that communicates with the target device through the proprietary switch fabric by logging on behalf of the host system so that the proprietary switch behaves as if it was directly communicating with the host system; and a second port that communicates with the host system and collects host bus adapter ("HBA") identification information, wherein the HBA identification information is used to map the first port to the second port so that when the host system communicates with the target device the Fibre Channel switch element is transparent to the proprietary switch fabric.
FIBRE CHANNEL TRANSPARENT SWITCH FOR MIXED SWITCH FABRICS

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BACKGROUND

1. Field of the Invention

The present invention relates to Fibre Channel networks, and more particularly to a transparent Fibre Channel switch that facilities communication in a Fibre Channel network that includes at least a proprietary Fibre Channel fabric switch.

Background of the Invention

Fibre Channel is a set of American National Standard Institute (ANSI) standards, which provide a serial transmission protocol for storage and network protocols such as HIPPI, SCSI, IP, ATM and others. Fibre Channel provides an input/output interface to meet the requirements of both channel and network users.

Fibre Channel supports three different topologies: point-to-point, arbitrated loop and Fibre Channel fabric. The point-to-point topology attaches two devices directly. The arbitrated loop topology attaches devices in a loop. The Fibre Channel fabric topology attaches host systems directly to a fabric,
which are then connected to multiple devices. The Fibre Channel fabric topology allows several media types to be interconnected.

In Fibre Channel, a path is established between two nodes where the path's primary task is to transport data from one point to another at high speed with low latency, performing only simple error detection in hardware.

Fibre Channel fabric devices include a node port or "N_Port" that manages fabric connections. The N_port establishes a connection to a fabric element (e.g., a switch) having a fabric port or F_port. Fabric elements include the intelligence to handle routing, error detection, recovery, and similar management functions.

A Fibre Channel switch is a multi-port device where each port manages a simple point-to-point connection between itself and its attached system. Each port can be attached to a server, peripheral, I/O subsystem, bridge, hub, router, or even another switch. A switch receives messages from one port and automatically routes it to another port. Multiple calls or data transfers happen concurrently through the multi-port Fibre Channel switch.
Fibre Channel switches use memory buffers to hold frames received and sent across a network. Associated with these buffers are credits, which are the number of frames that a buffer can hold per fabric port.

Storage area networks ("SANs") are commonly used where plural memory storage devices are made available to various host computing systems. Data in a SAN is typically moved from plural host systems (that include computer systems, servers etc.) to a storage system through various controllers/adapters. The Fibre Channel standard is commonly used in SANs today.

Figure 1A shows an example of a Fibre Channel network. In Figure 1A, host system 10 is coupled to a standard fabric switch 13. Host system 10 (and/or 10A) typically includes several functional components. These components may include a central processing unit (CPU), main memory, input/output ("I/O") devices (not shown), read only memory, and streaming storage devices (for example, tape drives).

Host systems (for example, 10 and 10A) often communicate with storage systems (for example, devices 15 and 27) via a host bus adapter ("HBA", may also be referred to as a "controller" and/or
"adapter") using an interface, for example, a "PCI" or PCI-X bus interface.

Figure 1A shows four HBAs, 11, 12, 20 and 22.

HBA 11 is coupled to switch 13 via port 17, HBA 12 is coupled via port 18, HBA 20 is coupled via port 19 and HBA 22 is coupled via port 21.

Fabric switch 13 is coupled to a proprietary Fibre Channel fabric switch 14 (may also be referred to as "Proprietary Switch 14" or "switch 14") via ports 23 and 16. Fabric switch 13 is also coupled to another proprietary Fibre Channel fabric 26 via ports 24 and 25. Proprietary Switch 14 is coupled to device 15 that may be a storage sub-system, while proprietary fabric switch 26 (may also be referred to as "proprietary switch 26" or "switch 26") is coupled to device 27 which may also be a storage sub-system.

Devices 15 and 27 may be coupled using the Small Computer Systems Interface ("SCSI") protocol and use the SCSI Fibre Channel Protocol ("SCSI FCP") to communicate with other devices/systems. Both the SCSI and SCSI_FCP standard protocols are incorporated herein by reference in their entirety. SCSI FCP is a mapping protocol for applying SCSI command set to Fibre Channel.
Although Fibre Channel is an industry standard, proprietary switches, for example, 14 and 26 are quite common. Such switches often use confidential internal switching technology that allows a host system to communicate with a target device and vice-versa. Often a Fibre Channel network has more than one proprietary switching technology. Brocade Communications Inc © and McData Corporation © are two such corporations that provide such proprietary switching technology.

Proprietary switches have shortcomings. For example, when a proprietary switch (for example, 14) locates/communicates with a non-proprietary switch (for example, fabric switch 13) there is a loss of functionality. This forces SAN builders to use the proprietary switching technology. This loss of functionality becomes severe in mixed vendor environment. For example, in Figure 1A, use of switch 13 will result in loss of functionality with respect to both switches 14 and 26.

Although standardization is the future of Fibre Channel networks, mixed vendor configurations are a commercial reality. Therefore, there is a need for a Fibre Channel switch that will allow host systems and devices to communicate in a configuration with mixed
vendor/proprietary switching technology without any loss of functionality.

SUMMARY OF THE PRESENT INVENTION

A network that allows communication between a proprietary switch fabric and a host system is provided. The network includes a Fibre Channel switch element that is operationally coupled to the host system and to the proprietary switch fabric. The Fibre Channel switch element’s presence is transparent to the proprietary switch fabric when the host system communicates with a target device that is coupled to the proprietary switch fabric. The proprietary switch fabric communicates through a port of the Fibre Channel switch element as if it was communicating directly with the host system.

In another aspect of the present invention, a Fibre Channel switch element that allows communication between a host system and a target device that is attached to a proprietary switch fabric is provided. The Fibre Channel switch element includes a first port that communicates with the target device through the proprietary switch fabric by logging on behalf of the host system so that the
proprietary switch behaves as if it was directly communicating with the host system.

The Fibre Channel switch element also includes a second port that communicates with the host system and collects HBA identification information, wherein the identification information is used to map the first port to the second port so that when the host system communicates with the target device the Fibre Channel switch element is transparent to the proprietary switch fabric. HBA identification information is collected during a FLOGI process of the second port. Also, the Fibre Channel switch element initiates a FLOGI procedure on behalf of the host system.

In yet another aspect of the present invention, a method of communication between a host system and a target device that is attached to a proprietary switch fabric is provided. The method includes, collecting a HBA's identification information during a FLOGI process of a first port that couples the host system to a Fibre Channel switch element; and initiating a FLOGI procedure across a second port that couples the proprietary switch fabric to the Fibre Channel switch element, wherein the Fibre Channel switch element initiates the FLOGI on behalf
of the host system and the second port records a
FC_ID that is received from the proprietary switch
fabric.

The Fibre Channel switch element maps the first
5 port to the second port allowing communication
between the host system and the target device,
wherein the Fibre Channel switch element is
transparent to the proprietary switch fabric.

This brief summary has been provided so that the
10 nature of the invention may be understood quickly. A
more complete understanding of the invention can be
obtained by reference to the following detailed
description of the preferred embodiments thereof
concerning the attached drawings.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features and other features of the
present invention will now be described with reference
to the drawings of a preferred embodiment. In the
drawings, the same components have the same reference
numerals. The illustrated embodiment is intended to
illustrate, but not to limit the invention. The
drawings include the following Figures:

Figure 1A shows an example of a Fibre Channel
network;
Figure 1B shows an example of a Fibre Channel switch element, according to one aspect of the present invention;

Figure 1C shows a block diagram of a 20-channel switch chassis, according to one aspect of the present invention;

Figure 1D shows a block diagram of a Fibre Channel switch element with sixteen GL_Ports and four 10G ports, according to one aspect of the present invention;

Figure 1E shows a block diagram of an overall Fibre channel system that can use one aspect of the present invention;

Figures 2A, 2C and 2D show block diagrams of various topologies using a transparent switch, according to one aspect of the present invention;

Figure 2B shows a block diagram of a port in a transparent switch, according to one aspect of the present invention; and

Figures 3, 4 and 5 shows process flow diagrams of using the transparent switch, according to one aspect of the present invention.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Definitions:
The following definitions are provided as they are typically (but not exclusively) used in the Fibre Channel environment, implementing the various adaptive aspects of the present invention.

"ALPA": Arbitrated Loop Physical Address as defined by the Fibre Channel Standards.

"D_ID": A 24-bit Fibre Channel header that contains the destination address for a frame.

"E_Port": A fabric expansion port that attaches to another Interconnect port to create an Inter-Switch Link.

"F_Port": A port to which non-loop N_Ports are attached to a fabric and does not include FL_ports.

"Fibre Channel ANSI Standard": The standard (incorporated herein by reference in its entirety) describes the physical interface, transmission and signaling protocol of a high performance serial link for support of other high level protocols associated with IPI, SCSI, IP, ATM and others.

"Fabric": The structure or organization of a group of switches, target and host devices (NL_Port, N_ports etc.).

"Fabric Topology": This is a topology where a device is directly attached to a Fibre Channel fabric that uses destination identifiers embedded in frame
headers to route frames through a Fibre Channel fabric to a desired destination.

"FC_ID": A generic Fibre Channel address identifier, for example, the D_ID and S_ID.

"FLOGI": Before a Fibre Channel port can send data, the port determines information regarding its operating environment. This includes factors like interconnect topology; other ports in the environment; classes of Service and error recovery services that may be available. To determine this information, a port performs a login procedure. The login procedure includes Fabric Login ("FLOGI") and N_Port Login ("FLOGI, defined below). The Port requesting FLOGI sends Extended Link Service Commands, which includes a Sequence in its own Exchange with a header and Payload format. A recipient of the FLOGI accepts the login by sending an accept ("ACC") command. The format for FLOGI is defined by the Fibre Channel standards.

"Initiator": A device that initiates an input/output ("IO" or "I/O") operation, for example, a HBA.

"L_Port": A port that contains Arbitrated Loop functions associated with the Arbitrated Loop topology.
"OX_ID": An Originator (i.e., a device/port that originates an exchange) Exchange identification field in a Fibre Channel frame header.

"Name Server": Fibre Channel Generic Services (FC-GS-3) specification describes in section 5.0 various Fibre Channel services that are provided by Fibre Channel switches including using a Name Server to discover Fibre Channel devices coupled to a fabric. A Name server provides a way for N_Ports and NL_Ports to register and discover Fibre Channel attributes. Request for Name server commands are carried over the Common Transport protocol, also defined by FC-GS-3. The Name Server information is distributed among fabric elements and is made available to N_Ports and NL_Ports after the ports have logged in. Various commands are used by the Name Server protocol, as defined by FC-GS-3, for registration, de-registration and queries. Fiber Channel Switched Fabric (FC-SW-2) specification describes how a Fabric consisting of multiple switches implements a distributed Name Server.

"N-Port": A direct fabric attached port, for example, a disk drive or a HBA.

"NL_Port": A L_Port that can perform the function of a N_Port.

"PLOGI": Standard Fibre Channel N_Port to N_Port login. The N_Port login is performed after the
FLOGI. PLOGI determines the N_port to N_Port parameters and provides a specific set of operating parameters for communicating between N_ports. The port requesting PLOGI sends a PLOGI Extended Link Service Request addressed to the D_ID of an N_Port with which it needs to communicate. The addressed N_Port then returns an ACC reply. The request and reply contain operating parameters for communication between the N_Ports. The format for the request and reply are provided by the Fibre Channel standards.

"Port": A general reference to N. Sub.-- Port or F.Sub.--Port.

"SAN": Storage Area Network

"SCSI FCP": A standard protocol, incorporated herein by reference in its entirety for implementing SCSI on a Fibre Channel SAN.

"S_ID": A 24-bit field in a Fibre Channel frame header that contains the source address for a frame.

"Switch": A fabric element conforming to the Fibre Channel Switch standards.

"Target": A device that accepts IO operations from Initiators, for example, storage devices such as disks and tape drives.

Fibre Channel System:
To facilitate an understanding of the preferred embodiment, the general architecture and operation of a Fibre Channel system will be described. The specific architecture and operation of the preferred embodiment will then be described with reference to the general architecture of the Fibre Channel system.

Figure 1E is a block diagram of a Fibre Channel system 100 implementing the methods and systems in accordance with the adaptive aspects of the present invention. System 100 includes plural devices that are interconnected. Each device includes one or more ports, classified as node ports (N_Ports), fabric ports (F_Ports), and expansion ports (E_Ports). Node ports may be located in a node device, e.g. server 103, disk array 105 and storage device 104.

Fabric ports are located in fabric devices such as switch 101 and 102. Arbitrated loop 106 may be operationally coupled to switch 101 using arbitrated loop ports (FL_Ports).

The devices of Figure 1E are operationally coupled via “links” or “paths”. A path may be established between two N_ports, e.g. between server 103 and storage 104. A packet-switched path may be established using multiple links, e.g. an N-Port in
server 103 may establish a path with disk array 105 through switch 102.

**SWITCH ELEMENT**

Figure 1B is a block diagram of a 20-port ASIC fabric element according to one aspect of the present invention. Figure 1B provides the general architecture of a 20-channel switch chassis using the 20-port fabric element. Fabric element includes ASIC 20 with non-blocking Fibre Channel class 2 (connectionless, acknowledged) and class 3 (connectionless, unacknowledged) service between any ports. It is noteworthy that ASIC 20 may also be designed for class 1 (connection-oriented) service, within the scope and operation of the present invention as described herein.

The fabric element of the present invention is presently implemented as a single CMOS ASIC, and for this reason the term "fabric element" and ASIC are used interchangeably to refer to the preferred embodiments in this specification. Although Figure 1B shows 20 ports, the present invention is not limited to any particular number of ports.

ASIC 20 has 20 ports numbered in Figure 1B as GL0 through GL19. These ports are generic to common Fibre Channel port types, for example, F_Port,
FL_Port and E-Port. In other words, depending upon what it is attached to, each GL port can function as any type of port.

For illustration purposes only, all GL ports are drawn on the same side of ASIC 20 in Figure 1B. However, the ports may be located on both sides of ASIC 20 as shown in other figures. This does not imply any difference in port or ASIC design. Actual physical layout of the ports will depend on the physical layout of the ASIC.

Each port GL0-GL19 has transmit and receive connections to switch crossbar 50. One connection is through receive buffer 52, which functions to receive and temporarily hold a frame during a routing operation. The other connection is through a transmit buffer 54.

Switch crossbar 50 includes a number of switch crossbars for handling specific types of data and data flow control information. For illustration purposes only, switch crossbar 50 is shown as a single crossbar. Switch crossbar 50 is a connectionless crossbar (packet switch) of known conventional design, sized to connect 21 x 21 paths. This is to accommodate 20 GL ports plus a port for
connection to a fabric controller, which may be external to ASIC 20.

In the preferred embodiments of switch chassis described herein, the fabric controller is a firmware-programmed microprocessor, also referred to as the input/output processor ("IOP"). IOP 66 is shown in Figure 1C as a part of a switch chassis utilizing one or more of ASIC 20. As seen in Figure 1B, bi-directional connection to IOP 66 is routed through port 67, which connects internally to a control bus 60. Transmit buffer 56, receive buffer 58, control register 62 and Status register 64 connect to bus 60. Transmit buffer 56 and receive buffer 58 connect the internal connectionless switch crossbar 50 to IOP 66 so that it can source or sink frames.

Control register 62 receives and holds control information from IOP 66, so that IOP 66 can change characteristics or operating configuration of ASIC 20 by placing certain control words in register 62. IOP 66 can read status of ASIC 20 by monitoring various codes that are placed in status register 64 by monitoring circuits (not shown).

Figure 1C shows a 20-channel switch chassis S2 using ASIC 20 and IOP 66. S2 will also include other elements, for example, a power supply (not shown).
The 20 GL_Ports correspond to channel C0-C19. Each GL_Port has a serial/deserializer (SERDES) designated as S0-S19. Ideally, the SERDES functions are implemented on ASIC 20 for efficiency, but may alternatively be external to each GL_Port. The SERDES converts parallel data into a serial data stream for transmission and converts received serial data into parallel data. The 8 bit to 10 bit encoding enables the SERDES to generate a clock signal from the received data stream.

Each GL_Port may have an optical-electric converter, designated as OE0-OE19 connected with its SERDES through serial lines, for providing Fibre optic input/output connections, as is well known in the high performance switch design. The converters connect to switch channels C0-C19. It is noteworthy that the ports can connect through copper paths or other means instead of optical-electric converters.

Figure 1D shows a block diagram of ASIC 20 with sixteen GL ports and four 10G (Gigabyte) port control modules designated as XG0-XG3 for four 10G ports designated as XGP0-XGP3. ASIC 20 include a control port 62A that is coupled to IOP 66 through a PCI connection 66A.

Loop Based Fabric Interface:
Figure 2A shows a top-level block diagram using a transparent switch 13A, according to one aspect of the present invention. Transparent switch 13A (may also be referred to as "switch 13A") may be implemented using ASIC switch element 20 in chassis S2. Transparent switch 13A is coupled to HBA 11 via port 17A and HBA 12 via port 18A. Switch 13A is also coupled to HBA 20 via port 19A and HBA 22 via port 21A. Ports 17A, 18A, 19A and 21A are designated as TH_Ports (Transparent host ports), while ports 23A and 24A are designated as transparent fabric ports (TF_Ports or TFL_Ports (used interchangeably throughout this specification) (for loop functionality). Virtualized ALPAs for each HBA is shown as 11A, 12A, 20A and 22A, respectively.

Proprietary Fibre Channel fabric 14 communicates with ports 23A and 24A that function as NL_Ports. Proprietary switch 14 (or 26) believes that it is communicating with a host system directly and hence, there is no loss of functionality. It is noteworthy that although TH_Ports are shown as being linked with host systems, these ports may also be linked to storage devices.

Figure 2B shows an example of a port (for example, 17A), according to one aspect of the present
invention. Port 17A includes a receive pipeline 25A that receives Fibre Channel frames/data 29. Received data 29 is processed and then via crossbar 50 moves to the transmit pipeline 28. The transmit pipeline 28 transmits data 30 to the destination. Details of the pipelines and how frames are transmitted using alias cache 27A are provided in the patent application serial number 10/894,546, filed on July 20, 2004, the disclosure of which is incorporated herein by reference in its entirety. Alias cache 27A is used to facilitate communication between a host and a device.

Figure 3 shows a flow diagram of process steps that allow communication between a host system and a device behind a proprietary Fibre Channel fabric.

Transparent switch 13A acts as a proxy/bridge for attached host systems 10 and 10A. The fabric side ports (TFL_Ports) operate in a NL_Port link state mode. Each TFL_Port reserves ALPAS for all HBAs (11, 12, 20 and 22). Switch 13A FLOGIs on behalf of host system 10 and 10A across the TFL_Ports. FC_IDs are assigned by the TFL_Ports and stored in alias cache 27A and are used for communication between the hosts and target devices.
Turning in detail to Figure 3, in step S300, transparent switch 13A is powered up. In step S302, the fabric side (i.e., ports 23A and 24A) is brought up through loop initialization (Fibre Channel standard process). Switch 13A does not perform FLOGI (standard log-in procedure) during this step. Switch 13A inserts an ALPA request for every host port that it can service, shown as 11A, 12A, 20A and 22A in Figure 2A.

In step S304, switch 13A collects each supported HBA’s unique worldwide number ("WWN"), which is provided by the HBA manufacturer. Switch 13A collects the WWN information during FLOGI by the TH_Ports (i.e., 17A, 18A, 19A and 21A). HBAs send an ACC (accept) response to the TH_Ports with the WWN number.

In step S306, switch 13A maps the TH_Ports to the TFL_Ports (i.e., 23A and/or 24A). In step S308, the mapping information is set in routing module 26A so that each TH_Port points to the matching TFL_Port. Routing module 26A is similar to the steering state machine described in the aforementioned patent application.

In step S310, switch 13A initiates a FLOGI across the TFL_Ports on behalf of the host. In step S312,
the TFL_Ports record the FC_ID from the ACC response into alias cache 27A and then sets an entry to point to the matching TH_Port. In step S314, FLOGI is performed across TH_Ports. Switch 13A responds to the TH_Ports with the FC_ID acquired in step S310. At this point switch 13A becomes transparent.

In step S316, host (for example, 10) to target (for example, device 15) communication is established. Host N_Ports' PLOGI to the Name Server pass straight through to the TFL_Ports and then via the proprietary fabrics (14 and/or 15) to the devices (for example, 15 and/or 27).

If a TF_Port goes down, then the matching TH_ports are also brought down. The TH_ports are then re-assigned to the remaining TF_Ports and the routing module 26A is adjusted based on the new assignment. For example, if TFL_Port 23A assigned to TH_Port 17A goes down, then TH_port 17A may be re-assigned to port 24A.

If a TH_Port goes down then the corresponding TF_Port performs a loop initialization ("LIP") to remove any matching ALPA. The remaining TH_Ports wait until the TF_Port completes the LIP process.

Virtual N port ID Fabric Side Interface:
Virtual N_Port_ID ("VNPIID") is defined by the FC_FS standard, incorporated herein by reference in its entirety. VNPIID provides link level capability multiple N_Port identifiers (Fibre Channel addresses) to a N_Port device. Typically, this is accomplished after FLOGI when the N_Port device sends a FDISC command with a new WWPN (World Wide Port Number) and the S_ID is set to 0. The switch responds with a new N_Port_ID having the same Domain/Area values but a different Port_ID value (which is the ALPA field for all NL_Ports).

In one aspect of the present invention, TH_Ports and TFV_ports are defined by switch 13A. TFV_ports are shown in Figure 2C as 23B and 24B. VNPIIDS from HBAs 11, 12, 20 and 22 are shown as 11B, 12B, 20B and 22B, respectively. Switch 13A acts as a proxy/bridge for hosts 10 and 10A. TFV_ports request the VNPIIDs from hosts 10 and 10A and then place the VNPIIDs in alias cache 27A. The values are then used to route frames.

Figure 4 shows a flow diagram of process steps for using VNPIIDs, according to one aspect of the present invention. Turning in detail to Figure 4, in step S400, switch 13A is powered up. In step S402, TH_Ports are initialized and switch 13A collects WWN
information for HBAs 11, 12, 20 and 22. This is acquired during the FLOGI process. After the WWN information is collected, the TH_Ports are taken down (or disabled).

In step S404, switch 13A initializes the TFV_ports as if switch 13A was a host system. TFV_Ports send a FLOGI request to the fabric (i.e. 14 and 15) and then sends FDISC command with the WWPN information for each HBA. This includes a virtual N_Port identifier ("VNPID").

In step S406, TFV_Ports record a new VNPID in alias cache 27A. Each entry is set to a matching TH_port, i.e., each VNPID has a corresponding TH_Port entry.

In step S408, switch 13A maps each of the TH_port to a TFV_Port (for example, port 17A may be mapped to port 23B). Routing module 26A is set so that each TH_port points to a matching TFV_Port.

In step S410, the TH_Ports are re-initialized and the switch responds to the original FLOGI (step S402) with a reserved VNPID that can be allocated. The host PLOGI the Name Server and switch 13A initiates a PLOGI to the fabric switch (14 and/or 26). Switch 13A proxies the Name Server query commands between a TH_port and TFV_port. The change in HBA
configuration is registered with switch 13A. Thereafter, host to device communication is enabled.

If a TFV_Port goes down during communication or otherwise, then a matching TH_port is brought down. The TH_Ports are re-assigned to other TFV_Ports and the routing scheme is adjusted accordingly. Based on the re-assignment a new VNPID is assigned to the TH_Ports.

If a TH_Port goes down then the corresponding TFV_port sends a FLOGI for a matching VNPID.

In one aspect of the present invention, Virtual Port ID may be used for allowing communication between hosts and targets and vice versa in a proprietary fabric switch environment.

RAID Expansion:

Redundant array of inexpensive disks ("RAID") configuration can also use the transparent switch 13A, according to one aspect of the present invention. In this configuration a storage controller (or a RAID controller’s) target ports are mapped to one or more of fabric side ports. The fabric side port represents an alias of the target ports. Switch 13A multiplexes traffic to the appropriate port by using alias cache entries.
Two novel ports are defined for this configuration, a TT_PORT and a TFT_PORT, according to one aspect of the present invention. In Figure 2D TT_PORTS are shown as 17B and 18B and TFT_PORTS are shown as 23C, 23D, 24C and 24D.

Hosts 10 and 10A are coupled to TFT_PORTS 23C and 23D respectively. Proprietary fabric switches 14 and 26 are coupled to ports 24C and 24D, respectively. Also, hosts' 10B and 10C are coupled to proprietary switch fabric 14; and hosts 10D and 10E are coupled to proprietary switch fabric 26.

Figure 5 shows a flow diagram for using transparent switch 13A. In step S500, switch 13A is powered up. In step S502, switch 13A is set up with a defined world wide name ("WWN"). Switch 13A also assigns target ports to the fabric side port and obtains host side WWPN information.

In step S504, switch 13A performs FLOGI on the TFT_PORT side. Switch 13A uses the WWPN information to perform the FLOGI. In step S506, switch 13A receives FC_ID in response to the FLOGI.

In step S508, switch 13A sets an entry in alias cache 27A based on the FLOGI information. The FC_ID is matched to the D_ID to point to a corresponding TT_PORT. Switch 13A adds an entry in the alias cache.
27A of the TT_port to match the new FC_ID in the S_ID. This entry routes frames from TT_Port to the TFT_Port.

In step S510, target 1 and 2 are registered with the Name Server and communication is enabled.

It is noteworthy that the TT_Ports may be addressed by multiple FC_IDs and maintains distinct exchanges for the multiple FC_IDs.

In one aspect of the present invention, a transparent switch allows communication with proprietary switches without loss of functionality.

Although the present invention has been described with reference to specific embodiments, these embodiments are illustrative only and not limiting. Many other applications and embodiments of the present invention will be apparent in light of this disclosure and the following claims.
What is Claimed is:

1. A network that allows communication between a proprietary switch fabric and a host system, comprising:

   a Fibre Channel switch element that is operationally coupled to the host system and the proprietary switch fabric wherein the Fibre Channel switch element’s presence is transparent to the proprietary switch fabric when the host system communicates with a target device that is coupled to the proprietary switch fabric.

2. The network of Claim 1, wherein when the proprietary switch fabric communicates through a port of the Fibre Channel switch element as if it was communicating directly with the host system.

3. The network of Claim 1, wherein the Fibre Channel switch element ports that communicates with the proprietary switch fabric operate as a N_Port.

4. The network of Claim 1, wherein the Fibre Channel switch element logs into the proprietary switch fabric on behalf of the host system.

5. A Fibre Channel switch element that allows communication between a host system and a target device that is attached to a proprietary switch fabric, comprising:
a first port that communicates with the target device through the proprietary switch fabric by logging on behalf of the host system so that the proprietary switch behaves as if it was directly communicating with the host system; and

a second port that communicates with the host system and collects host bus adapter identification information, wherein the host bus adapter ("HBA") identification information is used to map the first port to the second port so that when the host system communicates with the target device the Fibre Channel switch element is transparent to the proprietary switch fabric.

6. The Fibre Channel switch element of Claim 5, wherein the HBA identification information is collected during a FLOGI process of the second port.

7. The Fibre Channel switch element of Claim 5, wherein the Fibre Channel switch elements initiates a FLOGI procedure on behalf of the host system.

8. The Fibre Channel switch element of Claim 5, wherein the first port provides a FC_ID to the second port.

9. A method of communication between a host system and a target device that is attached to a proprietary switch fabric, comprising:
collecting a host bus adapter's ("HBA's") identification information during a FLOGI process of a first port that couples the host system to a Fibre Channel switch element; and

5 initiating a FLOGI procedure across a second port that couples the proprietary switch fabric to the Fibre Channel switch element, wherein the Fibre Channel switch element initiates the FLOGI on behalf of the host system and the second port records a FC_ID that is received from the proprietary switch fabric.

10 The method of Claim 9, wherein the Fibre Channel switch element maps the first port to the second port allowing communication between the host system and the target device, wherein the Fibre Channel switch element is transparent to the proprietary switch fabric.

11 The method of Claim 9, wherein an alias cache is used to record the FC_ID.

12 A method of communication between a host system and a target device that is attached to a proprietary switch fabric, comprising:
collecting world wide number ("WWN") information from a host side port of a Fibre Channel switch element that is coupled to a host bus adapter and disabling the host side port after the WWN information is collected; initiating a FLOGI process, wherein the Fibre Channel switch element initiates the FLOGI process on behalf of the host system and a fabric side port of the Fibre Channel switch element records a virtual N_Port identifier; and mapping a fabric side port of the Fibre Channel switch element with a host side port of the Fibre Channel switch element.

13. The method of Claim 12, wherein the host side ports are re-initialized after the mapping.

14. The method of Claim 12, wherein if a fabric side port goes down during communication, then a matching host side port is also taken down.
FIGURE 1E
FIGURE 2B
S300
POWER UP

S302
PERFORM LIP AND INSERT ALPA REQUEST FOR HOST PORT

S304
COLLECT HOST HBA WWN INFORMATION

S306
MAP TH_PORT TO TFL_PORT

S308
SET ROUTING

S310
INITIATE FLOGI

S312
RECORD FC_ID IN ALIAS CACHE AND SET ENTRY TO MATCHING TH_PORT

S314
SEND FC_ID TO TH_PORT

S316
ESTABLISH HOST TO TARGET COMMUNICATION

FIGURE 3
POWER UP

INITIALIZE HOST SIDE AND COLLECT HBA INFORMATION

INITIALIZE FABRIC SIDE AND PERFORM FLOGI

RECORD VNPID

MAP THE _PORTS TO THE TF _PORTS AND SET ROUTING

ENABLE HOST TO TARGET COMMUNICATION

FIGURE 4
S500
POWER UP

S502
SET UP TRANSPARENT SWITCH

S504
PERFORM FLOGI ON FABRIC SIDE

S506
RECEIVE FC_ID IN RESPONSE TO FLOGI

S508
SET ENTRY IN ALIAS CACHE

S510
REGISTER TARGET WITH NAME SERVER AND ENABLE COMMUNICATION

FIGURE 5
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

HO4L12/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HO4L G06F H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 6 118 776 A (BERMAN ET AL) 12 September 2000 (2000-09-12) abstract column 1, line 6 - column 12, line 25 figures 1,2,13-15</td>
<td>1-14</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

*A* document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search

7 February 2006

Date of mailing of the international search report

14/02/2006

Name and mailing address of the ISA:

European Patent Office, P.B. 5818 Patentianz 2 NL - 2280 HV Hilversum
Tel: (+31)-70-340-2040, Tx: 31 561 art nl, Fax: (+31)-70-340-3016

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Mariggis, A
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**INTERNATIONAL SEARCH REPORT**

**Information on patent family members**

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