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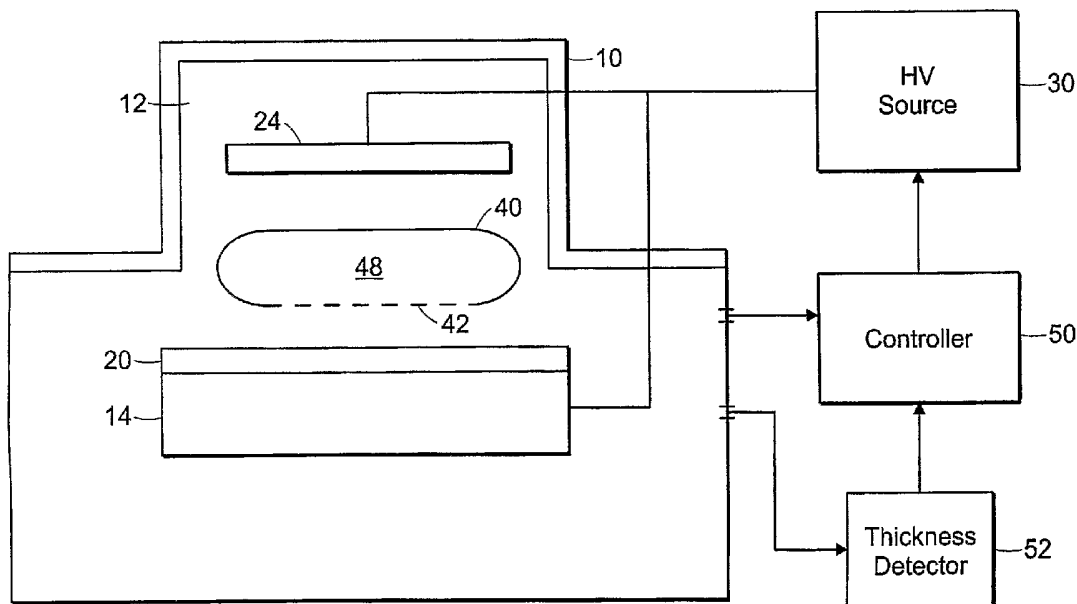
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(54) Title: PROFILE ADJUSTMENT IN PLASMA ION IMPLANTATION



(57) Abstract: A method and apparatus are directed to providing a dopant profile adjustment solution in plasma doping systems for meeting both concentration and junction depth requirements. Bias ramping and bias ramp rate adjusting may be performed to achieve a desired dopant profile so that shallow and abrupt junctions in vertical and lateral directions are realized that are critical to device scaling in plasma doping systems.

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## PROFILE ADJUSTMENT IN PLASMA ION IMPLANTATION

### BACKGROUND OF THE INVENTION

#### Related Applications

This application claims priority to U.S. Provisional Application No. 60/662,018, entitled "PROFILE ADJUSTMENT IN PLASMA ION IMPLANTATION," filed on March 15, 2005 the contents of which are herein incorporated by reference in their entirety.

#### Technical Field

The described apparatus and methods relate generally to providing profile adjustment solutions in plasma doping (PLAD) applications to meet both concentration and junction depth requirements. More particularly, the described apparatus and methods are directed to providing abrupt junctions in vertical and lateral directions which are critical to device scaling needs.

#### Background of the Invention

Plasma doping systems are known and used for forming shallow junctions in semiconductor wafers and for other applications requiring high current with relatively low energy ions. In plasma doping systems, a semiconductor wafer is placed on a conductive platen, which functions as a cathode and is located in a plasma doping chamber. An ionizable doping gas is introduced into the chamber, and a voltage pulse is applied between the platen and an anode or the chamber walls, causing formation of a plasma containing ions of the dopant gas. The plasma has a plasma sheath in the vicinity of the wafer. The applied pulse causes ions in the plasma to

be accelerated across the plasma sheath and to be implanted into the wafer. The depth of implantation is related to the voltage applied between the wafer and the anode. Very low implant energies can be achieved. Examples of such plasma doping systems are described in U.S. Patent No. 5,354,381 to Sheng, U.S. Patent No. 6,020,592 to Liebert et al., and U.S. Patent No. 6,182,604 to Goeckner. In the above described plasma doping systems, the applied voltage pulse generates a plasma and accelerates positive ions from the plasma toward the wafer. In other types of plasma systems, a continuous plasma is produced, for example, by inductively-coupled RF power from an antenna located internal or external to the plasma doping chamber. The antenna is connected to an RF power supply. At intervals, voltage pulses are applied between the platen and the anode, causing ions in the plasma to be accelerated toward the wafer.

Dopant gas species used for plasma implantation may decompose or dissociate during the implant process into atomic or molecular fragments which may be deposited on the surface of the wafer. Atomic or molecular fragments that result from dissociation of dopant gas molecules are referred to herein as "neutral particles." Examples of dopant gas species which dissociate during the implant process include  $\text{AsH}_3$ ,  $\text{PH}_3$ ,  $\text{BF}_3$ , and  $\text{B}_2\text{H}_6$ . For example, arsine gas  $\text{AsH}_3$  may dissociate into As, AsH and  $\text{AsH}_2$ , which may be deposited on the surface of the wafer being implanted. These deposited surface layers can cause a number of problems, including dose non-repeatability, poor dose uniformity and dose measurement problems. In particular, the neutral particles that form the deposited surface layers are not measured by the dose measurement system. Further, the depth profile of the dopant is altered by the deposited surface layer itself and by its effect on implanted ions. In addition, the deposited surface layers can cause contamination of other equipment, such as annealers, when the wafers are subsequently

processed in such equipment.

Accordingly, there is a need for providing a profile adjustment solution in plasma doping applications to meet both concentration and junction depth requirements.

### SUMMARY OF THE INVENTION

The invention includes methods and apparatuses for providing a dopant profile adjustment solution in plasma doping systems for meeting both concentration and junction depth requirements. Bias ramping and bias ramp rate adjusting may be performed to achieve a desired dopant profile so that shallow and abrupt junction in vertical and lateral directions are realized that are critical to device scaling in plasma doping systems. The ramping of the implanting voltage bias may be linear or non-linear ramping. The rate of ramping the implanting voltage bias may be adjusted and the rate may vary with respect to the deposition rate. Specifically, the rate of ramping the implanting voltage bias may be faster, slower or match the deposition rate. The implanting voltage bias may be ramped in combination with ramping the duty cycle and in combination with changing at least one implant process parameter. The ramping and adjustments are performed to maximize the retained dose and near surface concentration while minimizing dopant spread in vertical and lateral directions.

A first aspect of the invention is directed to a method for plasma implantation of a workpiece comprising the steps of introducing a dopant gas into a plasma doping chamber and ramping an implanting voltage bias to accelerate the dopant gas ions toward the workpiece. The implanting voltage bias is ramped to maximize the retained dose and near surface concentration of the implanted dopant gas ions into the workpiece.

A second aspect of the invention is directed to a plasma doping apparatus comprising a plasma doping chamber, a platen, a gas source and a voltage source for implanting dopant gas ions into a workpiece. The voltage source generates an implanting voltage bias to accelerate the dopant gas ions from the plasma toward the workpiece that is ramped to maximize the retained dose and near surface concentration of the implanted dopant gas ions into the workpiece.

The foregoing and other features of the invention will be apparent from the following more particular description of embodiments of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

FIG. 1 is a block diagram of a plasma doping system according to an embodiment of the present invention;

FIGs. 2(a) and 2(b) are graphs of implant ramping bias voltages according to embodiments of the present invention;

FIG. 3 shows SIMS and Rs data comparison for a five step bias ramping according to one embodiment of the present invention;

FIG. 4 shows a dopant profile for bias ramping according to one embodiment of the present invention;

FIGs. 5(a), 5(b), and 5(c) show bias ramping combined with duty cycle ramping according to embodiments of the present invention;

FIG. 6 shows effects on the dopant profile for various deposition rates tied with the bias

ramping according to embodiments of the present invention;

FIG. 7 shows a junction profile for reverse bias ramping according to an embodiment of the present invention; and

FIG. 8 shows a junction profile for bias ramping with a process having an initial deposition according to an embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

A box-shape dopant profile is desirable in ion implantation processes for semiconductor device manufacturing. For mono-energetic incident ions, such as those from a beamline implanter, the dopant profile is typically Gaussian. PLAD profiles tend to peak near the surface, with the tail of its profile approaching the beamline tail of the same implant energy. In applications where a certain profile shape is desired, profile adjustment can be made by changing implant energy and dose. In PLAD applications, surface deposition may occur during the implant and by applying a bias voltage that changes with deposition thickness a box-like profile may be achieved. According to one embodiment of the present invention, a method is described to control the ramping and/or rate of ramping the bias voltage in PLAD applications to maximize retained dose and near surface concentration, while minimizing dopant spread in vertical and lateral directions.

During plasma implant processes, deposition typically occurs on the wafer surface due to neutrals and low energy ions from the plasma. This deposition progressively increases through the implant from zero at the beginning of the implant to a small value, 100 Angstroms for instance, towards the end of a high dose implant, such as  $2 \times 10^{16}$  for instance. The depositing film

on the wafer surface may impede the penetration depth of the implanting ions which may make the ion implant progressively shallower through the implant process. One embodiment of the present invention compensates for increasing deposition by progressively increasing the implant voltage through the implant step. Such compensating accounts for the fact that the deposition rates are different in different chemistries and conditions. The compensating may be achieved by either a pre-programmed software look up table or an in-situ monitor device installed in the implanting system. By varying the thickness of surface deposition through the plasma implant step, the implant depth of the ions may change accordingly through the plasma implant step. The implant characteristics are thereby changed to make the implant sensitive to dose, bias frequency, pulse width and other process parameters that impacts the implant time.

For typical implant processes, an increase of dopant concentration near the surface may cause a proportional increase at the tail region profile. Junction depths, both vertical and lateral, are sensitive to ion energy and tail concentration. A deep junction usually negative impacts on device performance. For applications that require a high dopant concentration near the surface, a high implant dose is needed but the implant energy is limited by the junction target. One problem for low energy, high dose implants is the resulting low wafer throughput. In PLAD, low energy ions can also be blocked by surface deposition, leading to low retained dose problems. High bias voltages may satisfy the dose target but not the junction target.

High dose or surface concentration is needed to achieve low contact resistance and low spreading resistance. Shallow and abrupt junctions in vertical and lateral directions are critical to device scaling. According to one embodiment of the present invention, a profile adjustment solution for PLAD is provided to meet both concentration and junction depth needs. One

example of a plasma ion implantation system suitable for the embodiments of the present invention is illustrated in Fig. 1. A process chamber 10 defines an enclosed volume 12. A platen positioned within the process chamber 10 provides a surface for holding a substrate, such as a semiconductor wafer 20. An anode 24 may be positioned with the process chamber 10 in spaced relation to the platen 14. The anode 24 may be connected to electrically conductive walls of the process chamber 10, both of which may be connected to ground. Alternatively, the platen may be connected to ground, and the anode 24 pulsed to a negative voltage. In further embodiments, both the anode 24 and the platen 14 may be biased with respect to ground. The semiconductor wafer 20 and the anode may be connected to a high voltage source 30 via the platen 14 so that the semiconductor wafer 20 functions as a cathode. The voltage source 30 may provide pulses in a range of about 20 to 20,000 volts in amplitude, for about 1 to 200  $\mu$ seconds and a pulse repetition rate of about 100 Hz to 20kHz. However, it should be understood that these pulse parameter values are given by way of example only and other values may be utilized within the scope of the present invention by those skilled in the art.

A controller 50 regulates the rate at which gas is supplied from a gas source (not shown) to the process chamber 10 for supplying an ionizable gas containing a desired dopant for implantation into the semiconductor wafer 20. This configuration provides a continuous flow of process gas at a desired flow rate and constant pressure. It should be realized by those skilled in the art that other configurations may be utilized for regulating gas pressure and flow. A thickness detector 52 communicates with the process chamber 10 and provides the detected information to the controller 50. The thickness detector 52 may be an in-situ film thickness monitor based on reflectivity, however, other known sensors may be used for observing the

wafer surface for the deposition rate. The plasma ion implantation system may also include additional components, depending on the configuration of the system. The system typically includes a process control system (not shown) which controls and monitors the components of the plasma ion implantation system to implement a desired implant process. Systems which utilize continuous or pulsed RF energy include an RF source coupled to an antenna or an induction coil. The system may also include magnetic elements which provide magnetic fields that confine electrons and control plasma density and spatial distribution.

In operation, the semiconductor wafer 20 is positioned on the platen 14 and the pressure control system produces the desired pressure and gas flow rate within the process chamber 10. The voltage source 30 applies a series of high voltage pulses to the semiconductor wafer 20, causing formation of a plasma 40 in a plasma discharge region 48 between the semiconductor wafer 20 and the anode 24. The plasma 40 contains positive ions of the ionizable gas and includes a plasma sheath 42 in the vicinity, typically at the surface, of the semiconductor wafer 20. The electric field that is present between the anode 24 and the platen 14 during the high voltage pulse accelerates positive ions from the plasma 40 across the plasma sheath 42 toward the platen 14. The accelerated ions are implanted into the semiconductor wafer 20 to form regions of impurity material. The pulse voltage is selected to implant the positive ions to a desired depth in the semiconductor wafer 20. The number of pulses and the pulse duration are selected to provide a desired dose of impurity material in the semiconductor wafer 20. The current per pulse is a function of pulse voltage, pulse width, pulse frequency, gas pressure and species and any variable position of the electrodes. For example, the cathode to anode spacing may be adjusted for different voltages.

As noted above, dopant gas species typically used for plasma implantation may dissociate into neutral particles during the implant process and form deposited surface layers on the semiconductor wafer 20. Examples of dopant gas species which form deposited surface layers include  $\text{AsH}_3$ ,  $\text{PH}_3$  (phosphine) and  $\text{B}_2\text{H}_6$ . Some fluorides such as  $\text{BF}_3$  may form deposit surface layers under certain plasma doping conditions. For example, arsine gas may dissociate into As, AsH and  $\text{AsH}_2$ , which may be deposited on the surface of the semiconductor wafer 20. Similarly,  $\text{BF}_3$  may dissociate into B, BF and  $\text{BF}_2$  which may be deposited on the surface of the semiconductor wafer 20. These deposited surface layers cause dose non-repeatability, poor dose uniformity and metrology problems.

In the present embodiment, the deposition rates as a function of chemistry and plasma doping conditions are characterized. The stopping power of the deposition layer to the incident ions are also characterized. A first implant bias (V1) is used to complete a predetermined first target dose, allowing a first deposition layer to be grown during the first implant period  $t_1$  as shown in Fig. 2(a). Next a second implant bias (V2) is used to complete a second dose, with the second implant energy adjusted according to the deposition layer thickness. Subsequent implant bias and times are repeated until the total implant dose is reached. The number of iterations,  $n$ , may be selected according to the particular application. In characterizing the deposition rates as a function of chemistry and plasma doping conditions, a knowledge base may be developed. The plasma doping system may access this knowledge base for estimating the deposition rate which depends on the recipe required by the implantation process. The implant bias voltage or bias frequency are typically ramped up through the implant process to compensate for the deposition which starts at zero and progressively increases as the implant progresses.

In another embodiment of the present invention, the bias voltage is adjusted continuously, following either a linear or non-linear curve, until the total dose is reached as illustrated in Fig. 2(b). A feedback control system, including the in-situ film thickness detector 52 and other process monitors may be used so that the increase of implant bias or frequency is just enough for ions gaining extra momentum to penetrate the surface film. The amount of bias increase may be more or less than what is needed to compensate for the deposition layer to achieve a desired dopant profile.

In one implementation of the present invention, the method is tested in a  $B_2H_6$  plasma doping system with a five-step bias ramping, from 4kV to 6kV, with 0.5 kV steps. In Fig. 3, SIMS results show retained dose and surface concentration similar to 6kV, but junction depths shallower than at 5kV and these results can be confirmed by  $R_s$  data. The embodiments of the present invention may also be implemented for PLAD processes that require a box-like profile, such as ultra-shallow junction (USJ) formation, source drain extensions (SDE), source drain and poly gate doping, and material modification using high dose, low energy implant.

For one aspect of the present invention, the desired dopant profile is achieved by bias ramping. In this embodiment, linear bias ramping tied to the deposition rate is performed and in another embodiment, non-linear bias ramping also tied to the deposition rate is performed to maximize the retained dose. The bias ramping rate may also be adjusted to be faster or slower than the deposition rate. Also, reverse bias ramping may be performed for processes with net etching. The bias ramping may also be combined with duty cycle ramping to prevent wafer surface arcing which may occur at high duty cycle bias ramping. The bias ramping may also be combined with changing one or more process parameters to maximize the retained dose without

a deep dopant profile. Examples of process parameters that may be changed include pressure, gas flow, gas composition, RF power, and temperature. It should be realized that other process parameters may be changed and the present invention is not limited by the above referenced process parameters which are provided as some examples. Also, profile engineering in any situation, deposition, etching or none, may be performed for high surface concentration or a deep profile tail. An initial deposition may be performed to reduce channeling. Open and closed loop control may be utilized for bias ramping. In-situ and ex-situ deposition measurements may be used in these control loops.

As shown in Fig. 4, the bias voltage increases during plasma implantation as indicated by the arrow length. The energy gain for each ion is equivalent to energy loss through the deposition layer so that ion distribution within the substrate remains largely the same. As described above, the increase of bias voltage can be linear or non-linear with time, depending on the deposition rate, which can also be linear or non-linear with time. Accordingly, the retained dose is maximized without a deep dopant profile.

Figs. 5(a), 5(b), and 5(c) illustrate bias ramping combined with duty cycle ramping for achieving a higher duty cycle at lower ramping bias for improving wafer throughput and photoresist conditioning of the wafers. The bias voltage is applied only during the "on" period as shown in Fig. 5(a). However, the amplitude of the bias voltage may be controlled separately by the controller 50. Also, the bias voltage may start with a lower duty cycle as shown in Fig. 5(b) and end with a higher duty cycle as shown in Fig. 5(c) or the bias voltage may start with the higher duty cycle of Fig. 5(c) and end with the lower duty cycle of Fig. 5(b).

Fig. 6 illustrates the effects on the dopant profile when the bias ramping is varied with

respect to the deposition rate. In Fig. 6, line I shows bias ramping that is slower than the deposition rate, line II shows bias ramping that matches the deposition rate and line III shows bias ramping that is faster than the deposition rate. For lowering contact resistance, a surface peaked profile is desired while a shallow or deeper profile is desirable for junction depth control and activation.

Fig. 7 illustrates an embodiment of the present invention which utilizes reverse bias ramping in a process with net surface etching. The ion energy is reduced to match the surface removal rate so that ion distribution within the substrate remains largely the same. Again, the decrease of the bias voltage can be linear or non-linear with time, depending on the surface removal rate. Accordingly, the retained dose is maximized without a deep dopant profile resulting.

Fig. 8 illustrates an embodiment of the present invention in which an initial deposition may be made without a bias voltage being applied for a predetermined amount of time. When a single crystal substrate is used, the channeling tail may be reduced or even eliminated due to the angular spread of ions penetrating the initial deposition layer. Thereby, channeling may be reduced without the need of pre-amorphization implant which is critical for USJ formation in SDE doping. Also, the dopant lateral distribution can be modeled with the knowledge of incident ion energy, flux and deposition rate.

While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from

the spirit and scope of the invention as defined in the following claims.

## CLAIMS

What is claimed is:

1. A method for plasma implantation of a workpiece, comprising the steps of:  
introducing a dopant gas into a plasma doping chamber to form a plasma containing ions of the dopant gas, the plasma having a plasma sheath at or near a surface of the workpiece; and  
ramping an implanting voltage bias to accelerate the dopant gas ions across the plasma sheath toward the workpiece and implant the dopant gas ions into the workpiece, wherein the ramping of the implanting voltage bias maximizes retained dose and near surface concentration of the implanted dopant gas ions into the workpiece.
2. The method of claim 1, wherein the step of ramping the implanting voltage bias comprises linear ramping.
3. The method of claim 1, wherein the step of ramping the implanting voltage bias comprises non-linear ramping.
4. The method of claim 1, wherein the step of ramping the implanting voltage bias comprises adjusting the rate of the ramping.
5. The method of claim 1, wherein the step of ramping the implanting voltage bias further comprises the step of ramping the duty cycle in combination therewith.

6. The method of claim 1, wherein the step of ramping the implanting voltage bias further comprises the step of changing at least one implant process parameter in combination therewith.
7. The method of claim 6, wherein the at least one implant process parameter comprises pressure, gas flow, gas composition, RF power and temperature parameters.
8. The method of claim 1, wherein the rate of ramping the implanting voltage bias matches the deposition rate of neutral particles and the dopant gas ions.
9. The method of claim 1, wherein the rate of ramping the implanting voltage bias is faster than the deposition rate of neutral particles and the dopant gas ions.
10. The method of claim 1, wherein the rate of ramping the implanting voltage bias is slower than the deposition rate of neutral particles and the dopant gas ions.
11. The method of claim 1, wherein the step of ramping the implanting voltage bias comprises reverse ramping.
12. The method of claim 1, further comprising the step of an initial deposition of neutral particles and dopant gas ions before the step of introducing the dopant gas ions.
13. The method of claim 1, further comprising the step of monitoring the thickness of the

deposition layer and providing a feedback control to the ramping of the implanting voltage bias responsive to the monitored thickness.

14. A method of claim 1, wherein the workpiece is a semiconductor wafer.
15. A plasma doping apparatus, comprising:
  - a plasma doping chamber;
  - a platen located in the plasma doping chamber;
  - a gas source coupled to the plasma doping chamber for introducing a dopant gas into the plasma doping chamber and producing a plasma containing ions of the dopant gas;
  - a voltage source for generating an implanting voltage bias to accelerate the dopant gas ions from the plasma toward the workpiece and implant the dopant gas ions into the workpiece, wherein the implanting voltage bias is ramped to maximize retained dose and near surface concentration of the implanted dopant gas ions into the workpiece.
16. A plasma doping apparatus of claim 15, wherein the implanting voltage bias is linearly ramped.
17. A plasma doping apparatus of claim 15, wherein the implanting voltage bias is non-linearly ramped.
18. A plasma doping apparatus of claim 15, wherein rate of the implanting voltage bias is

adjusted.

19. A plasma doping apparatus of claim 15, wherein the implanting voltage bias is ramped in combination with ramping the duty cycle.

20. A plasma doping apparatus of claim 15, wherein the implanting voltage bias is ramped in combination with changing at least one implant process parameter.

21. A plasma doping apparatus of claim 20, wherein the at least one process parameter comprise pressure, gas flow, gas composition, RF power and temperature parameters.

22. A plasma doping apparatus of claim 15, wherein the rate at which the implanting voltage bias is ramped matches the deposition rate of neutral particles and the dopant gas ions

23. A plasma doping apparatus of claim 15, wherein the rate at which the implanting voltage bias is ramped is faster than the deposition rate of neutral particles and the dopant gas ions

24. A plasma doping apparatus of claim 15, wherein the rate at which the implanting voltage bias is ramped is slower than the deposition rate of neutral particles and the dopant gas ions

25. A plasma doping apparatus of claim 15, wherein the implanting voltage bias is ramped reversely.

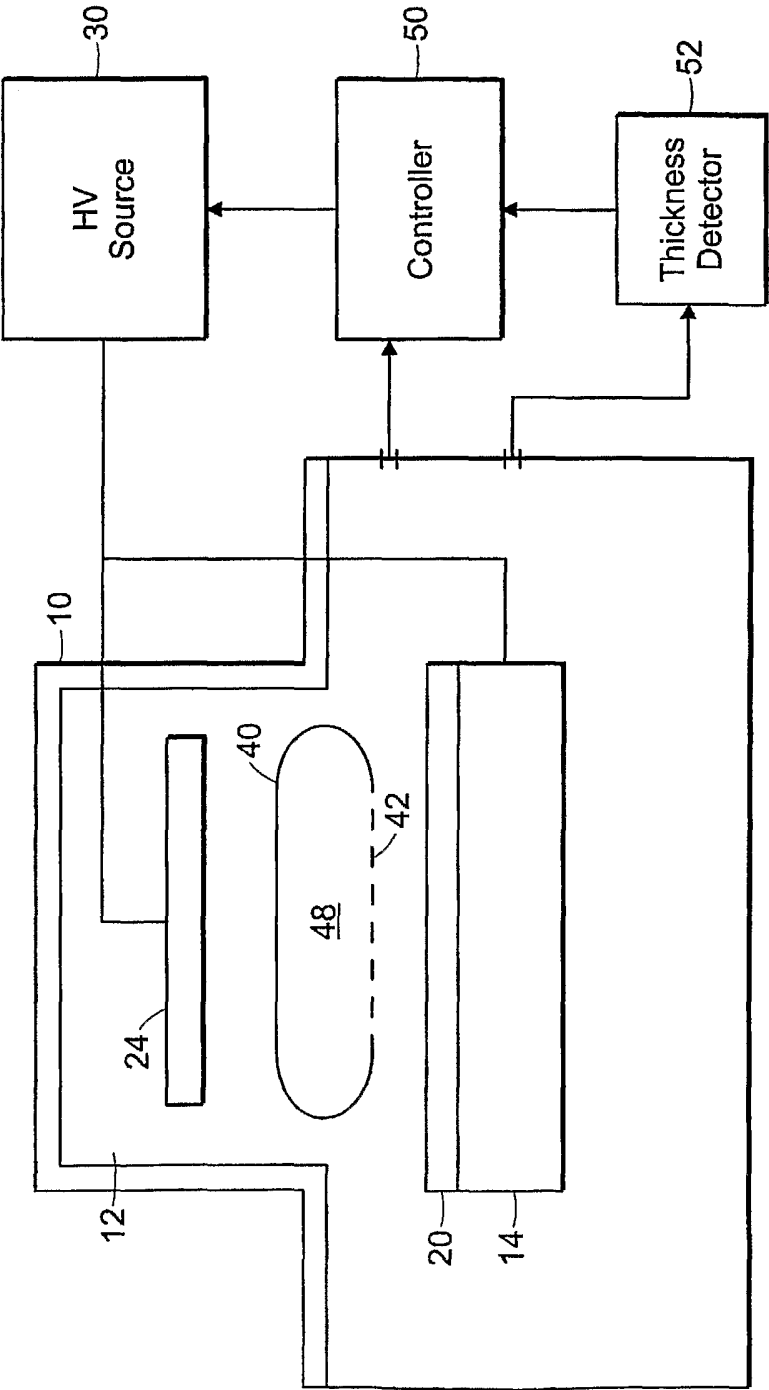


FIG. 1

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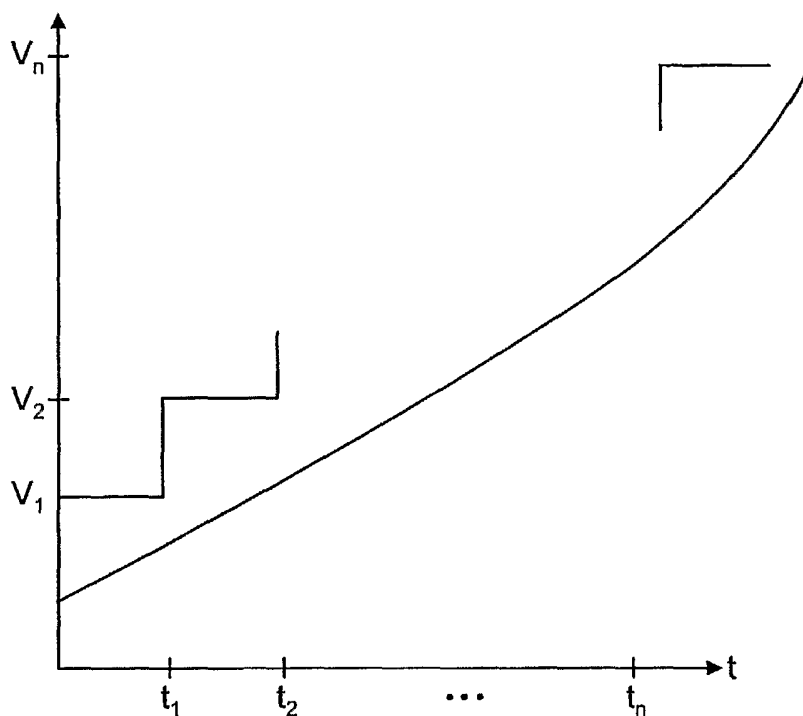


FIG. 2A

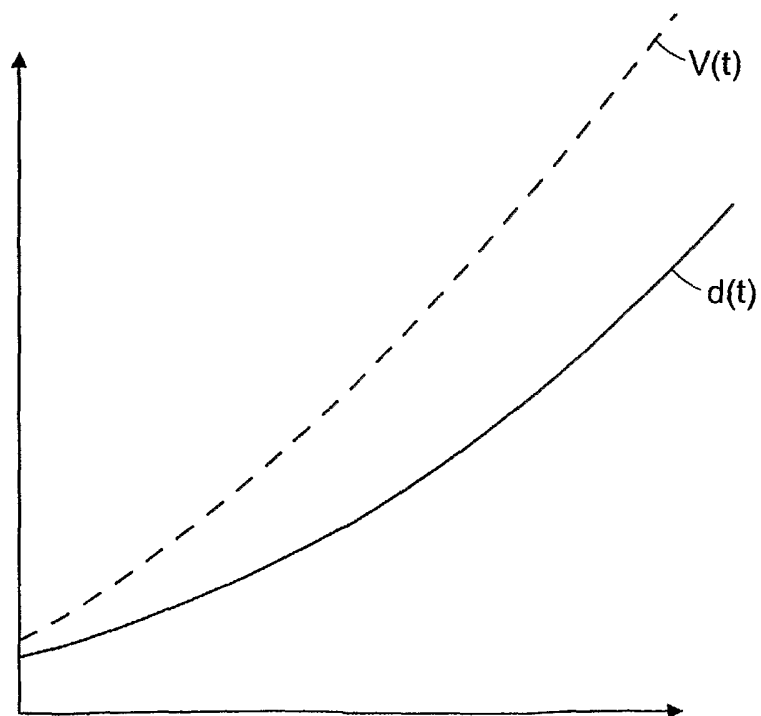


FIG. 2B

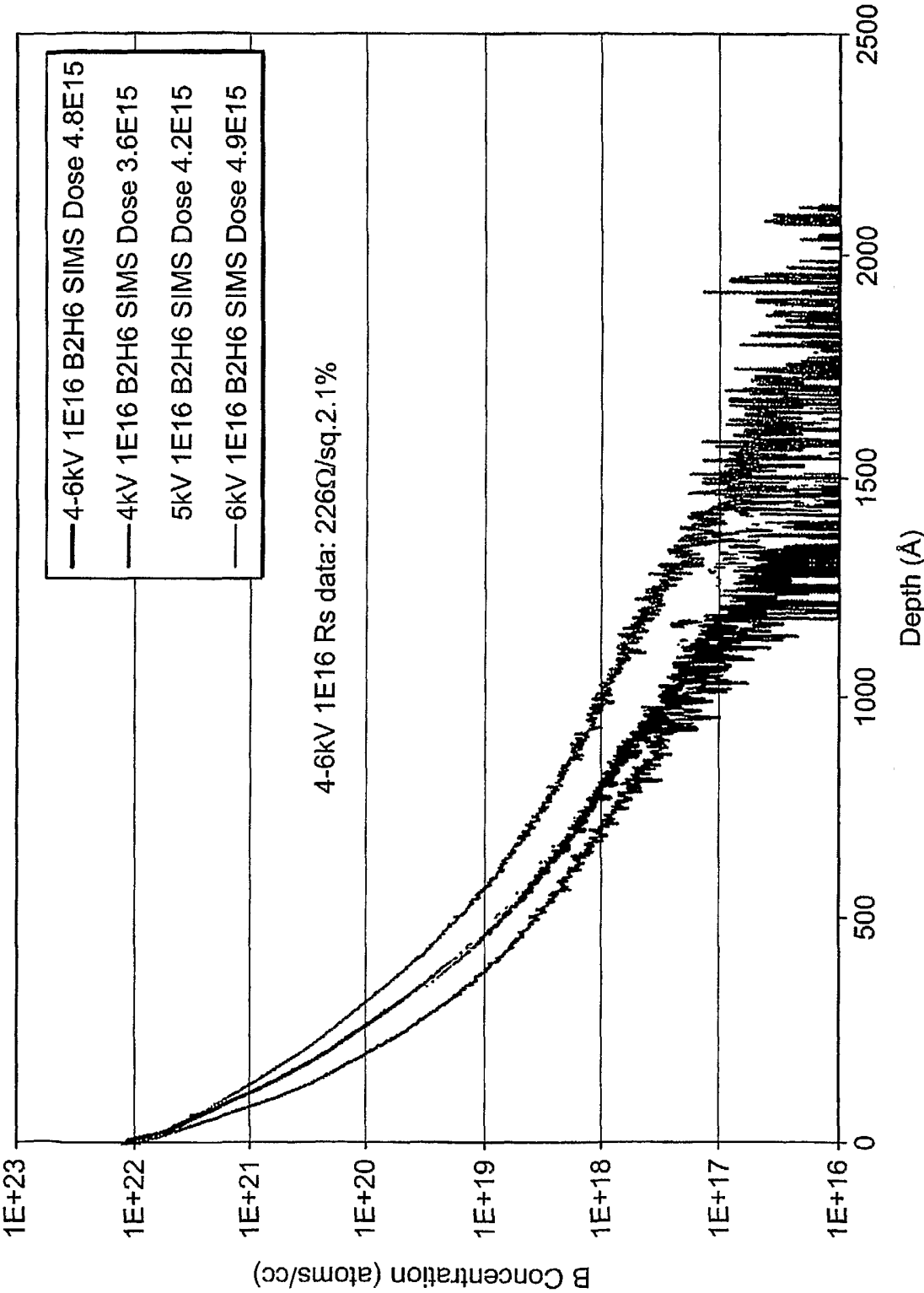


FIG. 3

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FIG. 5A



FIG. 5B

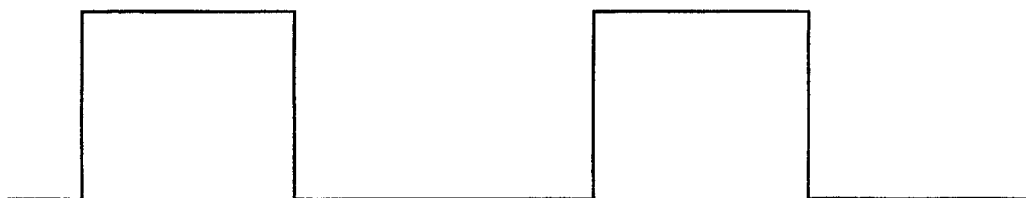


FIG. 5C

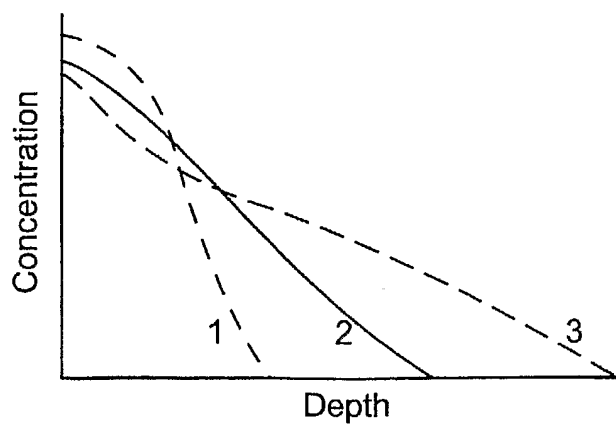


FIG. 6

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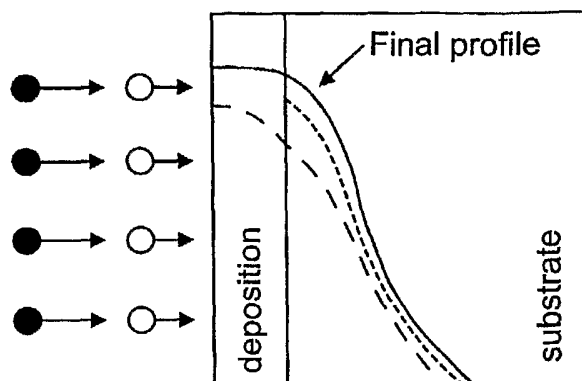


FIG. 4

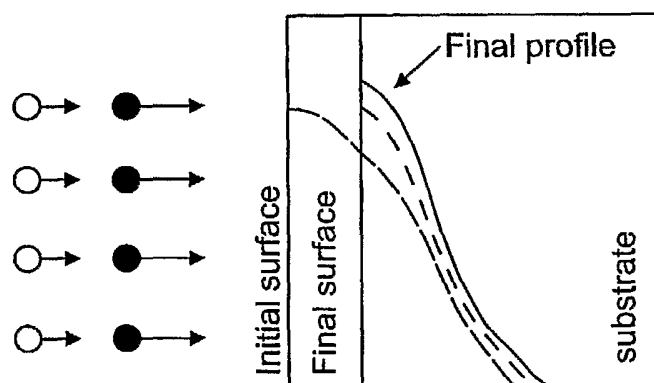


FIG. 7

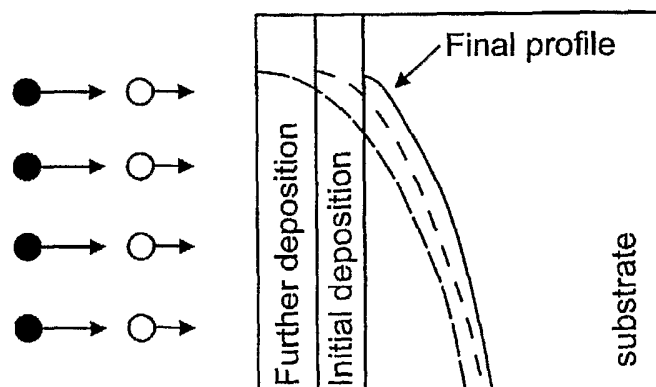


FIG. 8

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2006/009182

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01J37/32

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                | Relevant to claim No.  |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|
| X<br>Y    | WO 02/25694 A (AXCELIS TECHNOLOGIES, INC;<br>EATON LIMITED) 28 March 2002 (2002-03-28)<br>abstract; figure 1<br>page 8, line 15 - page 10, line 17<br>-----                       | 1-12,<br>14-25<br>13   |
| X         | EP 1 055 745 A (SONY CORPORATION)<br>29 November 2000 (2000-11-29)<br><br>paragraphs [0076] - [0079], [0058],<br>[0019] - [0020]; figures 10,4,2<br>-----                         | 1-4,<br>6-10,<br>15-25 |
| X         | US 6 182 604 B1 (GOECKNER MATTHEW J ET AL)<br>6 February 2001 (2001-02-06)<br>cited in the application<br>column 3, line 63 - column 5, line 25;<br>figure 1<br><br>-----<br>-/-- | 15-25                  |

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

12 June 2006

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# INTERNATIONAL SEARCH REPORT

International application No

PCT/US2006/009182

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                                                  | Relevant to claim No.             |
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Information on patent family members

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