

[54] **CURRENT DRIVER SYSTEM FOR A CORE MEMORY**

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Related U.S. Application Data

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[52] U.S. Cl. **340/174 TB, 340/174 AC**

[51] Int. Cl. **G11c 5/02, G11c 7/00, G11c 11/06**

[58] Field of Search **340/174 TB, 174 AC; 307/270**

References Cited

UNITED STATES PATENTS

3,239,681 3/1966 Bond..... 340/174 TB

3,331,966	7/1967	Pechacek.....	340/174 TB
3,332,074	7/1967	Arnold.....	340/17 TB
3,482,118	12/1969	Mathamel.....	307/270
3,603,938	9/1971	Cooper.....	340/174 TB

OTHER PUBLICATIONS

IBM Technical Disclosure Bulletin "Current Source Compensation" by Hoffman Vol. 10. No. 6. Nov. 1967 pp. 778

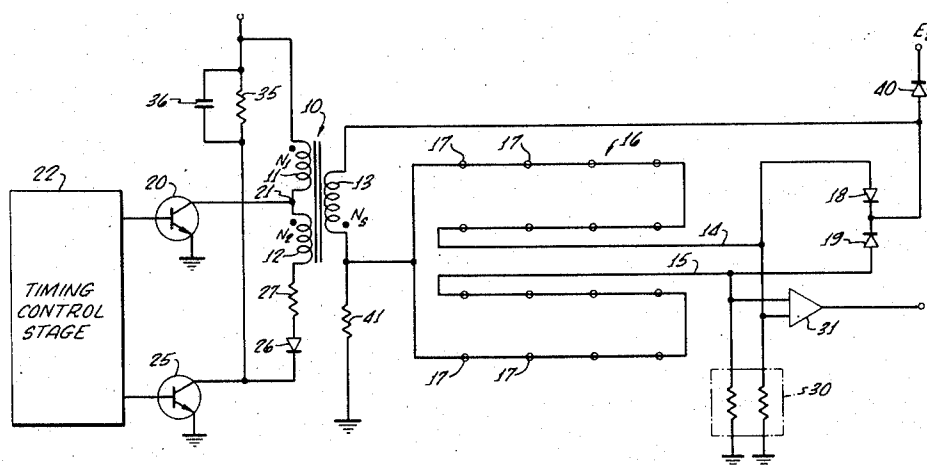
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[57] **ABSTRACT**

A system for supplying a current to a core memory stack having substantial inductance including a transformer having a selectively variable primary/secondary turns ratio. The variable turns ratio permits the current buildup time interval in the core state to be minimized while reducing the power required to drive the stack.

15 Claims, 3 Drawing Figures



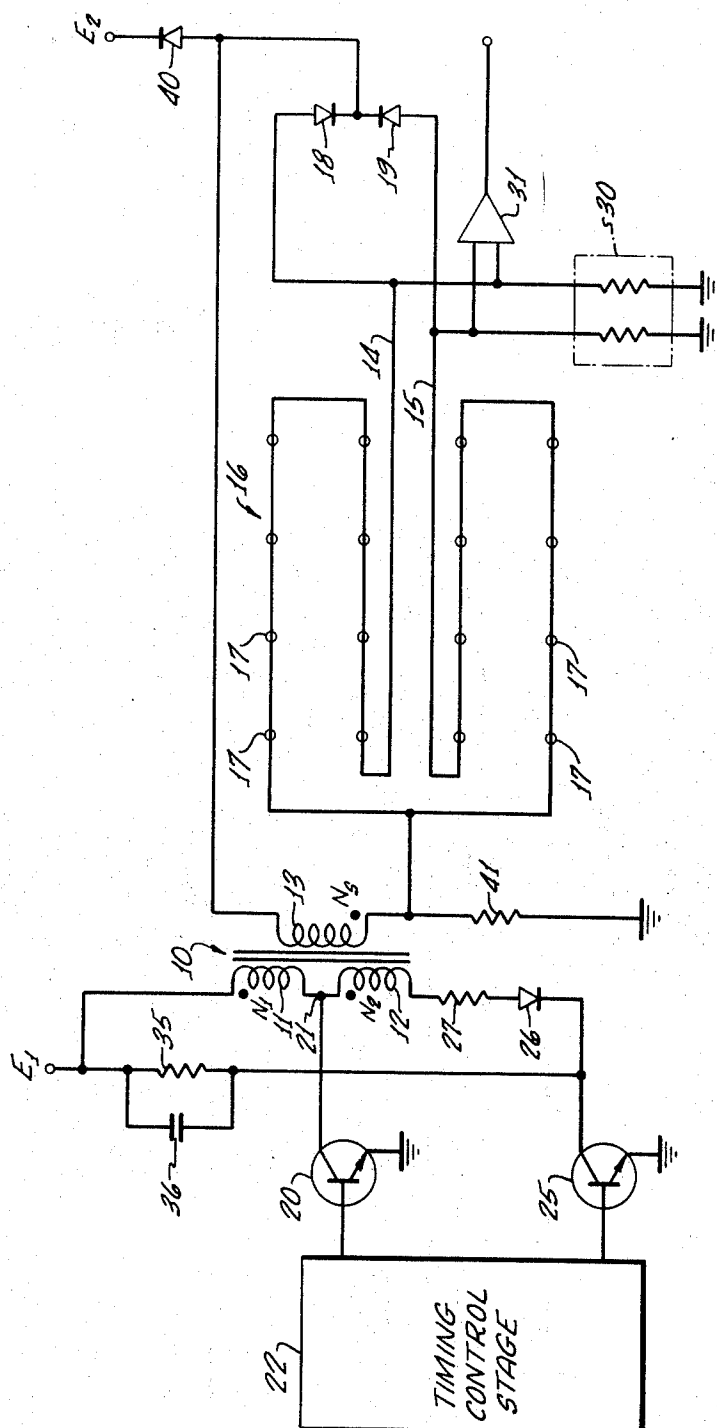
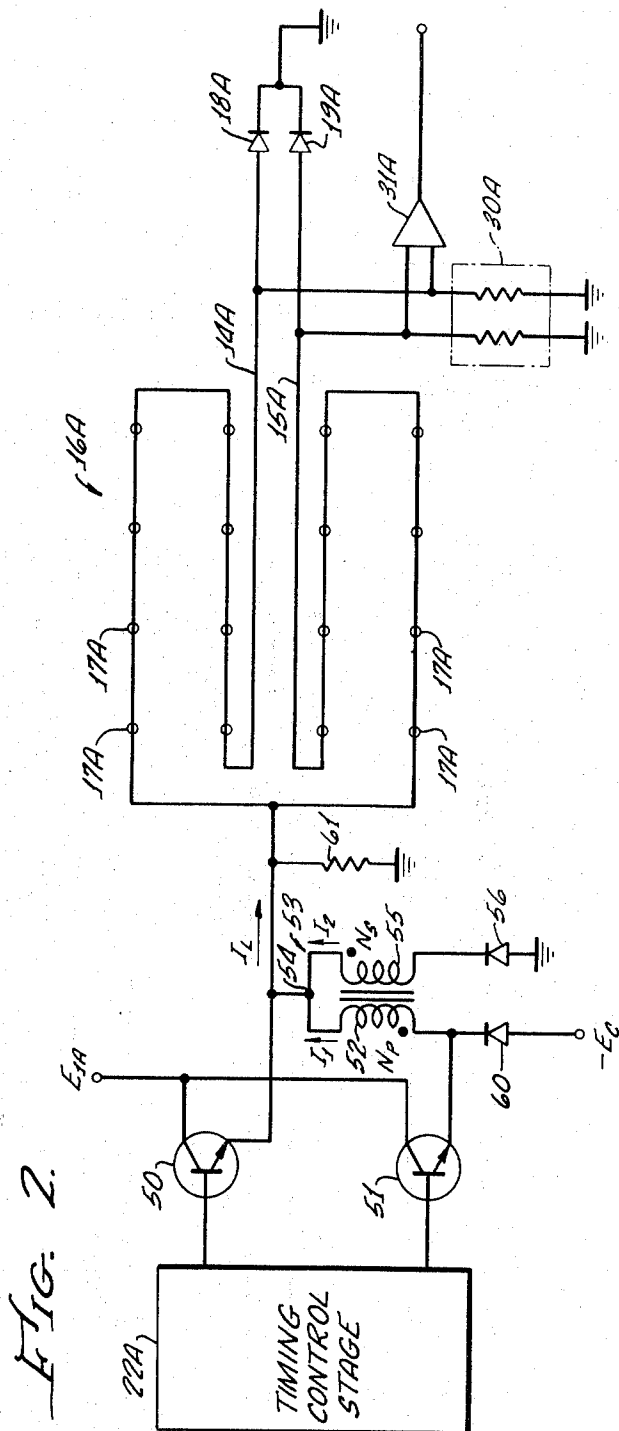
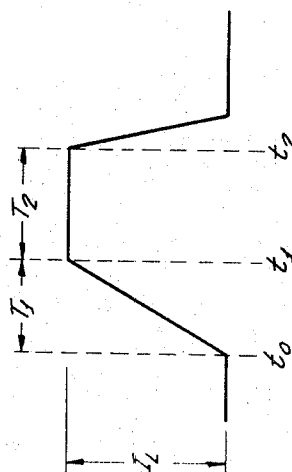


FIG. 1.



CURRENT DRIVER SYSTEM FOR A CORE MEMORY

RELATED APPLICATION

This application is a continuation-in-part of copending application Ser. No. 128,030, filed Mar. 25, 1971 and now U.S. Pat. No. 3,697,966, entitled IMPROVED CURRENT DRIVER SYSTEM FOR A CORE MEMORY.

FIELD OF THE INVENTION

This invention relates to improvements in magnetic core memories wherein an electrical conductor is threaded through a plurality of cores. Particular examples are coincident-current memories, linear-selection memories, and read-only core memories.

SUMMARY OF THE INVENTION

Digital data processing systems require means for storing large quantities of digital data. Memories using a plurality of magnetic cores or core stacks are commonly used for this purpose. Although such memory systems have been very extensively used for more than a decade and have several inherent advantages, factors which limit their functional utility include their electrical power requirements and their read-write cycle time.

A feature of the present invention is that it provides a simple, but elegant solution for the problem of reducing the power required to drive a core stack while minimizing the time interval required to build up the stack current drive to desired magnitude. As a result, core memories utilizing the present invention can operate on a very short read-write cycle time while drawing minimal power.

Particular features of this invention are that it provides a balanced drive and is adapted for supplying core stacks characterized by a very substantial inductive load. Thus, a single system constructed in accordance with the invention can supply a current pulse through over 8,000 cores with a current buildup time of 100 nanoseconds while using less power than prior art devices.

In a first embodiment of the present invention, the core stack is connected to the secondary of the transformer and the primary of the transformer is initially energized through a current path having a minimal L/R time constant. As a result, a current of predetermined value is driven through the secondary winding and core stack within a very short time interval. The primary/secondary turns ratio is then changed while simultaneously reducing the current flow through the primary winding so that the power drain is reduced while maintaining the desired magnitude of current flow in the core stack.

In a preferred embodiment of the present invention, the core stack is initially energized directly from the power supply through a first switch. As a result, a current of predetermined value is driven through the core stack within a minimal time interval. After a short time interval the first switch is turned off and current is supplied via a second switch to a transformer which in turn is coupled to the core stack. The turns ratio of the transformer is such that the desired magnitude of current flow is maintained in the core stack while the drain from the power supply is reduced.

These embodiments are described in reference to the attached drawings in which:

FIG. 1 is a schematic diagram of the first embodiment of an improved current driver system for a core memory according to the present invention;

FIG. 2 is a schematic diagram of the preferred embodiment of an improved current driver system for a core memory according to the present invention; and

FIG. 3 is a graphical illustration of the relationship between the current flow in the core stack of FIG. 2 and the timing control provided by the timing control stage.

DESCRIPTION OF THE FIRST EMBODIMENT

Referring to FIG. 1, a transformer 10 having the dot convention shown includes series connected first primary winding 11 of N_1 turns and second primary winding 12 of N_2 turns and a secondary winding 13 of N_s turns. The secondary winding 13 provides a balanced output, i.e., neither output lead is grounded, which is very desirable for rejecting the common mode voltages generally present in a core stack. Advantageously, one end of the secondary 13 is connected to a pair of windings 14 and 15 of a core stack 16. Each of these windings 14, 15 are respectively threaded through a plurality of memory cores 17, as shown. A return current path to the other side of the secondary 13 is provided via diodes 18, 19. By way of particular example, cores 17 may represent a single bit plane of a coincident current memory and each of the windings 14, 15 represent the inhibit sense windings which are pulsed with a relatively short, e.g. 300 nanosecond, current pulse to inhibit the write current (on other windings not shown) in the bit plane when binary ZEROS are to be stored. While only a few cores 17 are shown for illustrative purposes, each of the windings 14, 15 may be threaded through literally thousands of cores. For example, in a core plane of 8,192 cores, each winding will be threaded through one-half of the total number of cores, e.g. 4,096 cores. As a result, the core stack and particularly the inhibit windings of a large core stack are characterized by a very substantial inductance.

The power for this current pulse is provided by a power supply voltage which supplies a voltage E_1 between ground and the first primary winding 11. The current pulse is initiated by turning on transistor 20 which serves as a first switch. The collector of this transistor is connected to node 21 between the first and second primary windings 11, 12, its emitter is connected to ground, and its base to timing control stage 22. Accordingly, when transistor 20 is turned on by stage 22 a first current path is provided from voltage source E_1 through the first primary winding 11 and transistor 20 to ground. This path has a minimal resistance and therefore a minimal L/R time constant. As a result, the current flow in the primary winding 11 and resulting current flow in secondary winding 13 build up to the desired magnitude in a minimal time interval.

After a predetermined time interval, typically the relatively short interval required to buildup the current in the secondary winding to the desired magnitude, the timing control stage 22 turns transistor 20 off. Advantageously, transistor 25, serving as a second switch, has already been turned on by this same stage. The emitter of this transistor is grounded and its collector is connected through a series connected diode 26 and resistor 27 to the second primary winding 12. Accordingly, when transistor 25 is on and transistor 20 is off, a second current path is provided from voltage power supply

E_1 through the first and second primary windings 11, 12, resistor 27, diode 26 and transistor 25 to ground. This path, having a higher resistance provided by current limiting resistance 27, draws less current and therefore less power from the power supply than when current flows in the first current path provided by the first switch transistor 20.

Notwithstanding the reduced current and power drain when the first switch 20 is off and the second switch 25 is on, the magnitude of current flow through the secondary winding 13 is maintained at the desired value because of the increase in primary to secondary turns ratio. Thus, the relationship between the current and turns ratio are defined by the following equation:

$$I_p/I_s = N_s/N_p \quad (1)$$

or

$$I_s = N_p/N_s I_p \quad (2)$$

where I_p is the current flowing through the primary, I_s is the current flowing through the secondary, N_p is the number of primary turns and N_s is the number of secondary turns. N_p is the sum of the turns in the first and second primary windings or,

$$N_p = N_1 + N_2 \quad (3)$$

If, for example, a current pulse of constant magnitude is desired, N_1 , N_2 and N_s may be made equal, and resistor 27 may be selected to reduce the primary current I_p by one-half when the first switch is opened. Substituting these circuit ratios in equation (2), when switching transistor 20 is on

$$I_s = N_1/N_s I_p \quad (4)$$

If N_1 equals N_s ,

$$I_s = I_p \quad (5)$$

When switching transistor 20 is off and switching transistor 25 is on, the secondary current is defined as follows, assuming the turns and current ratios given above:

$$I_s = (N_1 + N_2)/(N_s) (I_p)/(2) \quad (6)$$

Since it has been assumed that $N_1 = N_2 = N_s$,

$$I_s = (2)/(1) (I_p)/(2) \quad (7)$$

or

$$I_s = I_p \quad (8)$$

the same value derived in equation (5).

The first switch 20 achieves the desired rapid current buildup in the core by minimizing the resistance in its circuit. Since this buildup requires a maximum power delivery from the power supply E_1 , the first switching transistor 20 is advantageously turned on for only the relatively short time interval required to build up the secondary current to the desired value. By way of specific example, for a current pulse width of 300 nanoseconds, the first switching transistor 20 is turned on for only 100 nanoseconds, a typical time required to buildup the desired current magnitude in the secondary, after which the first transistor 20 is turned off and the second transistor 25 turned on for the 300 nanosecond pulse width. Accordingly, most of the power is delivered to the core stack while the system is drawing minimum power from the power supply.

It will thus be seen that the system of the invention provides a primary/secondary turns ratio which is selectively varied over the pulse width of the output current pulse to provide the desired amplitude current flow through the memory core stack connected to secondary winding while limiting the overall power drain.

In the specific example above, a constant amplitude current is maintained over the pulse width. Similarly, the amplitude of the output current pulse may be increased or decreased over the pulse width by varying the number of turns on the two primary and secondary windings and/or by selecting a different value for the current limiting resistor 27.

Diode 26 is biased off when the first switching transistor is on; therefore, this diode prevents any current flow through the second current path regardless of the state of the second switching transistor 25. Thus, transistor 25 may be advantageously turned on at the same time that transistor 20 is turned on, since no current will pass through the second current path until the first switching transistor 20 is turned off resulting in forward bias on diode 26.

Also shown in FIG. 1 is a resistive network 30 connected between respective ends of the stack windings 14, 15 and ground, and sense amplifier 31 connected between the sense windings 14, 15 for distinguishing between ONE and ZERO signals in the voltage outputs of the bit plane.

The remaining circuit elements are not used functionally during the production of the current pulse but instead decrease the magnitude and time duration of the voltage transients which occur when the timing control stage 22 terminates the current pulse by turning off the second switching transistor 25. The current then flowing through the large inductance of the stack causes a voltage to be induced in the secondary winding 13 which in turn induces a voltage in primary windings 11 and 12.

On the primary side of the circuit, resistor 35 and capacitor 36 are connected in parallel with the primary windings 11, 12 current limiting resistor 27 and diode 26. The capacitor 36 is charged when the transient voltage is induced on the primary windings 11, 12, thereby minimizing the transient voltage buildup at the collector of transistor 25. Resistor 35 and capacitor 36 together critically damp the voltage across the primary windings when the second switching transistor 25 is turned off.

On the secondary side of the circuit, one side of the secondary winding 13 is connected to a diode 40 clamped to a voltage E_2 . The other side of the second-

ary is connected through a resistor 41 to ground. These additional circuit components substantially limit the magnitude of the transient induced voltages induced when the second switching transistor 25 is turned off and also substantially decreases the time required for the circuit to recover to its non-energized quiescent state.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, a core stack 16A is shown having a pair of windings 14A and 15A. Each of these windings 14A, 15A are respectively threaded through a plurality of memory cores 17A, as shown, and a return current path through ground is provided by diodes 18A, 19A. As described with reference to FIG. 1, cores 17A may represent a single bit plane of a coincident current memory and each of the windings 14A, 15A may represent the inhibit sense windings which are pulsed with a relatively short, e.g. 300 nanosecond, current pulse to inhibit the write current (on other windings not shown) in the bit plane when binary ZEROS are to be stored.

The power for this current pulse is provided by a power supply which supplies a voltage E_{1A} between ground and the emitters of transistors 50 and 51. The current pulse is initiated at time t_0 (FIG. 3) when timing control stage 22A (connected to the bases of respective transistors 50, 51) turns on transistor 50 which serves as a first switch. Advantageously, transistor 51 is also turned on at time t_0 although this switch does not supply current to the core stack until transistor 50 is turned off at time t_1 as described hereinafter. The collector of transistor 50 is connected directly to the core stack 16A. Accordingly, when transistor 50 is turned on by timing control stage 22A, a first current path is provided from voltage source E_{1A} through transistor 50 to the core stack 16A. This path has both minimal resistance and no inductance. As a result, the current flow in the core stack 16A builds up to the desired magnitude I_L in a minimum time interval between time t_0 and t_1 as graphically shown in FIG. 3.

After a predetermined time interval T_1 required to reach the desired current level in the core stack, transistor switch 50 is turned off. The collector of transistor 51 is connected to one side of a primary winding 52 of transformer 53. The other end of this primary winding is connected to a common junction 54 of the core stack and one end of the transformer secondary winding 55, the respective windings being wound in accordance with the dot convention shown. The other end of the secondary winding 55 is connected to ground by diode 56.

While both transistor switches 50 and 51 are on, the same voltage appears at both ends of the primary winding 52; hence, no current flows therethrough. However, at time t_1 at the end of time interval T_1 , when transistor switch 50 is turned off, the voltage at junction 54 due to transistor 50 being on is removed and a current I_1 flows through the primary winding 52 and induces a voltage in the secondary winding 55 which causes a current I_2 to flow therein. As a result of the manner in which these respective windings are wound with respect to each other with the dot convention as shown, the currents I_1 and I_2 add to produce a total current I_L through the core stack 16A or stated in equation form:

$$I_1 + I_2 = I_L$$

(9)

By choosing an appropriate number of turns on the primary and secondary windings 52, 53, the level of current flow through the core stack can be maintained during time interval T_2 with a substantial reduction in power from the power source which supplies E_{1A} . This power reduction is calculated as follows:

$$I_1/I_2 = N_s/N_p$$

(10)

where N_s is the number of turns in the secondary winding 55 and N_p is the number of turns in the primary winding 52. Equation (9) may be substituted into equation (10) to give an expression for I_1 in terms of I_L , N_p and N_s as follows:

$$I_1 = (I_L - I_2) (N_s)/(N_p)$$

(11)

$$N_p I_1 = I_L N_s - I_2 N_s$$

(12)

$$I_1 (N_p + N_s) = I_L N_s$$

(13)

$$I_1 = I_L N_s / (N_p + N_s)$$

(14)

In a similar manner, I_2 may be shown to be defined by the following equation:

$$I_2 = I_L N_p / (N_p + N_s)$$

(15)

In prior art current driver systems, the total power drain from the power supply is the product of the voltage source and the current being drawn therefrom, or $E_{1A} I_L$. In the embodiment of FIG. 2, a substantial portion (I_2) of the core stack current is not drawn from the power supply during time period T_2 . Accordingly, there is a reduction in the power drain during time period T_2 as follows:

$$\text{Power Drain Reduction} = E_{1A} I_2$$

(16)

or substituting equation (15),

$$\text{Power Drain Reduction} = E_{1A} I_L (N_1)/(N_1 + N_2)$$

(17)

In a typical system N_1 is 12, N_2 is 7, and time periods T_1 and T_2 are 100 and 300 nanoseconds respectively, and more than half the power is saved over the power drain of prior art current driver systems delivering the same level of current for the same period of time.

The resistive network 30A is connected between respective ends of the core stack windings 14A, 15A and sense amplifier 31A is connected between the sense windings 14A, 15A for distinguishing between ONE

and ZERO signals in the voltage outputs of the bit plane.

Diode 60 clamped to a voltage $-E_c$ prevents the voltage transient which occurs when switch 51 is closed at time t_2 from damaging transistor 51.

Resistor 61 terminates the common mode noise and also assists in recovery of the inhibit sense current when transistor 51 is closed at time t_2 .

The polarity of diodes 56 and 60 opposes the flow of current in both the primary and secondary windings 53, 55 when transistor 50 is turned on and thus prevents any power drain through the transformer windings during time period T_1 .

What is claimed is:

1. A system for supplying a predetermined magnitude of current to a core memory, said system having minimal current buildup time interval and minimal power supply drain, comprising:

a transformer having a primary and a secondary winding;

a first switch connected in series between said core memory and said power supply;

a second switch connected in series with said power supply and said primary winding of said transformer;

means connecting said transformer to said core stack so that the total current driven through said core stack when said primary winding is energized is greater than the current flow in said primary winding;

control means coupled to said first and second switches for

i. closing said first switch for a sufficient interval to drive a current of predetermined value through said core memory, and

ii. opening said first switch after said second switch has been closed.

2. The system described in claim 1 wherein said first switch provides a first current path to said core memory having minimal L/R time constant so that a current of predetermined value is driven through said core memory within a very short time interval.

3. The system described in claim 1 wherein said second switch and said transformer provide a second current path to said core memory when said first switch is opened, said second current path providing a current flow through said core memory greater in magnitude than the current drawn from said power supply.

4. The system described in claim 3 including means connected in said second current path for preventing the flow of current therethrough when said first switch is closed.

5. The system described in claim 4 wherein said means connected in said second current path is a diode.

6. The system described in claim 1 wherein said first and second switches are transistors.

7. The system described in claim 1 wherein said primary and secondary windings are so wound with respect to each other that a current flowing in said primary winding induces a voltage in said secondary winding which causes a current to flow in said secondary winding in a direction such that the total current flowing through the core stack is the sum of said currents flowing in said primary and secondary windings.

8. The system described in claim 7 wherein both said primary and secondary windings are connected to said core stack.

9. The system described in claim 1 wherein said control means opens said second switch after a predetermined time period.

10. A system for supplying a current pulse to a core memory, said system having a minimal current buildup time interval and a minimal power supply drain, comprising:

means for initially energizing the core stack from said power supply through a current path having a minimal L/R time constant so that a current of predetermined value is driven through said core stack within a very short time interval; and

means for maintaining said magnitude of current flowing through said core stack while reducing the power drain from said power supply, said means comprising a transformer coupled to said core stack and having a primary/secondary turns ratio such that current flowing through said core stack is greater in magnitude than the current drawn from said power supply.

11. A system drawing minimal power for supplying a current pulse of predetermined magnitude and minimal buildup time interval to the high inductance inhibit windings of a bit plane of a coincident current memory, comprising:

a transformer having a primary and a secondary winding;

means for connecting one end of said primary and secondary windings to a pair of inhibit windings of said bit plane, one of said windings being respectively threaded through a plurality of memory cores of said bit plane and the other of said windings being respectively threaded through the remaining memory cores of said bit plane;

a power supply supplying a voltage of predetermined magnitude;

a first transistor switch connected in series with said power supply and said pair of inhibit windings of said bit plane to provide a first current path through said inhibit windings when said first transistor switch is on;

a second transistor switch connected in series with said power supply and said primary winding of said transformer to provide a second current path to said pair of inhibit windings of said bit plane when said second transistor is on and said first transistor switch is off; and

time control means coupled to said first and second switches for

i. turning said first transistor switch on for a sufficient time interval to drive a current of predetermined value through said pair of inhibit windings of said bit plane, and

ii. turning off said first transistor switch after said second transistor switch has been turned on to decrease the current drawn from said power supply and thereby draw less power from said power supply while maintaining the desired magnitude of current through said pair of inhibit windings.

12. The system described in claim 11 wherein said primary and secondary windings are so wound with respect to each other that a current flow in said primary winding induces a voltage in said secondary winding which causes a current to flow in said secondary winding in a direction such that the total current flowing through said pair of inhibit windings is the sum of the

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current flowing in said primary and secondary windings.

13. The system described in claim 11 wherein said time control means turns on said first and second switches substantially simultaneously.

14. The method for generating a current pulse of predetermined magnitude for driving a high inductance winding of a memory core stack comprising the steps of:

energizing said core stack through a current path of minimum resistance and inductance so that a current of predetermined value flows through the core stack within a very short time interval; and subsequently energizing a transformer connected to said core stack so that the power drain is reduced while maintaining a desired magnitude of current

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flow through said core stack.

15. The method for generating a current pulse of predetermined magnitude for driving a high inductance winding of a memory core stack comprising the steps of:

energizing said core stack through a current path of minimum resistance and inductance so that a current of predetermined value flows through the core stack within a very short time interval; and subsequently energizing the primary winding of a transformer so that a current is caused to flow in the secondary winding such that the current flowing in said core stack is the sum of the currents flowing through said primary and secondary windings of said transformer.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,774,181 Dated November 20, 1973

Inventor(s) George H. Wells and Perry B. Persons

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 1, line 49, after "primary/" delete "-";
Col. 5, line 26, "emitters" should be --collectors--; line 29,
"whichserves" should be --which serves--; lines 34 and 35,
"collector" should be --emitter--; line 46 "collector" should be
--emitter--.

Signed and sealed this 23rd day of April 1974.

(SEAL)

Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents