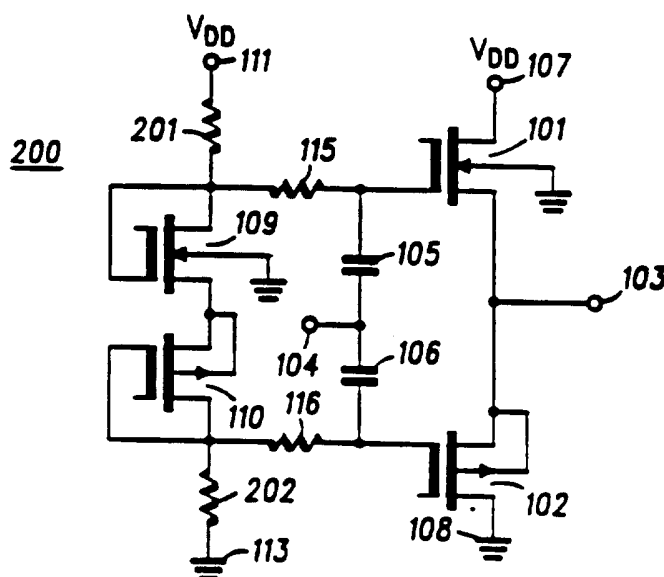




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(21) International Application Number: PCT/US93/06583 (22) International Filing Date: 13 July 1993 (13.07.93) (30) Priority data: 07/936,805 27 August 1992 (27.08.92) US (71) Applicant: MOTOROLA INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US). (72) Inventors: REESER, Glen, O. ; 241 North Bothwell, Palatine, IL 60067 (US). CONNELL, Lawrence, E. ; 2464 Rio Grande Circle, Naperville, IL 60565 (US). (74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept./JWH, 1303 East Algonquin Road, Schaumburg, IL 60196 (US).	(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>	

(54) Title: PUSH PULL BUFFER WITH NOISE CANCELLING SYMMETRY**(57) Abstract**

A buffer (200) having output devices (101 and 102) exhibiting complementary symmetry and configured as voltage-followers in push pull is biased for class AB operation by a bias network including two substantially equal resistors (201 and 202) arranged and configured to substantially reduce noise attributable to the bias circuit.

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5 PUSH PULL BUFFER WITH
 NOISE CANCELLING SYMMETRY

 Field of the Invention

10 This invention relates generally to amplifiers and
 in particular to push pull buffer amplifiers, and is more
 particularly directed toward a push pull buffer with a
 symmetrical bias network and symmetrical output
 device geometry designed to cancel internally generated
15 noise voltages.

 Background of the Invention

 Modern RF (radio frequency) communication units,
20 such as cellular telephones and conventional and trunked
 RF transceivers, generally employ frequency
 synthesizers rather than depending upon well-known
 crystal control technology. With a frequency
 synthesizer, reconfiguring a communication unit for
25 operation on a new frequency is a simple matter of
 reprogramming, whereas, with crystal control, a new
 pair of crystals is generally needed.

 In cellular telephone communication systems, it
 would simply be impracticable to provide a
30 communication unit with the enormous set of crystals
 required to cover a cellular system's 866 possible
 operating frequencies. Even trunked communication
 systems often employ a large number of possible
 operating frequencies. Furthermore, users of
35 conventional RF transceivers have come to view

synthesized communication units as desirable, since the ability to reprogram operating frequencies makes it easy to move communication units from system to system.

As is well known, a frequency synthesizer system
5 is only as good as its reference oscillator. A synthesizer's accuracy and stability is directly traceable to the accuracy and stability of the reference. Much work has been done to improve reference oscillator design, to the point where excellent accuracy and
10 stability over temperature have been achieved.

Even after a reference oscillator design has been perfected, however, the reference output must be buffered and distributed to various subsystems within a communication unit. For small, battery powered
15 communication units, such as portable cellular phones, at least two important design considerations immediately surface. First, the reference oscillator and associated buffering and signal distribution circuitry must use minimal power in order to conserve battery
20 life. Second, the distributed reference oscillator signal must have excellent spectral purity to minimize spurious signals and attendant denigration of system operation.

Reference signal buffer amplifiers are generally
25 biased for class AB operation in order to limit output stage power consumption. Furthermore, since space is often at a premium in hand-held communication units, most subassemblies, including reference oscillators and associated output buffers, are implemented using
30 integrated circuit (IC) or hybrid designs. This need to conserve space dictates that transistor geometries, particularly in low current applications such as bias networks, be kept as small as possible.

Unfortunately, the small geometry and low
35 operating current of transistors used in bias networks

yield poor noise characteristics that degrade overall amplifier noise figure. Accordingly, a need arises for a buffer stage that will exhibit good noise performance despite size and power constraints.

5

Summary of the Invention

This need and others are satisfied by the buffer amplifier of the present invention, which comprises a class AB amplifier circuit having a bias circuit operably coupled thereto, wherein the bias circuit includes two substantially equal resistors arranged and configured to substantially reduce noise attributable to the bias circuit.

15

Brief Description of the Drawings

FIG. 1 is a schematic diagram of a buffer stage of the prior art;

FIG. 2 is a schematic diagram of a buffer stage constructed in accordance with the present invention; and

FIG. 3 depicts, in block diagram form, an RF transceiver.

25

Description of a Preferred Embodiment

FIG. 1 illustrates an output buffer amplifier of the prior art, generally depicted by the numeral 100. A pair of output transistors (101 and 102) are connected together as voltage followers in push pull configuration, with an output (103) provided between the two devices (101 and 102). An input (104) is AC (alternating current) coupled to the output devices (101 and 102) through coupling capacitors (105 and 106). The output

30
35

transistors (101 and 102) are connected to a supply voltage (107) at one end, and to ground (108) at the other.

5 The output devices (101 and 102) are enhancement mode MOSFETs (metal-oxide-semiconductor field effect transistors) displaying complementary symmetry. That is, one device (101) is n-type and the other (102) is p-type. In push pull configuration, the transistors (101 and 102) are biased for class AB operation; that is,
10 neither output device conducts for a full cycle of the amplifier's sinusoidal input signal, but each device conducts for more than one-half cycle. This configuration is generally selected to limit power consumption. To minimize distortion while conserving
15 power, each device is generally biased close to its cut-in voltage (the point where the device begins to conduct) in order to eliminate crossover distortion.

In order to provide the appropriate bias voltages to the output devices (101 and 102), a pair of diode-
20 connected, complementary transistors (109 and 110) are series-connected as part of a bias network. The transistors used to provide bias (bias transistors) (109 and 110) are connected to supply voltage (111) at one end, through a series resistor (114), and to a current
25 source (112) at the other. The current source is then coupled to ground (113). This collection of components, including the bias transistors (109 and 110), the series resistor (114) and the current source (112), along with two resistors (115 and 116) that couple bias voltages to
30 the output devices (101 and 102), may be termed a bias network.

A bias network of the type just described performs adequately in terms of providing proper bias voltages to the output devices over a relatively wide temperature
35 range. Unfortunately, the geometry of the bias

transistors (109 and 110) is deliberately kept small to conserve valuable IC real estate, and the current level provided by the current source (112) is kept small to conserve power. Under these operating conditions,
5 excessive noise voltages generated within the bias network are transferred to the output devices (101 and 102). It is for just such a problem that the buffer of the present invention offers relief.

The excessive noise voltages just described are
10 due in part to thermal noise within the bias transistors (109 and 110), and in part to flicker noise traceable to trapped charges in the oxides formed during IC construction. In fact, flicker noise is even more pronounced in devices of small geometry.

15 The circuit of FIG. 2 is a push pull buffer constructed in accordance with the present invention and generally depicted by the numeral 200. Although MOSFET devices are depicted, the invention is equally applicable to circuitry constructed using bipolar transistors. The
20 output devices shown in FIG. 2 (101 and 102) are configured and biased for class AB operation, similar to the configuration of FIG. 1. In fact, much of the circuit of FIG. 2 functions in the same way described in conjunction with FIG. 1, so further description will be
25 limited for the sake of brevity.

The bias networks of FIGS. 1 and 2 differ in order to overcome the excessive noise generation phenomenon associated with bias networks of the prior art. In the circuit of FIG. 2, in addition to two diode-connected
30 transistors (109 and 110) in the bias network, there are two closely matched (equal in value) resistors (201 and 202) connected in series with the bias transistors (109 and 110). Generally, resistance values greater than
35 application. In the preferred embodiment, resistors

having a value of 25K are used. One of the resistors (201) couples the bias transistors (109 and 110) to supply voltage, while the other resistor (202) couples the bias transistors (109 and 110) to ground (113).

- 5 Resultant bias voltages are coupled to the output devices (101 and 102) through coupling resistors (115 and 116).

Since symmetry is maintained throughout, not only in the bias network, but in the output stage as well, noise voltages generated in the bias network are
10 cancelled at the output. The matched bias resistors (201 and 202) present equal impedances at the top and bottom of the bias network, so that noise voltages generated in between the two resistors (i.e., within the bias transistors) couple in equal but opposite senses to the
15 amplifier transistors (101 and 102). Since the output devices (101 and 102) are complementary and have similar transconductances, the noise voltages will have no effect on the signal output (103). Qualitatively, one can categorize the balanced, unwanted noise voltages as
20 fully differential mode signals that have been rejected by a common mode only amplifier.

As mentioned previously, precision reference oscillators and their associated low-noise buffer amplifiers find widespread application in RF
25 communication equipment, with low-current oscillator and buffer implementations being especially well-suited to portable applications. FIG. 3 depicts, in block diagram form, an RF communication unit generally depicted by the numeral 300.

30 The RF communication unit (300) includes an antenna (301) for transmission and reception of RF signals. The antenna generally couples to an antenna switch (302) that switches the signal path between a transmitter (303) and a receiver (304), well known in
35 the art. Of course, for full-duplex communication, the

antenna switch (302) would be replaced by a directional coupler. Of course, if the communication unit (300) were designed for receiving RF signals only, as is a radio pager, neither the antenna switch (302) nor the
5 transmitter portion (303) would be required.

Modern communication units generally employ a well-known frequency synthesizer (305) to control operating frequency. It is even possible, in some applications, for separate synthesizers to be used for
10 transmitter and receiver. In either case, a frequency synthesizer requires a reference oscillator (306), for which designs are well-developed in the pertinent art, to provide an accurate, temperature-independent reference signal for maximum frequency accuracy and stability.

15 In conjunction with the reference oscillator (306), a buffer (200) such as the one depicted in FIG. 2 is used to ensure that a sinusoidal reference signal with minimal harmonic content and with a level output over variations in temperature is distributed to the
20 synthesizer (305), as well as to any other subsystems (not shown) that may require an accurate, stable reference signal of relatively high spectral purity.

What is claimed is:

Claims

1. An apparatus comprising:
 - a class AB amplifier circuit;
 - 5 a bias circuit operably coupled to the class AB amplifier circuit, wherein the bias circuit includes two substantially equal resistors arranged and configured to substantially reduce noise attributable to the bias circuit.

2. The apparatus of claim 1, wherein the bias circuit includes two active elements coupled between a voltage source and ground, with the two substantially equal resistors configured in series with the two active
5 elements.

3. The apparatus of claim 2, wherein a first one of the two substantially equal resistors couples the two active elements to the voltage source, and a second one
10 of the two substantially equal resistors couples the two active elements to ground.

4. The apparatus of claim 2, wherein both of the two active elements are diode-connected
15 transistors.

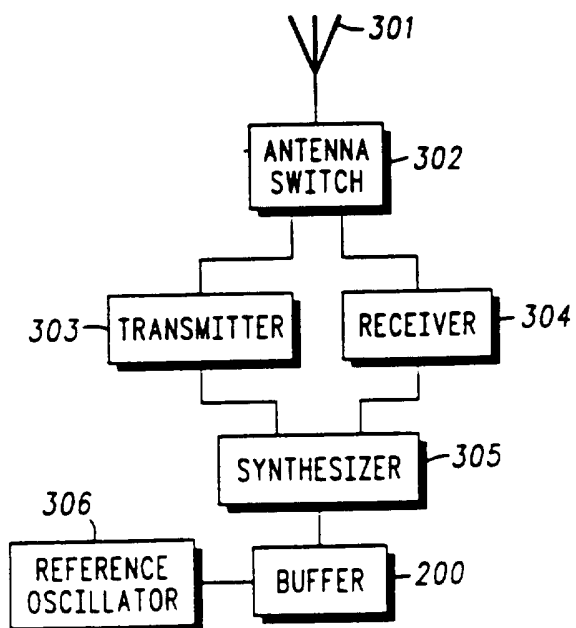
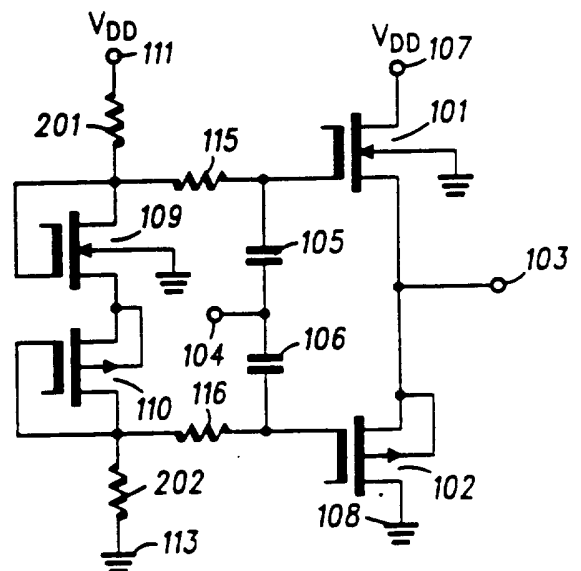
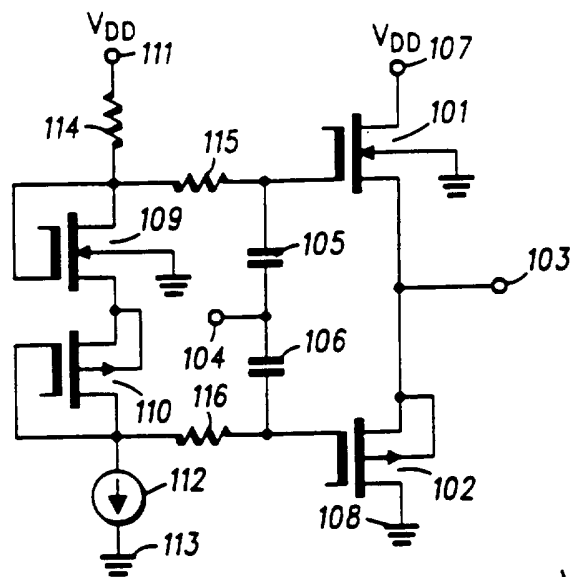
5. The apparatus of claim 4, wherein the transistors are MOSFETs.

20 6. The apparatus of claim 1, wherein each of the substantially equal resistors has a resistance greater than 10K.

7. The apparatus of claim 1, wherein each of
25 the substantially equal resistors has a resistance substantially equal to 25K.

8. A push pull buffer comprising:
an output stage including:
a pair of complementary MOSFETs configured
as voltage followers and connected together in push pull
5 with an output between the pair;
a bias network including:
a pair of diode-connected complementary
MOSFETs arranged in series;
a pair of matched resistors, with one of the
10 pair of resistors connected to one side of the pair of
diode-connected MOSFETs, and the other of the pair of
resistors connected to the other side of the pair of
diode-connected MOSFETs;
a pair of coupling resistors operably
15 interconnecting the bias network and the output stage to
bias the complementary MOSFETs of the output stage for
class AB operation;
such that noise voltages generated between the
pair of matched resistors are substantially equally
20 divided between the complementary MOSFETs of the
output stage, resulting in essentially no net change in
voltage at the output.

9. An RF communication unit comprising:
- an antenna;
 - a receiver portion coupled to the antenna that receives and demodulates RF signals;
 - 5 a synthesizer coupled to the receiver that controls receiver operating frequency;
 - a reference oscillator that provides an accurate, stable reference signal for the synthesizer, the reference oscillator coupled to the synthesizer through a
 - 10 buffer that includes:
 - a class AB amplifier circuit;
 - a bias circuit operably coupled to the class AB amplifier circuit, wherein the bias circuit includes two substantially equal resistors arranged and
 - 15 configured to substantially reduce noise attributable to the bias circuit.



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06583

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : H03F 3/18; H03B 5/00; H04B 1/06

US CL : 455/260, 330/264, 331/117R

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/260; 330/264; 331/117R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
E, Y	US, A, 5,230,088 (Kramer, Jr. et al) 20 July 1993. See figure 1 and column 2, lines 47-68.	9
Y	US, A, 4,403,198 (Muller) 06 September 1983. See figure 3 and entire document.	1-9
Y	US A, 4,433,303 (Sasaki) 21 February 1984. See column 2, lines 1-68.	1-9
Y	US A, 4,939,790 (Sgrignoli) 03 July 1990. See figure 3 and column 3.	9
Y	US, A, 4,335,360 (Hoover) 15 June 1982. See figure 2 and entire document.	1-9

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/06583

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,542,531 (Fukumura) 17 September 1985. See figure 1 and column 2.	9
A	US, A, 3,432,759 (Stone) 11 March 1969. See entire document	
Y	US, A, 5,107,228 (Pham et al) 21 April 1992. See figure 2 and entire document.	9
P, Y	US, A, 5,218,325 (Trelewicz et al) 08 June 1993. See entire document and figure 1.	9