(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
05 April 2018 (05.04.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/064458 A1

(51) International Patent Classification:
H01L 21/66 (2006.01)

(21) International Application Number:
PCT/US2017/054264

(22) International Filing Date:
29 September 2017 (29.09.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/281,175 30 September 2016 (30.09.2016) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

(54) Title: THREE DIMENSIONAL MAPPING OF A WAFER

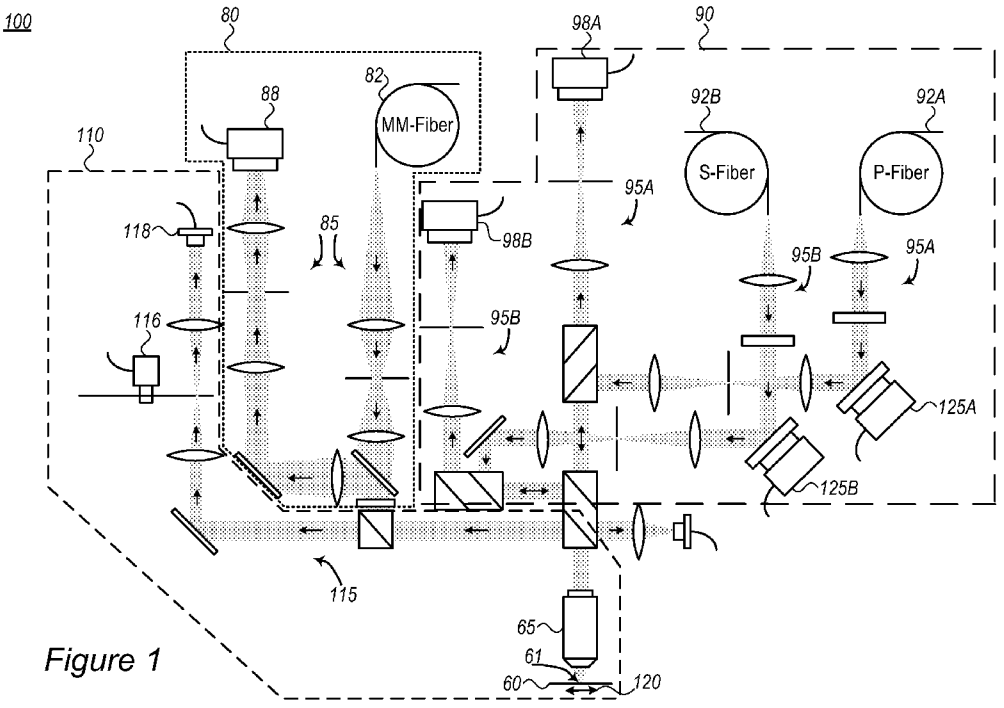

Figure 1

(57) Abstract: Methods and scatterometry overlay metrology tools are provided, which scan a wafer region, perform focus measurements during the scanning to extract therefrom phase information, and derive depth data of the scanned wafer region from the extracted phase information. The depth information, relating to a dimension perpendicular to the wafer, may be derived along lines or surfaces, providing profilometry and surface data, respectively. The depth data may be used to locate metrology targets, as well as to provide material properties concerning wafer layers, to estimate process variation and to improve the overlay measurements.

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[Continued on next page]

MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

THREE DIMENSIONAL MAPPING OF A WAFER

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

[0001] The present invention relates to the field of metrology, and more particularly, to scatterometry overlay metrology.

2. DISCUSSION OF RELATED ART

[0002] Scatterometry overlay metrology tools use focus measurements to determine the degree of focus on the metrology targets on which overlay data is measured.

[0003] Kocher 1983 (Automated Foucault test for focus sensing, Applied Optics 22(12): 1887-1892) teaches focus measurements using a chopper wheel, a bicell photodetector, and an electronic phase detector to obtain a linear focus error voltage for an isolated point image, also known as knife edge focusing due to their utilization of the dependency of the direction of the knife-edge shadow motion (e.g., chopper wheel member) on the axial position of the edge relative to the focus.

SUMMARY OF THE INVENTION

[0004] The following is a simplified summary providing an initial understanding of the invention. The summary does not necessarily identify key elements nor limits the scope of the invention, but merely serves as an introduction to the following description.

[0005] One aspect of the present invention provides a method comprising: scanning a wafer region by a metrology tool, performing focus measurements by the metrology tool during the scanning and extracting therefrom phase information, and deriving depth data of the scanned wafer region from the extracted phase information.

[0006] These, additional, and/or other aspects and/or advantages of the present invention are set forth in the detailed description which follows; possibly inferable from the detailed description; and/or learnable by practice of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] For a better understanding of embodiments of the invention and to show how the same may be carried into effect, reference will now be made, purely by way of example, to the accompanying drawings in which like numerals designate corresponding elements or sections throughout.

[0008] In the accompanying drawings:

[0009] **Figure 1** is a high level schematic illustration of a metrology tool, according to some embodiments of the invention;

[0010] **Figure 2** is an exemplary schematic illustration of focus signals and the linearity of its phase on calibration curve, according to some embodiments of the invention;

[0011] **Figure 3** is a high level flowchart illustrating a method, according to some embodiments of the invention; and

[0012] **Figure 4** is a high level schematic block diagram of scatterometry overlay metrology tools, according to some embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] In the following description, various aspects of the present invention are described. For purposes of explanation, specific configurations and details are set forth in order to provide a thorough understanding of the present invention. However, it will also be apparent to one skilled in the art that the present invention may be practiced without the specific details presented herein. Furthermore, well known features may have been omitted or simplified in order not to obscure the present invention. With specific reference to the drawings, it is stressed that the particulars shown are by way of example and for purposes of illustrative discussion of the present invention only, and are presented in the cause of providing what is believed to be the most useful and readily understood description of the principles and conceptual aspects of the invention. In this regard, no attempt is made to show structural details of the invention in more detail than is necessary for a fundamental understanding of the invention, the description taken with the drawings making apparent to those skilled in the art how the several forms of the invention may be embodied in practice.

[0014] Before at least one embodiment of the invention is explained in detail, it is to be understood that the invention is not limited in its application to the details of construction and the arrangement of the components set forth in the following description or illustrated in the drawings. The invention is applicable to other embodiments that may be practiced or carried out in various ways as well as to combinations of the disclosed embodiments. Also, it is to be understood that the phraseology and terminology employed herein is for the purpose of description and should not be regarded as limiting.

[0015] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing", "computing", "calculating", "determining", “enhancing” or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulates and/or transforms data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

[0016] Methods and scatterometry overlay metrology tools are provided, which scan a wafer region, perform focus measurements during the scanning (e.g., using the knife edge method based on the Foucault test as taught by Kocher 1983) to extract therefrom phase information, and derive depth data of the scanned wafer region from the extracted phase information. The depth information, relating to a dimension perpendicular to the wafer, may be derived along lines or surfaces, providing profilometry and surface data, respectively. The depth data may be used to locate metrology targets, as well as to provide material properties concerning wafer layers, to estimate process variation and to improve the overlay measurements.

[0017] **Figure 1** is a high level schematic illustration of a metrology tool **100**, according to some embodiments of the invention. Metrology tool **100** comprises, schematically, an overlay measurement part **90**, a wafer imaging part **80** and a focus measurement part **110**. Overlay measurement part **90** may be implemented using polarized illumination sources **92A**, **92B** (e.g., S- and P- polarized optical fibers, with S- and P- denoting different, e.g., orthogonal, polarization states) and corresponding detectors **98A**, **98B**, with optical paths **95A**, **95B** that include optical elements for controlling the respective beams, directing the

illumination via an objective **65** onto a wafer region **61** on a wafer **60**, and delivering collected scattered radiation to corresponding detectors **98A**, **98B** via the optical elements. The optical elements, which comprise e.g., corresponding apodizers, aperture and field stops, lenses and beam splitters (polarizing beam splitters where polarized radiation is handled), are arranged to control and optimize the respective beams along optical paths **95A**, **95B**. Wafer imaging part **80** utilizes non-polarized illumination, e.g., by a multimode (MM) optical fiber **82**, for imaging a wafer region **61** on a camera **88** such as a CCD (charge coupled detector) via an optical path **85** with optical elements configured to control the corresponding illumination and collection beams directed via objective **65** to wafer region **61**.

[0018] Focus measurement part **110** uses the illumination from overlay measurement part **90** (e.g., laser polarized illumination) and/or from wafer imaging part **80** (e.g., non-polarized white light illumination), which is guided via a separate optical path **115**, to derive a focus signal relating to the degree of focus of wafer region **61**. Focus measurement part **110** typically comprises a chopper **116** at field plane and a focus detector **118** such as a bi-cell which measures the reflected illumination from wafer **60** which passes through chopper **116**. When a laser beam (e.g., from any of illumination sources **82**, **92A**, **92B**) hits wafer **60**, part of the reflected light is collected through focus channel **110**, modulated by chopper **116** and is collected by detector **118** (e.g., bi-cell with two photodiodes). The focus signal provides the phase between the signals of the two photodiode and is used to measure the vertical position of wafer **60** in relation to objective **65**, due to its nearly linear relationship therewith.

[0019] **Figure 2** is an exemplary schematic illustration of focus signals **111** and the linearity of its phase on calibration curve **112**, according to some embodiments of the invention. Signal **111A** illustrates a case in which wafer region **61** is out of focus, resulting in a phase **112** (marked φ) between the signals measured by the cells (marked A and B); while signal **111B** illustrates a case in which wafer region **61** is in focus, resulting in a zero phase between the signals measured by the cells (which therefore overlap). The dependency of the degree of de-focus on phase **112** is shown to be linear, at least in the region of $\varphi=0$ (in-focus). Phase curve **112** or similar curves, may be used to calibrate the distance of wafer region **61** (i.e., the wafer de-focus) from objective **65**, according to

measured phase (depending on wavelength and apodizer, the illustrated non-limiting example is for wavelength of 685nm and a 0.2 top hat apodizer).

[0020] Focus measurement part **110** may be configured to provide two or three dimensional measurements of the surface of a certain wafer region, which provide information concerning the vertical dimension (perpendicular to the wafer plane) as well. For this purpose, metrology tool is configured to (i) enable scanning wafer region **61** (possibly including one or more metrology target cells), (ii) perform focus measurements by focus measurement part **110** during the scanning and extracting phase information therefrom (as exemplified in **Figure 2**), and (iii) derive depth data (i.e., topographic information, such as 2D profilometry data and/or 3D surface data, relating to a vertical direction, perpendicular to the wafer region) of the scanned wafer region from the extracted phase information.

[0021] Metrology tool may be further configured to derive material properties of wafer region **61** from the extracted phase information, such as data concerning the refractive index of wafer region **61**, or ratios of segmentation of wafer region **61**.

[0022] The scanning of wafer region **61** may be carried out by moving a stage (illustrated schematically in **Figure 1** by double-headed arrow **120**) that supports wafer **60**. Stage movements **120** may be horizontal, in a plane parallel to wafer **60**. Alternatively or complementarily, the scanning of wafer region **61** may be carried out using scan mirrors **125A**, **125B** (see **Figure 1**, and/or scan mirrors **125** in **Figure 4**) of overlay measurement part **90** in metrology tool **100**. In particular, the focus measurements may be carried with non-polarized and/or with polarized illumination from MM fiber **82** and/or single mode fiber(s) (e.g., S- and/or P- fibers **92A**, **92B**), respectively.

[0023] Metrology tool **100** may be configured, e.g., via a metrology module, to utilize the derived depth data (i.e., topographic information, or surface mapping) for any of: (i) locating metrology targets in wafer region **61**, e.g., using signal edges, possibly avoiding the current need to grab additional images, and particularly in low accuracy cases such as dark wafer region **61**; (ii) estimate process variation in wafer region **61**, e.g., process variation in term of thickness, refractive index, segmentation ratio; and (iii) improve overlay measurements by the metrology tool, e.g., by obtaining better overlay

correctables, possibly by including corrections for process variation, and possibly all across wafer **60** in consecutive measurements.

[0024] In certain embodiments, a laser beam may be scanned across the wafer surface while focus signal **111** (e.g., the bi-cell signal) is recorded in order to calculate the phase signal and from it the distance signal. The laser scanning may be carried out in one direction to obtain (2D) profilometry information, and/or the laser scanning may be carried out in two directions to obtain (3D) surface information. The scanning may be realized with the help of the machine stage (**120**) and/or by scanning mirrors (**125A**, **125B**). Calibration curve **112** (see example in **Figure 2**) may be used to relate the phase of focus signal **111** to the vertical distance between wafer region **61** and objective **65** (depending on wavelength and apodizer). Focus signal **111** and depth data may be used to derive various material properties of wafer region **61** such as layer thickness, refractive index and segmentation ratio (part of developed photoresist in relation of non-developed photoresist), as well as any other property which influences the effective thickness signal.

[0025] **Figure 3** is a high level flowchart illustrating a method **200**, according to some embodiments of the invention. The method stages may be carried out with respect by metrology tool **100** described above, which may optionally be configured to implement method **200**. Method **200** may be at least partially implemented by at least one computer processor, e.g., in a metrology module. Certain embodiments comprise computer program products comprising a computer readable storage medium having computer readable program embodied therewith and configured to carry out of the relevant stages of method **200**. Certain embodiments comprise target design files of respective targets designed by embodiments of method **200**.

[0026] Method **200** comprises scanning a wafer region (possibly including one or more metrology target cells) by a metrology tool (stage **210**), performing focus measurements by the metrology tool during the scanning and extracting therefrom phase information (stage **220**), and deriving depth data (i.e., topographic information such as 2D profilometry data and/or 3D surface data, relating to a vertical direction, perpendicular to the wafer region) of the scanned wafer region from the extracted phase information (stage **230**).

[0027] Method **200** may further comprise deriving material properties of the wafer region from the extracted phase information (stage **235**), such as data concerning the refractive index of the wafer region.

[0028] Scanning **210** may be carried out by moving a stage that supports the wafer (stage **212**). Stage movements **120** may be horizontal, in a plane parallel to wafer **60**. Scanning **210** may be carried out using scan mirrors of the metrology tool (stage **214**).

[0029] Method **200** may further comprise any of: locating metrology targets in the wafer region using the derived depth data (stage **240**), estimating process variation in the wafer region from the derived depth data (stage **250**), and improving overlay measurements by the metrology tool, using the derived depth data (stage **260**).

[0030] **Figure 4** is a high level schematic block diagram of scatterometry overlay metrology tool **100**, according to some embodiments of the invention. Elements from **Figures 1** and **4** may combined to provide embodiments of the invention. Scatterometry overlay metrology tool **100**, comprising at least overlay measurement part **90** and focus measurement part **110**, may be configured to scan wafer region **61** and/or wafer **60**, performing focus measurements during the scanning and extract phase information from the focus measurements (e.g., by focus measurement part **110**), and derive depth data of the scanned wafer region from the extracted phase information, e.g., by a metrology module **130** associated with at least one computer processor **135**.

[0031] The scanning may be carried out by moving stage **120** supporting wafer **60** (e.g., horizontally, parallel to wafer **60**) and/or using scan mirrors **125** and the depth data may be two or three dimensional - providing profilometry and/or surface information, respectively.

[0032] Metrology module **130** may be further configured to derive material properties of wafer region **61** from the extracted phase information, such as layer thickness of one or more layer, refractive indices of one or more layer, segmentation ratios in one or more layers, etc. Metrology module **130** may be configured to use the derived depth data to locate metrology targets on wafer **60**, estimate process variation in wafer **60** and/or improve overlay measurements.

[0033] Certain embodiments comprise a computer program product comprising a non-transitory computer readable storage medium having computer readable program

embodied therewith (and be possible run be processor(s) **135**), the computer readable program configured to derive depth data of a scanned wafer region from phase information extracted from focus measurements, wherein the derived depth data is with respect to at least a vertical direction, perpendicular to the wafer region. The computer readable program may be further configured to derive material properties of the wafer region from the extracted phase information, the derived material properties being related to at least one of a refractive index and a segmentation ratio, of at least one wafer layer. The computer readable program may be further configured to provide from the derived depth data 2D profilometry information and/or 3D surface information. The computer readable program may be further configured to locate metrology targets in the wafer region using the derived depth data. The computer readable program may be further configured to estimate process variation in the wafer region from the derived depth data. The computer program product may be integrated in metrology module **130** of scatterometry overlay metrology tool **100** and the computer readable program may be further configured to improve overlay measurements by metrology tool **100**, using the derived depth data. Certain embodiments comprise scatterometry overlay metrology tool 100 comprising the computer program product.

[0034] Advantageously, disclosed metrology tools **100** and methods **200** implement focus measurements for measuring wafer topography with scatterometry overlay metrology tools, thus simplifying wafer topography measurements on one hand, in particular making it less time consuming with respect e.g., to Linnik interferometers and imaging tools (which use white light interferometry), while, on the other hand, improving scatterometry overlay measurements and/or enhancing target and/or wafer positioning.

[0035] Aspects of the present invention are described above with reference to flowchart illustrations and/or portion diagrams of methods, apparatus (systems) and computer program products according to embodiments of the invention. It will be understood that each portion of the flowchart illustrations and/or portion diagrams, and combinations of portions in the flowchart illustrations and/or portion diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions,

which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart and/or portion diagram or portions thereof.

[0036] These computer program instructions may also be stored in a computer readable medium that can direct a computer, other programmable data processing apparatus, or other devices to function in a particular manner, such that the instructions stored in the computer readable medium produce an article of manufacture including instructions which implement the function/act specified in the flowchart and/or portion diagram or portions thereof.

[0037] The computer program instructions may also be loaded onto a computer, other programmable data processing apparatus, or other devices to cause a series of operational steps to be performed on the computer, other programmable apparatus or other devices to produce a computer implemented process such that the instructions which execute on the computer or other programmable apparatus provide processes for implementing the functions/acts specified in the flowchart and/or portion diagram or portions thereof.

[0038] The aforementioned flowchart and diagrams illustrate the architecture, functionality, and operation of possible implementations of systems, methods and computer program products according to various embodiments of the present invention. In this regard, each portion in the flowchart or portion diagrams may represent a module, segment, or portion of code, which comprises one or more executable instructions for implementing the specified logical function(s). It should also be noted that, in some alternative implementations, the functions noted in the portion may occur out of the order noted in the figures. For example, two portions shown in succession may, in fact, be executed substantially concurrently, or the portions may sometimes be executed in the reverse order, depending upon the functionality involved. It will also be noted that each portion of the portion diagrams and/or flowchart illustration, and combinations of portions in the portion diagrams and/or flowchart illustration, can be implemented by special purpose hardware-based systems that perform the specified functions or acts, or combinations of special purpose hardware and computer instructions.

[0039] In the above description, an embodiment is an example or implementation of the invention. The various appearances of "one embodiment", "an embodiment", "certain

embodiments" or "some embodiments" do not necessarily all refer to the same embodiments. Although various features of the invention may be described in the context of a single embodiment, the features may also be provided separately or in any suitable combination. Conversely, although the invention may be described herein in the context of separate embodiments for clarity, the invention may also be implemented in a single embodiment. Certain embodiments of the invention may include features from different embodiments disclosed above, and certain embodiments may incorporate elements from other embodiments disclosed above. The disclosure of elements of the invention in the context of a specific embodiment is not to be taken as limiting their use in the specific embodiment alone. Furthermore, it is to be understood that the invention can be carried out or practiced in various ways and that the invention can be implemented in certain embodiments other than the ones outlined in the description above.

[0040] The invention is not limited to those diagrams or to the corresponding descriptions. For example, flow need not move through each illustrated box or state, or in exactly the same order as illustrated and described. Meanings of technical and scientific terms used herein are to be commonly understood as by one of ordinary skill in the art to which the invention belongs, unless otherwise defined. While the invention has been described with respect to a limited number of embodiments, these should not be construed as limitations on the scope of the invention, but rather as exemplifications of some of the preferred embodiments. Other possible variations, modifications, and applications are also within the scope of the invention. Accordingly, the scope of the invention should not be limited by what has thus far been described, but by the appended claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A method comprising:

   scanning a wafer region by a metrology tool,

   performing focus measurements by the metrology tool during the scanning and extracting therefrom phase information, and

   deriving depth data of the scanned wafer region from the extracted phase information.
2. The method of claim 1, further comprising deriving material properties of the wafer region from the extracted phase information.
3. The method of claim 2, wherein the derived material properties are related to at least one of a refractive index and a segmentation ratio, of at least one wafer layer.
4. The method of claim 1, wherein the wafer region comprises at least one metrology target cell.
5. The method of claim 1, wherein the scanning is carried out by moving a stage supporting the wafer.
6. The method of claim 1, wherein the scanning is carried out using scan mirrors of the metrology tool.
7. The method of claim 1, wherein the derived depth data is with respect to at least a vertical direction, perpendicular to the wafer region.
8. The method of claim 1, wherein the deriving is carried out with respect to one surface direction of the wafer region to provide 2D (two dimensional) profilometry information.
9. The method of claim 1, wherein the deriving is carried out with respect to one surface direction of the wafer region to provide 3D (three dimensional) surface information.
10. The method of claim 1, further comprising locating metrology targets in the wafer region using the derived depth data.
11. The method of claim 1, further comprising estimating process variation in the wafer region from the derived depth data.

12. The method of claim 1, further comprising improving overlay measurements by the metrology tool, using the derived depth data.
13. A scatterometry overlay metrology tool configured to carry out the method of any one of claims 1-12.
14. A computer program product comprising a non-transitory computer readable storage medium having computer readable program embodied therewith, the computer readable program configured to derive depth data of a scanned wafer region from phase information extracted from focus measurements, wherein the derived depth data is with respect to at least a vertical direction, perpendicular to the wafer region.
15. The computer program product of claim 14, wherein the computer readable program is further configured to derive material properties of the wafer region from the extracted phase information, the derived material properties being related to at least one of a refractive index and a segmentation ratio, of at least one wafer layer.
16. The computer program product of claim 14, wherein the computer readable program is further configured to provide from the derived depth data 2D profilometry information and/or 3D surface information.
17. The computer program product of claim 14, wherein the computer readable program is further configured to locate metrology targets in the wafer region using the derived depth data.
18. The computer program product of claim 14, wherein the computer readable program is further configured to estimate process variation in the wafer region from the derived depth data.
19. The computer program product of claim 14, integrated in a metrology module of a scatterometry overlay metrology tool, wherein the computer readable program is further configured to improve overlay measurements by the metrology tool, using the derived depth data.
20. A scatterometry overlay metrology tool comprising the computer program product of any one of claims 14-19.

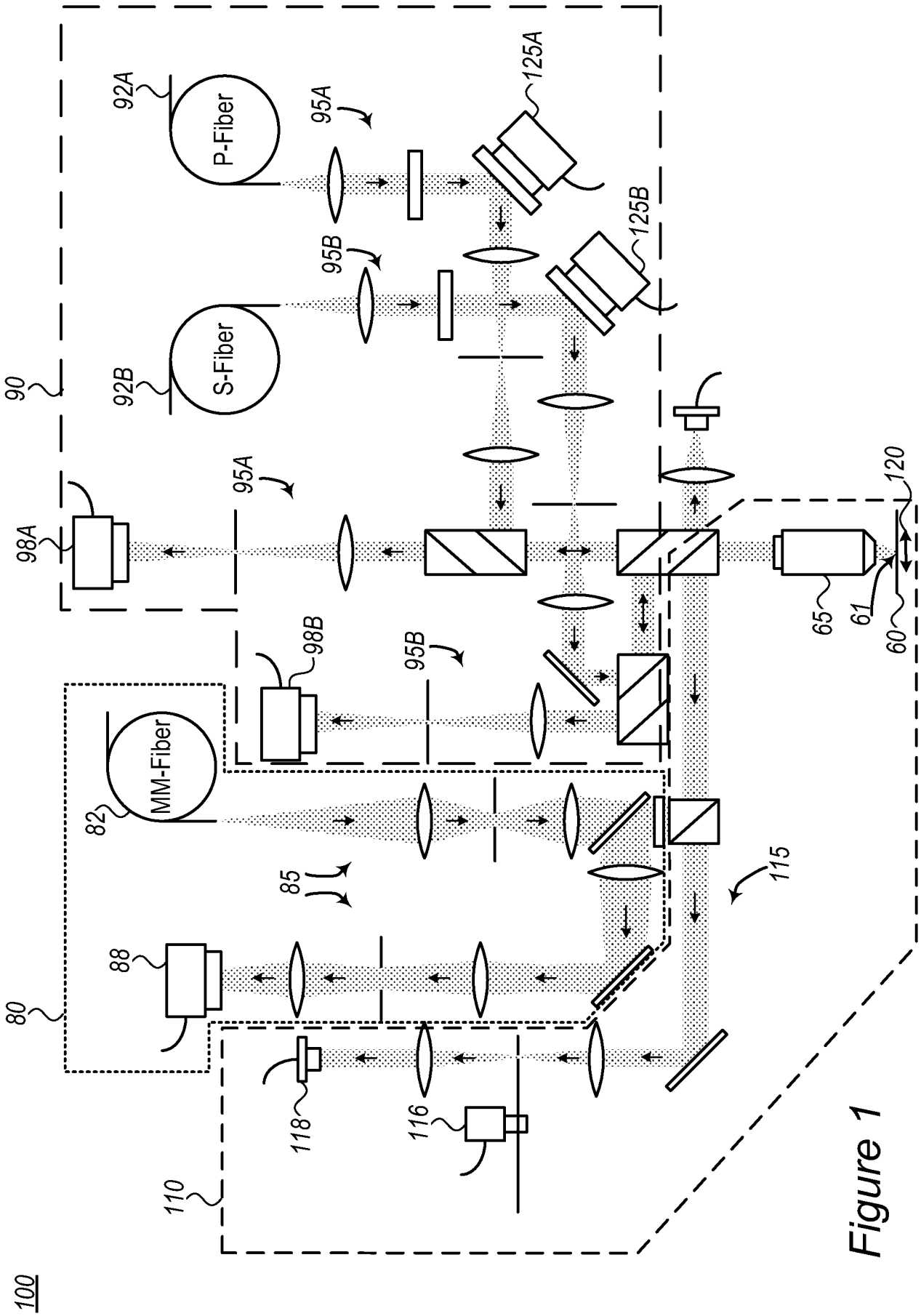
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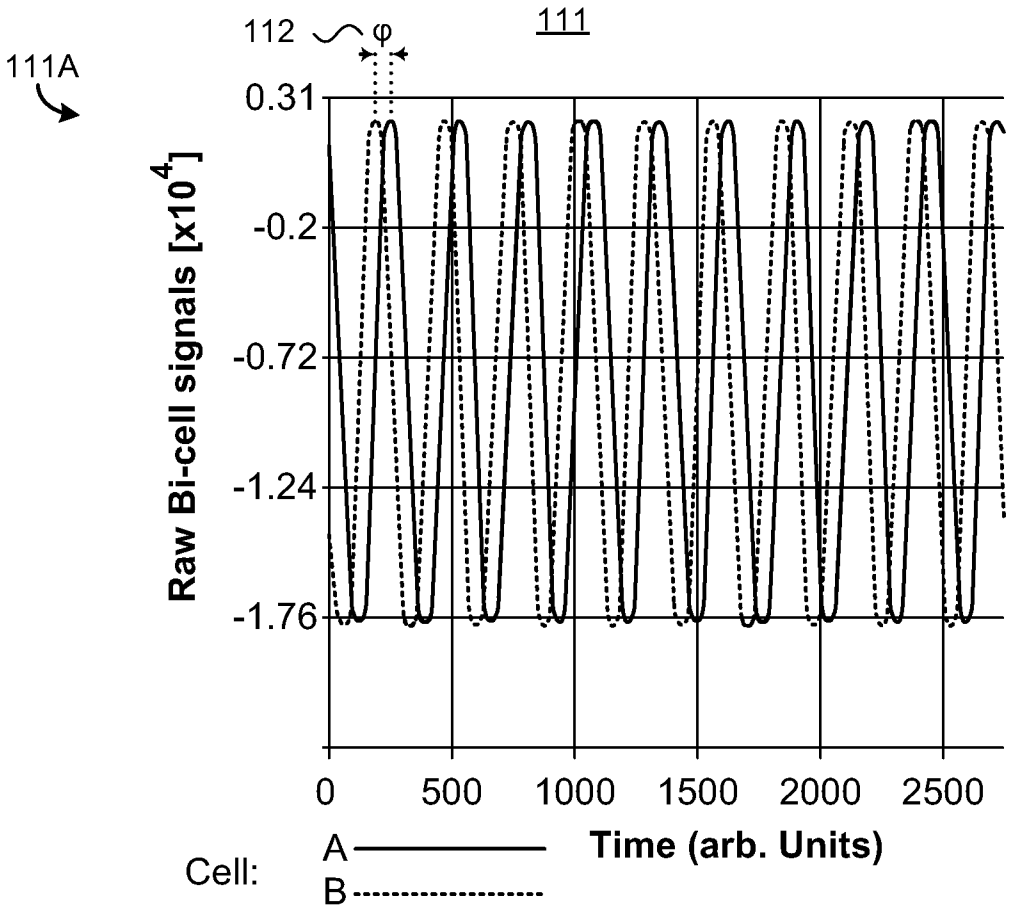
Figure 1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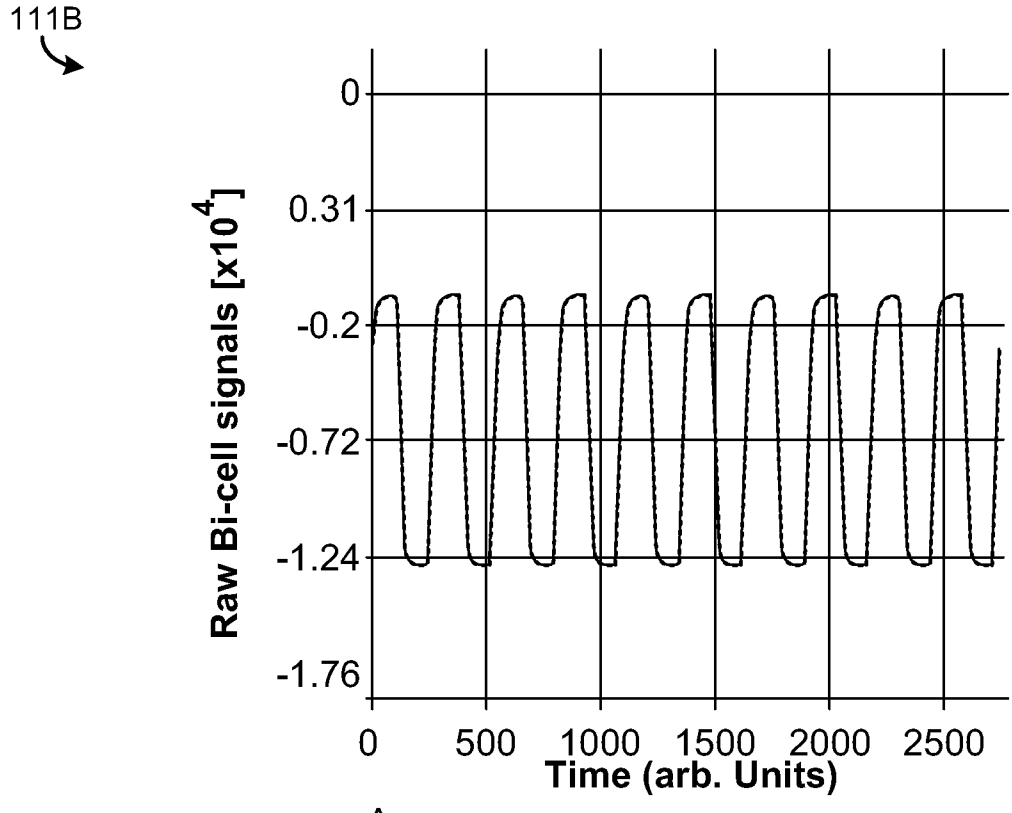
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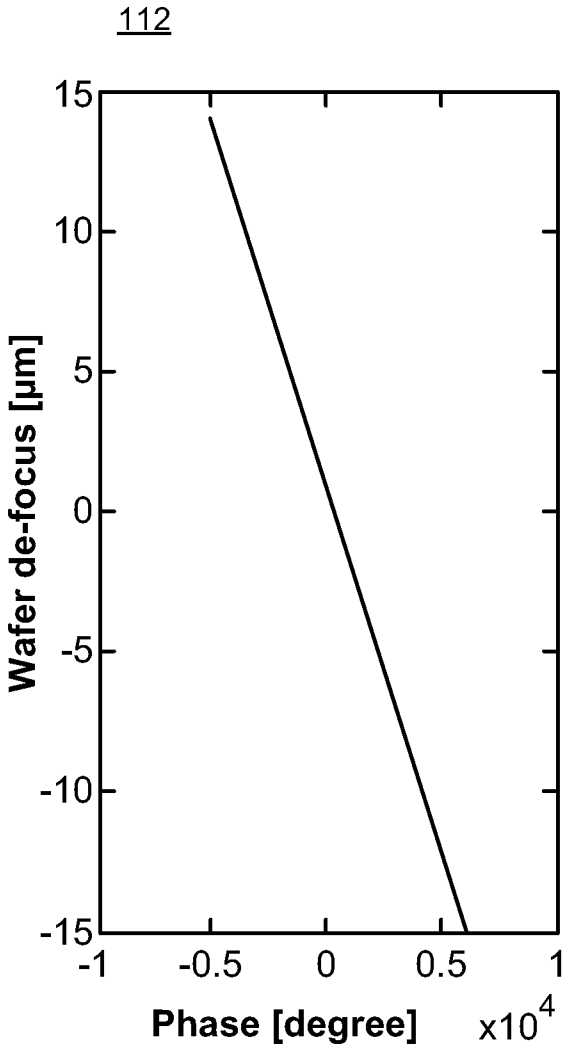
A
B

Figure 2



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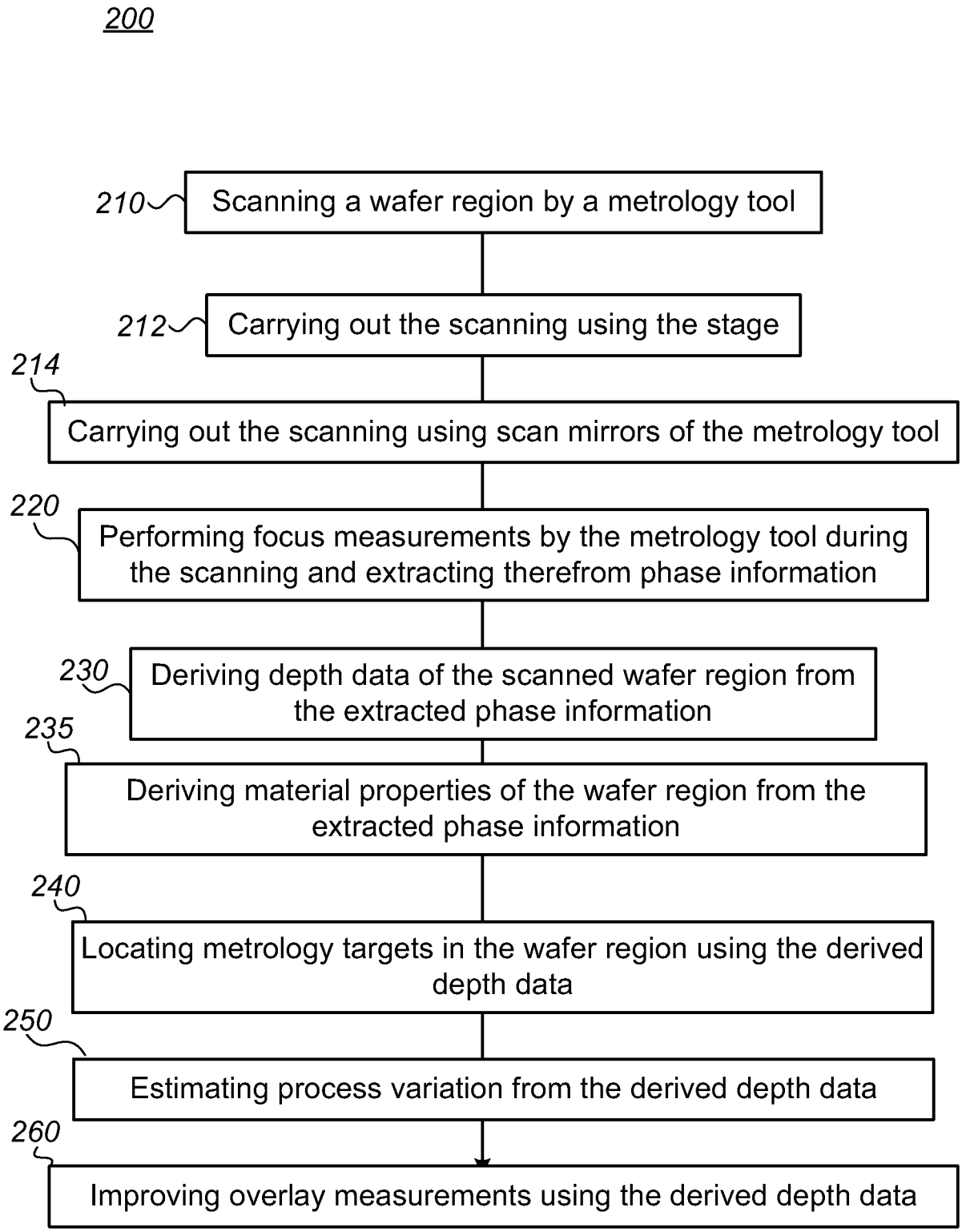
200
210
Scanning a wafer region by a metrology tool
212
Carrying out the scanning using the stage
214
Carrying out the scanning using scan mirrors of the metrology tool
220
Performing focus measurements by the metrology tool during the scanning and extracting therefrom phase information
230
Deriving depth data of the scanned wafer region from the extracted phase information
235
Deriving material properties of the wafer region from the extracted phase information
240
Locating metrology targets in the wafer region using the derived depth data
250
Estimating process variation from the derived depth data
260
Improving overlay measurements using the derived depth data

Figure 3

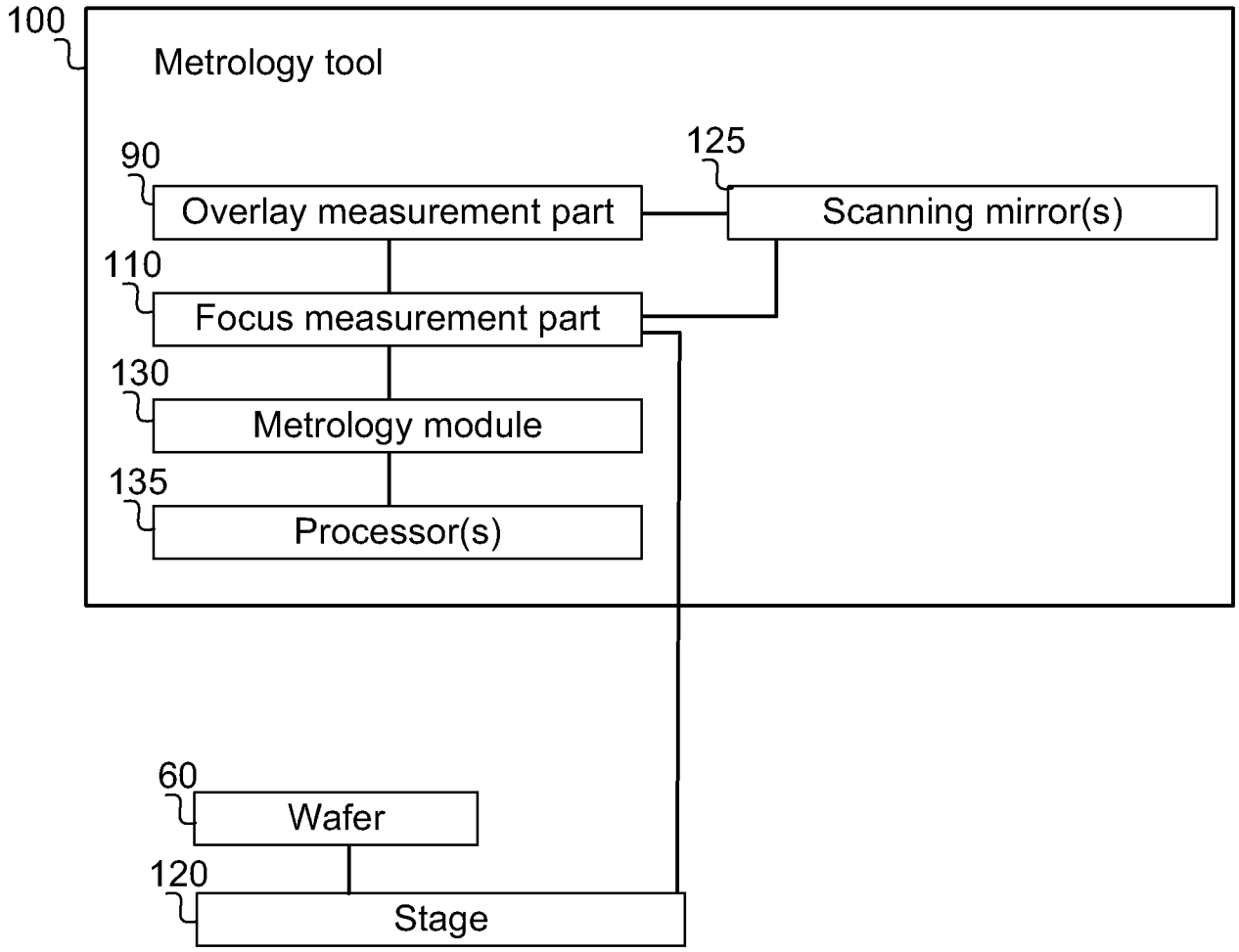
100
Metrology tool
90
Overlay measurement part
125
Scanning mirror(s)
110
Focus measurement part
130
Metrology module
135
Processor(s)
60
Wafer
120
Stage

Figure 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/054264

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/66; G03B 27/52; H01L 21/027; G01J 3/28; G01N 21/47; G03F 9/00; G03F 1/26; G03F 1/42; G03F 7/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: focus measurement, phase information, depth, wafer topography

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0261339 A1 (JOHAN MARIA VAN BOXMEER et al.) 27 October 2011 See paragraphs [0058], [0059], [0067], claims 9, 10 and figure 5.	1-20
A	JP 4792833 B2 (NIKON CORP.) 12 October 2011 See paragraphs [0019]-[0037].	1-20
A	US 2016-0282731 A1 (KLA-TENCOR CORPORATION) 29 September 2016 See paragraphs [0034]-[0053] and figure 3.	1-20
A	US 2016-0011523 A1 (ASML NETHERLANDS B.V.) 14 January 2016 See paragraphs [0066]-[0074] and figure 3.	1-20
A	KR 10-2016-0014471 A (SAMSUNG ELECTRONICS CO., LTD.) 11 February 2016 See paragraphs [0098]-[0111] and figure 7.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 January 2018 (11.01.2018)	**11 January 2018 (11.01.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/054264

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