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(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors; and

(71) Applicants *(for US only)*: **COWLEY, Nicholas P.** [GB/GB]; 3 Priors Hill, Wroughton Wiltshire SN4 0RT (GB). **ALI, Isaac** [GB/GB]; 17 Blenheim, Redland, Bristol Avon BS6 7JL (GB). **SUETINOV, Viatcheslav I.** [RU/GB]; 44 Larchmore Close, Swindon Wiltshire Sn25 3QG (GB). **PINSON, Keith** [GB/GB]; 15 The Mews, Lydiard Millicent, Swindon Wiltshire SN5 3NQ (GB).

(74) Agent: **RAMIREZ, Ellis B.**; Prass LLP, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

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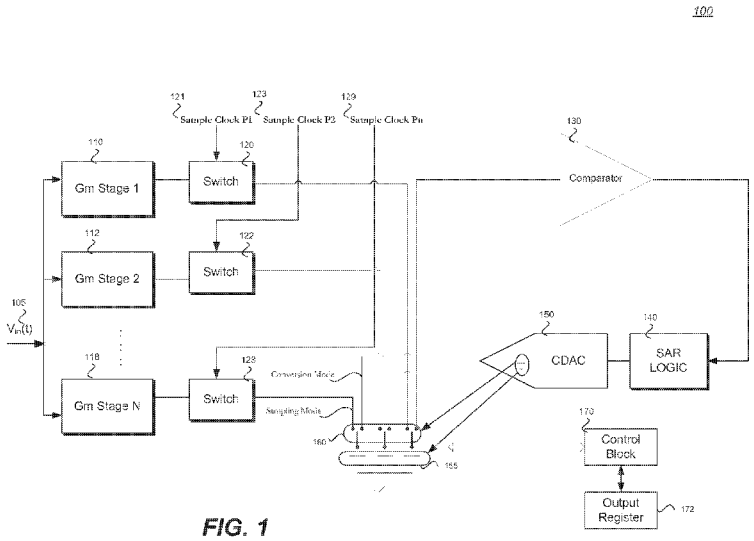

FIG. 1

(57) Abstract: An apparatus and method of successive approximation analog-to-digital conversion for receivers comprising that during a sample mode, connecting an array of capacitors to a plurality of sampling switches coupled to a plurality of amplified input signals, and during a conversion mode, connecting in common the array of capacitors to a comparator and isolating the array of capacitors from the plurality of sampling switches. Additionally, filtering is done by the summation of samples at phase offsets.

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A SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION ARCHITECTURAL ARRANGMENT FOR RECEIVERS

BACKGROUND

Embodiment generally relate to electronic circuit designs, and more specifically to improvements in architectural arrangements which enable enhanced performance and/or features for sampling receivers, and specifically to direct conversion sampling receivers which include a successive approximation analog-to-digital converter (SAR-ADC) to enhance quality of sampling receivers, where the SAR-ADC incorporates a current redistribution digital-to-analog converter (DAC) and where filtering is implemented in the radio frequency (RF) domain by at least reusing a capacitor arrays which form all or part of the DAC within the SARADC.

Direct conversion sampling receivers are a relatively new realization and are highly suited to implementation on an ultra-high speed digital process since the receiver architecture eliminates the requirement for significant analogue circuits such as operational amplifier (op-amp) based continual time filters. However, current direct conversion receivers suffer from frequency spikes caused by aliasing components which may manifest around the s3*Flo range, where a Flo is 1GHz. This pattern will be repeated for every 2*Flo increase in frequency offset and fundamentally relates to the harmonics of the sampling clock. Such decrease in the attenuation delivered by the sampled filter characteristic will lead to an increase in aliasing components, both noise and any discrete signals folding on to the desired channel. A further problem in conventional direct conversion receivers is that the characteristic response cannot be easily modified within the present architectural arrangement therefore there is no opportunity to adaptively modify the characteristic response in dependence on received signal conditions, i.e. to maximize attenuation at a given frequency.

Therefore, there is a need in the art for an architectural arrangement which substantially overcomes the aforementioned undesired characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is an illustration of a direct sampling receiver having charge redistribution SAR-

ADC architecture with capacitor segment redeployment and two modes of operation (i.e., a sampling mode and a conversion mode) in accordance to an embodiment;

FIG. 2 is an illustration of a charge redistribution SAR-ADC architecture during a sampling phase in accordance to an embodiment;

FIG. 3 is an illustration of a derivation of independent sampling during a sampling phase in accordance to an embodiment;

FIG. 4 is an illustration of the direct sampling receiver with SAR-ADC architecture of FIG. 1 modified with only three gm stages in accordance to an embodiment;

FIG. 5 is an illustration of the charge redistribution SAR-ADC architecture during a conversion phase in accordance to an embodiment;

FIG. 6 is a comparison of attenuation at different frequencies between the direct sampling receiver with SAR-ADC architecture of FIG. 1 and conventional direct conversion receivers;

FIG. 7 is a comparison of filter characteristic for example weighted filter and prior art fixed weights filters used in direct conversion;

FIGs. 8A-8C illustrates the vector relationship for fundamental and harmonics of sampling clock signals in accordance to an embodiment; and

FIG. 9 is a flow diagram illustrating actions in a method for performing analog to digital conversion based on the architecture of FIG. 1 according to an embodiment.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present inventions.

Although embodiments of the invention are not limited in this regard, discussions utilizing terms such as, for example, “processing,” “computing,” “calculating,” “determining,” “establishing”, “analyzing”, “checking”, or the like, may refer to operation(s) and/or process(es)

of a computer, a computing platform, a computing system, or other electronic computing device, that manipulate and/or transform data represented as physical (e.g., electronic) quantities within the computer's registers and/or memories into other data similarly represented as physical quantities within the computer's registers and/or memories or other information storage medium that may store instructions to perform operations and/or processes.

Although embodiments of the invention are not limited in this regard, the terms "plurality" and "a plurality" as used herein may include, for example, "multiple" or "two or more". The terms "plurality" or "a plurality" may be used throughout the specification to describe two or more components, devices, elements, units, parameters, or the like. For example, "a plurality of stations" may include two or more stations. The terms "first," "second," and the like, herein do not denote any order, quantity, or importance, but rather are used to distinguish one element from another. The terms "a" and "an" herein do not denote a limitation of quantity, but rather denote the presence of at least one of the referenced item.

FIG. 1 is an illustration of a direct sampling receiver having charge redistribution SAR-ADC architecture with capacitor segment redeployment and two modes of operation (i.e., a sampling mode and a conversion mode) in accordance to an embodiment. FIG. 1 is a diagram of a direct sampling receiver (DSR) 100 with charge redistribution SAR ADC implemented to process received signals 105 such as signal $V_{in}(t)$. DSR 100 is shown containing charge redistribution DAC (CDAC 150) and SAR logic 140. For clarity, power supplies (positive Vdd, negative Vee), as well as ground connections, are assumed to be present, but not shown in the Figure. CDAC 150 is shown associated with comparator 130, capacitor banks or array of capacitors 155, mode switches 160 each coupled to a capacitor in the array of capacitors, and sampling switches 120-128 where each sampling switch is associated with one element of a low noise amplifier (LNA) and one element of the array of capacitors. An input of comparator 130 is coupled to a reference voltage Vref. The closing or opening of each of the mode switches 160 is controlled by control block 170. The closing or opening of each of the sampling switches 120-128 is controlled by a sampling clock signal to selectively activate the sampling switches. The sampling clock signal may be externally generated, generated by control block 170, or by a programmed multivibrator in DSR 100. The sampling clock signals are used to activate the sampling switches as shown by sample clock P1 121 to activate sample switch 120; sample clock P2 123 to activate sample switch 122; and sample clock Pn 129 to activate sample switch 128. An input signal is split into N parallel segments, where $N \geq 2$, and each segment has an independent associated gain stage (Gm) (110, 112, ...118) that is associated with a sample

switch (120, 122, ... 128) which in turn is associated with a capacitor in the array of capacitors.

This arrangement allows for independent setting of all critical parameters for each of the N parallel segments (paths) without any one path interfering with any other path; i.e., each Gm stage (gm) can be independently set, the frequency and/or phase and/or mark space ratio of each sampling clock signal can be independently set, the capacitor segment selected from the array of capacitors that is redeployed to each path output (Sample switch) can be independently set.

A control block 170 based on the stored instructions relating to parameters such as the number of samples that correspond to a predetermined resolution, determines the switching of switch 160. The opening and closing of the switch is primarily determined by the number of samples from sample switch 120 which sets the sampling phase duration, and the number of cycles required to run the logic to switch the charge redistribution digital-to-analog converter (CRDAC) output. Switch 160 is controlled to two distinct configurations or phases. These configurations are (a) a sampling mode configuration and (b) a conversion mode configuration.

In the first configuration, referred to as the sampling mode/phase, the CDAC 150 charge redistribution array of capacitors 155 are connected to the output of the sampling switches (120, 122, ... 128) to integrate the current output sampled by the sampling switches; each capacitor in the array of capacitors is normally discharged before this period. After sampling the N capacitor segments are then recombined and operated in the same manner as conventional successive approximation analog-to-digital converters.

In the second configuration, referred to as the conversion mode/phase, After the requisite number of samples the DAC array of capacitors is then isolated from the input sampling switches and transitioned back to normal charge distribution function within the SAR-ADC wherein the array of capacitors are switched between supply voltage (Vdd) and ground (Vss) which redistributes the stored charge between the elements such that the resultant voltage on the capacitor is V= Q/C trends towards the reference voltage of the comparator 130. The output of comparator 130 then processed through quantization loop of SAR logic 140 and CDAC 150 until the number of iterations is produced and a predetermined resolution. Since the illustrated architecture is based on charge sampling and redistribution around the SAR-ADC capacitors the performance can be enhanced by redistribution of the capacitors and amplifiers (gm) during the sampling phase. The

segments can be combined to perform harmonic attenuation like shown in FIG. 6 and to perform filtering like shown in FIG. 7.

FIG. 2 is an illustration of a charge redistribution SAR-ADC architecture during a sampling phase 200 in accordance to an embodiment. During the sampling mode as selected through mode switch 160 as explained in FIG. 1 one (1) or more samples of the input are passed to the array of capacitors by activating the sampling clock signal. As illustrated the mode switch 160 is set to the sampling mode and the capacitors in the array of capacitors are coupled to a plurality of sampling switches that are coupled to a plurality of amplified input signals. In this switch position (mode) the only obstacle to the charging of the array of capacitors is the state of the sampling switches (120, ... 128). Each sampling switch can be set to select a capacitor segment from the array of capacitors allowing the signal (sample) from the selected Gm stage to charge the capacitor.

FIG. 3 is an illustration of a derivation of independent sampling during a sampling phase in accordance to an embodiment. FIG. 3 illustrates mathematically 310 the gain for each segment. The gain for each segment is simply the gain (gm) times (*) the total impedance $gm*Z_{Ctotal}$, where Ctotal is the total capacitance such as C_1, C_2, and C_4. The actual segment capacitor value has no influence on the gain and hence contribution from each segment since the charge stored during sampling phase on the independent segments are redistributed to the total capacitance before conversion phase.

FIG. 4 is an illustration of the direct sampling receiver with SAR-ADC architecture of FIG. 1 modified with only three gm stages in accordance to an embodiment. With reference to Figure 4 the front end gm stage contains three parallel gm stages, i.e., Gm Stage1 110, Gm Stage2 112, and Gm Stage3 118. Each gm stage has an associated output switch (120, 122, 128) with sampling clock signal like Sample ClockP1 121, Sample ClockP2 123 and Sample ClockP3 126 of phase relationship -45 0 and 45 degrees respectively. The capacitor ratio may be for example deployed with most significant bits (MSB) capacitor to segment 2 (Gm stage2 and sampling switch 122), "MSB-1" capacitor to segment 1 and the remaining capacitance to segment 3, which would be a simple switching arrangement; the ratios however are not limited to this arrangement and other more complex arrangements could be deployed whereby the capacitor ratios approximate more closely to the inverse of the gm ratios, such that the amplitude on each segment are substantially equal during the sampling phase.

Each Gm Stage contributes to the overall filter characteristic based upon the amplitude, duration (mark space ratio) and phasing of the individual sample of the input

signal 105, referred to as the weight of each sample. There are a number of ways this can be implemented. One example, with reference to FIG. 1, is the 1 through N gm stages (110,112 …118) could be configured to provide a small number of different weights of the input signal. The required sample weight is then selected either by activating the associated switch or group of switches. In FIG. 4 the gm ratios for stage1, stage2 and stage3 are set to 1, $\sqrt{2}$, 1 respectively and offset in phase to eachother.

Other configurations and weights are possible. For example, a system deploying eight (8) samples per cycle is shown in Table 1 for an architecture with each weight being provided by a separate gm/switch and in Table 2 for an architecture where the weights are constructed by two gm/switches of equal amplitude.

TABLE 1 (One switch per Gm stage)

Gm weight	Sample							
	1	2	3	4	5	6	7	8
0.5	on	on	on	off	off	on	on	on
1	off	off	off	on	on	off	off	off
Total sample weight	1	0.5	0.5	0.5	0.5	0.5	0.5	1.0

TABLE 2(Two switches per Gm stage)

Gm weight	Sample							
	1	2	3	4	5	6	7	8
0.5	on	on	on	on	on	on	on	on
0.5	off	off	off	on	on	off	off	off
Total sample weight	1	0.5	0.5	0.5	0.5	0.5	0.5	1.0

Both these options provide the same resultant weight per sample of 1 unit for 1st and 8th samples and 0.5 unit for all others. The first option (Table 1) may be simpler to implement however the second option (Table 2) offers a greater degree of flexibility, for example if 3 gm/switches are provided the first option only offers three weights whereas the second option offers 8, so allowing a greater degree of flexibility in the implemented characteristic.

FIG. 5 is an illustration of the charge redistribution SAR-ADC architecture during a conversion phase in accordance to an embodiment. In the conversion phase the array of capacitors 155 is shown isolated from the sampling switches (120, 122, ... 128) and shorted together and transitioned back to normal charge distribution function within the SAR-ADC. The capacitors in the array of capacitors are switched between supply voltage (Vdd) and ground (Vss) which redistributes the stored charge between the elements such that the resultant voltage on the capacitor is V= Q/C trends towards a voltage and by connecting in common the array of capacitors to the input of comparator 130 where it is compared to a reference voltage for K clock cycles. A resulting code of a digital approximation of the sampled input voltage Vin (t) 105 can be outputted at the end of a conversion to output register 172. Also register 172 can supply an approximate digital code of the input voltage Vin(t) 105 to internal CDAC 150

FIG. 6 is a comparison of attenuation at different frequencies between the direct sampling receiver with SAR-ADC architecture of FIG. 1 and conventional direct conversion receivers. The performance advantage of this new configuration shown in FIG 1 is illustrated in FIG. 6 by comparison with conventional direct sampling receiver. As can be seen the filtering afforded improves across the frequency spectrum, with significant benefit at the third harmonic frequency (in this example at an offset of 2000 MHz with the desired frequency of 1000 MHz) so offering an improved rejection of aliasing components in a receiver implementing this configuration. That is because at the third and fifth harmonic the summation from the three segments like shown in FIG. 4 equal zero but contributions from all three segments are substantially added constructively at the fundamental frequency. Other configurations with additional segments can be implemented which also offer improvement at 7^{th} and 9th harmonics and the like.

FIG. 7 is a comparison of filter characteristic for example weighted filter and prior art fixed weights filters used in direct conversion. As can be seen by modifying the weights the filter notch has been both shifted in frequency and widened. This is particularly advantageous in systems where it is desirable to suppress blocking signals which may lie at a different frequency to the notches present in an equal weighted filter or where the blocking signal may vary. In the latter case this architecture will allow the notch to be adjusted in dependence on the actual offset frequency of the blocker.

FIGs. 8A-8C illustrates the vector relationship for fundamental and harmonics of sampling clock signal in accordance to an embodiment. FIG. 8A is a vector diagram of samples from the three segment arrangement shown in FIG. 4. The sampled vectors are phase offset (0,-45, and

45) and the sum of segment 1 and segment 3 is in phase with segment 2 so leading to constructive addition and a maximum amplitude in phase with segment 2. FIGs 8B-8C show how the sum vector can be rotated and reduced in amplitude with increasing sampling frequency. FIG. 8b shows how combining sample1 and sample3 for the three segment vectors equal zero where they constructively add for the fundamental like shown in FIG 8A. In FIG 8B since the frequency is 3 times higher the vector phase angles are three times greater, so for segment 3 45 degrees rotates to 135 degrees and sector 1 at 315 rotates to 945 degrees or 135 degrees counter rotation. Now since the weights of the vectors are 1: √2:1 segments 1 and 3 add to create a vector at 180 degrees rotation of amplitude √2 which cancels with segment 2.

FIG. 8C shows the same response in the 5^{TH} harmonic and how filtering by summing the positive and negative charge packets can be combined to add (coherent) and subtract (destructive) to achieve RF filtering. Like the 3RD harmonic since the frequency is 5 times higher the vector phase angles are five times greater, so for segment 3 45 degrees rotates to 225 degrees and sector 1 at 315 rotates to 1575 degrees or 225 degrees counter rotation. Now since the weights of the vectors are 1: √2:1 segments 1 and 3 add to create a vector at 180 degrees rotation of amplitude √2 which cancels with segment 2. While some harmonics are illustrated other configurations with additional segments can be implemented which also offer improvements at 5^{th} and 7^{th} harmonics and the like.

FIG. 9 is a flow diagram illustrating actions in a method 900 for performing analog to digital conversion based on the architecture of FIG. 1 according to an embodiment. Method 900 begins with start 910. Control is then passed to action 915. Action 915 is implemented by positioning the mode switch 160 to the sampling mode. If the sampling mode has been selected then control is passed to action 920 for further processing in accordance to a sampling process. In action 920, connecting an array of capacitors to a plurality of sampling switches coupled to a plurality of amplified input signals. During action 920 (sampling period), the DAC charge redistribution capacitor is segmented into N independent capacitors and each segment then switched to the output of one of the sampling switches and so independent of other segments integrates the current output sampled by that switch. After action 920 control is passed to action 925. In action 925 if switch 160 is in the conversion mode then control is passed to action 930 for further processing. If switch 160 is not set to conversion mode then control is passed to action 915 for further processing. When control is passed to action 930 the array of capacitors 155 is isolated from the array of capacitors 155 and the capacitors are discharged through comparator 130. Control is then passed to action 950 where SAR-ADC is performed on the

charges (Q) in the array of capacitors. After a predetermined number of iterations control is then passed to action 910.

The techniques described herein may be embodied in a computer-readable medium for configuring a computing system to execute the method. The computer readable media may include, for example and without limitation, any number of the following: magnetic storage media including disk and tape storage media; optical storage media such as compact disk media (e.g., CDROM, CDR, and the like) and digital video disk storage media; holographic memory; nonvolatile memory storage media including semiconductor-based memory units such as FLASH memory, EEPROM, EPROM, ROM; ferromagnetic digital memories; volatile storage media including registers, buffers or caches, main memory, RAM, and the like; and data transmission media including permanent and intermittent computer networks, point-to-point telecommunication equipment, carrier wave transmission media, the Internet, just to name a few. Other new and various types of computer-readable media may be used to store and/or transmit the software modules discussed herein. Computing systems may be found in many forms including but not limited to mainframes, minicomputers, servers, workstations, personal computers, notepads, personal digital assistants, various wireless devices and embedded systems, just to name a few. A typical computing system includes at least one processing unit, associated memory and a number of input/output (I/O) devices. A computing system processes information according to a program and produces resultant output information via I/O devices.

Realizations in accordance with the present invention have been described in the context of particular embodiments. These embodiments are meant to be illustrative and not limiting. Many variations, modifications, additions, and improvements are possible. Accordingly, plural instances may be provided for components described herein as a single instance. Boundaries between various components, operations and data stores are somewhat arbitrary, and particular operations are illustrated in the context of specific illustrative configurations. Other allocations of functionality are envisioned and may fall within the scope of claims that follow. Finally, while certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents may occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

We Claim:

1. A method of successive approximation analog to digital conversion, the method comprising:

during a sampling mode, connecting an array of capacitors to a plurality of sampling switches coupled to a plurality of amplified input signals; and

during a conversion mode, connecting in common the array of capacitors to a comparator and isolating the array of capacitors from the plurality of sampling switches.

2. The method in accordance to claim 1, wherein the plurality of amplified input signals are coupled to the array of capacitors in accordance with a sampling clock signal to selectively activate the sampling switches.

3. The method in accordance to claim 2, wherein sampling clock frequency, sampling clock phase, and sampling clock mark space ratio for each sampling clock signal can be independently set.

4. The method in accordance to claim 2, wherein gain for each input signal can be independently set.

5. The method in accordance to claim 2, wherein by selectively activating with the sampling clock signal some of the plurality of switches a capacitor in the array of capacitors can be independently selected.

6. The method in accordance to claim 5, wherein during the sampling mode further comprises charging the selected capacitor in the array of capacitors.

7. The method in accordance to claim 6, wherein in the conversion mode the comparator compares a voltage across the array of capacitors to a reference voltage for k clock cycles.

8. The method in accordance to claim 7, wherein during the conversion mode converting a first sampled signal to a digital output signal over a number of iterations through a quantization loop, wherein the number of iterations corresponds to a predetermined resolution.

9. An apparatus comprising:

a comparator;

an array of capacitors, each capacitor being coupled between a corresponding mode switch and a first input terminal of the comparator, and each being arranged to receive an amplified input signal during a sample phase; and

a control circuitry arranged to control a plurality of mode switches such that a capacitor is coupled to a sampling switch coupled to an amplified input signal during the sample phase and isolated from the sampling switch during a conversion phase,

wherein the apparatus is a successive approximation register (SAR) analog to digital converter (ADC).

10. The apparatus in accordance to claim 9, wherein during the sample phase a plurality of amplified input signals being coupled to the array of capacitors in accordance with a sampling clock signal to selectively activate the sampling switches.

11. The apparatus in accordance to claim 10, wherein sampling clock frequency, sampling clock phase, and sampling clock mark space ratio for each sampling clock signal can be independently set.

12. The apparatus in accordance to claim 10, wherein gain for each input signal can be independently set.

13. The apparatus in accordance to claim 10, wherein by selectively activating with the sampling clock signal some of the plurality of switches a capacitor in the array of capacitors can be independently selected.

14. The apparatus in accordance to claim 13, wherein during the sample phase further comprises charging the selected capacitor in the array of capacitors

15. The apparatus in accordance to claim 14, wherein in the conversion phase the comparator compares a voltage across the array of capacitors to a reference voltage for K clock cycles.

16. The apparatus in accordance to claim 15, wherein the conversion phase further

comprises converting a first sampled signal to a digital output signal over a number of iterations through a quantization loop, wherein the number of iterations corresponds to a predetermined resolution.

17. A circuit comprising:

a comparator;

an array of capacitors, each capacitor being coupled between a corresponding mode switch and a first input terminal of the comparator, and each being arranged to receive an amplified input signal during a sample phase; and

a successive approximation analog-to-digital converter (SAR-ADC), to filter the input signal by summing samples at phase offsets after applying weights to some of the samples, and configurable to convert the amplified input signal into a digital representation using a binary search and outputting the digital representation to an output register.

18. The circuit in accordance to claim 17, wherein the plurality of amplified input signals are coupled to the array of capacitors in accordance with a sampling clock signal to selectively activate the sampling switches.

19. The circuit in accordance to claim 18, wherein sampling clock frequency, sampling clock phase, and sampling clock mark space ratio for each sampling clock signal can be independently set.

20. The circuit in accordance to claim 18, wherein gain for the at least one amplifier can be independently set.

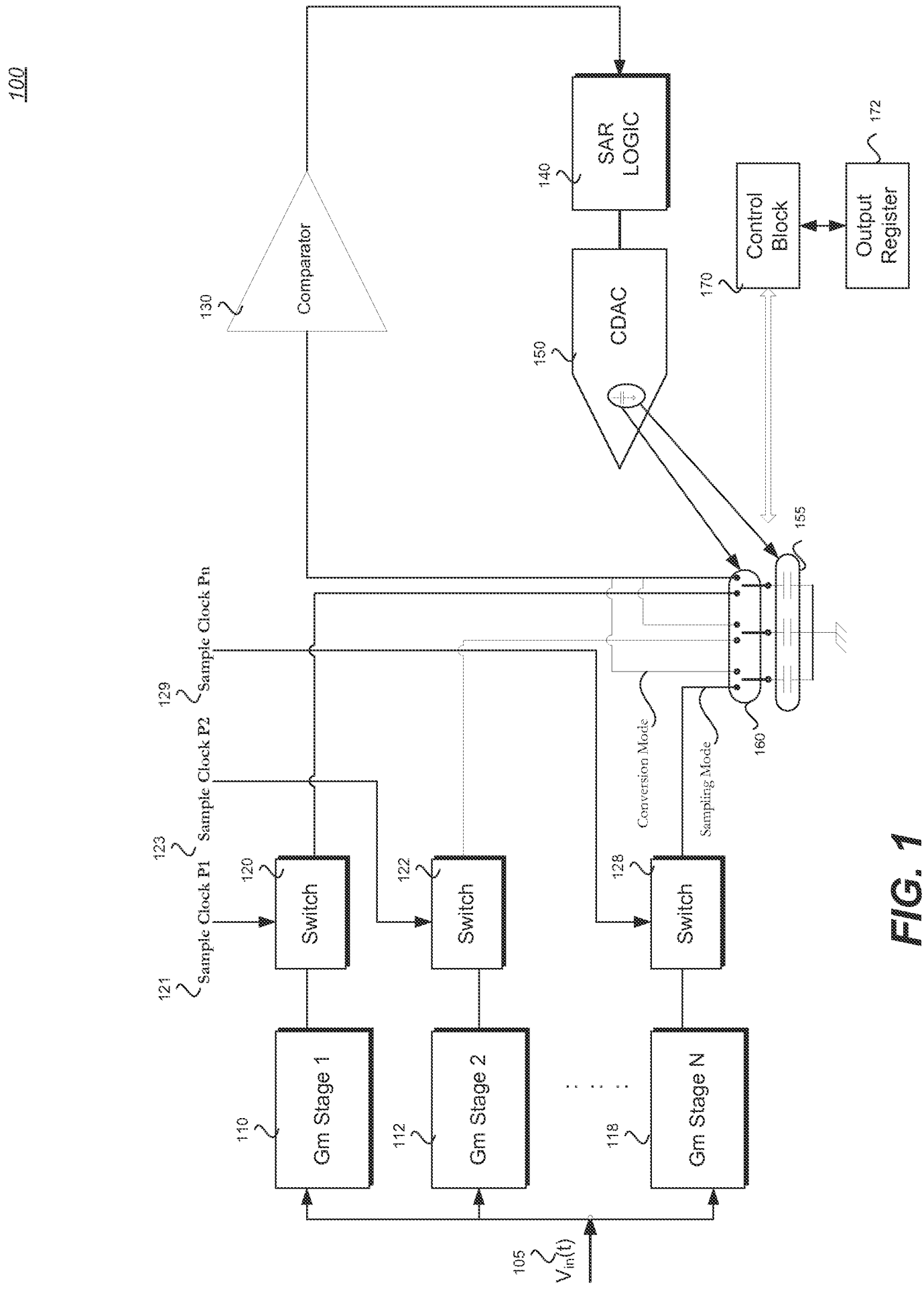
21. The circuit in accordance to claim 18, wherein by selectively activating with the sampling clock signal some of the plurality of switches a capacitor in the array of capacitors can be independently selected.

22. The circuit in accordance to claim 21, wherein the sample mode further comprises charging the capacitor segment.

23. The circuit in accordance to claim 22, wherein in the conversion mode the comparator compares a voltage across the array of capacitors to a reference voltage for k clock

cycles.

24. The circuit in accordance to claim 23, wherein the conversion phase further comprises converting a first sampled signal to a digital output signal over a number of iterations through a quantization loop, wherein the number of iterations corresponds to a resolution selected.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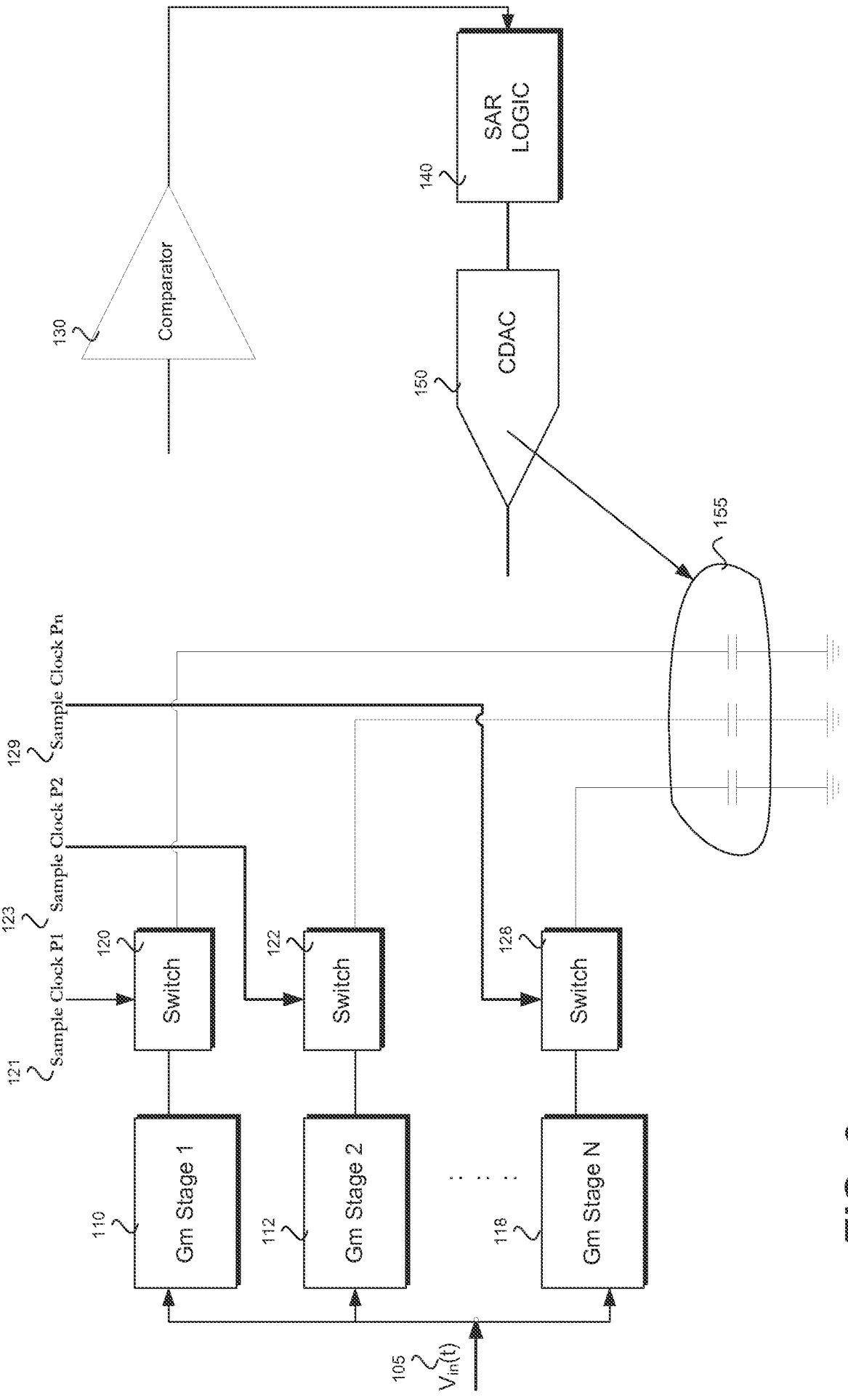
Comparator
130
SAR LOGIC
140
CDAC
150
Control Block
170
Output Register
172
155
160
Conversion Mode
Sampling Mode
Sample Clock Pn
129
Sample Clock P2
123
Sample Clock P1
121
Switch
120
Switch
122
Switch
128
Gm Stage 1
110
Gm Stage 2
112
Gm Stage N
118
105
$V_{in}(t)$

FIG. 1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Comparator
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SAR LOGIC
140
CDAC
150
155
Sample Clock Pn
129
Sample Clock P2
123
Sample Clock P1
121
Switch
120
Switch
122
Switch
128
Gm Stage 1
110
Gm Stage 2
112
Gm Stage N
118
$V_{in}(t)$
105

FIG. 2

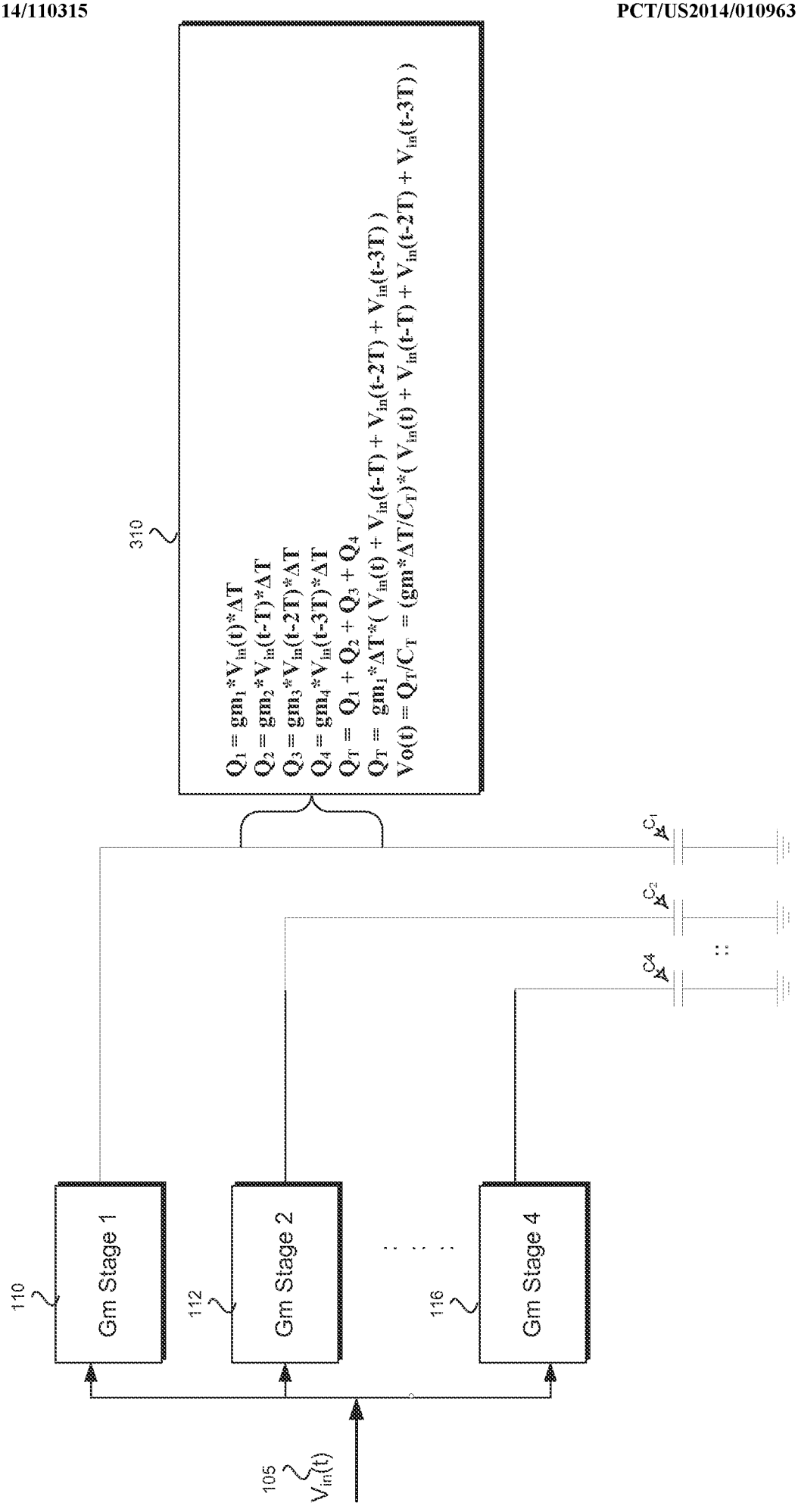
105
$V_{in}(t)$
110
Gm Stage 1
112
Gm Stage 2
116
Gm Stage 4
C_1
C_2
C_4
310
$Q_1 = gm_1 * V_{in}(t) * \Delta T$
$Q_2 = gm_2 * V_{in}(t-T) * \Delta T$
$Q_3 = gm_3 * V_{in}(t-2T) * \Delta T$
$Q_4 = gm_4 * V_{in}(t-3T) * \Delta T$
$Q_T = Q_1 + Q_2 + Q_3 + Q_4$
$Q_T = gm_1 * \Delta T * (V_{in}(t) + V_{in}(t-T) + V_{in}(t-2T) + V_{in}(t-3T))$
$Vo(t) = Q_T / C_T = (gm * \Delta T / C_T) * (V_{in}(t) + V_{in}(t-T) + V_{in}(t-2T) + V_{in}(t-3T))$

FIG. 3

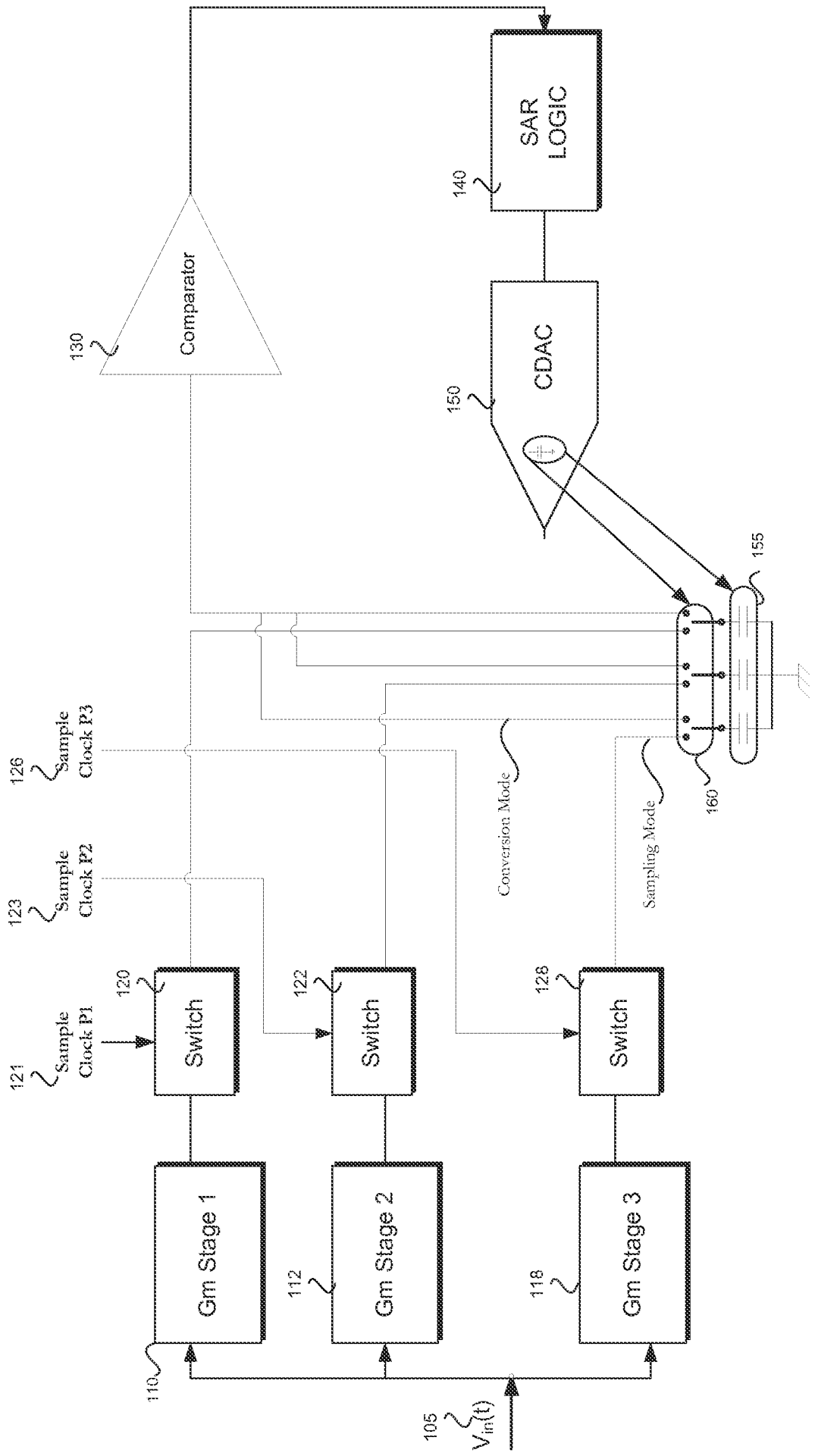
105
$V_{in}(t)$
110
Gm Stage 1
112
Gm Stage 2
118
Gm Stage 3
120
Switch
122
Switch
128
Switch
121
Sample Clock P1
123
Sample Clock P2
126
Sample Clock P3
Conversion Mode
Sampling Mode
160
155
130
Comparator
140
SAR LOGIC
150
CDAC

FIG. 4

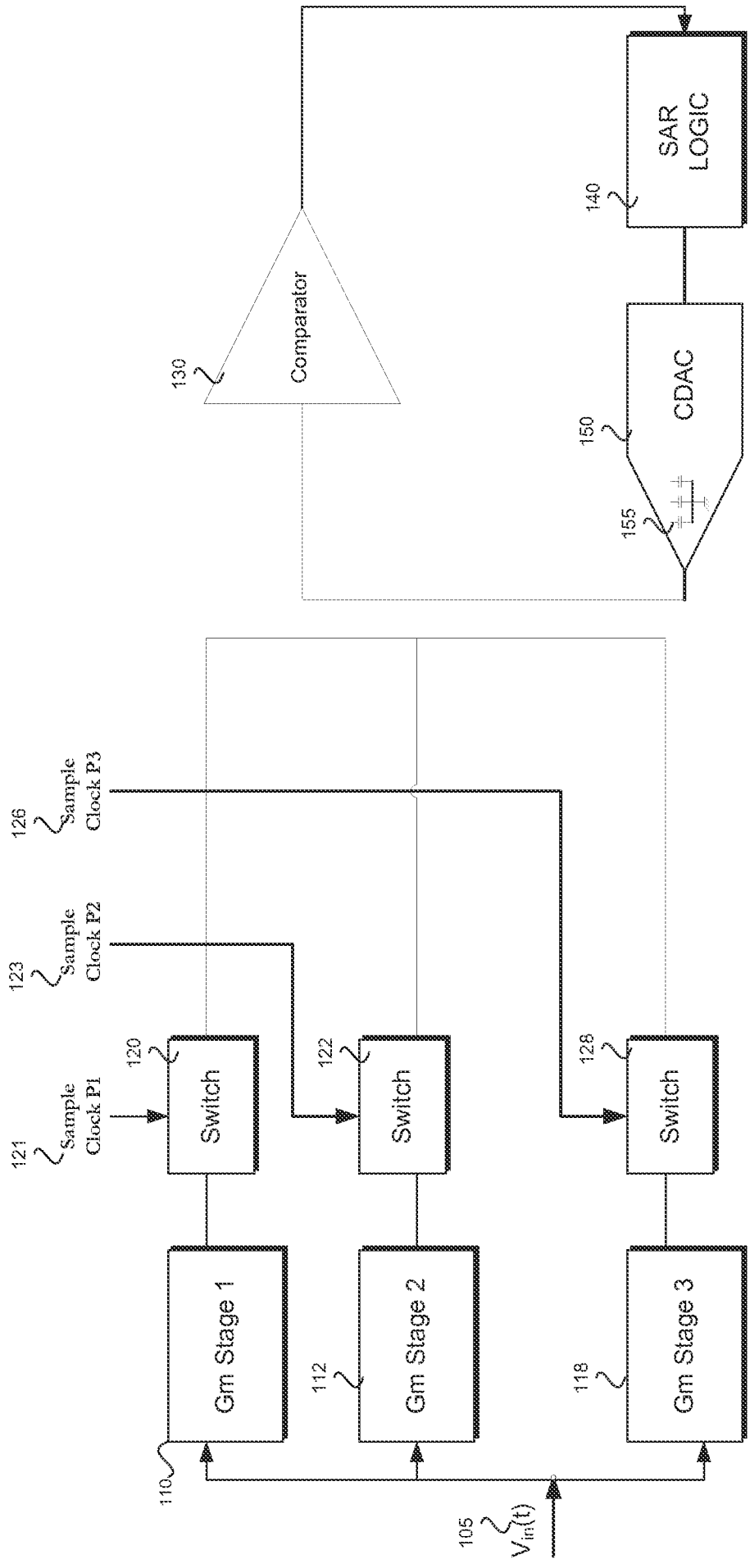
105
$V_{in}(t)$
110
Gm Stage 1
112
Gm Stage 2
118
Gm Stage 3
121
Sample Clock P1
123
Sample Clock P2
126
Sample Clock P3
120
Switch
122
Switch
128
Switch
130
Comparator
140
SAR LOGIC
150
CDAC
155

FIG. 5

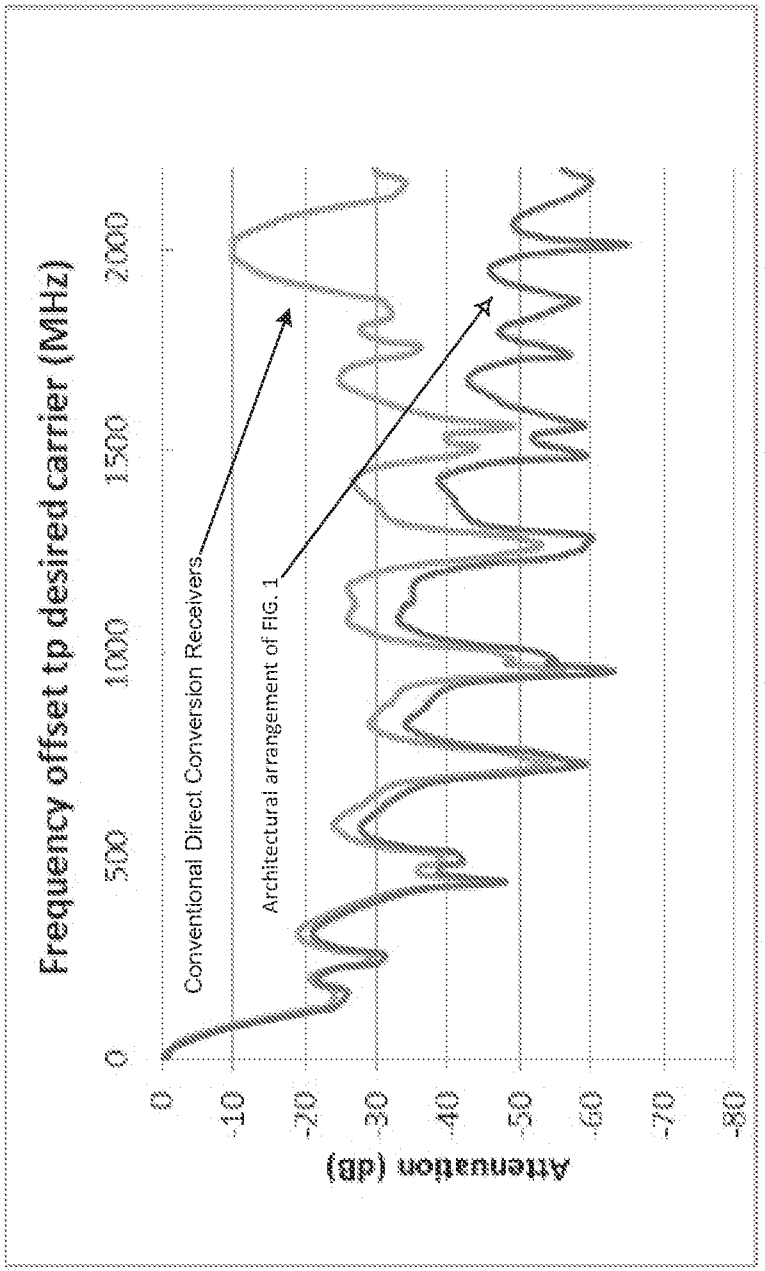
Frequency offset tp desired carrier (MHz)
0
500
1000
1500
2000
Attenuation (db)
0
-10
-20
-30
-40
-50
-60
-70
-80
Conventional Direct Conversion Receivers
Architectural arrangement of FIG. 1

FIG. 6

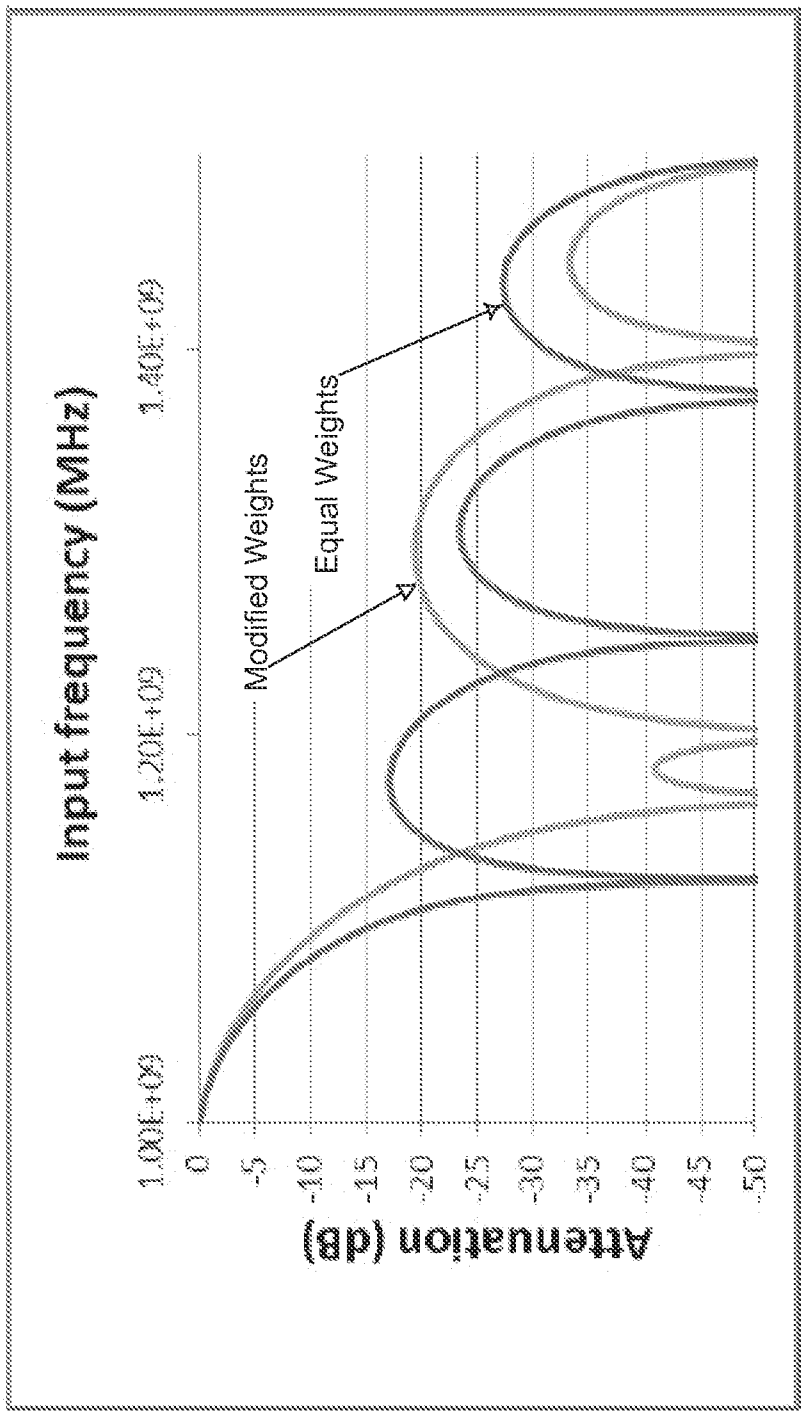
Input frequency (MHz)
1.00E+09
1.20E+09
1.40E+09
Attenuation (dB)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
Modified Weights
Equal Weights

FIG. 7

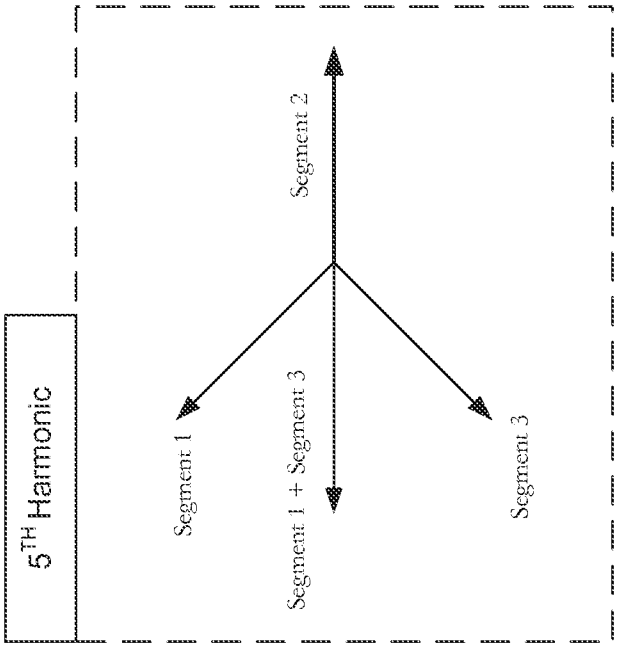

FIG. 8C

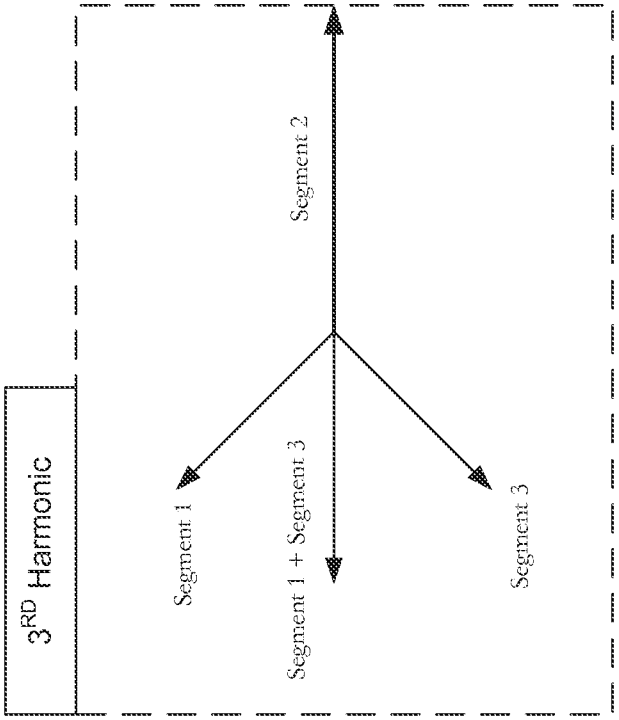

FIG. 8B

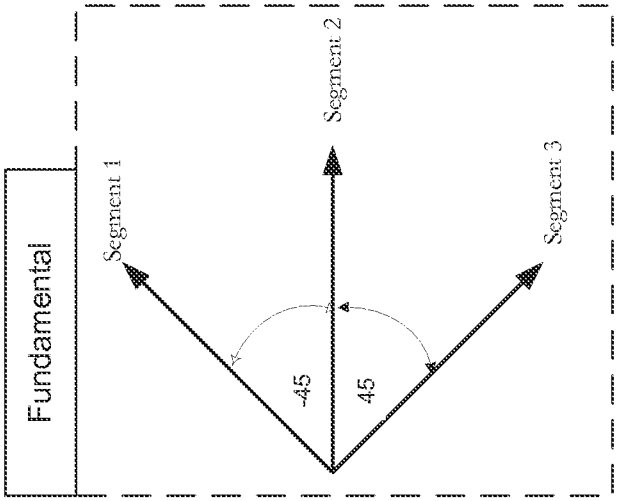

FIG. 8A

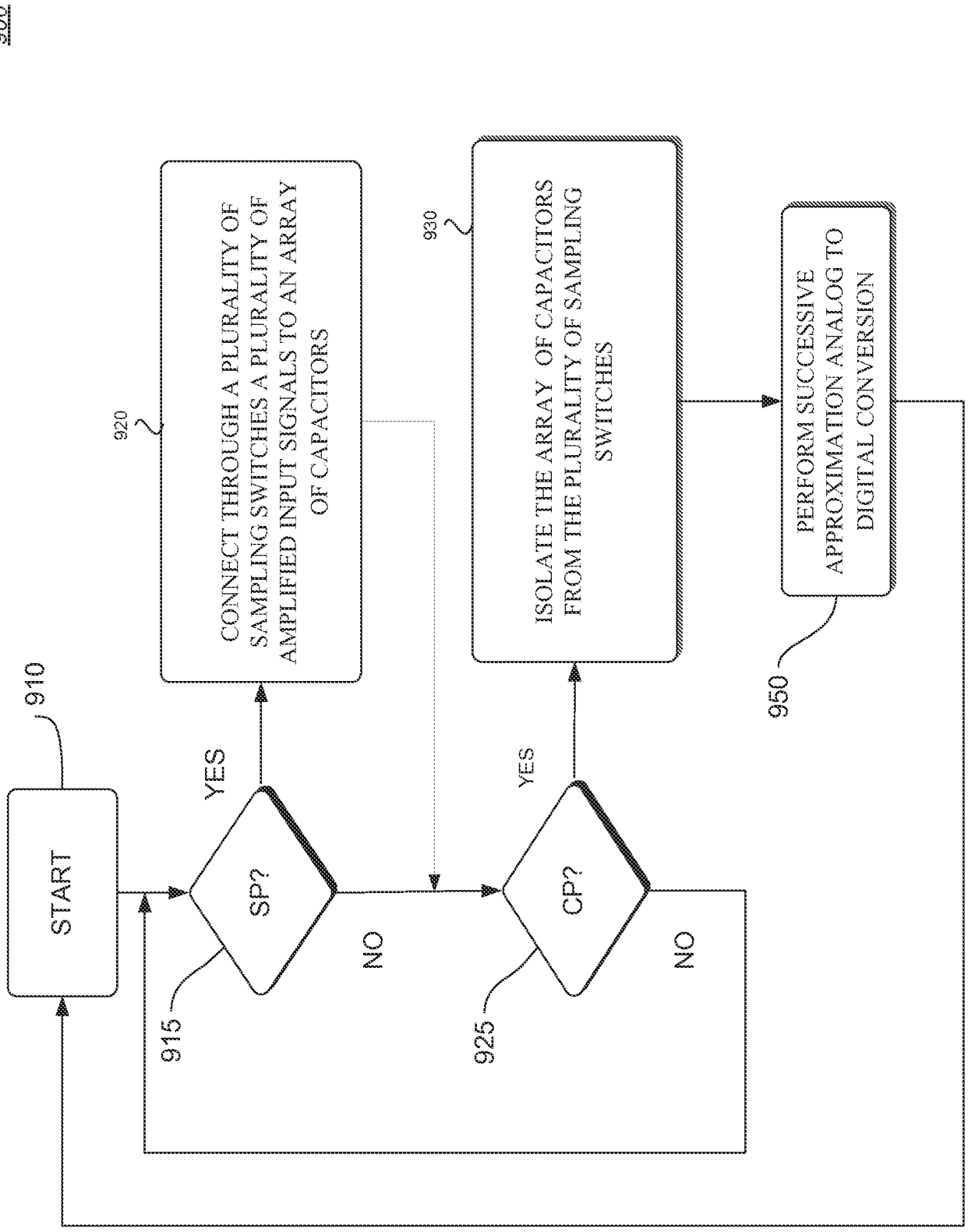
900
START
910
SP?
915
YES
NO
CONNECT THROUGH A PLURALITY OF SAMPLING SWITCHES A PLURALITY OF AMPLIFIED INPUT SIGNALS TO AN ARRAY OF CAPACITORS
920
CP?
925
YES
NO
ISOLATE THE ARRAY OF CAPACITORS FROM THE PLURALITY OF SAMPLING SWITCHES
930
PERFORM SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERSION
950

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/010963

A. CLASSIFICATION OF SUBJECT MATTER

H03M 1/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M 1/12; H03K 5/00; H03M 1/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: SAR-ADC, capacitor, sampling mode, conversion mode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0026027 A1 (JESPER STEENSGAARD-MADSEN) 02 February 2012 See paragraphs [0002], [0012], [0031]-[0045]; claims 1, 7; and figures 1, 3.	1-24
A	US 2012-0112948 A1 (STEPHANE LE TUAL et al.) 10 May 2012 See paragraphs [0030]-[0070]; and figures 1-4.	1-24
A	US 2012-0280846 A1 (JIN-FU LIN) 08 November 2012 See paragraphs [0019]-[0034]; and figures 3A-5.	1-24
A	US 2010-0026546 A1 (FRANK OHNHAEUSER et al.) 04 February 2010 See paragraphs [0024]-[0036]; and figures 2-5.	1-24
A	US 2012-0218137 A1 (EUISIK YOON et al.) 30 August 2012 See paragraphs [0026]-[0030]; and figures 2-4.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 May 2014 (23.05.2014)	**23 May 2014 (23.05.2014)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701,
Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
KIM, Do Weon
Telephone No. +82-42-481-5560

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/010963

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0026027 A1	02/02/2012	US 8130133 B2	06/03/2012
US 2012-0112948 A1	10/05/2012	FR 2965427 A1	30/03/2012
		FR 2965427 B1	21/06/2013
		US 8514123 B2	20/08/2013
US 2012-0280846 A1	08/11/2012	US 8344930 B2	01/01/2013
US 2010-0026546 A1	04/02/2010	DE 102008035215 A1	11/02/2010
		DE 102008035215 B4	09/09/2010
		US 7965218 B2	21/06/2011
US 2012-0218137 A1	30/08/2012	WO 2011-028674 A2	10/03/2011
		WO 2011-028674 A3	16/06/2011