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(54) **Title:** A METHOD OF ANODISING A SURFACE OF A SEMICONDUCTOR DEVICE

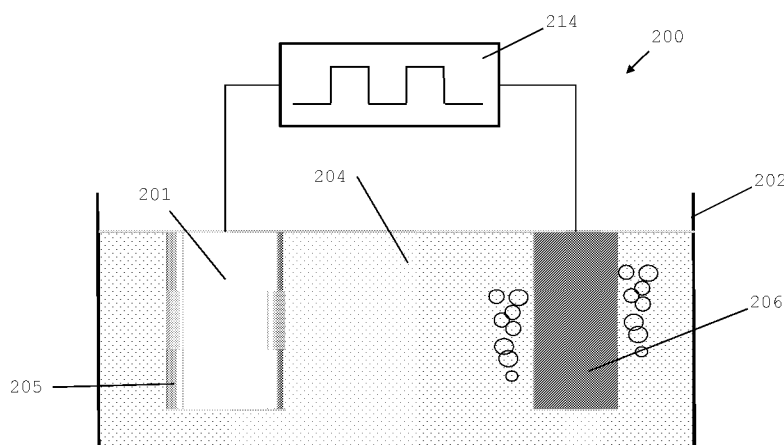


FIGURE 2

(57) **Abstract:** The present disclosure provides a method of anodising a surface comprising a metallic material. The method comprises the step of exposing a portion of the surface to an electrolytic solution that is suitable for anodising the metallic material. Further, the method comprises the steps of exposing a portion of an electrode to the electrolytic solution; selecting one or more parameters of an alternate waveform; and applying an electric wave having the alternate waveform to the exposed portion of the surface to anodise the portion of the surface. The one or more parameters of the alternate waveform are selected in a manner to influence an amount of stored charge embedded in the anodised material.

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A METHOD OF ANODISING A SURFACE OF A SEMICONDUCTOR DEVICE

Technical Field of the Invention

5 The present invention relates generally to the field of anodisation of surfaces containing a metallic material, in particular, to a method and apparatus for anodising a surface of a device containing a metallic material.

10 Background of the Invention

Dielectric layers are used in electronic devices to perform a variety of functions. In silicon solar cells, for example, dielectric layers are used to 'passivate'
15 surfaces of the cell and ensure high operating voltages. In MOSFETs a very thin dielectric layer is used to separate the gate electrode from the channel of the device and form a metal-oxide-semiconductor capacitor.

20 Dielectric layers can be fabricated by direct deposition, thermal growth or anodisation. No matter which fabrication technique is used, dielectric layers always contain a residual amount of stored charge. Thermally-grown layers of silicon dioxide and PECVD layers of silicon nitride,
25 for example, can store positive charges. PECVD or ALD aluminium oxide layers can contain stored negative charges.

In many applications, the residual charge stored in the
30 dielectric layers, can be used to improve the performance of the devices. For example, in solar cells, stored charge can be used to repel electrical carriers of one polarity from a surface of the device to decrease the probability of carrier recombination at that surface.

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Anodisation provides a series of advantages, such as atmospheric pressure and room temperature operation and low environmental impact. For the fabrication of solar cells, for example, anodisation allows meeting the
5 challenging cost/volume production requirements and can be integrated in existing cell production lines. However, the amount of residual stored charge in dielectric layers grown by anodisation, and also by other techniques, is not controllable, preventing the optimisation of device
10 properties and performance.

Different methods have been previously used in the art to control stored charge in dielectric layers. For example, the stored charge in $\text{Al}_2\text{O}_3/\text{SiO}_2$ stacks, deposited by ALD on
15 Si substrates, can be controlled in both magnitude and polarity, by varying the SiO_2 thickness. However, this requires a very accurate control of the ALD SiO_2 thickness which makes the process costly and time consuming. A corona discharge has been shown to create and store
20 negative charge in $\text{SiN}_x/\text{SiO}_2$ stacks, grown by PECVD on Si substrates. This method however may introduce extra damages to the interfaces as the negative charge origins from the tunneling of electrons from silicon to silicon nitride. Furthermore the stored negative charge appears to
25 be unstable at elevated temperatures.

Improved anodisation methods and apparatuses are needed in the art to allow for enhanced device performance.

30 Summary of the Invention

In accordance with a first aspect, the present invention provides a method of anodising a surface comprising a metallic material, the method comprising the steps of:
35 exposing a portion of the surface to an electrolytic solution that is suitable for anodising the metallic

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material;

exposing a portion of an electrode to the electrolytic solution;

5 selecting one or more parameters of an alternate waveform; and

applying an electric wave having the alternate waveform to the exposed portion of the surface to anodise the portion of the surface;

10 wherein the one or more parameters of the alternate waveform are selected in a manner to influence an amount of stored charge embedded in the anodised material.

In accordance with a second aspect, the present invention provides a method of controlling stored charge in an anodised material comprising the steps of:

15 selecting one or more parameters of an alternate waveform; and

20 applying an electric wave having the alternate waveform between a metallic material and an electrode while the metallic material is being anodised.

In embodiments, the electrode can be made of one or a combination of nickel, copper or aluminium. In alternative embodiments, the electrode can be an inert electrode, such as a platinum, palladium or graphite electrode.

In an embodiment, the one or more parameters of the alternate waveform are selected in a manner to influence sign and magnitude of stored charge embedded in the anodised material. The alternate waveform may be a square waveform and the step of selecting one or more parameters of the alternate waveform may comprise selecting one or a combination of:

- 35 i. a positive value of the waveform;
ii. a negative value of the waveform;
iii. a duty cycle value of the waveform; and

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iv. a frequency value of the waveform.

The selected value of duty cycle may be between 30% and 100%. The selected value of frequency may be between
5 0.05Hz and 10Hz. Furthermore, the alternate waveform may be a pulsed waveform.

In an embodiment, the step of selecting one or more parameters of the alternate waveform comprises at least
10 selecting the positive value or the negative value.

In embodiments, the alternate waveform is a current waveform. The positive current value may be between 1 mA/cm² and 5 mA/cm² and the negative current value may be
15 between -1 mA/cm² and -5 mA/cm².

In other embodiments, the alternate waveform is a voltage waveform. The positive voltage value may be between 10 V and 50 V. The negative voltage value may be between -10 V
20 and -50 V.

In an embodiment, the one or more parameters of the alternate waveform are selected in a manner such that the stored charge embedded in the anodised material has an
25 effective density between $-10 \cdot 10^{11} \text{ q/cm}^2$ to $10 \cdot 10^{12} \text{ q/cm}^2$.

In accordance with the third aspect, the present invention provides an apparatus for anodising a surface comprising a metallic material, the apparatus comprising:

30 a container for containing an electrolytic solution;
 an electrode element positioned for contacting the electrolytic solution; and
 an alternate waveform generator arranged to apply an electric wave having an alternate waveform to the exposed
35 portion while the metallic material is being anodised.

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In an embodiment, the generator is arranged to apply a current waveform through the surface comprising the metallic material and the electrode and to provide tunability of one or more parameters of the alternate
5 waveform.

The alternate waveform may be a square waveform and the generator may be arranged to provide tunability of one or a combination of:

- 10 i. a positive current value of the waveform;
- ii. a negative current value of the waveform;
- iii. a duty cycle value of the waveform; and
- iv. a frequency value of the waveform.

15 By tuning one or a combination of parameters i to iv the amount of stored charge embedded in the anodised material may be influenced. In embodiments, the amount of stored charge embedded in the anodised material is controllable between $-10 \cdot 10^{11} \text{ q/cm}^2$ to $10 \cdot 10^{12} \text{ q/cm}^2$.

20 In embodiments, the apparatus further comprises a support arranged to support a device, the surface comprising the metallic material being part of the device, such that in use the surface is exposed to the electrolytic solution
25 when the container is charged with the electrolytic solution.

In embodiments, the apparatus further comprises a radiation source arranged to illuminate a portion of the
30 device in a manner such that a radiation-induced current is generated in the device to promote anodisation of the surface comprising the metallic material.

In accordance with a fourth aspect, the present invention
35 provides a charge filtering structure for separating positive charge carriers from negative charge carriers

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comprising an anodised material which is anodised in accordance with the first aspect.

In accordance with a fifth aspect, the present invention provides a Perovskite based photovoltaic cell comprising a charge filtering structure in accordance with the fourth aspect.

In accordance with a sixth aspect, the present invention provides a kesterite based photovoltaic cell comprising a charge filtering structure in accordance with the fourth aspect.

In accordance with a seventh aspect, the present invention provides a photovoltaic cell device comprising an anodised layer formed by a method in accordance with the first aspect.

In accordance with an eighth aspect, the present invention provides a photovoltaic cell device comprising a negatively doped base region and a positively doped emitter region wherein the emitter region is in contact with an anodised layer formed by a method in accordance with the first aspect, the anodised layer having a net negative stored charge and being arranged to electrically passivate at least a portion of the emitter region.

In accordance with a ninth aspect, the present invention provides a photovoltaic cell device comprising a positively doped base region and a negatively doped emitter region wherein the emitter region is in contact with an anodised layer formed by a method in accordance with the first aspect, the anodised layer having a net positive stored charge and being arranged to electrically passivate at least a portion of the emitter region.

In accordance with a tenth aspect, the present invention

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provides a photovoltaic cell device comprising:

a base region;

an emitter region;

5 a contacting region, the contacting region comprising a plurality of interdigitated negatively doped and positively doped semiconducting portions; and

an anodised layer, disposed in proximity of the contacting region, the anodised layer being formed by a method in accordance with the first aspect.

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In an embodiment, the anodised layer has a quasi-neutral net stored charge.

15 In accordance with an eleventh aspect, the present invention provides a metal-oxide-semiconductor capacitor structure comprising:

a semiconducting substrate or a semiconducting layer;

20 a thin dielectric layer disposed on a surface portion of the semiconducting substrate or semiconducting layer, the thin dielectric layer being formed by a method in accordance with the first aspect; and

an electrode disposed in contact with at least a portion of the thin dielectric layer.

25 In accordance with a twelfth aspect, the present invention provides a metal-oxide-semiconductor field effect transistor comprising a metal-oxide-semiconductor capacitor in accordance with the eleventh aspect.

30 Brief Description of the Drawings

The embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

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Figure 1 is a flow chart of an anodisation process;

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Figure 2 is a schematic representation of an anodisation apparatus;

Figure 3 is a schematic illustration of an alternate waveform generator;

5 Figure 4 is an illustration on an alternate pulsed current waveform;

Figures 5 and 6 are simplified schematic illustrations of solar cell devices comprising an anodised layer;

10 Figure 7 is an illustration of the band structure of a solar cell comprising carrier filtering contacts;

Figure 8 shows current and voltage profiles of a sample anodised by a pulsed current with a 50% duty cycle;

Figure 9 shows a comparison of voltage profiles for pulsed anodisation;

15 Figure 10 shows plots of the effective stored charge density and dark saturation current density as a function of positive cycle percentage for different anodised samples;

20 Figure 11 shows a schematic diagram of a stacked dielectric structure used to determine the stored charge distribution;

Figure 12 is a plot showing the measured flat-band voltage as a function of dielectric thickness; and

25 Figure 13 is a plot showing the simulated effective charge as a function of the anodised layer thickness for different dielectric inter-layer thicknesses.

Detailed Description of Embodiments

30 Embodiments of the present invention relate to a method and an apparatus for anodising a surface comprising a metallic material. The method uses an electrolytic bath with an electrolytic solution. The surface to be anodised is put into contact with the solution together with an
35 additional electrode. The electrode can be made of one or a combination of nickel, copper or aluminium.

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Alternatively, the electrode can be an inert electrode, such as a platinum, palladium or graphite electrode.

5 A wave with an alternate waveform is then applied to the system comprising the surface to be anodised, the bath and the electrode. The waveform can be obtained from a current generator, in which case a predetermined current will be flowing through the system. Alternatively, the waveform
10 can be a voltage waveform, in which case the current flowing through the system will be related to specific properties of the electrolytic bath, the surface being anodised and the electrode.

Prior to the application of the waveform to the system,
15 the waveform is 'tailored' by selecting one or more 'waveform parameters'. The selection of these parameters allows influencing the amount of stored charge embedded in the anodised material.

20 Embodiments of the method allow controlling the sign and magnitude, with a certain level of precision, of the stored charge in the material being anodised using the tailored waveform. Parameters of the waveform which can be tailored include the positive value of the waveform, the
25 negative value of the waveform, the duty cycle value and the frequency of the waveform. In advantageous embodiments, the waveform is a square waveform with a positive and a negative value.

30 Referring now to figure 1, there is shown a flow chart 100 of an anodisation process in accordance with an embodiment. A portion of the surface of the device to be anodised is exposed to the electrolytic solution in the electrolytic bath at step 105 and the electrode is also
35 exposed to the solution 110. At step 115 the one or more parameters of the alternate waveform are selected based on

- 10 -

the sign and magnitude of the stored charge desired in the final anodised layer. At step 120 the alternate waveform is applied to the system and the anodisation process is commenced.

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Referring now to figure 2, there is shown a schematic representation of an anodisation apparatus 200 suitable to perform method 100 in accordance with an embodiment.

Apparatus 200 comprises a container 202 for containing an electrolytic solution 204. An electrode 206 is partially submerged in solution 204. The system includes alternate waveform generator 214 which applies an alternate waveform to the surface 205 being anodised and the electrode 206. The system may also include a support to support device 201 in a manner such that a specific surface of device 201 is exposed to the electrolytic solution.

Chemical solution 204 is typically an electrolytic solution containing an oxygen source. Chemical solution 204 may for example comprise an electrolyte with 0.5 M sulphuric acid. However, concentrations in the range of 0.2 M and 2.0 M can also be used. Sulphuric acid is known to result in faster anodisation compared to other electrolytes (i.e., phosphoric acid and oxalic acid).

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In the example of figure 2, the device being anodised could be a silicon solar cell or a silicon substrate. The surfaces of device 201 could comprise a thin oxide and a metallic layer, such as an aluminium layer which is exposed to the electrolytic solution to be anodised. Device 201 could be positioned on a support in a manner such that only the aluminium layer is exposed to electrolytic solution 204 during the anodisation process.

35 In some embodiments, apparatus 200 includes a radiation source arranged to illuminate a portion of the device

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being anodised. If the device being anodised is capable of generating a photocurrent, such as a solar cell, the photocurrent is used to promote anodisation of the surface portion. In some embodiments the radiation source and the alternate waveform generator 214 generator are used in synergy and the radiation source may be driven using a specular waveform to the one applied by waveform generator 214. In some other embodiments, the photocurrent may be sufficient to sustain the anodisation process and the radiation induced current may be the primary or sole drive of the process.

In the embodiment illustrated in figure 2, alternate waveform generator 214 is a current generator which provides a current with a square waveform (pulsed) through the electrochemical circuit comprising device 201, electrolytic solution 204 and electrode 206.

Referring now to figure 3, there is shown a schematic of a simplified implementation of an alternate waveform current generator 300 in accordance with an embodiment. Current generator 300 comprises a pulse generator 302 capable of generating currents with an alternate waveform and, in particular, pulsed waveforms. Generator 300 also comprises a metering function implemented by ammeter unit 304 and volt meter unit 306. The metering function allows monitoring the applied current and the equivalent resistance at the output of the waveform generator. In addition, generator 302 includes a data logging module 308 to store data related to the applied waveforms.

An example of current waveform 400 used to anodise a metallic surface is shown in figure 4. In the example of figure 4, the waveform is designed to be symmetric in respect to the amplitude axis, meaning that the positive value of current applied to the circuit has the same

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magnitude of the negative value of current. The duty cycle of waveform 400 is 50%. This means that the duration of the positive current equals the duration of the negative current. Depending on the material being anodised, and the
5 electrochemical solution being used, waveform 400 provides a different value of stored charge in the anodised layer.

The ability to control the magnitude and also the sign of the stored charge simultaneously provides a great
10 advantage for the fabrication of numerous electronic devices. In the case of silicon solar cells, for example, anodised layers can be used to passivate silicon surfaces. Generally highly doped silicon surfaces are positioned in proximity of electrical contacts to minimise minority
15 carrier recombination. Depending on the type of doping of the silicon material, anodised layers with a different type of residual charge are required to improve the passivation performance.

20 Referring now to figure 5, there are shown two schematic representations of solar cell devices 500 and 550. Figure 5(a) shows a solar cell with a phosphorous doped emitter 502. For this type of emitter an anodised layer 504 containing a high positive stored charge ($+Q_{eff}$) is used
25 for passivation. In the case of the solar cell device 550 of figure 5(b), the highly boron doped emitter 552, must be passivated with a dielectric layer 554 with a highly negative stored charge to provide optimal performance ($-Q_{eff}$).

30 Referring now to figure 6(a), there is shown a schematic representation of a solar cell device 600. The back surface 602 of solar cell 600 has a plurality of closely spaced n^+ (604) and p^+ (606) regions. For surface 602 a
35 passivation layer containing a high amount of positive or negative stored charge is not suitable. An anodised layer

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with a quasi-neutral stored charge 608 provides better performance in this case. Figure 6(b) shows an actual implementation of device 600. In the Interdigitated Back Contact (IBC) Cell 650, n-type regions 652 and p-type regions 654 are interdigitated at the back of the device. The rear surface can be passivated by an anodic aluminium oxide layer 656 which can be in accordance with method 100 to obtain an interface with very low interface defects and a neutral stored charge.

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Anodised layers manufactured in accordance with method 100 can be used in other electronic devices and, in particular in other types of solar cells where a control over the stored charge of the anodised layer is desirable. These solar cell structures include perovskite and kesterite based photovoltaic cells.

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In general, semiconducting metal oxides realised by anodising a metallic material by method 100 provide the possibility of creating a charge type filtering structure for separating positive charge carriers from negative charge carriers. These types of structures can be used as charge type selective contacts in a plurality of photovoltaic devices. In particular, these structures can be beneficial to form charge type selective molybdenum oxide layers, tungsten oxide layers and titanium oxide layers. Charge type filtering is provided by the capability of tuning the electronic environment of the O atoms using method 100 and apparatus 200. Current deposition methods of sputtering and evaporation allow little material control.

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Referring now to figure 7, there is shown a schematic band diagram 700 of a photovoltaic device comprising two charge type selective contacts. These can also be referred to as 'hole selective membrane' 702 and 'electron selective

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membrane' 704, depending on whether they are designed to filter electrons or holes. Carrier-selective contacts for silicon solar cells require aligned band edges for electron/hole transport. They need to minimise recombination at the silicon interface and provide a good diffusion barrier for the metal contact. In addition they need to comply with the series resistance requirements of the device.

By tuning the parameters of the alternate waveform provided by alternate waveform generator 214, the amount of stored charge in the anodised layer can be engineered and so the carrier selectivity of semiconductive metal oxides layers realised in accordance with method 100.

Figure 8 shows a plot 800 with a current profile 702 (dashed line) and a voltage profile 704 (full line) of a sample anodised by a pulsed waveform with a 50% duty cycle used in a series of experiments performed on solar cells. In these experiments, an alternate waveform generator was used in constant current mode with $I = 30 \text{ mA}$ with a voltage limit of 30V. The duty cycle was varied between 50% and 95%. Cycle lengths of 20 s and 10 s were used.

Figure 9 shows a plot 900 with a comparison of two voltage profiles for anodised layers formed by conventional and pulsed (with negative cycles removed from the graph) anodisation techniques. The voltage profiles of the two anodisation processes have a similar shape while the pulsed anodisation 904 takes longer time to complete. This indicates that the introduced negative portion of the cycle in the pulsed waveform is likely to stimulate reverse reactions for which the positive cycle has to compensate.

Referring now to Figure 10, there are shown two plots 130

and 150 of the effective stored charge density and dark saturation current density for different MIS structures comprising a silicon dioxide interlayer and an anodised metallic layer. Plot 130 shows the effective stored charge density as a function of positive cycle percentage for samples with three different of AAO thicknesses: 400 nm (triangles 132); 280 nm (circles 134) and 50 nm (squares 136) on 17 nm intervening SiO₂ layer. Error bars indicate the standard deviation of independent samples.

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The Q_{eff} of the SiO₂/AAO dielectric stack varied as a function of the duty cycle of the applied waveform for dielectric stacks with different AAO thickness. With decreasing duty cycle, the magnitude of the positive Q_{eff} decreases and then, for thicker AAO layers, is inverted to a net negative charge at low duty cycle values.

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In these specific experiments, for the MIS structures with a 50 nm AAO layer, however, varying the duty cycle was only able to change the magnitude of Q_{eff} but not the polarity even at a 30% positive duty cycle. For the MIS structures with thicker AAO layers, the magnitudes of the achieved negative Q_{eff} were similar in all cases, indicating the presence of limiting factors other than duty cycle and AAO thickness. The SiO₂ interlayers, for example, have been found to have strong impact on the limiting Q_{eff} range. By reducing the SiO₂ from 17 nm to 12 nm, more negative Q_{eff} can be achieved, as shown in plot 150.

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Plot 150 shows the effective stored charge density as a function of duty cycle for samples with two types of AAO thicknesses: 300 nm (squares 152) and 100 (circles 154) nm on 12 nm intervening SiO₂ layer. Error bars indicated the standard deviation of independent samples. The Q_{eff} follows a similar trend with the varying positive pulse percentage

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for the two different AAO thicknesses. However, the 300 nm AAO samples demonstrated high positive stored charge under low positive pulse condition. A prolonged negative DC bias can cause an increase in both interface defect density and positive Q_{eff} . In this case, the samples with 300 nm AAO experienced a longer anodisation process in which a negative bias was applied for 70% of the total duration. This relates to the increase in Q_{eff} shown in plot 150 for the 300 nm AAO samples. The 100 nm AAO samples did not go through a longer anodisation process, thus the interface damages were less severe and could be readily regenerated by the subsequent annealing process.

Figure 11 shows a schematic diagram of a test structure used to determine the stored charge distribution. In the experiments discussed above, the amount of stored charge has been calculated using the model discussed below. This model focuses on the effective value of stored charge at the SiO_2/Si interface. Structure 180 consists of an interface charge of Q_{SiO} at SiO_2/Si interface, Q_{AlO} at $\text{AlO}_x/\text{SiO}_2$ interface and bulk stored charge ρ .

The test structures consist of a series of AAO layers formed by 85% positive pulse anodisation with different thicknesses. AAO layers were deposited on a SiO_2 interlayer that forms a gate dielectric for a MOS CV structure with p-type silicon layer. Two interface charges and a bulk stored charge are the main contributors to the induced surface voltage, and thus the measured effective stored charge (Q_{eff}). Based on this model, the flatband voltage is given as:

$$V_{FB} = \phi_{MS} - \frac{1}{C_{\text{tot}}} (Q_{\text{SiO}} + Q_{\text{AlO}} \frac{t_{\text{effAlO}}}{t_{\text{eff}}} + \int_0^{t_{\text{effAlO}}} \frac{\rho(x) \cdot x}{t_{\text{eff}}} dx)$$

where C_{tot} is the total capacitance of the stack; t_{effAlO} is

the effective oxide thickness of the AlO_x layers. $t_{\text{eff\_AlO}}$ is calculated by multiplying the physical thickness of the AlO_x layer by a ratio between the dielectric constants of Si and Al_2O_3 . The total effective oxide thickness, t_{eff} , is the physical thickness of the interlayer oxide: t_{SiO_2} plus $t_{\text{eff\_AlO}}$. The position, x , is defined to be zero at the outmost surface of the AlO_x layers. The AlO_x bulk stored charge is assumed to be constant through the AAO thickness. With a few rearrangements, the previous equation can be simplified to:

$$V_{FB} = \phi_{MS} - \frac{1}{\epsilon_{Si}} (Q_{SiO} \cdot t_{eff} + Q_{AlO} \cdot t_{eff\_AlO} + \frac{\rho \cdot t_{eff\_AlO}^2}{2})$$

Based on this equation, the flatband voltage of the step MIS structures shall display a parabolic relationship to the total effective oxide thickness.

Referring now to figure 12, there is shown a plot comprising a parabolic fitting of the measured V_{FB} as a function of t_{eff} . The fitting can be used to extract Q_{SiO} , Q_{AlO} and ρ by comparing the fitted analytic formula to the last equation. The extracted parameters are shown in table I.

Q_{SiO}	Q_{AlO}	ρ
$-4.42 \times 10^{11} \text{ q/cm}^2$	$1.79 \times 10^{11} \text{ q/cm}^2$	$2.30 \times 10^{16} \text{ q/cm}^3$

Table I. Parameters extracted from a parabolic fitting of flatband voltage as a function of effective oxide thickness.

Referring now to figure 13, there is shown a plot of the simulated effective charge as a function of the anodised layer thickness for different dielectric inter-layer thicknesses. The measured Q_{eff} is related to Q_{SiO} , Q_{AlO} and ρ by the following equation:

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$$Q_{eff} = Q_{SiO} + Q_{AlO} \cdot \frac{t_{effAlO}}{t_{eff}} + \frac{\rho \cdot t_{effAlO}^2}{t_{eff}}$$

The input parameters for this equation can be extracted from the fitting in figure 12, (85% duty cycle). Figure 13 shows the behaviour of Q_{eff} for interlayer thicknesses of 30 nm (352), 20 nm (354), 17 nm (356), 12 nm (358) and 3 nm (360). Plot 350 demonstrates that with a thinner interlayer SiO_2 , a higher value of negative charge can be achieved.

The anodisation method described herein can be also used to control the stored residual charge in the channel oxide of metal-oxide-semiconductor (MOS) capacitors and other types of capacitors. The accurate control of the stored residual charge in the channel oxide is important to optimise the performance of MOS based devices, such as MOS field effect transistors.

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

Throughout this specification the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

The Claims:

1. A method of anodising a surface comprising a metallic material, the method comprising the steps of:
- 5 exposing a portion of the surface to an electrolytic solution that is suitable for anodising the metallic material;
- exposing a portion of an electrode to the electrolytic solution;
- 10 selecting one or more parameters of an alternate waveform; and
- applying an electric wave having the alternate waveform to the exposed portion of the surface to anodise the portion of the surface;
- 15 wherein the one or more parameters of the alternate waveform are selected in a manner to influence an amount of stored charge embedded in the anodised material.
2. A method of controlling stored charge in an anodised material comprising the steps of:
- 20 selecting one or more parameters of an alternate waveform; and
- applying an electric wave having the alternate waveform between a metallic material and an electrode
- 25 while the metallic material is being anodised.
3. The method of claim 1 or claim 2 wherein the one or more parameters of the alternate waveform are selected in a manner to influence sign and magnitude of stored charge
- 30 embedded in the anodised material.
4. The method of claim 3 wherein the alternate waveform is a square waveform and the step of selecting one or more parameters of the alternate waveform comprises selecting
- 35 one or a combination of:
- i. a positive value of the waveform;

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- ii. a negative value of the waveform;
- iii. a duty cycle value of the waveform; and
- iv. a frequency value of the waveform.

5 5. The method of claim 4 wherein the selected value of duty cycle is between 30% and 100%.

6. The method of claim 4 or claim 5 wherein the selected value of frequency is between 0.05Hz and 10Hz.

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7. The method of any one of claims 4 to 6 wherein the alternate waveform is a pulsed waveform.

8. The method of any one of claims 4 to 7 wherein the
15 alternate waveform is a square waveform and the step of selecting one or more parameters of the alternate waveform comprises at least selecting the positive value or the negative value.

20 9. The method of claim 8 wherein the alternate waveform is a current waveform.

10. The method of claim 9 wherein the positive current value is between 1 mA/cm² and 5 mA/cm².

25

11. The method of claim 9 or claim 10 wherein the negative current value is between -1 mA/cm² and -5 mA/cm².

12. The method of claim 8 wherein the alternate waveform
30 is a voltage waveform.

13. The method of claim 12 wherein the positive voltage value is between 10 V and 50 V.

35 14. The method of claim 12 or claim 13 wherein the negative voltage value is between -10 V and -50 V.

15. The method of any one of the preceding claims wherein the one or more parameters of the alternate waveform are selected in a manner such that the stored charge embedded
5 in the anodised material has an effective density between $-10 \cdot 10^{11} \text{ q/cm}^2$ to $10 \cdot 10^{12} \text{ q/cm}^2$.

16. The method of any one of the preceding claims wherein the electrode comprises one or a combination of nickel,
10 copper and aluminium.

17. An apparatus for anodising a surface comprising a metallic material, the apparatus comprising:
a container for containing an electrolytic solution;
15 an electrode element positioned for contacting the electrolytic solution; and
an alternate waveform generator arranged to apply an electric wave having an alternate waveform to the exposed portion and the electrode while the metallic material is
20 being anodised.

18. The apparatus of claim 17 wherein the generator is arranged to apply a current waveform through the surface comprising the metallic material and the electrode and to
25 provide tunability of one or more parameters of the alternate waveform.

19. The apparatus of claim 18 wherein the alternate waveform is a square waveform and the generator is
30 arranged to provide tunability of one or a combination of:
i. a positive current value of the waveform;
ii. a negative current value of the waveform;
iii. a duty cycle value of the waveform; and
iv. a frequency value of the waveform.

35
20. The apparatus of claim 19 wherein by tuning one or a

- 22 -

combination of parameters i to iv the amount of stored charge embedded in the anodised material is influenced.

21. The apparatus of claim 20 wherein the amount of
5 stored charge embedded in the anodised material is
controllable between $-10 \cdot 10^{11} \text{ q/cm}^2$ to $10 \cdot 10^{12} \text{ q/cm}^2$.

22. The apparatus of any one of claims 17 to 21 wherein
10 the electrode comprises one or a combination of nickel,
copper and aluminium.

23. The apparatus of any one of claims 17 to 22 further
comprising a support arranged to support a device, the
surface comprising the metallic material being part of the
15 device, such that in use the surface is exposed to the
electrolytic solution when the container is charged with
the electrolytic solution.

24. The apparatus of claim 23 further comprising a
20 radiation source arranged to illuminate a portion of the
device in a manner such that a radiation-induced current
is generated in the device to promote anodisation of the
surface comprising the metallic material.

25. A charge filtering structure for separating positive
charge carriers from negative charge carriers comprising
an anodised material which is anodised in accordance with
any one of claims 1 to 16.

26. A Perovskite based photovoltaic cell comprising a
30 charge filtering structure in accordance with claim 25.

27. A kesterite based photovoltaic cell comprising a
charge filtering structure in accordance with claim 25.
35

28. A photovoltaic cell device comprising an anodised

layer formed by a method in accordance with any one of claims 1 to 16.

29. A photovoltaic cell device comprising a negatively
5 doped base region and a positively doped emitter region
wherein the emitter region is in contact with an anodised
layer formed by a method in accordance with any one of
claims 1 to 16, the anodised layer having a net negative
stored charge and being arranged to electrically passivate
10 at least a portion of the emitter region.

30. A photovoltaic cell device comprising a positively
doped base region and a negatively doped emitter region
wherein the emitter region is in contact with an anodised
15 layer formed by a method in accordance with any one of
claims 1 to 16, the anodised layer having a net positive
stored charge and being arranged to electrically passivate
at least a portion of the emitter region.

20 31. A photovoltaic cell device comprising:
a base region;
an emitter region;
a contacting region, the contacting region comprising
a plurality of interdigitated negatively doped and
25 positively doped semiconducting portions; and
an anodised layer, disposed in proximity of the
contacting region, the anodised layer being formed by a
method in accordance with any one of claims 1 to 16.

30 32. The photovoltaic cell of claim 31 wherein the
anodised layer has a quasi-neutral net stored charge.

33. A metal-oxide-semiconductor capacitor structure
comprising:
35 a semiconducting substrate or a semiconducting layer;
a thin dielectric layer disposed on a surface portion

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of the semiconducting substrate or a semiconducting layer,
the thin dielectric layer being formed by a method in
accordance with any one of claims 1 to 16; and

an electrode disposed in contact with at least a
5 portion of the thin dielectric layer.

34. A metal-oxide-semiconductor field effect transistor
comprising a metal-oxide-semiconductor capacitor in
accordance with claim 33.

10

1/13

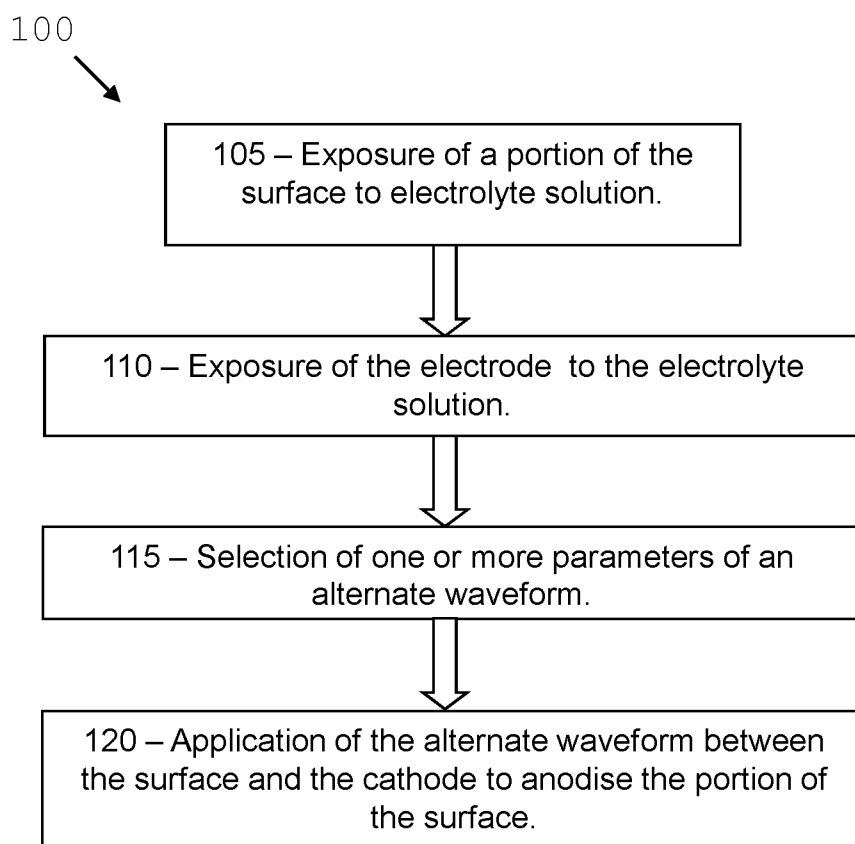


FIGURE 1

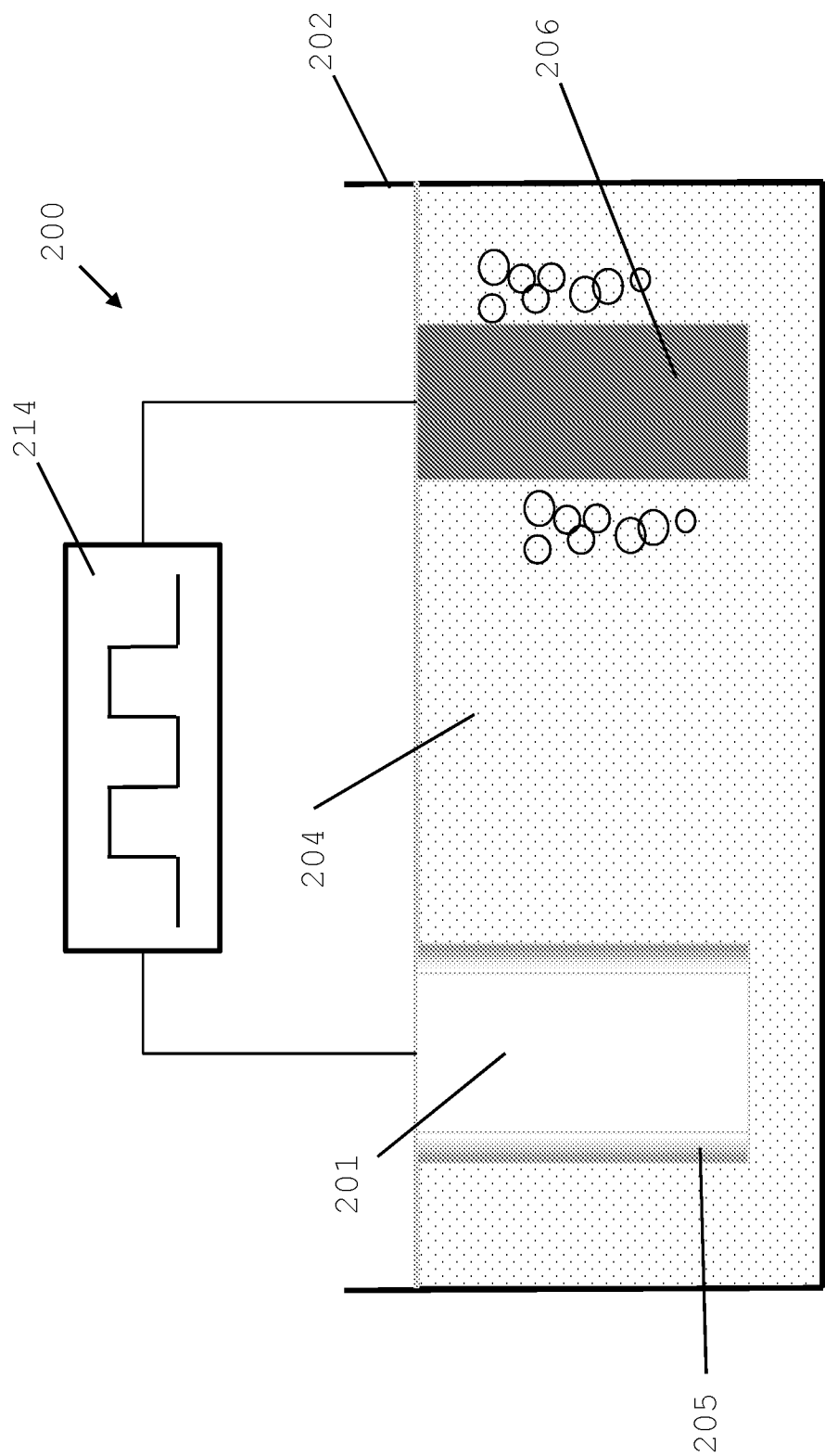


FIGURE 2

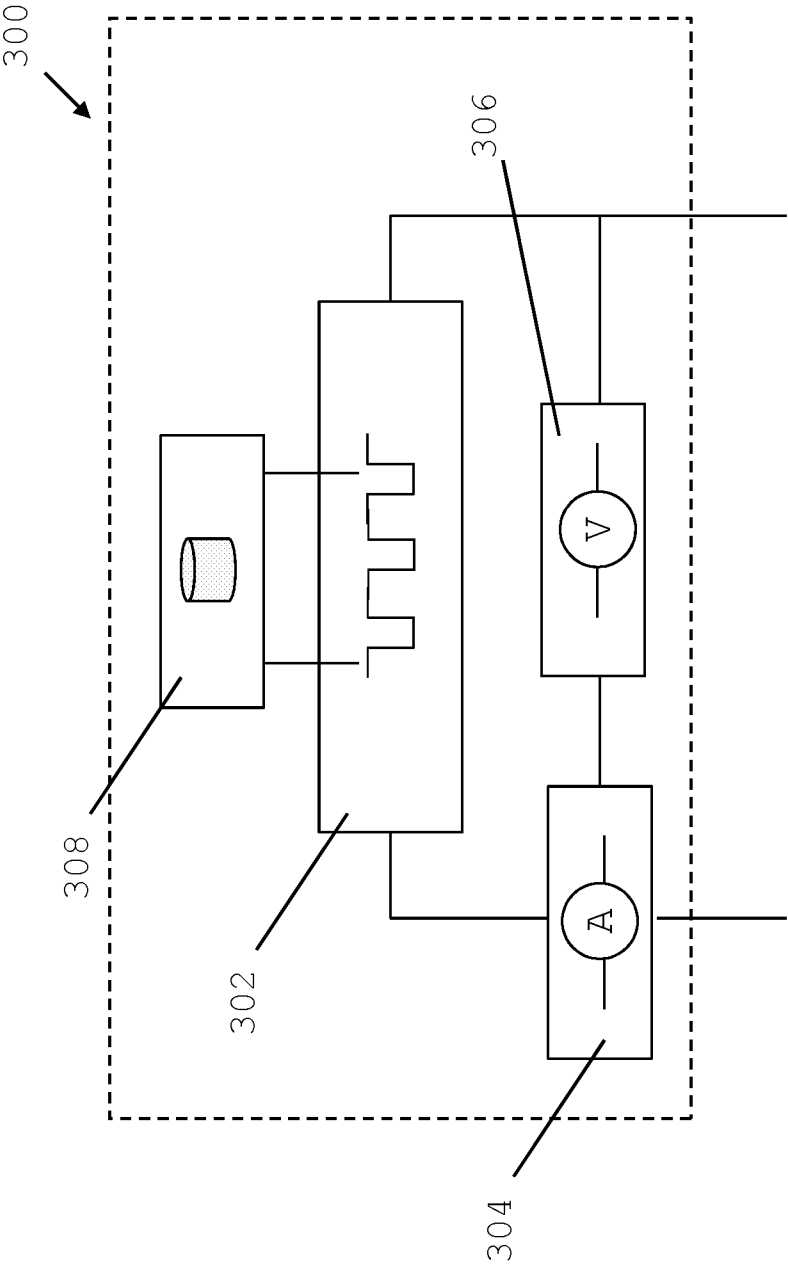


FIGURE 3

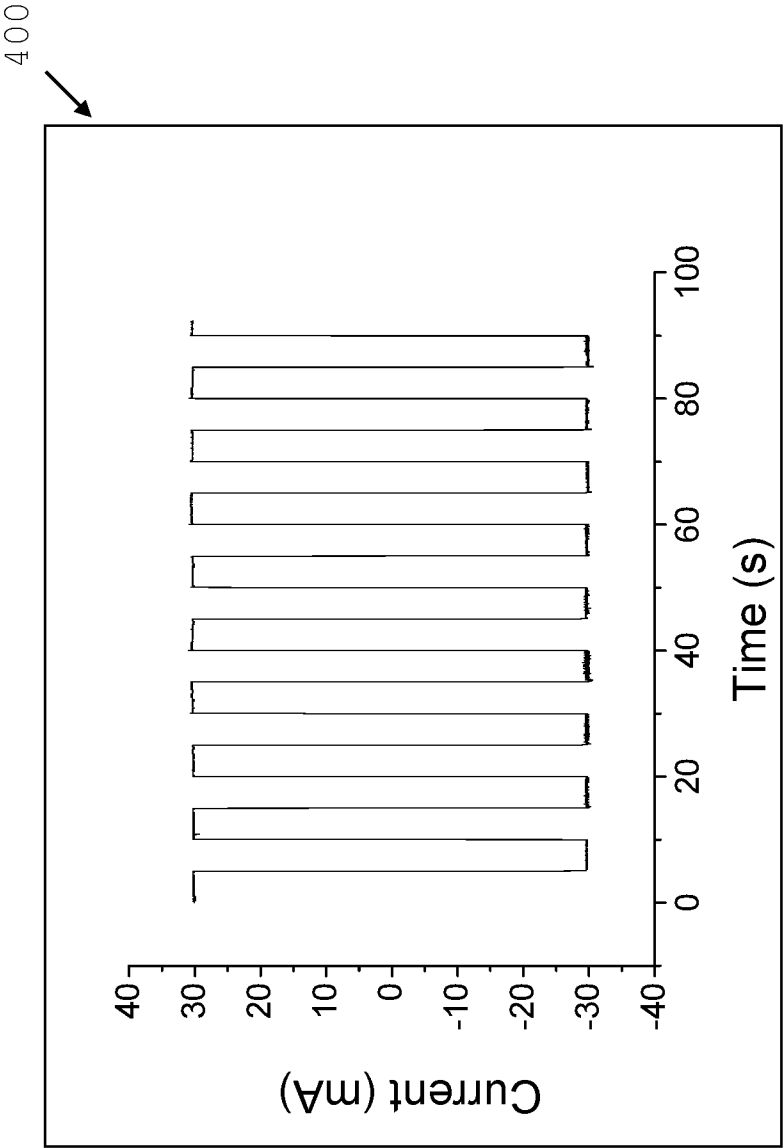


FIGURE 4

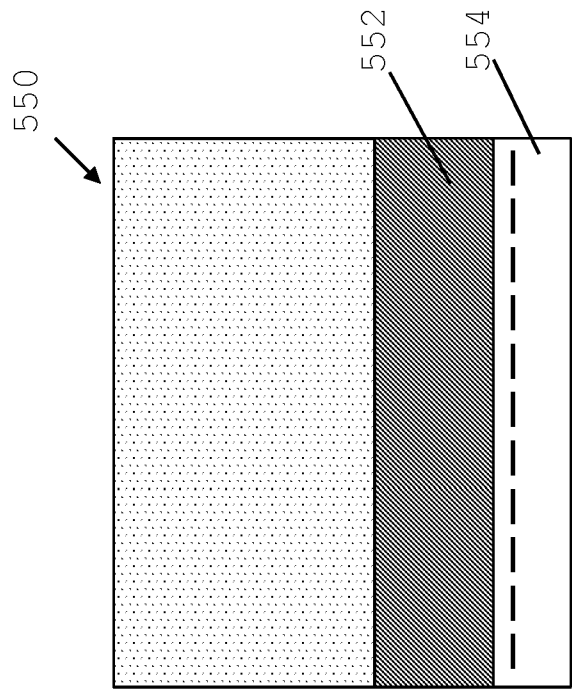


FIGURE 5(b)

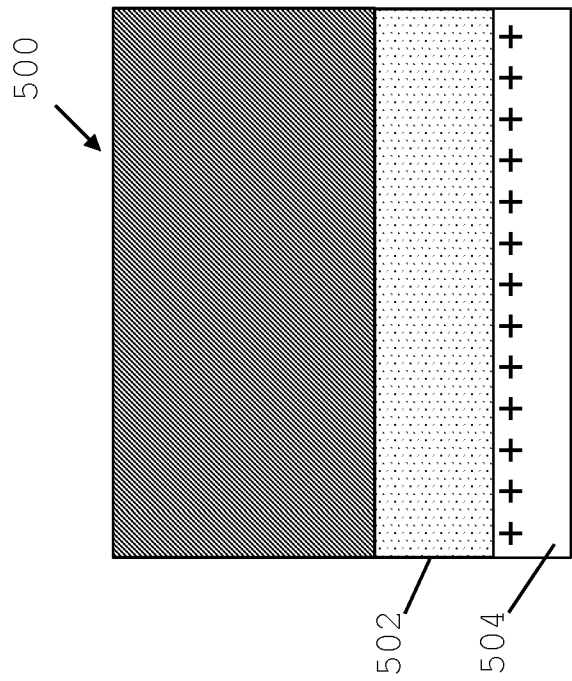


FIGURE 5(a)

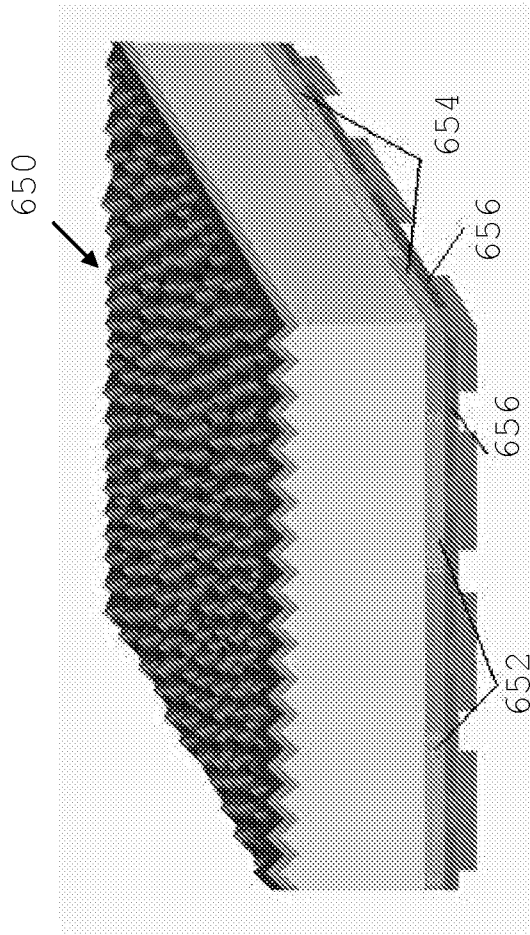


FIGURE 6(b)

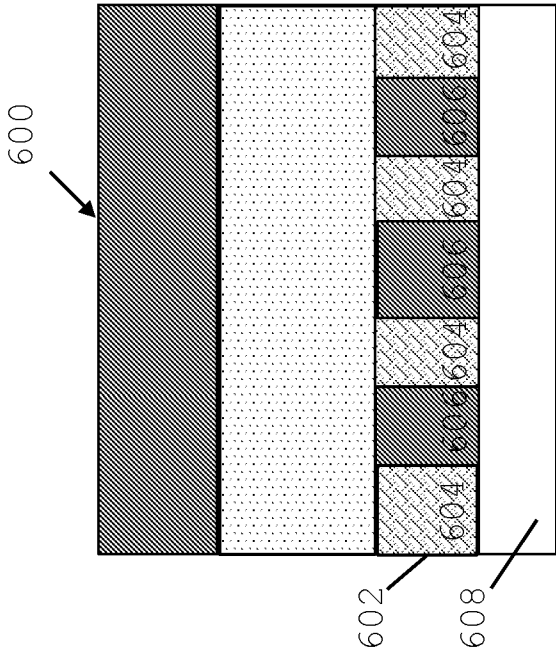


FIGURE 6(a)

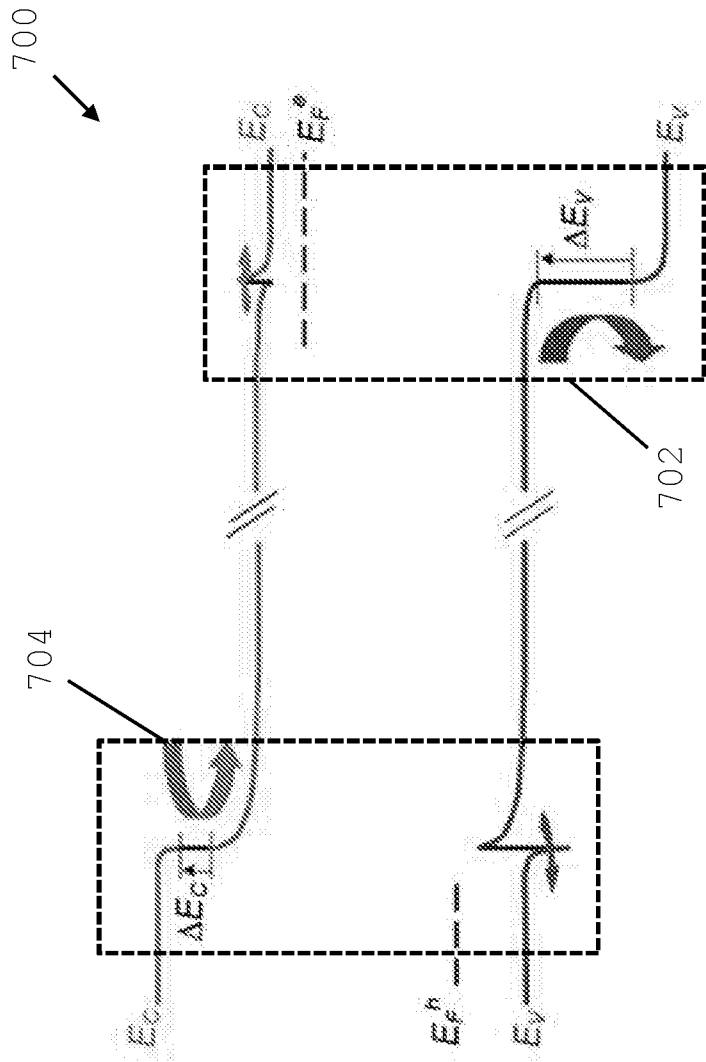


FIGURE 7

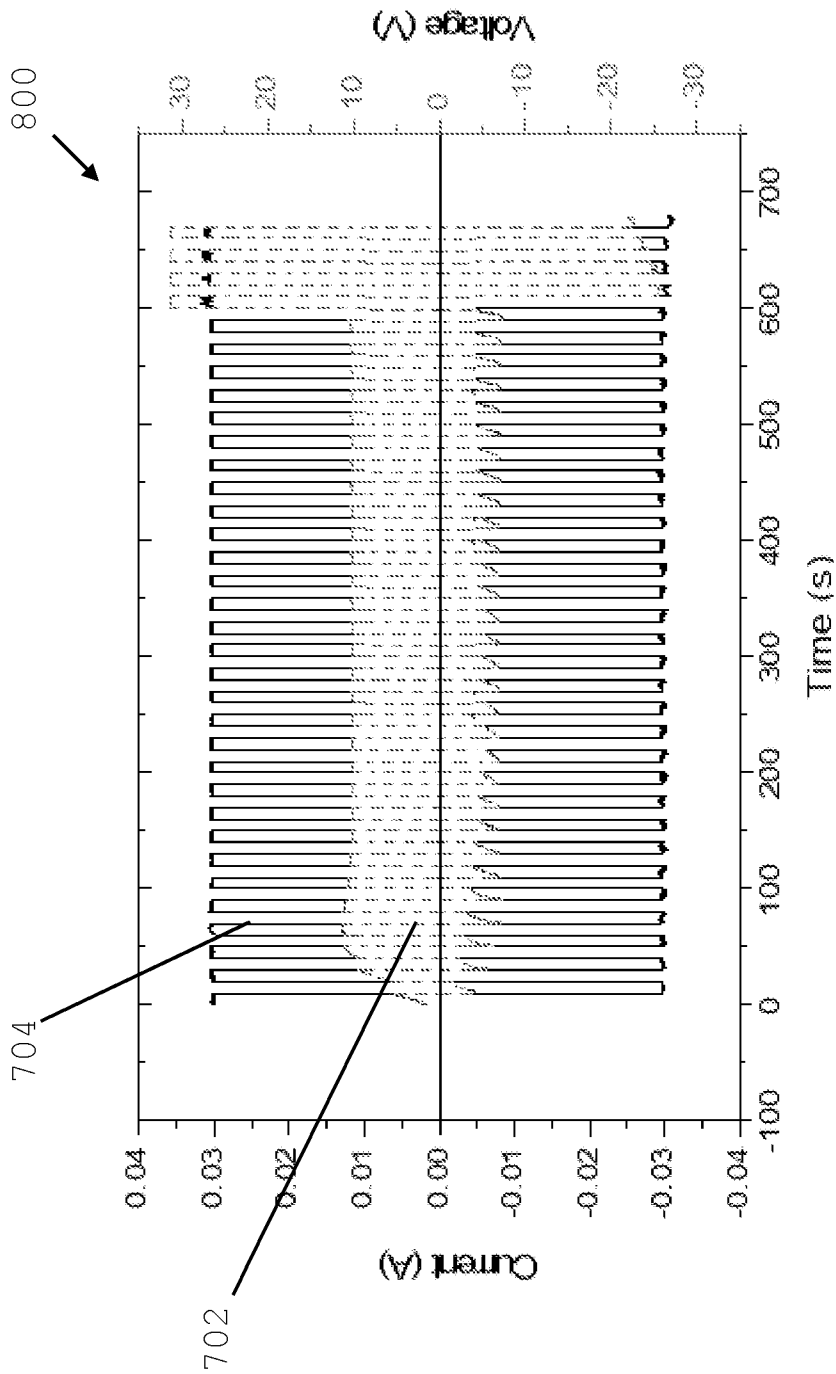


FIGURE 8

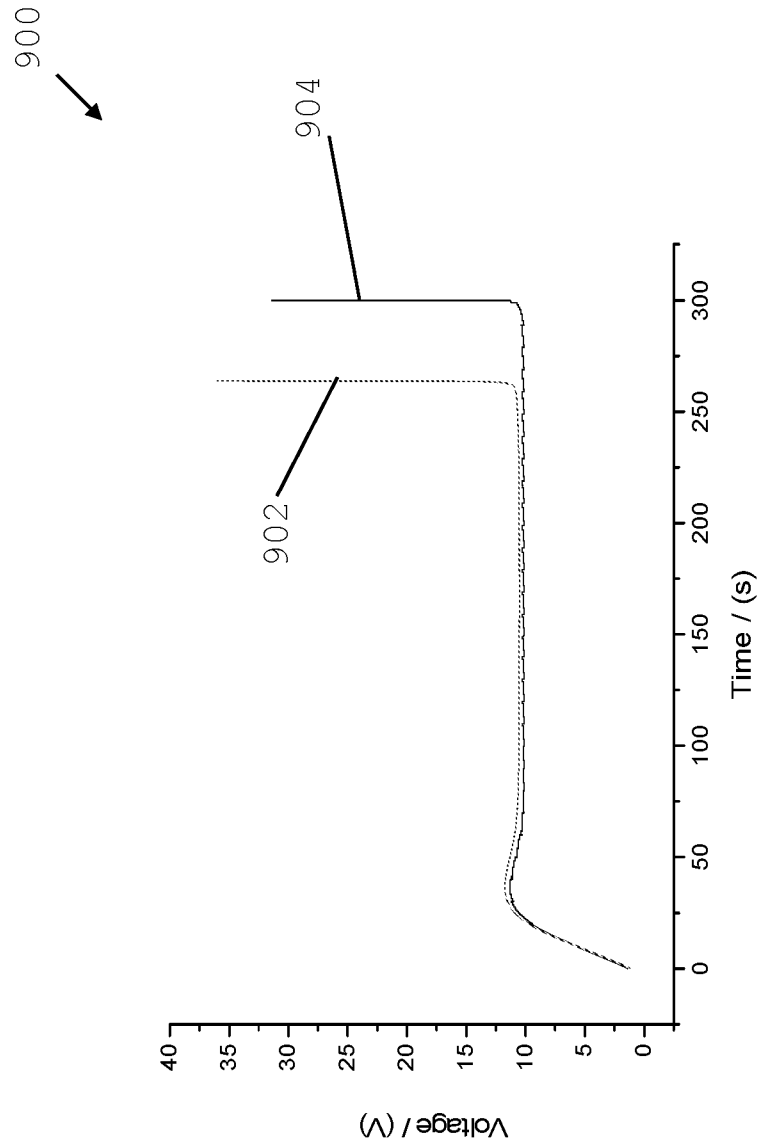


FIGURE 9

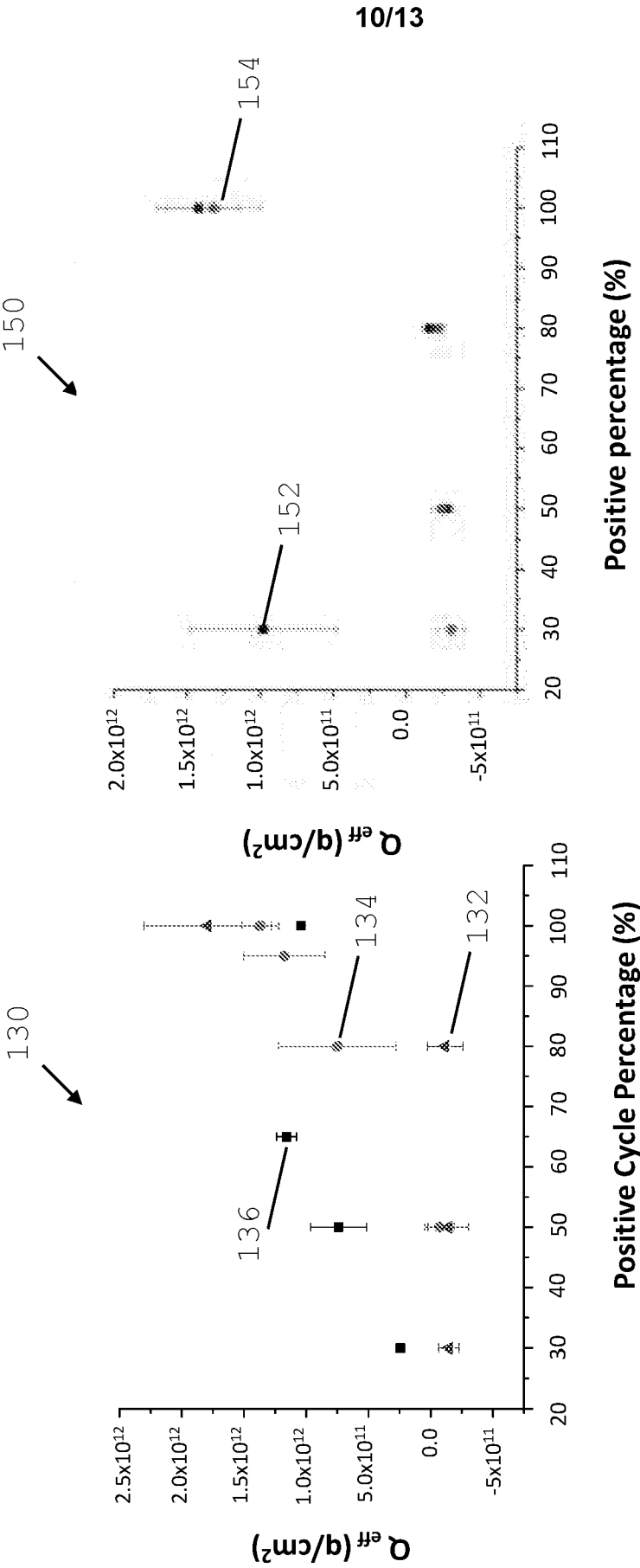


FIGURE 10(a)

FIGURE 10(b)

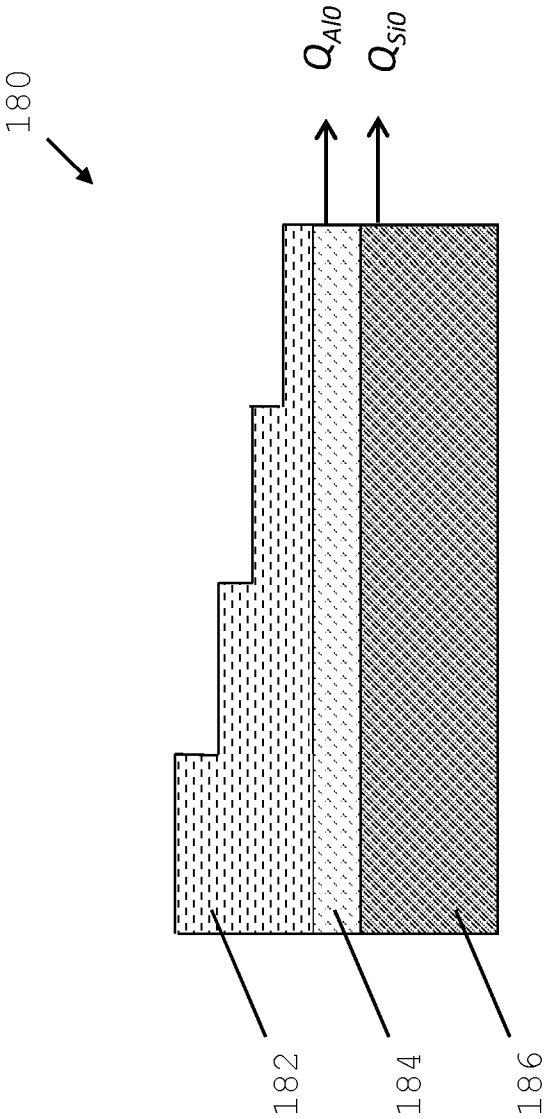


FIGURE 11

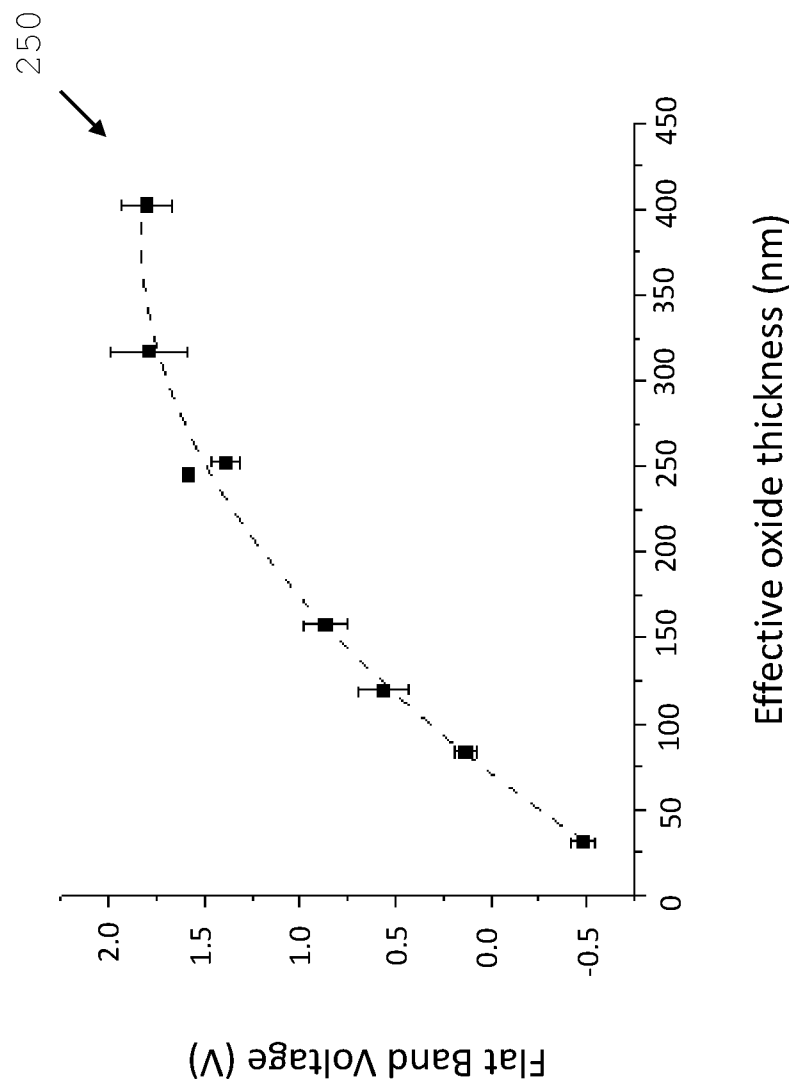


FIGURE 12

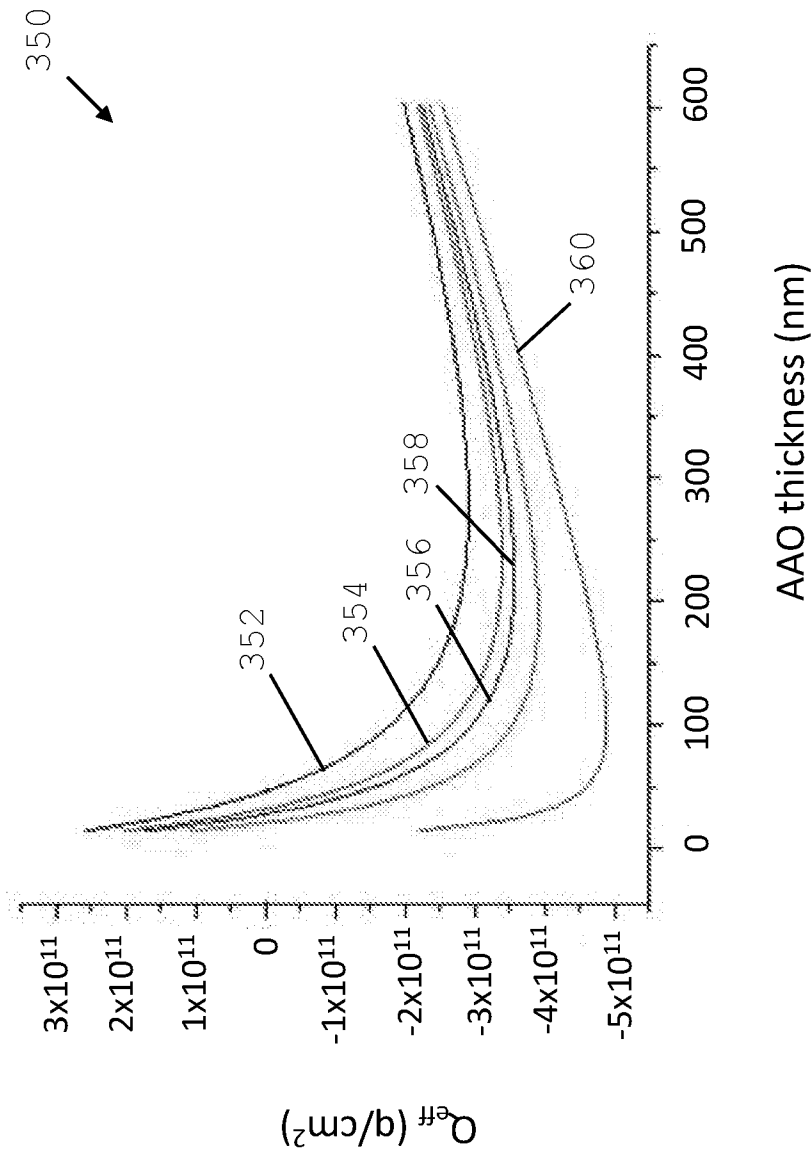


FIGURE 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/AU2016/050027

A. CLASSIFICATION OF SUBJECT MATTER

C25D 11/02 (2006.01) H01L 21/31 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPOQUE X-FULL: Databases: TXPEA, TXPEB, TXPEC, TXPEE, TXPEF, TXPEH, TXPEI, TXPEP, TXPEPEA, TXPES, TXPUSE0A, TXPUSE1A, TXPUSEA, TXPUSEB, TXPW0EA, WPIAP, EPODOC; class mark: C25D, keywords: anodiz(s)ation, electrode, cathode, electrolyte, solution, fluid, liquid, pool, wave, charge, store, carry, contain, embed. Espacenet and Google Patent searches: IPC mark: H01L; KW: anodiz(s)ation, dielectric constant, passivation, wave, pulse, alternate, charge, store, carry, contain, density, and like terms. AusPat, PAMS NOSE, Espacenet, and INTESS applicant and inventor searches: Applicant name: newsouth innovations; Inventor name: alison lennon, zhong lu; keywords: anodiz(s)ation.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* "A"	Special categories of cited documents: document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
29 February 2016

Date of mailing of the international search report
29 February 2016

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INTERNATIONAL SEARCH REPORT		International application No.
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		PCT/AU2016/050027
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5165991 A (FUKUDA ET AL.) 24 November 1992 Abstract, column 2, line 64 - column 3, line 34, examples Abstract, column 2, line 64 - column 3, line 34, examples	1-23, 25-34 24
X Y	CN 101478114 A (CHANGCHUN UNIVERSITY OF SCIENCE AND TECHNOLOGY) 08 July 2009 Abstract, page 4, Figures Abstract, page 4, Figures	17-19, 22-23 24
X Y	GB 1519832 A (RIKEN KEIKINZOKU KOGYO KABUSHIKI) 02 August 1978 Figures, page 1, lines 8-26 Figures, page 1, lines 8-26	17-19, 22-23 24
Y	WO 2014/153597 A1 (NEWSOUTH INNOVATIONS PTY LIMITED) 02 October 2014 Abstract, page 3, claims	24
A	US 5185075 A (ROSENBERG ET AL.) 09 February 1993 Abstract, columns 2-3	1-34

INTERNATIONAL SEARCH REPORT		International application No.	
Information on patent family members		PCT/AU2016/050027	
This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.			
Patent Document/s Cited in Search Report		Patent Family Member/s	
Publication Number	Publication Date	Publication Number	Publication Date
US 5165991 A	24 November 1992	US 5165991 A	24 Nov 1992
		JP H05210245 A	20 Aug 1993
		JP 2739792 B2	15 Apr 1998
CN 101478114 A	08 July 2009	CN 101478114 A	08 Jul 2009
GB 1519832 A	02 August 1978	GB 1519832 A	02 Aug 1978
		AU 500211 B2	17 May 1979
		AU 8356875 A	03 Feb 1977
		DE 2534248 A1	12 Feb 1976
		FR 2280720 A1	27 Feb 1976
		JP S5116242 A	09 Feb 1976
		JP S5424695 B2	23 Aug 1979
		WO 2014/153597 A1	02 October 2014
		TW 201506208 A	16 Feb 2015
US 5185075 A	09 February 1993	US 5185075 A	09 Feb 1993
End of Annex			