(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2007 (27.12.2007)

PCT

(10) International Publication Number
WO 2007/148156 A1

(51) International Patent Classification:
H04L 7/02 (2006.01) *H03K 3/356* (2006.01)
H03K 3/037 (2006.01)

(21) International Application Number:
PCT/IB2006/051992

(22) International Filing Date: 20 June 2006 (20.06.2006)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **FREESCALE SEMICONDUCTOR, INC.** [US/US]; 6501 William Cannon Drive West, Austin, Texas 78735 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PRIEL, Michael** [IL/IL]; Shmuel Hanagid 18/15, 46498 Hertzelia (IL). **KUZMIN, Dan** [IL/IL]; Rahavat Ilan 18/32, 54056 Givat Shmuel (IL). **ZALTZMAN, Amir** [IL/IL]; Doar-na Menashe, 37830 Moshav Amikam (IL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

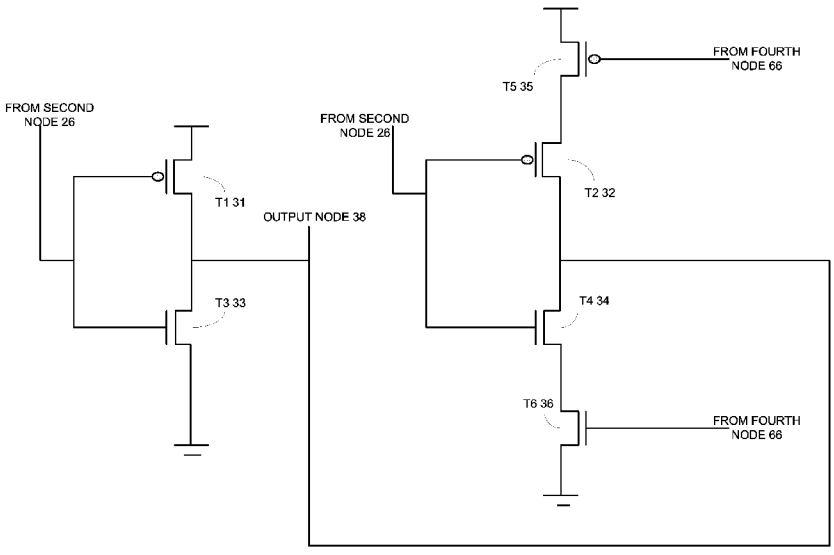
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** DEVICE AND METHOD FOR HADLING METASTABLE SIGNALS



(57) **Abstract:** A method and device for managing metastable signals. The device (10) includes: a first latch (11) and a second latch (12), a multiple switching point circuit (30), connected between an output node of the first latch (11) and an input node of the second latch (12), wherein the multiple switching point circuit (30) includes at least one pull up transistor and at least one pull down transistor that are selectively activated in response to a feedback signal provided from the second latch (12) and in response to a an output signal of the first latch (11) such as to define at least a low switching point that is lower than a high switching point of the multiple- switching point circuit (30); wherein a switching point of an inverter within the first latch is between the high and low switching points.

WO 2007/148156 A1

DEVICE AND METHOD FOR HADLING METASTABLE SIGNALS

FIELD OF THE INVENTION

The present invention relates to devices and methods for handling metastable signals.

BACKGROUND OF THE INVENTION

Synchronized devices sample or receive data by sampling the data at sampling points that are usually defined by a clock signal. In order to sample the data correctly timing constraints (such as setup period and hold period) are imposed. These timing constraints define the timing difference between data signal transitions and clock signal transitions. In a nutshell, sampling requires that there is a minimal timing difference between said transitions.

Synchronizers are commonly used for interfacing different circuits that reside into clock domains that are mutually asynchronous. Typically, a synchronizer receives a data signal from an asynchronous circuit that is not clocked at all, but this is not necessarily so. This a-synchronicity complicates the imposition of the mentioned above timing constraints. Accordingly, the synchronizer can sample the data signal while the data signal is not properly defined - it is within a meta-stable range. The synchronizer will eventually converge into a stable position but the convergence period is not indeterminable.

Various methods and devices were suggested for coping with metastability. Some include level sensitive circuits, some include complex circuits that are characterized by a finite and predictable metastable time and some include oscillation suppressors and decentration

circuits. The following U.S. patents, all being incorporated herein by reference, illustrates some prior art circuits: U.S. patent 482093 of Sowell et al., U.S patent 6072346 of Ghahremani and U.S. 5045801 of Mowery.

There is a need to provide efficient methods and devices for methods handling meta-stable signals.

SUMMARY OF THE PRESENT INVENTION

A device and a method for handling metastable signals, as described in the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

FIG. 1 illustrates an apparatus according to an embodiment of the invention;

FIG. 2 illustrates a multiple switching point circuit according to an embodiment of the invention;

FIG. 3 illustrates a transfer function of a synchronizer and of an inverter within a first latch according to an embodiment of the invention.

FIG. 4 is a flow chart of a method for handling meta-stable signals according to an embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention illustrated in the accompanying drawings provide an information processing apparatus such as a mobile phone, a personal data accessory or a media player that includes a device that is capable of managing meta-stable sates.

The device includes a multiple switching point circuit that outputs definite output signals. The multiple switching point circuit can receive a metastable signal but is capable of outputting definite signals. The multiple switching point circuit is connected between a first latch and a second latch and is adapted to receive a feedback signal from the second latch and a first output signal from the first latch. These signals determine which pull up transistors and pull down transistors within the multiple switching point circuit are activates. The activated pull up and pull down transistors force either a low switching point or a high switching point. An inverter within the first latch has a switching point between the high and low switching points of the multiple switching point device. The difference between these switching points enables the multiple point switching circuit to change its output signal from a first definite output signal to another definite output signal after the first latch converges or at least starts to converge to a definite state.

FIG. 1 illustrates apparatus 9 according to an embodiment of the invention. Apparatus 9 includes device 10 that in turn may include one or more integrated circuits and may include one or more processors, memory units, DMA controllers and the like. Device 10 can include at least two clock domains that are mutually asynchronous, or can be adapted to receive information from another device, another integrated circuit or another circuit that are mutually asynchronous to device 10.

For simplicity of explanation FIG.1 illustrates a single synchronizer 13, but device 10 may include many synchronizers. The number of synchronizers depends upon

the design of device 10 and especially depends upon the amount of interfaces between mutually asynchronous clock domains.

FIG. 1 illustrates synchronizer 13 that includes first latch 11, second latch 12, first transfer gate 20, second transfer gate 60, output inverter 70 and multiple switching point circuit 30.

First latch 11 includes first inverter 24 and second inverter 28 that are inversely connected to each other such that the input of first inverter 24 is connected to the output of second inverter 28 (at first node 22) while the input of second inverter 28 is connected to the output of first inverter 24 (at second node 26). Second node 26 is an output node of first latch 11 while first node 22 is an input node of first latch 11.

Second node 26 is connected to an input of multiple switching point circuit 30 while the output of multiple switching point circuit 30 is connected to an input of second transfer gate 60. Multiple switching point circuit 30 receives a feedback signal from the output node of second latch 12 - from fourth node 66.

The output of second transfer gate 60 is connected to third node 62 that is the input node of second latch 12. Second latch 12 includes third inverter 64 and fourth inverter 68 that are inversely connected to each other such that the input of third inverter 64 is connected to the output of fourth inverter 68 (at third node 62) while the input of fourth inverter 68 is connected to the output of third inverter 64 (at fourth node 66). Fourth node 66 is an output node of second inverter 12 while third node 62 is an input node of second inverter 12.

Second inverter 28 is also referred to as the feedback inverter of first latch 11. Fourth inverter 68

is also referred to as the feedback inverter of second latch 12.

Output node 66 of second latch 12 is connected to inverter 70. The output node 72 of inverter 70 is the output node of synchronizer 13.

First latch 11 samples an input data signal that arrives from a clock domain that is asynchronous to the clock domain of first latch 11. This can cause first latch 11 to sample that data signal while the data signal is not properly defined. Conveniently, the multiple switching point circuit 30 does not propagate not-defined signals to second latch 12.

The multiple switching point circuit 30 is designed such as to change its output signal from one stable value to another stable value only after second inverter 28 of first latch enters a stable state. In other words the multiple switching point circuit 30 switches after second inverter 28 as well as first latch 11 enter a stable state. The margin between the switching points of multiple switching points circuit 30 and the switching point of second inverter 28 enables first latch 11 to converge to a stable state before multiple switching points circuit 30 switches its state.

According to an embodiment of the invention the first transfer gate 20 is activated by a first clock signal (CLK) and a complementary clock signal (CLK_) while the second transfer gate 26 is activated by the complementary clock signal (CLK_) and the first clock signal (CLK) such that the first transfer gate is opened while the second transfer gate is closed and vice verse.

According to another embodiment of the invention the first transfer gate 20 and the second transfer gate 60 receive a first and second clock signals whereas there

are time gaps between transitions of the first clock signals and transitions of the second clock signal.

Multiple switching point circuit 30 includes at least one pull up transistor (for example PMOS transistor T6 36 of FIG. 2) and at least one pull down transistor (for example NMOS transistor T5 35 of FIG. 2) that are selectively activated in response to a feedback signal provided from second latch 12 such as to define at least a low switching point that is lower than a high switching point of the multiple-switching point circuit 30. Especially, the low switching point of multiple switching point circuit 30 is lower than the switching point of second inverter 28 while the high switching point of multiple switching point circuit 30 is higher than the switching point of second inverter 28.

FIG. 1 further illustrates that multiple switching point circuit 30 includes pull down circuit 43 and pull up circuit 46. First portion 44 of pull down circuit 43 and first portion 47 of pull up circuit 46 are activated when the feedback signal (from fourth node 66) has a first value. Second portion 45 of pull down circuit and second portion 48 of pull up circuit 46 are activated when the feedback signal (from fourth node 66) has a second value that differs from the first value. Conveniently, the first portion 44 of pull down circuit 43 differs from second portion 45 of pull down circuit 43. First portion 47 of pull up circuit 46 differs from second portion 48 of pull up circuit 46.

Conveniently, the pull up portions include pull up transistors that are connected to a voltage supply while the pull down portions include pull down transistors that are grounded. This is not necessarily so.

The high switching point of the multiple switching point circuit 30 is affected by first portions 47 and 44, whereas first portion 47 of pull up circuit 46 is stronger than first portion 44 of pull down circuit 43. The low switching point of the multiple switching point circuit 30 is affected by second portions 45 and 48, whereas second portion 48 of pull up circuit 46 is weaker than second portion 45 of pull down circuit 43.

The switching point of first latch 11 and especially of feedback inverter 28 (of first latch 11) is positioned between the high and low switching points of multiple switching point circuit 30. Accordingly, when the output signal of first latch 11 starts to rise the high switching point of multiple switching point circuit 30 will cause multiple switching point circuit 30 to switch after feedback inverter 28 switches. When the output signal of first latch 11 starts to fall the low switching point of multiple switching point circuit 30 will cause multiple switching point circuit 30 to switch after feedback inverter 28 switches.

FIG. 2 illustrates multiple switching point circuit 30 according to an embodiment of the invention.

Multiple switching point circuit 30 includes: (i) pull up transistors such as PMOS transistors T1 31, T2 32 and T5 35, and (ii) pull down transistors such as NMOS transistors T3 33, T4 34 and T6 36.

First transistor T1 31 and third transistor T3 33 form input inverter 41. Input inverter 41 does not receive a feedback signal from fourth node and is activated regardless of the feedback signal. The gates of first transistor T1 31 and third transistor T3 33 are connected to second node 26 and receive the output voltage (V_out_first_latch 126) of first latch 11.

Fifth transistor T5 35, second transistor T2 32, fourth transistor T4 34 and sixth transistor T6 36 form a cascade of transistors 42. The gates of fifth transistor T5 35 and sixth transistor T6 36 are connected to fourth node 66 to receive feedback signal (V_out_second_latch 166) from second latch 12. The gates of second transistor T2 32 and fourth transistor T4 34 are connected to second node 26.

The output node 38 of multiple switching point circuit 30 is connected to the drains of transistors T1 31, T3 33, T2 32 and T4 34.

Assuming an initial state in which V_out_first_latch 126 and V_out_second_latch 166 are low ('0'). At this initial state transistors T1 31, T2 32 and T5 are open while transistors T3 33, T4 34 and T6 36 are closed. Even if V_out_first_latch 126 starts to rise to a level in which pull down transistors T3 33 and T4 34 will start to conduct then pull up transistors T5 35, T1 31 and T2 32 will conduct such as to define a relatively high switching point. This high switching point is higher then the switching points of second inverter 28 and first inverter 24. Accordingly, the switching point of multiple switching point circuit 30 will occur after first latch 11 converges to output a high output signal.

The level of V_out_second_latch 166 will be low only after multiple switching point circuit 30 switches its state and after second latch 12 switches its state accordingly.

Assuming another initial state in which V_out_first_latch 126 and V_out_second_latch 166 are high ('1').

At this initial state transistors T1 31, T2 32 and T5 are closed while transistors T3 33, T4 34 and T6 36

are open. Even if V_out_first_latch 126 starts to fall to a level in which pull up transistors T1 31 and T2 32 will start to conduct then pull down transistors T3 33, T4 34 and T6 36 will conduct such as to define a relatively low switching point. This low switching point is lower then the switching points of second inverter 28 and of first inverter 24. Accordingly, the switching point of multiple switching point circuit 30 will occur after first latch 11 converges to output a low output signal.

The level of V_out_second_latch 166 will be high only after multiple switching point circuit 30 switches its state and after second latch 12 switches its state accordingly.

FIG. 3 illustrates the transfer function of synchronizer 13 and inverter 28, according to an embodiment of the invention.

Curve 202 illustrates an equilibrium between an input voltage and an output voltage. Curve 204 illustrates the relationship between the input voltage (V_out_first_latch 126) and the output voltage (V_first node 122) of second inverter 28. Curve 202 crosses curve 204 at the switching point (211) of second inverter 28.

Curves 206 and 208 illustrate the relationships between the input voltage (V_out_first_latch 126) and the output voltage (V_out 138) of multiple switching point circuit 30. Curve 206 illustrates the behavior of multiple switching point circuit 30 when V_out_first_latch 126 rises from a low level towards a high level. Curve 208 illustrates the behavior of multiple switching point circuit 30 when V_out_first_latch 126 falls from a high level to a low level. Curve 202 crosses curve 206 at a high switching point (221) of multiple switching point circuit 30.

Curve 202 crosses curve 208 at a low switching point (222) of multiple switching point circuit 30.

FIG. 4 is a flow chart of method 300 for managing metastable signals according to an embodiment of the invention.

Method 300 starts by optional stage 305 of providing a first clock signal to the first latch and providing a second clock signal to the second latch and wherein there is a time gap between a transition of the first clock signal and a transition of the second clock signal. It is noted that this is not necessarily so and that both latches can receive complementary clock signals.

Stage 305 is followed by stage 310 of receiving a data signal by a first latch. This data signal can cause the first latch to output a metastable signal.

Stage 310 is followed by stage 320 of providing to a multiple switching point circuit, a feedback signal from a second latch and providing a first output signal from the first latch. It is noted that the first output signal can be a metastable signal.

Conveniently, stage 320 of providing includes providing the feedback signal from an output node of the second latch.

Conveniently, stage 320 of providing is followed by activating a first inverter in response to the first output signal and regardless of the feedback signal.

Stage 320 is followed by stage 340 of outputting a definite output signal from the multiple switching point circuit in response to the feedback signal and to the first output signal. The feedback signal and the first output signal selectively activate at least one pull up transistor and at least one pull down transistor that define at least a low switching point that is lower than

a high switching point of the multiple switching point circuit; wherein a switching point of an inverter within the first latch is between the high and low switching points.

Variations, modifications, and other implementations of what is described herein will occur to those of ordinary skill in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the invention is to be defined not by the preceding illustrative description but instead by the spirit and scope of the following claims.

WE CLAIM

1. A device (10) having metastable signal handling capabilities, the device (10) comprises a first latch (11) and a second latch (12), wherein the device (10) is characterized by comprising a multiple switching point circuit (30), coupled between an output node of the first latch (11) and an input node of the second latch (12), wherein the multiple switching point circuit (30) comprises at least one pull up transistor and at least one pull down transistor that are selectively activated in response to a feedback signal provided from the second latch (12) and in response to a an output signal of the first latch (11) such as to define at least a low switching point that is lower than a high switching point of the multiple-switching point circuit (30); wherein a switching point of an inverter within the first latch is between the high and low switching points.

2. The device (10) according to claim 1 wherein an output node of the second latch (12) provides the feedback signal.

3. The device (10) according to any claim of claims 1-2 wherein the multiple switching point circuit (30) further comprises a first inverter that is activated regardless of the feedback signal.

4. The device according to any claim of claims 1-3 wherein the first latch (11) receives a first clock signal and the second latch (12) receives a second clock signal and wherein there is a time gap between a transition of the first clock signal and a transition of the second clock signal.

5. The device (10) according to any claim of claims 1-4 wherein the multiple switching point circuit (30) comprises a pull down circuit (43) and a pull up circuit

(46); wherein a first portion (44) of the pull down circuit and a first portion (47) of the pull up circuit are activated when the feedback signal has a first value and wherein a second portion (45) of the pull down circuit and a second portion (48) of the pull up circuit are activated when the feedback signal has a second value that differs from the first value; wherein the first portion (44) of the pull down circuit differs from the second portion (45) of the pull down circuit; and wherein the first portion (47) of the pull up circuit differs from the second portion (48) of the pull up circuit.

6. The device according to claim 5 wherein the first portion (46) of the pull up circuit is stronger than the first portion (44) of the pull down circuit and wherein the second portion (48) of the pull up circuit is weaker than the second portion (45) of the pull down circuit.

7. The device according to any claim of claims 1-6 wherein a feedback inverter (28) of the first latch (11) switches before the multiple switching point circuit (30).

8. The device (10) according to any claim of claims 1-7 wherein the multiple switching point circuit (30) comprises an input inverter (41) coupled to a sequence of transistors (42) that comprises at least two transistors (35, 36) that are selectively activated in response to a level of the feedback signal.

9. The device (10) according to claim 8 wherein the sequence of transistors (42) further comprises at least two transistors (32, 34) that are selectively activated in response to a level of a signal provided from an output node of the first inverter (11).

10. Information processing apparatus (9) comprising a device (10) according to any of claims 1-9.

11. A method (300) for managing metastable signals, the method (300)comprises: receiving (310) a data signal by a first latch; wherein the method (300) is characterized by providing (320) to a multiple switching point circuit, a feedback signal from a second latch and a first output signal from the first latch and outputting (340) a definite output signal from the multiple switching point circuit in response to the feedback signal and to the first output signal; wherein the feedback signal and the first output signal selectively activate at least one pull up transistor and at least one pull down transistor that define at least a low switching point of the multiple switching point circuit that is lower than a high switching point of the multiple switching point circuit; wherein a switching point of an inverter within the first latch is between the high and low switching points.

12. The method (300) according to claim 11 wherein the providing (320) comprises providing the feedback signal from an output node of the second latch.

13. The method (300) according to any claim of claims 11-12 wherein the providing (320) is followed by activating a first inverter in response to the first output signal and regardless of the feedback signal.

14. The method (300) according to any claim of claims 11-13 further comprising providing (305) a first clock signal to the first latch and providing a second clock signal to the second latch and wherein there is a time gap between a transition of the first clock signal and a transition of the second clock signal.

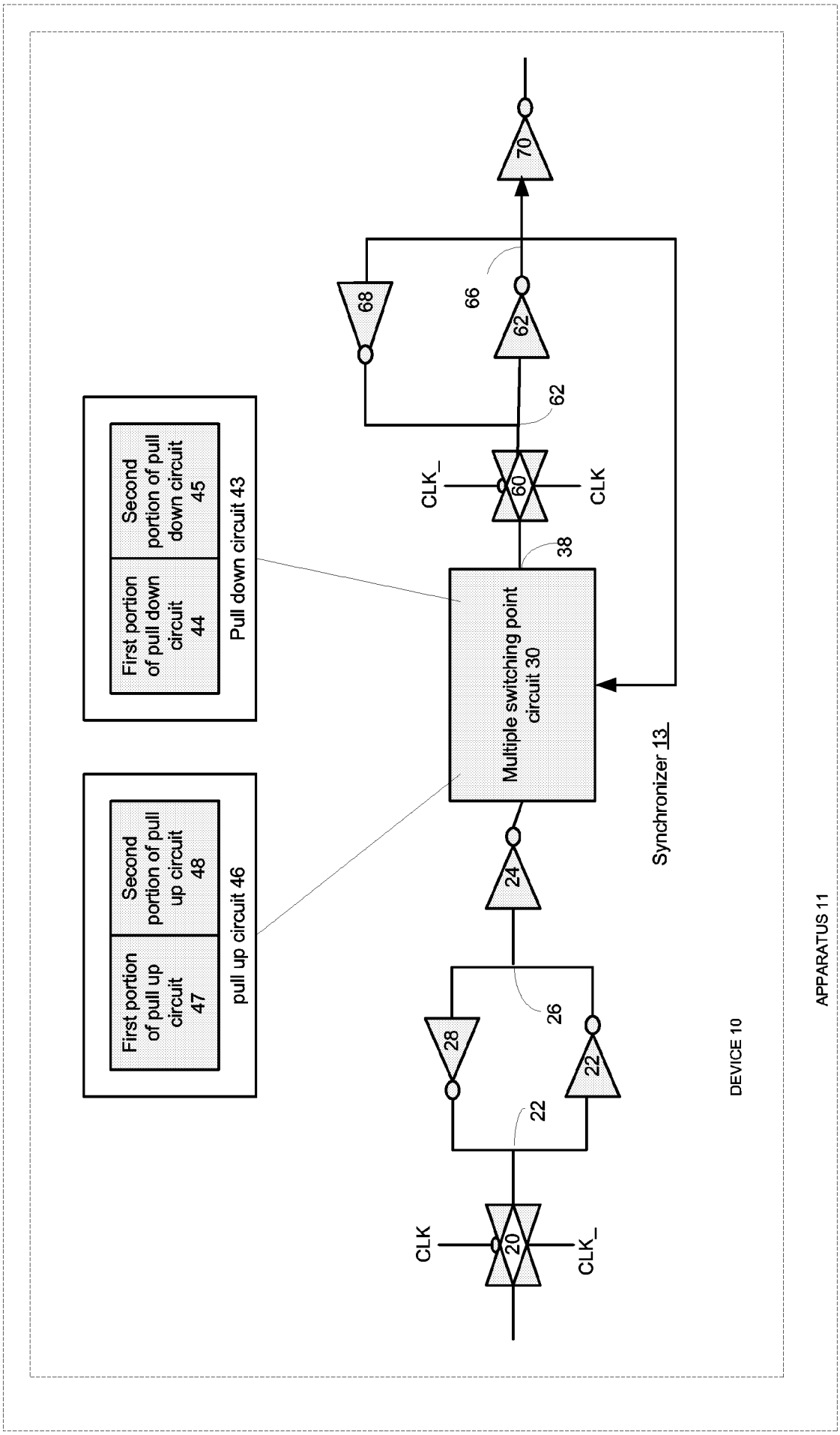
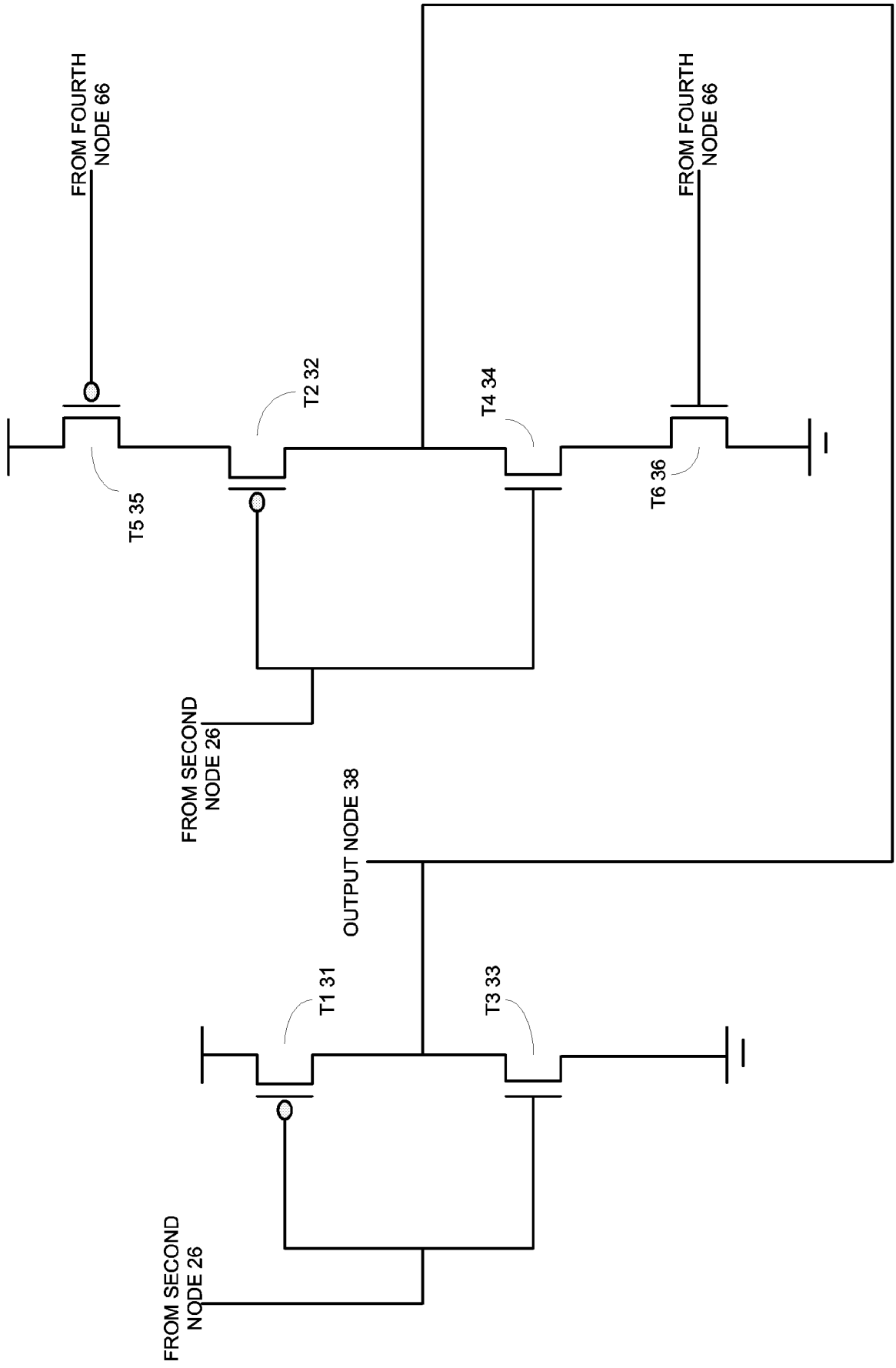
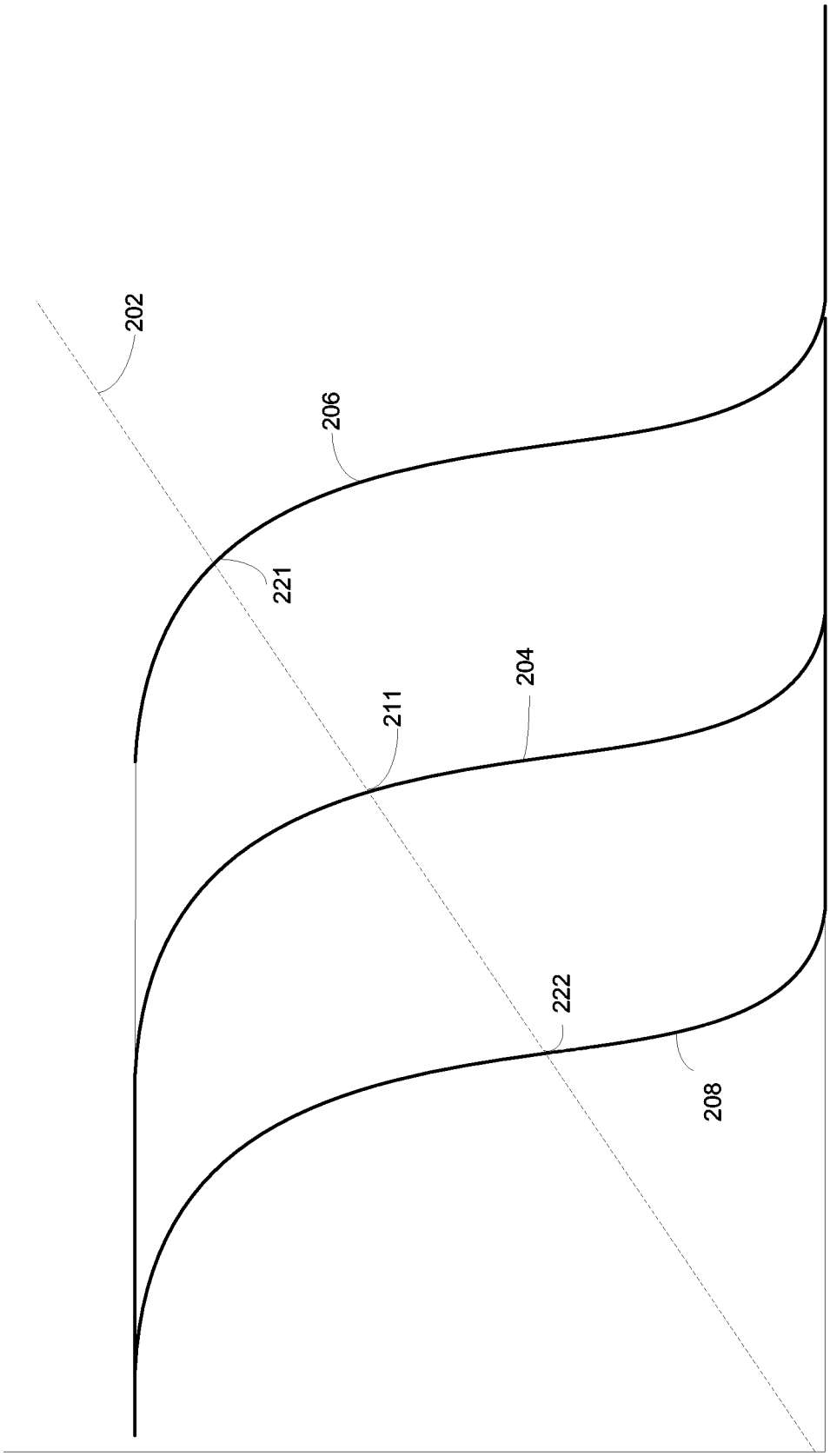

APPARATUS 11
DEVICE 10
Pull down circuit 43
First portion of pull down circuit 44
Second portion of pull down circuit 45
pull up circuit 46
First portion of pull up circuit 47
Second portion of pull up circuit 48
Multiple switching point circuit 30
Synchronizer 13
CLK
CLK_
20
22
24
26
28
38
60
62
66
68
70

FIG. 1


FROM FOURTH NODE 66
FROM FOURTH NODE 66
T2 32
T4 34
T5 35
T6 36
FROM SECOND NODE 26
OUTPUT NODE 38
T1 31
T3 33
FROM SECOND NODE 26


202
206
221
204
211
222
208

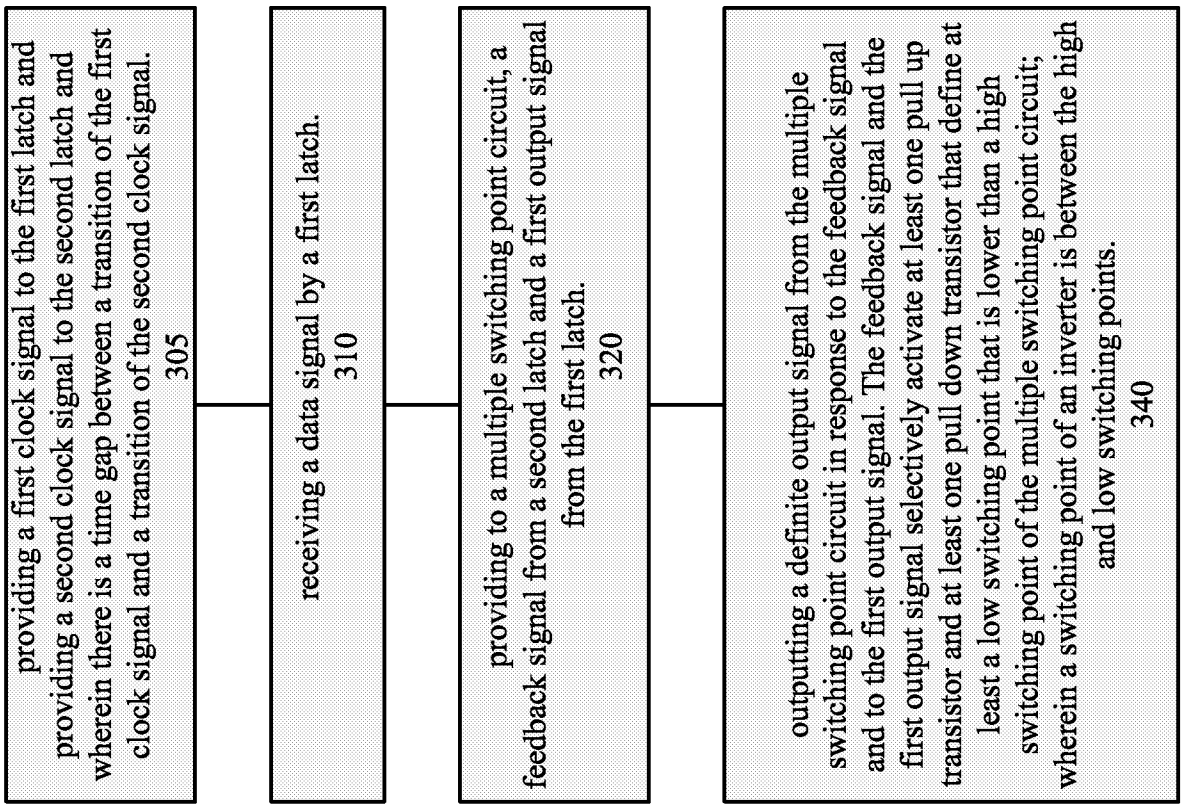

providing a first clock signal to the first latch and providing a second clock signal to the second latch and wherein there is a time gap between a transition of the first clock signal and a transition of the second clock signal.
305
receiving a data signal by a first latch.
310
providing to a multiple switching point circuit, a feedback signal from a second latch and a first output signal from the first latch.
320
outputting a definite output signal from the multiple switching point circuit in response to the feedback signal and to the first output signal. The feedback signal and the first output signal selectively activate at least one pull up transistor and at least one pull down transistor that define at least a low switching point that is lower than a high switching point of the multiple switching point circuit; wherein a switching point of an inverter is between the high and low switching points.
340
300

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051992

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L7/02 H03K3/037 H03K3/356

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H03K G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 045 801 A (MOWERY DAVID L [US]) 3 September 1991 (1991-09-03) cited in the application abstract; claims 1-4; figures 1,2 column 1, line 43 - column 2, line 3 column 3, line 35 - column 4, line 16	1-14
A	US 6 072 346 A (GHAHREMANI SHAHRAM [US]) 6 June 2000 (2000-06-06) cited in the application abstract; claims 1,2,5,6,9-11; figures 5,6 column 2, line 24 - line 49 column 4, line 53 - column 5, line 65	1-14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 December 2006	15/12/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Wolters, Robert

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051992

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 745 302 A (HANAWA MAKOTO [JP] ET AL) 17 May 1988 (1988-05-17) abstract; claims 1-4,7; figures 1,2,5 column 1, line 46 - column 2, line 19 column 3, line 38 - column 4, line 4	1-14
A	US 6 518 810 B1 (TAKAHASHI HIROYUKI [JP]) 11 February 2003 (2003-02-11) abstract; claims 1,10,11; figures 4,6 column 2, line 66 - column 3, line 63	1-14
A	US 2002/163372 A1 (BOERSTLER DAVID WILLIAM [US] ET AL) 7 November 2002 (2002-11-07) abstract; claims 1-3,7-9,14; figures 1,3,4 paragraphs [0011] - [0015]	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2006/051992

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5045801 A	03-09-1991	NONE	
US 6072346 A	06-06-2000	NONE	
US 4745302 A	17-05-1988	NONE	
US 6518810 B1	11-02-2003	JP 3530422 B2 JP 2000357943 A TW 478254 B	24-05-2004 26-12-2000 01-03-2002
US 2002163372 A1	07-11-2002	NONE	