

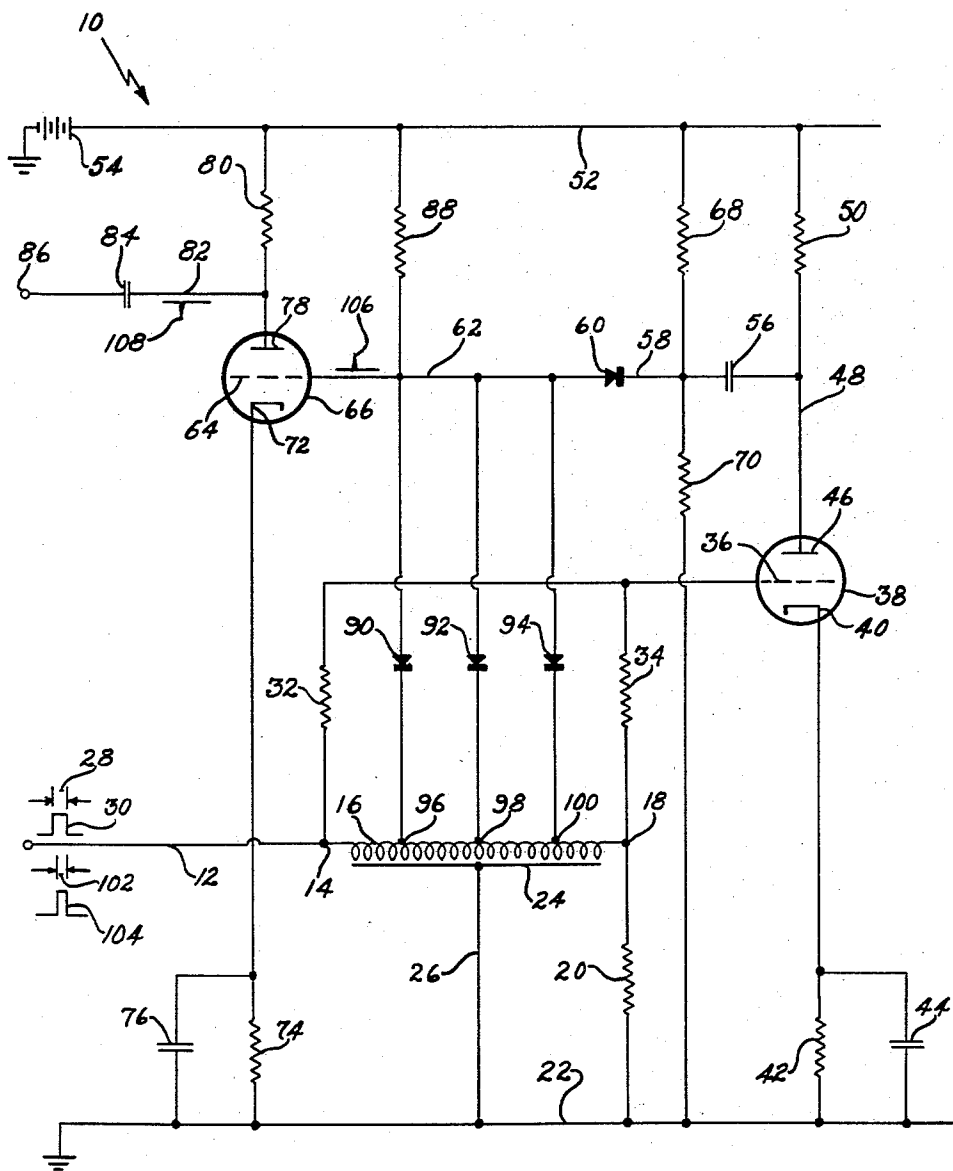
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PULSE WIDTH DISCRIMINATOR CIRCUIT

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PULSE WIDTH DISCRIMINATOR CIRCUIT

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This invention relates to pulse width discriminators, and more particularly to circuits for separating pulses of a selected width from interfering pulses of narrower or broader widths.

In electrical pulse systems using constant width information pulses, the problem of erratic operation due to noise and other interfering pulses is usually present. To prevent erratic operation, it is desirable to separate out the desired width pulses from other interfering pulses and noise. Such separation is particularly desirable in military command and remote control guidance systems where maximum reliability is vital.

Pursuant to the present invention, the foregoing problems have been overcome and a highly efficient pulse discrimination system has been achieved in a circuit which also incorporates other desirable features and characteristics.

Accordingly, a primary object of the present invention is the provision of a circuit which distinguishes between pulses of a preselected width and pulses having widths different from the selected width.

Another object is the provision of a circuit which distinguishes not only between pulses of a preselected width and those having widths different from the preselected width, but also capable of distinguishing between the preselected width pulses and noise.

A further object is the provision of a pulse width discriminating circuit which lends itself to being set for a selected tolerance of pulse widths to which the circuit will respond.

Another object is the provision of a pulse width discriminator circuit which lends itself to a relatively simple arrangement for increasing the pass band to improve noise discrimination characteristics to substantially any degree desired.

And a still further object is the provision of a pulse width discriminator circuit which is relatively inexpensive and easy to construct, rugged and substantially foolproof in its operation.

These objects, features and advantages are achieved generally by providing an electric signal input circuit, an electric signal output circuit, an electric circuit pulse width standard coupled to the input circuit, an arrangement for comparing the width of input pulses to the standard, and a further circuit responsive to the comparing arrangement to effect an output pulse in the output circuit for each input pulse matching the standard.

By making the pulse width standard in the form of a delay line with terminals on the delay line forming a spaced interval having a slightly smaller time value than the preselected pulse width, a relatively foolproof standard is thereby achieved.

By providing unidirectional current valve circuit means coupled to the terminals on the standard, a comparing arrangement for blocking all electric signals except those above a selected width is achieved.

By providing additional delay elements on each side of the spaced interval on the standard and coupling the

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extremities of the additional delay elements through another unidirectional current valve to the pulse responsive means, an arrangement for blocking pulses having widths greater than those of the selected value is thereby achieved.

By providing additional unidirectional current valve circuit means between the above mentioned spaced interval terminals on the standard, band pass and noise discrimination characteristics are improved.

By providing an electron tube with control grid coupled through the unidirectional current valve circuit means to the standard, a relatively simple signal responsive arrangement is achieved.

These and other objects, features and advantages of the invention will be more clearly understood from the following description taken in connection with the accompanying drawing of a preferred embodiment of the invention and wherein the figure is a schematic diagram of a pulse width discriminator circuit made in accordance with the present invention.

Referring to the figure in more detail, a pulse width discriminator circuit made in accordance with the present invention is designated generally by the numeral 10. The pulse width discriminator 10 has an input circuit electric line or cable 12 connected at a terminal 14 to one end of an electric signal delay line 16, the other end of which is connected through a terminal 18 and a load resistor 20 to a line 22 which may be grounded. The resistor 20 has preferably the characteristic impedance value of the delay line 16 to prevent signal reflections. The delay line 16 may be of the type having a thin inductive coil surrounded by a cylindrical outer conductor or shield 24 connected by a line 26 to the line 22. The time delay value of the delay line 16 between the terminals 14 and 18 is preferably equal to the time value or width 28 of the widest desired information pulse 30 for operation of the discriminator 10 as will be hereinafter more fully described. The terminals 14 and 18 are connected through resistors 32 and 34 respectively to a control grid 36 in an electron current device such as a triode 38. The triode 38 has a cathode 40 connected through a cathode biasing resistor 42 and a stray signal bypass condenser 44 to the line 22.

Triode 38 has an anode or plate 46 connected through a line 48 and a plate circuit voltage dropping resistor 50 to a positive potential power line 52 connected to a positive terminal of a power source such as a battery 54, the negative terminal of which is connected to ground.

The plate circuit line 48 of the triode 38 is also connected through a capacitor 56, a line 58, a unidirectional current valve such as a diode 60, and a line 62 to a control grid 64 in an electron current device such as a triode 66. The line 58 between the diode 60 and capacitor 56 is also connected to a point between voltage divider resistors 68 and 70 which are in series between the positive potential line 52 and the ground line 22 for purposes to be hereinafter described.

The triode 66 may be similar to the triode 38 and similarly has a cathode 72 connected through a cathode biasing resistor 74 and bypass condenser 76 to the ground line 22. The triode 66 also has an anode or plate 78 connected through a plate circuit voltage dropping resistor 80 to the positive potential line 52. Plate 78 is also connected through an output circuit line 82 and a capacitor 84 to an output terminal 86.

The grid biasing line 62 is also connected through a grid biasing resistor 88 to the positive potential line 52. The grid biasing line 62 is also connected through unidirectional current valves such as diodes 90, 92 and 94 to electric contact terminals 96, 98 and 100 on the delay line 16. The diodes 90, 92 and 94 are all oriented to pass

current when the voltage at terminals 96, 98 and 100 is lower than the voltage at the grid biasing line 62.

The time value of the delay line 16 between the points 96 and 100 is preferably slightly smaller than the time value or width 102 of a pulse 104 having the narrowest width desired for passage through the discriminator circuit 10 as will be hereinafter more fully described.

In the operation of the pulse discriminator circuit 10, the triode 38 conducts current as in class A amplifier operation. The voltage divider resistances 68 and 70 are so chosen that the voltage in line 58 is at the maximum positive value desired for operation of the output circuit triode 66. However, the triode 66 will normally be preferably nonconductive due to the passage of current from the positive potential line 52 through the voltage biasing resistor 83, the diodes 90, 92, 94, delay line 16 and resistor 29 to the ground line 22.

With the passage of a minimum width pulse 104 through the input circuit line 12 and the delay line 16, there will be no resulting biasing effect of the grid 64 above cut-off until the pulse 104 exists simultaneously across the terminals 96, 98 and 100 in the delay line 16. At that instant of time, the positive pulse 104 will prevent the diodes 90, 92 and 94 from conducting and thereby shorting out a positive voltage which otherwise would appear in the grid biasing line 62. The voltage in line 62 will thereby go positive and cause the appearance of a positive spike or signal 106 at the grid 64 and thereby cause a corresponding negative voltage spike or output signal 108 to appear through the output circuit line 82, the output capacitor 84 at the output terminal 86.

The diode 60 serves to isolate the grid 64 from the low impedance associated with the plate circuit of the triode 38 for a positive rise in the grid biasing line 62 up to, but not exceeding the voltage in the line 58 from the voltage divider resistors 68 and 70.

In the case of pulses greater than the correct or maximum desired width 28, a positive voltage will appear at the terminals 14 or 18 or both to cause the grid 36 of the triode 38 to go positive. As a result, the voltage at plate 46 in the triode 38 will drop. This drop in voltage at the plate 46 will appear through line 48, capacitor 56, the line 58, diode 60, and line 62 at the grid 64 to drive the grid 64 negative and thereby prevent an output for such undesired overly broad pulses. Pulses which are narrower than the time value 102, will also be too narrow to simultaneously prevent the shorting effect of one or more of the diodes 90, 92 or 94 and thereby will likewise be blocked from appearing at the grid 64 of the triode 66. Thus noise spikes and pulses of insufficient width will not simultaneously reach across the terminals 96, 98 and 100 and will thereby produce no positive signal spikes at the grid 64 of the triode 66.

As many additional terminals 98 as necessary, depending on band pass desired, can be used between the terminals 96 and 100 to improve noise discrimination.

This invention is not limited to the specific details of construction and operation disclosed, as equivalents will suggest themselves to those skilled in the art.

What is claimed is:

1. In a pulse width discriminator, the combination of an output circuit including an electron tube having a control grid, a delay line having a length with time value to include the widest desired pulse, pulse responsive means coupled to the delay line at the extremities of said length for depressing said grid below cutoff, pulse responsive means coupled to the delay line between said extremities for providing at said grid a voltage above cutoff, and means including a second electron tube for limiting the output circuit pulses to "spike" widths which are only a small fraction of the width of said widest desired pulse.

2. In a pulse width discriminator, the combination of

an output circuit including an electron tube having a control grid, means coupled to the control grid for biasing said control grid below cutoff, pulse receiving means, a pulse width standard in said pulse receiving means, means for comparing the width of pulses appearing in said receiving means to said pulse width standard, means coupled to said biasing means responsive to said comparing means for raising the bias on said control grid above cutoff for pulses of a preselected pulse width comparison, and means including a second electron tube for limiting the output circuit pulses to "spike" widths which are only a small fraction of the width of said widest desired pulse.

3. In a pulse width discriminator, the combination of an output circuit including an electron tube having a control grid, means for biasing said control grid at a normally continuous substantially constant voltage, pulse receiving means, a pulse width standard in said pulse receiving means, means for comparing the width of pulses appearing in said receiving means to said pulse width standard, means coupled to said biasing means responsive to said comparing means for changing the bias on said control grid for pulses of a preselected pulse width, and means including a second electron tube for limiting the output circuit pulses to "spike" widths which are only a small fraction of the width of said widest desired pulse.

4. In a pulse width discriminator, the combination of a pair of triodes, each having a plate, cathode and control grid, voltage means across the plate and cathode of said triodes, a delay line having a time value equal to the widest desired pulse, each end of said delay line coupled to the control grid of one of said triodes, circuit means coupling the control grid of the other triode to points in spaced relation on the delay line providing a time value slightly smaller than the narrowest desired pulse, voltage divider resistors across said voltage means coupled to said circuit means for biasing the control grid of said other triode, unidirectional current valve means in the circuit between each of the coupling points on the delay line and the control grid of said other triode and in the coupling between the circuit means and the voltage resistors, a capacitor coupling said voltage divider resistors and the plate of the one triode, an output circuit coupled to the plate of the other triode, and means including said second triode for limiting the output circuit pulses to "spike" widths which are only a small fraction of the width of said widest desired pulse.

5. In a pulsing system for pulses of preselected time width, the combination of an input circuit and an output circuit for electric signal pulses, electric signal responsive means coupled to the output circuit, electric signal delay means coupled to said input circuit, unidirectional current means coupled to the signal responsive means and to positions on the delay means to include a pulse travel period slightly smaller in time value than the preselected time width of the desired pulses, additional unidirectional current means coupled to the signal responsive means and to the delay means between the positions on said delay means having coupling with said first mentioned unidirectional current means to improve noise discrimination characteristics, and means to limit the output circuit pulses to "spike" widths which are only a small fraction of said pre-selected time width.

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