



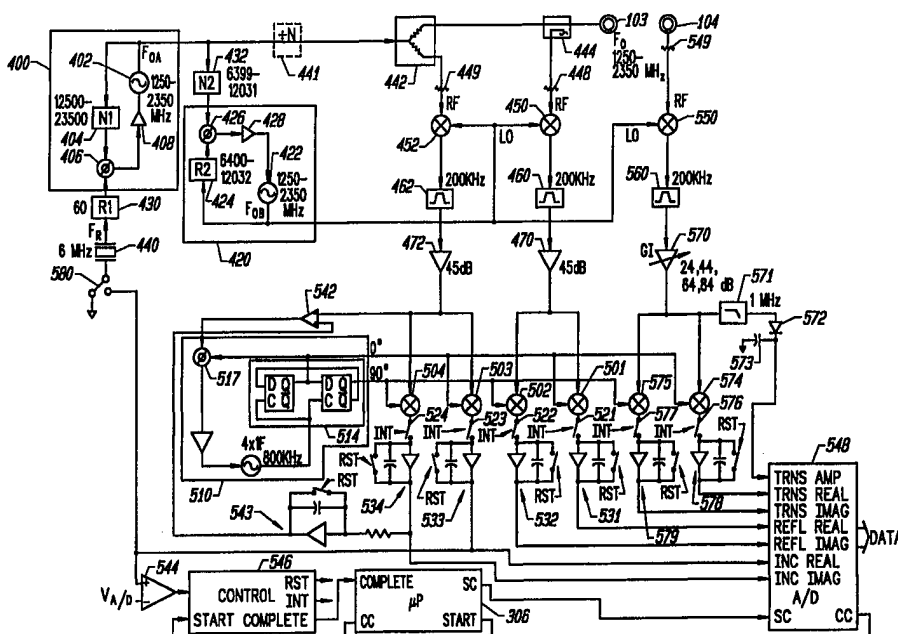
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(54) Title: TWO PORT HANDHELD VECTOR NETWORK ANALYZER WITH FREQUENCY MONITOR MODE

(57) Abstract

A two port handheld VNA enabling both reflection and transmission measurements to be made over a range of 25 MHz to 3.3 GHz frequency range. The handheld VNA includes a tracking synthesizer which generates an LO signal without a direct connection to a reference oscillator, enabling resolution of the LO signal to be independent of a generated RF test signal. Synchronous detectors are further included to provide incident, reflected, and transmitted IF signals to an A/D converter. To enable operation in the presence of external signals, a feedback dither line is provided from one of the synchronous detector outputs to sweep the frequency of the reference oscillator. The handheld VNA also is configured to optionally operate as a frequency monitor to determine the frequency range and power level of incoming signals without upconverting and downconverting to eliminate images as typically done in a spectrum analyzer. The frequency monitoring circuit operates by dividing the frequency range to be monitored into bins. The LO signal is then stepped for each bin until RF signals within the bin frequency range can generate an IF signal. The maximum IF signal power level detected during measurements for the bin is then stored as a power level for signals in each bin.



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TWO PORT HANDHELD
VECTOR NETWORK ANALYZER
WITH FREQUENCY MONITOR MODE

5 CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation-in-part of U.S. Patent Application Serial Number 08/362,179 entitled "Handheld Vector Network Analyzer", by Bradley et al., filed December 22, 1994, (hereinafter the cross-referenced handheld VNA application), and claims priority therefrom.

10

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a vector network analyzer (VNA) with components utilized to limit size, weight and power consumption. More particularly, the present invention relates to components utilized to provide such a VNA with two measurement ports and to enable the VNA to alternatively function to monitor the frequency and power level of a received signal.

2. Description of the Related Art

20 Wireless networks for telephone or computer local area network (LAN) communications have been adopted worldwide in the 0-3 GHz frequency range. For instance, cellular telephones in the United States operate in the 800 MHz range, pagers operate in the 900 MHz range, and personal communication services (PCS) telephones are allocated operation frequencies in the 1850-2200
25 MHz range.

Wireless communications networks such as for cellular telephones, pagers, or PCS require remotely located antennas which transmit signals from cell sites to provide services to individual users. To reduce service costs for the remote

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antennas, it is desirable to test the remote antenna and its associated microwave components at its remote location and locate and repair portions which fail.

VNAs enable a user to easily identify a fault and to measure the distance from the test device to a fault or discontinuity. A fault may result from environmental conditions such as corrosion of a connector, or from faulty
5 installation or repair, for example, where a coaxial cable is punctured by an installer. Test measurements are first typically made using a VNA operating in the frequency domain to determine whether a fault exists as indicated by an undesirable standing wave ratio (SWR). If a fault is discovered, an analysis of
10 the results derived from the frequency domain measurement is made in the time domain to locate the position of the fault.

A VNA also enables calibration to extend the test port connection to the end of a cable connected to the test port. By using a VNA to extend the test port to the end of the cable, errors in the cable will not be taken into account when
15 measuring a device through the cable. Scalar devices which measure only amplitude do not enable extension of the test port to the end of a cable.

Because a remote antenna may be constantly providing signals for communications devices once it is installed, it is desirable that the remote antenna not be disabled for testing. By measuring both phase and amplitude, a VNA
20 provides the ability to distinguish extraneous signals, enabling tests to be performed with the remote antenna active. Scalar devices cannot distinguish the extraneous signals, requiring that scalar tests be performed with the remote antenna disabled.

Most VNAs are large and not easily transportable. Typical VNAs have a
25 housing greater than two feet on a side, and with a power supply may weigh 50 pounds or more. The VNAs are typically transported by truck to the remote antenna sight and carried by two people to the remote antenna. With remote

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antennas located on top of towers, transportation of the large VNA proves especially difficult.

The SiteMaster manufactured by Wiltron Company of Morgan Hill, California, in contrast, is a single measurement port VNA having dimensions
5 equal to or less than 8 inches by 6 inches by 2 ½ inches and a weight of less than three pounds, including batteries, when operating over a 25 MHz to 3.3 GHz frequency range. With such weight and size, the SiteMaster can be easily transported by one person to make test measurements at a remote sight. Components used in the currently manufactured SiteMaster are described in the
10 cross-referenced handheld VNA application.

With one VNA measurement port, the SiteMaster can be utilized to discover the existence of a fault or discontinuity using frequency domain measurements, and locate the position of the fault using time domain measurements. The SiteMaster can also be used to extend a test port to the end of a cable, and to
15 make measurements on an active device by distinguishing extraneous signals.

However, it would further be desirable to have a handheld VNA with two measurement ports enabling transmission measurements to be made. For instance in a cell site, a low noise amplifier (LNA) is utilized to provide a signal from a transmitter to an antenna. Although no faults may be discovered when
20 making a one port reflection measurement through the LNA, the LNA may not be properly amplifying a signal from the transmitter, a fact which cannot be easily discovered using a one port VNA. By transmitting a signal through the LNA from a first VNA measurement port, and receiving the transmitted signal from the LNA at a second VNA measurement port, one can determine whether
25 the LNA is properly amplifying an input signal.

A two measurement port handheld VNA would also be desirable to measure antenna gain at a cell cite. As with the LNA, when making a one port reflection

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measurement through an antenna, no faults may be discovered, but the power delivered by the antenna may be below a desired level in a particular direction from the antenna. By transmitting a signal through the cell site antenna from a first VNA measurement port, and receiving the transmitted signal with another
5 antenna at a second VNA measurement port, antenna gain in different directions from the antenna can be determined.

Even if a cell site is functioning properly, signals from another antenna may be interfering with signals transmitted from or received by the cell site. A cell site antenna is typically located in close proximity with a significant number of
10 other antennas. For instance, a remote location at which a cellular telephone cell antenna is located may also be the location for transmitter antennas for pagers, PCS, and AM and FM radio stations. Measurements at a cell site are, thus, also typically made to determine if interfering signals are present utilizing a spectrum analyzer.

15 The SiteMaster currently manufactured by Wiltron is designed to reject signals from external sources when making measurements, so the currently manufactured SiteMaster cannot be used to measure the frequency and power level of signals from external devices. Further, a spectrum analyzer typically uses upconverting and downconverting signals to reject undesired images
20 generated when mixing. Such upconverting and downconverting typically requires generating a signal with a frequency significantly higher than a desired test signal. Components to generate such a high frequency signal if combined with components of a handheld VNA would add an unacceptable amount of weight and size to the handheld VNA.

25

SUMMARY OF THE INVENTION

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The present invention provides a two port handheld VNA enabling both reflection and transmission measurements to be made while maintaining a size of 8 inches by 6 inches by 2 1/2 inches and a weight of less than three pounds, including batteries, when a test signal from 25 MHz to 3.3 GHz is desired.

5 The present invention further includes components enabling measurements to be made to monitor the frequency and power level of external signals without adding significant additional weight.

To provide a handheld device, the present invention includes components described in the cross-referenced handheld VNA application including a tracking
10 synthesizer which generates a LO signal without a direct connection to a reference oscillator. The tracking synthesizer receives a signal from the reference oscillator as reduced in frequency by a test signal synthesizer which provides a RF test signal. With a reference signal not being provided directly to the tracking synthesizer, overall circuit complexity is reduced, and resolution of
15 the LO signal can be made independent from RF test signal resolution.

The RF signal from the test signal synthesizer is provided to a mixer along with the LO signal from the tracking synthesizer to form an incident IF signal. The RF signal is also provided through a first measurement port, and a return signal from the first measurement port coupled to a mixer along with the LO
20 signal to form a reflected IF signal. Synchronous detectors are then utilized which receive the IF signals and produce both real and imaginary incident and reflected signals to an A/D converter.

To enable reduced measurement error in the presence of an external signal, a dither line control feedback is provided to the reference oscillator from the
25 incident real signal output of the synchronous detector to sweep the frequency of the reference oscillator. With the frequency of the reference oscillator swept,

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only a small portion of the test signal frequency range will interfere with the external signal.

The present invention further includes a second test port to receive transmitted signals. The transmitted signal provided to the second port is
5 provided to a mixer along with the LO signal from the tracking synthesizer to provide a transmitted IF signal. Additional synchronous detectors are then utilized to receive the transmitted IF signal and produce both real and imaginary transmitted signals to the A/D converter.

To enable a signal from the test signal synthesizer to be adequately detected
10 when received at the second test port, since the RF signal received may be significantly attenuated, the transmitted IF signal is provided through a variable gain amplifier to the synchronous detectors. To control gain of the variable gain amplifier, the signal from the variable gain amplifier is provided through a peak detector to an input of the A/D converter. The A/D converter output is then
15 utilized to adjust the gain of the variable gain amplifier to a desired level.

The present invention also functions as a frequency monitor utilizing the variable gain amplifier. To provide the frequency monitor, a switch is included to disconnect the dither line during the frequency monitoring process. To limit the overall weight and size of circuitry for the frequency monitor, instead of
20 using upconverting and downconverting typically provided in a spectrum analyzer, the present invention includes a unique measuring scheme. In the measurement scheme, the frequency range to be monitored is divided into bins. For each bin, measurements are made of IF signals with the LO signal stepped in frequency until IF signals are detected for all RF signals which may be
25 received over the frequency width of the bin. During each measurement, the gain of the variable gain amplifier is stepped until a signal is received above a desired voltage value from the peak detector and a power level is then

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determined. The maximum power level detected during measurements for a bin is then stored as the power level for the signals for each bin.

5

BRIEF DESCRIPTION OF THE DRAWINGS

Further details of the present invention are explained with the help of the attached drawings in which:

Fig. 1 shows the exterior of a handheld vector network analyzer of the present invention;

10

Fig. 2 illustrates how a VNA of the present invention is handheld and may be utilized at a remote antenna sight to enable vector testing of the antenna in the presence of signals being received by the remote antenna;

Fig. 3 shows a block diagram further illustrating components utilized in the VNA of the present invention;

15

Fig. 4 shows components for the test circuitry shown in block diagram in Fig. 3 for the present invention;

Fig. 5 shows signals received and produced by the A/D converter, control circuit, and microprocessor of Fig. 4;

20

Fig. 6 illustrates operation of the circuitry of Fig. 4 with and without the dither line connected;

Fig. 7 illustrates the frequency monitoring measurement scheme for the present invention.

DETAILED DESCRIPTION

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Fig. 1 shows the exterior of a two port handheld vector network analyzer (VNA) 100 of the present invention. The configuration of components in the VNA 100 of the present invention enables the size of the VNA housing 102 to

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have an approximate length of 6 inches, width of 8 inches and depth of 2 ½ inches when a test signal from 25 MHz to 3.3 GHz is desired. Further, components contained within the VNA enable the VNA to weigh less than 3 pounds, including weight of the batteries. With such small dimensions and low weight, the VNA 100 of the present invention is handheld and easily portable to a remote antenna sight to enable vector testing of a remote antenna and its associated microwave components as illustrated in Fig. 2.

As further shown in Fig. 1, the VNA 100 of the present invention includes two measurement test ports 103 and 104. Further, the housing 102 of the VNA 100 enables user access to a keypad 106 and display 108. The keypad includes enables easy control for steps such as selecting a desired frequency range using the arrow keys, and calibration which can be performed by first pressing the START CAL button and then individually connecting a short, open, load and through and pressing the (CAL) button after each is connected. The keypad also enables control for measuring a standing wave ratio (SWR) and return or insertion loss (LOSS), return loss being measured during reflection measurements, and insertion loss being measured during transmission measurements (LOSS).

Fig. 3 shows a block diagram further illustrating components utilized in the VNA 300 of the present invention. Because the VNA is designed for use at a remote location, as shown in Fig. 2, power is provided to the VNA by a battery 302 having an associated charger. Power distribution circuitry 304 provides power from the battery 302 to electrical circuitry of the VNA. Electrical circuitry to which power is distributed by power distribution circuitry 304, in addition to the keypad 106 and display 1308 of Fig. 1, includes a processor 306, an EEPROM 308, test circuitry 310, and an optional disk drive 312.

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The processor 306 utilized is an 8051 microcontroller which includes its own internal memory. The processor memory includes both a scratchpad memory as well as a programmable read only memory (PROM). The memory of the processor 306 is utilized to store control software as well as software
5 containing a distance to fault calculation program and a vector error correction or calibration program. As shown connected to processor 306, the VNA also includes a serial I/O data port to enable communication to a personal computer for further data manipulation or archiving.

The EEPROM 308 is an electrically programmable and erasable PROM and
10 provides additional memory to the internal memory of processor 306. The PROM is programmed to store test results, for example including as many as seven displays of information.

The optional disk drive 312 is a floppy disk drive enabling test measurements to be made at a remote sight and stored on a floppy disk. The
15 floppy disk may then later be removed and easily transferred to a computer for further analysis of test data upon return from a remote test sight. Without the floppy disk, the 2 ½ depth dimension discussed previously for the housing 102 of Fig. 1 can be reduced.

The test circuitry 310 includes components which generate, send and receive
20 test signals and process the test signals to enable test measurements to be made. To keep size and weight of the VNA to a minimum, the test circuitry 310 utilizes a narrow swept frequency range covering the frequencies desired for testing, for example 0.025-3.3 GHz for cellular and PCS technology discussed in the background.

25 Fig. 4 shows components for the test circuitry 310 shown in block diagram in Fig. 3 for the present invention. The test ports 103 and 104 and processor 306 referenced in Figs. 1 and 3 are similarly labeled in Fig. 4. Further in Fig. 4,

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representative values for frequencies for oscillators, gains for amplifiers, and frequency division numbers for frequency dividers are shown for purposes of illustration, although other values may be used depending on desired operating conditions.

5 The test circuitry of Fig. 4 initially includes two downconverters in the form of phase locked loops (PLLs), or synthesizer, including a test signal synthesizer 400 and a tracking signal synthesizer 420. Each of frequency synthesizers 400 and 420 include respective oscillators 402 and 422 and phase detectors 406 and 426. A first input of each of phase detectors 406 and 426 is connected to a
10 reference signal. The first input of phase detector 406 is coupled to receive a reference signal from a reference signal oscillator 440, while the phase detector 426 is coupled to receive a reference signal from the output of oscillator 402. A second input of each of phase detectors 406 and 426 is connected through a
15 respective frequency divider 404 and 424 to the output of its respective oscillator 402 and 422 to divide the frequency of its oscillator output by a respective number N1 and R2 set to provide an output matching the frequency of the first input of its phase detector. Outputs of each of phase detectors 406 and 426 are provided through a respective amplifier and low pass filter 408 and 428 to the voltage control input of its respective oscillator 402 and 422.

20 The input to the test signal synthesizer 400 is coupled to the phase detector 406 of the reference oscillator 420 through a frequency divider 432. The test signal synthesizer 400, reference oscillator 440 and frequency divider 432 form a "variable R" frequency divider where R refers to the number R1 which the frequency divider divides the signal from reference oscillator 440.

25 The value for the RF output F_{OA} from the oscillator 402 is $F_{OA} = F_R N1/R1$. Resolution, or the steps between frequencies which can be provided for the RF signal F_{OA} can be defined as follows:

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$$\begin{aligned} \text{RES} &= F_R(N1-1)/(R1-1)-F_R N1/R1 \\ &= F_R(N1-R1)/(R1(R-1)) \end{aligned}$$

Wherein F_R is the frequency from the reference signal oscillator 440. Settling
5 time for the signal F_{OA} is further defined as $t_{\text{settle}} = 4.5/(2\pi F_R/10R1)$.

The values for $R1$ and $N1$ are chosen to optimize resolution and settling time for a particular frequency as described in detail in copending U.S. Patent Application No. 08/719,763 entitled "Frequency Synthesizer Using A Ratio Sum Topology, filed September 25, 1996, and incorporated herein by reference.

10 A frequency divider 432 further is used to connect the output of the test signal synthesizer 400 to the tracking signal synthesizer. The frequency divider 432 divides the frequency output from the oscillator 402 by a value $N2$.

Referencing the tracking synthesizer 400 to the tracking signal synthesizer 420 utilizing the frequency divider 432, rather than referencing the tracking
15 signal synthesizer 420 directly to the reference oscillator 440 reduces the complexity of circuitry needed to provide a LO signal and enables resolution of the LO signal to be controlled independent of the RF signal.

Further, by providing a connection between the test signal synthesizer 400 and tracking signal synthesizer 420 using the divide by $N2$ frequency divider
20 432, a multiple variable R synthesizer is created. By iteratively selecting $N1$, $N2$, $R1$ and $R2$, as further indicated the U.S. Patent Application No. 08/719,763 referred to above, output signal resolution and settling time for the LO signal F_{OB} provided from oscillator 422 in the test signal synthesizer 302 can be minimized. The values of $N1$, $N2$, $R1$ and $R2$ are controlled by a signal provided by
25 microprocessor 306.

To provide incident and reflected test signals, the signal F_{OA} from the oscillator 402 of the test signal synthesizer is provided to the input of a splitter

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442. To increase the frequency range of a signal provided to the splitter 442, and ultimately the test signal F_o provided from the VNA, the output from oscillator 402 can be provided to splitter 442 through an additional frequency divider 441 shown in dashed lines, or through a harmonic generator (not shown) as described in the cross-referenced handheld VNA application.

Power splitter 442 splits the signal from frequency divider 410 into two components. A first component provided from a first output of the splitter 442 is provided through coupler 444 to form the test signal F_o provided to a device connected to the first test port 103 for testing. A reflected RF signal from the device under test is then received by coupler 444 and directed through a pad 448 to a first input of mixer 450. The attenuation values for pads 448 and 449 are chosen to equalize the amplitude of the incident and reflected signals. A second output of the splitter 442 is provided as the incident RF signal through a pad 449 to a first input of mixer 452.

Second inputs of mixers 450 and 452 receive the LO signal from the output F_{OB} of tracking signal synthesizer 420. By mixing the incident and reflected RF signals originating from splitter 442 in mixers 452 and 450 with the LO signal from frequency divider 430, the mixers 450 and 452 provide reflected and incident IF test signals at their outputs. If the frequency divider 441 is utilized, note that the output F_{OB} would need to be provided through a similar frequency divider to mixers 450 and 452, or mixers 450 and 452 substituted with harmonic synthesizers.

The outputs of mixers 450 and 452 are connected to respective bandpass filters 460 and 462 to remove extraneous signals from the incident and reflected IF signals. The outputs of the bandpass filters 460 and 462 are then provided through respective amplifiers 470 and 472 to the inputs of synchronous detectors.

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In the synchronous detectors of the present invention, the reflected IF output of bandpass filter 470 is received at a first input of multipliers 501 and 502, while the incident IF output of bandpass filter 472 is received at the first input of multipliers 503 and 504. A second input of multipliers 501 and 503 is
5 connected to an output of a PLL 510 which provides a reference signal at the IF frequency phase shifted by 0 degrees. Multiplier 501, thus, outputs the reflected real component of the test signal while multiplier 503 outputs the incident real component of the test signal. A second input to multipliers 502 and 504 is
10 connected to another output of PLL 510 which provides a reference signal at the IF frequency phase shifted by 90 degrees. Multiplier 502, thus, outputs the reflected imaginary component of the test signal while multiplier 504 outputs the incident imaginary real component of the test signal.

The outputs of multipliers 501-504 are connected through respective switches 521-524 and integrators 531-534 to A/D converter 548. The switches
15 521-524 are controlled to be opened or closed by an integrate signal (INT) received from control circuit 546. Further, control circuitry 546 provides a reset signal (RST) to a switch connected in parallel with the capacitors of integrators 531-534.

The PLL 510 includes an oscillator 912 operating at 4 times the IF
20 frequency. The output of oscillator 512 is provided to a divide by four circuit 514 which provides a signal at the IF frequency with a phase shift of both 0 and 90 degrees.

The 0 degree output of frequency divider 514 is provided to one input of phase detector 517, while a second input at the IF frequency is provided from
25 comparator 542. Comparator 542 has a positive input connected to the output of bandpass filter 472 and a negative input connected through an integrator (or

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amplifier) 543 to the output of integrator 534 to assure the incident imaginary signal is held to a value of 0V.

5 The comparator 542 holds the incident imaginary signal to 0 volts when measurements are taken because with any difference in phase between the signal from bandpass filter 472 and the 90 degree output of PLL 910, the output of integrator 534 will increase in voltage. With an offset in the voltage from integrator 534, integrator 543 amplifies the voltage to comparator 542 which will function to provide an output with a compensating phase shift to return the output of integrator 534 to zero volts.

10 To assure the full operation range of A/D converter 548 is utilized, the output of integrator 533 is provided to a positive input of a comparator 544. The negative input of comparator 544 is connected to a voltage reference supplying the maximum voltage of the A/D converter, $V_{A/D}$. The output of comparator 544 is supplied to control circuitry 546 which provides the RST, INT and a complete signal (COMPLETE).
15 The COMPLETE signal is provided to a processor 306 along with a complete conversion (CC) from A/D converter 548. The processor provides a start signal (START) to control circuit 546 and a start conversion (SC) signal to the A/D converter 548.

20 Operation of the A/D converter 548 is described with reference to the signals shown in Fig. 5. Fig. 5 shows three START signals generated from processor 306 for measurements with the F_o signal generated at 990, 1000, and 1010 MHz. Upon receipt of each start signal, control circuit 546 generates a reset signal (RST) to discharge the capacitors of integrators 531-534 so the output of the integrators will have an initial value of 0V. Further, on the trailing edge
25 of each RST pulse, a integrate pulse (INT) is generated by control circuit 546, the INT signal closing switches 521-524 so that integrators 531-534 begin to function.

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With the output of integrator 534 being provided to comparator 542 as described previously, the incident imaginary signal (INC IMAG) signal input to the A/D converter 548 is at 0V. With INC IMAG set to 0V, the incident real (INC REAL) signal will obtain its maximum value and will rise toward the maximum voltage $V_{A/D}$ of the A/D converter 548. Once $V_{A/D}$ is reached, comparator 544 provides a signal to control circuit 546 to turn off the INT signal, thus holding the outputs of integrators 531-534 at their current value. Further, the complete signal is sent to the microprocessor 306 which sends the start conversion signal (SC) to the A/D converter. Upon completion of conversion of its inputs to a digital data signal (DATA), the A/D converter 548 returns a conversion complete (CC) signal causing the processor to send the START signal back to control circuit 546 so that the next RST signal can be generated and another measurement cycle initiated.

The circuitry of Fig. 4 additionally includes a dither line coupling the output of integrator 533 to a voltage control input of a reference oscillator 440 to enable operation of the VNA with minimal interference from external signals. Reference oscillator 440 operates at a frequency F_R which is a chosen reference frequency $\pm$ a 100 parts per million (ppm) offset. For example, if the desired reference frequency is 6 MHz, the $\pm$ 100 ppm offset would be $\pm$ 600 Hz. With the dither line connected to the output of integrator 533, the reference oscillator 440 will sweep the entire 100 ppm range during each measurement made by the A/D converter 548 due to the INC REAL signal always going from the 0V reference to $+V_{A/D}$. Note that although a $\pm$ 100 ppm range is suggested, different ranges may also be used.

Fig. 6 illustrates operation of the test circuitry of Fig. 4 with and without the dither line connected. Graph 601 shows the INC REAL signal received without receipt of an additional external signal. Graph 602 shows the INC

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REAL signal received in the presence of an external signal of frequency substantially equal to the reference frequency F_R with the dither line disconnected. In graph 602, interference of the signals occurs with error possibly occurring in the A/D measurement. Graph 603 shows the INC REAL
5 signal in the presence of the interfering signal with the dither line connected. As shown, with the dither line sweeping the frequency of reference oscillator 440, interference occurs only in a small range, substantially reducing the possibility of error.

The present invention further includes the second test port 104 to receive
10 transmitted signals. A signal received at test port 104 may be the signal F_{OA} from the test signal synthesizer 400 as transmitted from the first test port 103, or a signal from another source. The signal received at the second test port 104 is provided through a pad 549 to the first input of mixer 550. The attenuation of pad 549 is set to equalize attenuation seen by a signal F_{OA} when that signal is
15 provided as an incident signal through pad 449, as a reflected signal through pad 448, or as a transmitted signal through pad 549, assuming no attenuation occurs between ports 103 and 104.

A second input of mixer 550 receives the LO signal from the output F_{OB} of tracking signal synthesizer 420. By mixing a transmitted RF signal with the LO
20 signal, a transmitted IF test signal is provided at the output of mixer 550. Although the device 550 is shown as a mixer, harmonic samplers may also be substituted as indicated previously.

Similar to the incident and reflected IF signals provided from mixers 452 and 460, the transmitted IF signal from mixer 550 is provided through a
25 bandpass filter 560 and amplifier 570 to synchronous detectors. The bandpass filter has a bandwidth set to remove extraneous signals from the transmitted IF signals.

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The amplifier 570 is a variable gain device with a gain controlled by processor 306. The variable gain amplifier 570 is utilized because the signal F_o provided from port 103 may be significantly attenuated before reaching port 104, depending on components utilized to interconnect ports 103 and 104.

5 To determine the amount of gain $G1$ needed for amplifier 570, a peak detector made up of diode 572 and capacitor 573 couple the output of amplifier 570 to an input (TRNS AMP) of the A/D converter 548. An output of the A/D converter 548 is received by processor 306, and the processor 306 functions to increase the gain $G1$ of amplifier 570 when a signal is received in steps until a
10 signal of a desired level is received from the peak detector 572, 573. A filter 571 is utilized to couple amplifier 570 to peak detector 572, 573 to remove undesired signals not removed by filter 560.

In the synchronous detectors, the transmitted IF output from amplifier 570 is received at a first input of multipliers 574 and 575. A second input of
15 multiplier 574 is connected to an output of PLL 510 which provides a reference signal at the IF frequency phase shifted by 0 degrees. A second input of multiplier 575 receives an output of PLL 510 which provides a reference signal at the IF frequency phase shifted by 90 degrees. Multiplier 574, thus, outputs the transmitted real component of the transmitted signal, while multiplier 575
20 outputs the transmitted imaginary component of the transmitted signal.

The outputs of multipliers 574-575 are connected through respective switches 576-577 and integrators 578-579 to A/D converter 548. The switches 575-576 are controlled to be opened or closed by the integrate signal (INT) received from control circuit 546, the INT signal also being provided to switches
25 521-524 as described above. Further, control circuitry 546 provides a reset signal (RST) to a switch connected in parallel with the capacitors of integrators 578-579, the RST signal also being provided to switches 531-534 as described

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above. The A/D converter 548, upon receiving analog signals from integrators 578 and 579 as respective transmitted real (TRNS REAL) and transmitted imaginary (TRNS IMAG) signals provides a digital value for the analog values received.

5 The dither line connecting the output of integrator 533 to reference oscillator 440 sweeps the frequency of reference oscillator 440 to enable operation of the circuitry of Fig. 4 in the presence of external signals, as discussed above. With the LO signal provided to mixer 550 when the dither line is connected, signals received at port 104, other than signals provided from port
10 103 will be substantially removed.

So that the circuit of Fig. 4 can operate as a frequency monitor to detect the frequency and power level of external signals, a switch is included to connect or disconnect the dither line from reference oscillator 440 as controlled by processor 306. Further, instead of upconverting and downconverting typically performed
15 in a spectrum analyzer to eliminate undesired image frequencies, the present invention utilizes the circuitry of Fig. 4 along with a unique measuring scheme to detect frequency and power for external signals.

The unique measurement scheme of the present invention enables detection of signals along with a determination of the maximum power level of signals
20 within bins defined over a range of frequencies to be monitored. With the circuitry of Fig. 4, the frequency width of the bins will be greater than the typical fine resolution provided by a spectrum analyzer, and images will not be eliminated. However, size and weight will be reduced from circuitry typically found in a spectrum analyzer, and images created and measured can be identified
25 as a possible source of interference when a frequency monitor of the present invention is utilized for detecting interfering at a cell site.

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For the frequency monitor measurement scheme, the dither line is disconnected, and a frequency range to be monitored is divided into the bins, as indicated above. A first measurement of IF signals from amplifier 560 is then made with the LO signal set to a frequency value in the bin. The LO signal is then stepped in frequency so that the range of RF signals received at port 104 in the frequency range of the bin can produce IF signals from amplifier 560.

During each measurement for a bin, the gain of the variable gain amplifier 570 G1 is stepped until a desired voltage value is received from the peak detector 572,573. The gain G1 of the amplifier 570 along with the additional voltage value from peak detector 572,573 above the desired voltage value is stored and associated with a power level for each measurement for the bin. The maximum power level received during the measurements for the bin is then stored as the power level for signals detected for the bin. The measurement scheme is then applied to subsequent bins until power level measurements for each bin covering the entire frequency range to be monitored have been made.

The frequency monitoring measurement scheme of the present invention is further described with reference to Fig. 7. Fig. 7 includes a first line 700 representing a range of frequencies with 100 KHz per division. For purposes of illustration, it is first assumed a LO signal F_{LO} is provided as indicated on the line at 1000.0 MHz, and that RF external signals F_{RF} occur at 1000.2 MHz and 999.8 MHz, also as shown. With such signals provided to mixer 550 of Fig. 4, an IF signal will be generated at 200 KHz for both RF signals. With a bandpass filter such as 560 having a center frequency at 200 KHz, and a bandwidth of 200 KHz, RF signals within the range of the semicircles shown from 1000.1-1000.3 MHz and 999.7-999.9 MHz would be detected from IF signals from amplifier 570 when mixed with the LO signal at 1000.0 MHz.

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With a filter 560 having a 200 KHz center frequency and 200 KHz bandwidth, RF signals within the range 999.9-1000.1 would not be detected. Stepping of the LO frequency to assure that RF signals in the 999.7-1000.3 MHz range will be detected is thus further performed using the scheme of the present invention as described with reference to line 710 of Fig. 7.

Line 710 represents a range of frequencies with 100 KHz per division, and also shows the LO signal stepped up in frequency to 1000.2 MHz. With bandpass filter 560 having a center frequency at 200 KHz, and a bandwidth of 200 KHz, RF signals within the range of the semicircle from 999.8-1000.1 will be detected from IF signals from amplifier 570, effectively filling in the frequency range gap shown on line 700 between the semicircles where RF signals were not previously detected. Additionally, as shown on line 710 with the LO signal at 1000.2 MHz, RF signals will be received within the semicircle shown from 1000.3-1000.5 MHz.

With a bin defined from 999.7-1000.5 MHz, and with the IF filter 560 having a center frequency of 200 KHz and a bandwidth of 200 KHz, two LO signals at 1000.0 MHz and 1000.2 MHz can, thus, be utilized to enable RF signals within the 800 KHz frequency range of the bin to be detected.

To illustrate the effect of reducing the bandwidth of filter 560 on the measurement scheme of the present invention, additional lines 720-723 are included in Fig. 7 showing frequency divisions of 100 KHz, similar to lines 700 and 710. For purposes of illustration, the bandwidth of filter 560 is assumed reduced to 100 KHz, while its center frequency is assumed to remain at 200 KHz.

In line 700, with a LO frequency of 1000.0 MHz first utilized and the bandwidth of filter 560 reduced as indicated, RF signals will be detected in the range of 999.75-999.85 MHz and in the range of 1000.15-1000.25 MHz as

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shown by the semicircles. RF signals in the frequency range 999.85-1000.15 will, however, not be detected. By stepping the LO frequency in three 100 KHz steps using the measurement scheme of the present invention, as shown in lines 701-703, the 999.85-1000.15 range will be covered. In fact, RF signals through
5 an entire frequency range from 999.75-1000.55 MHz can be detected, enabling a bin to be defined over that 800 KHz range.

Note that for the signals of Fig. 7, even though the bandwidth of filter 560 is reduced, the measurement range, or bin width, covered by stepping the LO to assure no RF signals with the bin go undetected, remains at four times the IF
10 center frequency of filter 560, or at 800 KHz. Thus, to keep costs at a minimum, higher bandwidth filters may be selected for element 560 with out affecting resolution.

Although the invention has been described above with particularity, this was merely to teach one of ordinary skill in the art how to make and use the
15 invention. Many modifications will fall within the scope of the invention, as that scope is defined by the following claims.

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What Is Claimed Is:

1. A vector network analyzer (VNA) comprising:
 - a first test port;
 - a second test port;
 - 5 a test signal synthesizer including a series coupled phase detector, oscillator and synthesizer frequency divider;
 - a tracking synthesizer including a series coupled phase detector, oscillator and synthesizer frequency divider;
 - a first frequency divider coupling an output of the test signal synthesizer to
10 the first test port;
 - a second frequency divider for connecting an output of the test signal synthesizer to an input of the phase detector of the tracking synthesizer;
 - a first mixing means having a first input coupled to receive an output of the first frequency divider a second input coupled to an output of the tracking
15 synthesizer, and an output providing an incident IF signal;
 - a second mixing means having a first input coupled to receive a signal from the first test port, a second input coupled to receive the output of the tracking synthesizer, and an output providing a reflected IF signal; and
 - a third mixing means having a first input coupled to receive a signal from
20 the second test port, a second input coupled to receive the output of the tracking synthesizer, and an output providing a transmitted IF signal.
2. The VNA of Claim 1, further comprising:
 - a splitter having an input coupled to the first frequency divider output, a
25 first output connected to the first input of the first mixing means and a second output; and

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a coupler having a thru path connected from the second output of the splitter to the first test port and a coupling path coupling the first test port to the first input of the second mixing means.

- 5 3. A vector network analyzer (VNA) comprising:
- a first test port;
 - a second test port;
 - a test signal synthesizer having an output coupled to the first test port;
 - a tracking synthesizer;
 - 10 a first mixing means having a first input coupled to receive the output of the test signal synthesizer, a second input coupled to an output of the tracking synthesizer, and an output providing an incident IF signal;
 - a second mixing means having a first input coupled to receive a signal from the first test port, a second input coupled to receive the output of the tracking
 - 15 synthesizer, and an output providing a reflected IF signal;
 - a third mixing means having a first input coupled to receive a signal from the second test port, a second input coupled to receive the output of the tracking synthesizer, and an output providing a transmitted IF signal;
 - an analog to digital (A/D) converter;
 - 20 a first synchronous detector including a series connected multiplier and integrator, the multiplier having a first input receiving the incident IF signal, and a second input, and the integrator having an output providing an incident real voltage signal to an input of the A/D converter;
 - a second synchronous detector including a series connected multiplier and
 - 25 integrator, the multiplier of the second synchronous detector having a first input receiving the incident IF signal, and a second input, and the integrator of the

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second synchronous detector having an output providing an incident imaginary voltage signal to an input of the A/D converter;

5 a third synchronous detector including a series connected multiplier and integrator, the multiplier of the third synchronous detector having a first input receiving the reflected IF signal, and a second input, and the integrator of the third synchronous detector having an output providing a reflected real voltage signal to an input of the A/D converter;

10 a fourth synchronous detector including a series connected multiplier and integrator, the multiplier of the fourth synchronous detector having a first input receiving the reflected IF signal, and a second input, and the integrator of the fourth synchronous detector having an output providing a reflected imaginary voltage signal to an input of the A/D converter;

15 a fifth synchronous detector including a series connected multiplier and integrator, the multiplier of the fifth synchronous detector having a first input receiving the transmitted IF signal, and a second input, and the integrator of the fifth synchronous detector having an output providing a transmitted real voltage signal to an input of the A/D converter;

20 a sixth synchronous detector including a series connected multiplier and integrator, the multiplier of the sixth synchronous detector having a first input receiving the transmitted IF signal, and a second input, and the integrator of the sixth synchronous detector having an output providing a transmitted imaginary voltage signal to an input of the A/D converter; and

25 a synchronous detector control means coupled for receiving the incident IF signal and providing a first phase reference output to the second input of the multipliers of the first, third and fifth synchronous detectors, and a second phase reference output with approximately a 90 degree phase difference from the first

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phase reference output to the second input of the multipliers of the second, fourth and sixth synchronous detectors.

4. The VNA of Claim 3 wherein the synchronous detector control means is
5 further coupled for receiving the incident imaginary voltage from the output of the integrator of the second synchronous detector and providing the first and second phase reference outputs so that the incident imaginary voltage signal does not change substantially over time.

10 5. The VNA of Claim 4 wherein the synchronous detector control means comprises:

a comparator having a first input coupled by an integrator to receive the incident imaginary voltage from the output of the integrator the second synchronous detector, a second input receiving the incident IF signal and an
15 output; and

an I/Q synthesizer comprising:

an oscillator having a voltage control input and an output for providing an output with a frequency approximately four times a frequency of the incident IF signal based on a signal received at its voltage control input:

20 a phase detector having a first input connected to the output of the comparator and a second input connected receive the first phase reference output, the phase detector providing a voltage control signal coupled to the voltage control input of the oscillator based upon a phase comparison of the signals at the first and second inputs of the phase detector;

25 a first D-type flip-flop having a clock input receiving the oscillator output, a Q output providing the first phase reference output, and a D input; and

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a second D-type flip-flop having a clock input receiving the oscillator output, a D input receiving the Q output of the first D-type flip-flop, a Qoutput connected to the D input of the first D-type flip-flop and a Q output providing the second phase reference output.

5

6. The VNA of Claim 3 wherein the A/D converter operates to accurately convert an input signal up to a maximum voltage, the VNA further comprising:

an A/D converter range maximizing means having a first input receiving a voltage reference approximately equal to the maximum voltage, a second input
10 connected to the output of the integrator of the first synchronous detector, and an output providing an integrate signal at a beginning of a cycle of the incident IF signal and a reset signal when the incident real voltage reaches the maximum value, and

wherein the first, second, third, fourth, fifth and sixth synchronous
15 detectors each further comprise:

a first switch coupled for receiving the integrate signal from the A/D converter range maximizing means and for coupling the output of the multiplier of a respective one of the synchronous detectors to the input of the integrator of the respective one of the synchronous detectors, the first switch being controlled
20 to close when the integrate signal is enabled and to open when the integrate signal is disabled; and

a second switch coupled for receiving the reset signal from the A/D converter range maximizing means and for coupling the input to the output of the integrator of the respective one of the synchronous detectors, the second switch
25 being controlled to close when the reset signal is enabled and to open when the reset signal is disabled.

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7. The VNA of Claim 6 wherein the A/D converter range maximizing means comprises:

a comparator having a first input connected to receive the voltage reference, a second input connected to receive the output of the integrator of the first synchronous detector and an output; and

a processor receiving the output of the comparator and providing the integrate signal and the reset signal.

8. The VNA of Claim 3, wherein the VNA is handheld.

9. A vector network analyzer (VNA) comprising:

a first test port;

a second test port;

a test signal synthesizer;

a tracking synthesizer;

a first frequency divider positioned to couple an output of the test signal synthesizer to the first test port;

a first mixing means having a first input coupled to receive an output of the first frequency divider, a second input coupled to an output of the tracking synthesizer, and an output providing an incident IF signal;

a second mixing means having a first input coupled to receive a signal from the first test port, a second input coupled to receive an output of the tracking synthesizer, and an output providing a reflected IF signal; and

a third mixing means having a first input coupled to receive a signal from the second test port, a second input coupled to receive an output of the tracking synthesizer, and an output providing a transmitted IF signal.

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10. The VNA of Claim 9 further comprising:

a third frequency divider coupling the output of the tracking synthesizer to the second input of the first mixing means and to the second input of the second and third mixing means.

5

11. The VNA of Claim 9, wherein the first, second and third mixing means comprise harmonic samplers.

12. The VNA of Claim 9, wherein the tracking synthesizer and the test signal synthesizer have phase detector inputs, and wherein the test signal synthesizer and the tracking synthesizer each comprise:

10

an oscillator having a voltage control input and an output for providing the respective synthesizer output;

a phase detector having first and second inputs and providing a voltage control signal output coupled to the voltage control input of the oscillator, the first phase detector input providing the phase detector input of the respective synthesizer; and

15

a synthesizer frequency divider for connecting the output of the oscillator to the second input of the phase detector.

20

13. The VNA of Claim 9, wherein the first frequency divider has an input connected to the output of the test signal synthesizer, and an output, the VNA further comprising:

25

a splitter having an input connected to the first frequency divider output, a first output coupled to the first input of the first mixing means and a second output; and

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a coupler having a thru path connected from the second output of the splitter to the test port and a coupling path coupling the test port to the first input of the second mixing means.

- 5 14. A vector network analyzer (VNA) comprising:
- a first test port;
 - a second test port;
 - a test signal synthesizer having an output coupled to a first test port;
 - a tracking synthesizer;
 - 10 a first mixing means having a first input coupled to receive an output of the test signal synthesizer, a second input coupled to an output of the tracking synthesizer, and an output providing an incident IF signal;
 - a second mixing means having a first input coupled to receive a signal from the first test port, a second input coupled to receive the output of the tracking
 - 15 synthesizer, and an output providing a reflected IF signal; and
 - a third mixing means having a first input coupled to receive a signal from the second test port, a second input coupled to receive the output of the tracking synthesizer, and an output providing a transmitted IF signal
 - a reference oscillator for providing an output signal having a reference
 - 20 frequency with a varied offset to a phase detector input of the test signal synthesizer, the varied offset being varied as controlled by a voltage control input to the reference oscillator; and
 - a dither means coupled for receiving the incident IF signal and providing a voltage control signal changing from a minimum value to a maximum value
 - 25 during a cycle of the incident IF signal to the voltage control input of the reference oscillator.

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15. The VNA of Claim 14 wherein the dither means comprises:

an IQ detection synthesizer for providing a first phase reference output and a second phase reference output approximately 90 degrees out of phase with the first phase reference output, the first phase reference output being provided to a

5 first phase detector input of the IQ detection synthesizer;

a first multiplier coupled for receiving the incident IF signal and the first phase reference output and providing an incident real output signal;

a second multiplier coupled for receiving the incident IF signal and the second phase reference output and providing an incident imaginary output signal;

10 a first integrator coupled for receiving the incident real output signal and having an output providing the voltage control input of the reference oscillator;

a second integrator coupled for receiving the incident imaginary output signal and having an output; and

15 a comparator having a first input coupled by an integrator to an output of the second integrator, a second input receiving the incident IF signal and an output connected to a second phase detector input of the IQ detection synthesizer.

16. The VNA of Claim 15 wherein the IQ detection synthesizer comprises:

20 an oscillator having a voltage control input and an output for providing an output signal with a frequency approximately four times a frequency of the incident IF signal based on a signal received at its voltage control input:

a phase detector having a first input providing the first phase detector input and a second input providing the second phase detector input, the phase detector providing a voltage control signal coupled to the voltage control input of the oscillator based upon a phase comparison of signals at its first and second inputs;

25 a first D-type flip-flop having a clock input receiving the oscillator output, a Q output providing the first phase reference output, and having a D input; and

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a second D-type flip-flop having a clock input receiving the oscillator output, a D input receiving the Q output of the first D-type flip-flop, a Q output connected to the D input of the first D-type flip-flop and a Q output providing the second phase reference output.

5

17. The VNA of Claim 15, wherein the dither means is coupled to the voltage control input of the reference oscillator by a switch controlled to disconnect the dither means from the input of the reference oscillator when the VNA is utilized as a frequency monitor.

10

18. A method of monitoring the frequency and power level of RF signals occurring within a test frequency range comprising the steps of:

defining bins, each bin having a frequency range occupying a portion of the test frequency range, and for each bin:

15

(a) setting a local oscillator (LO) frequency to an initial value;

(b) mixing the LO frequency with the RF signals to provide IF signals;

(c) filtering the IF signals to create received IF signals generated from a portion of the RF signals occupying a portion of the frequency range of the respective bin;

20

(d) measuring the peak power level of the received IF signals and storing the measured power level value;

(e) determining if received IF signals have been provided for all the RF signals which can occupy the frequency range of the respective bin;

25

(f) resetting the LO frequency when the determining step indicates that received IF signals have not been provided for all the RF signals which can occupy the frequency range of the respective bin and proceeding to step (b), and otherwise proceeding to step (g)

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(g) storing a maximum measured power level value measured in step (e) as the power level value for the respective bin.

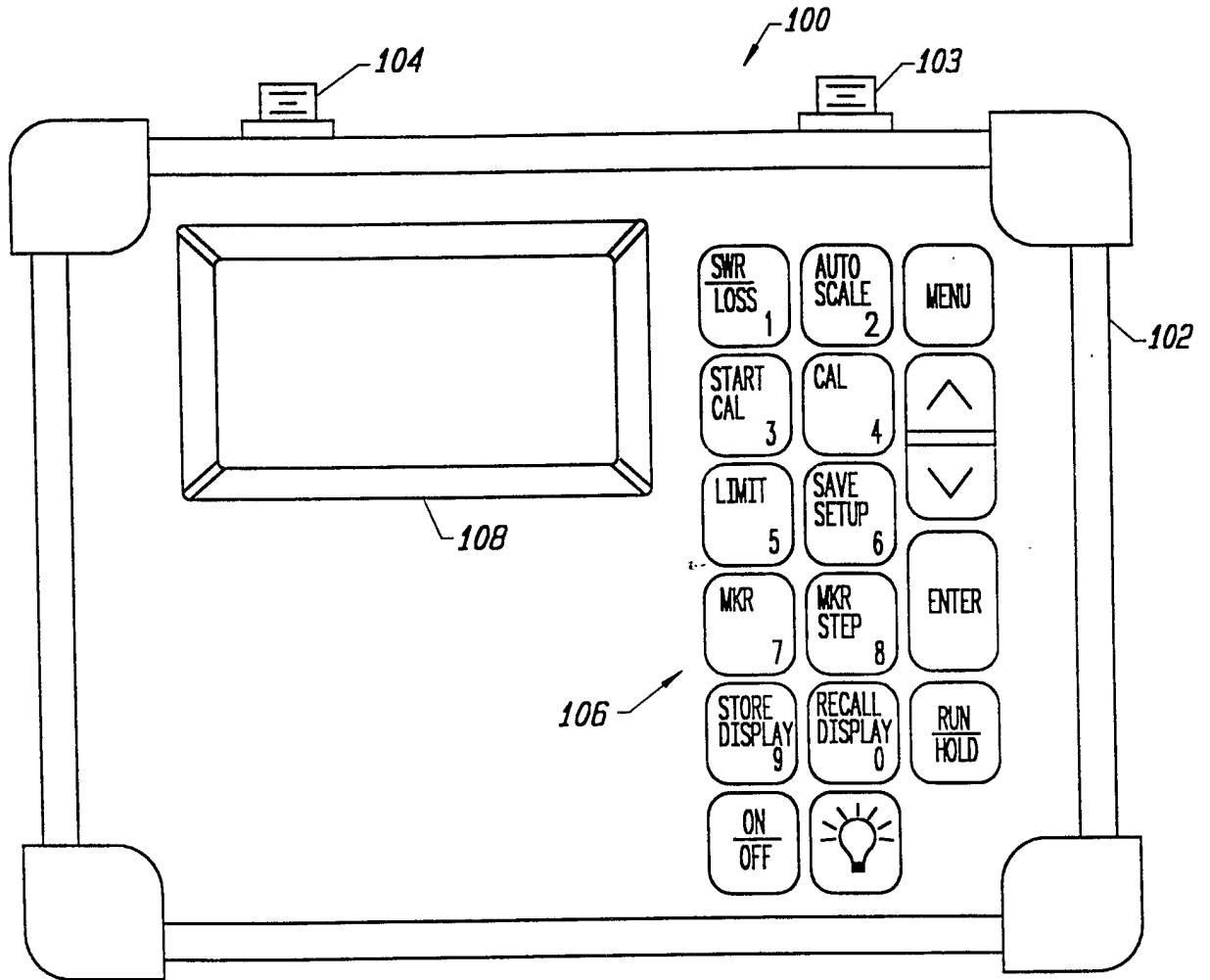


FIG. 1

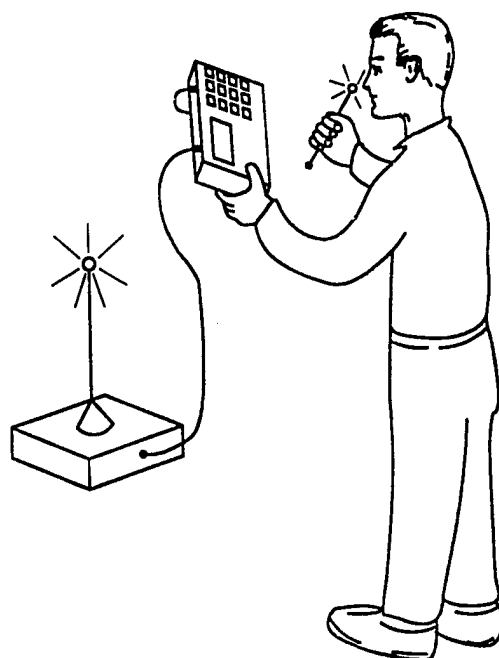
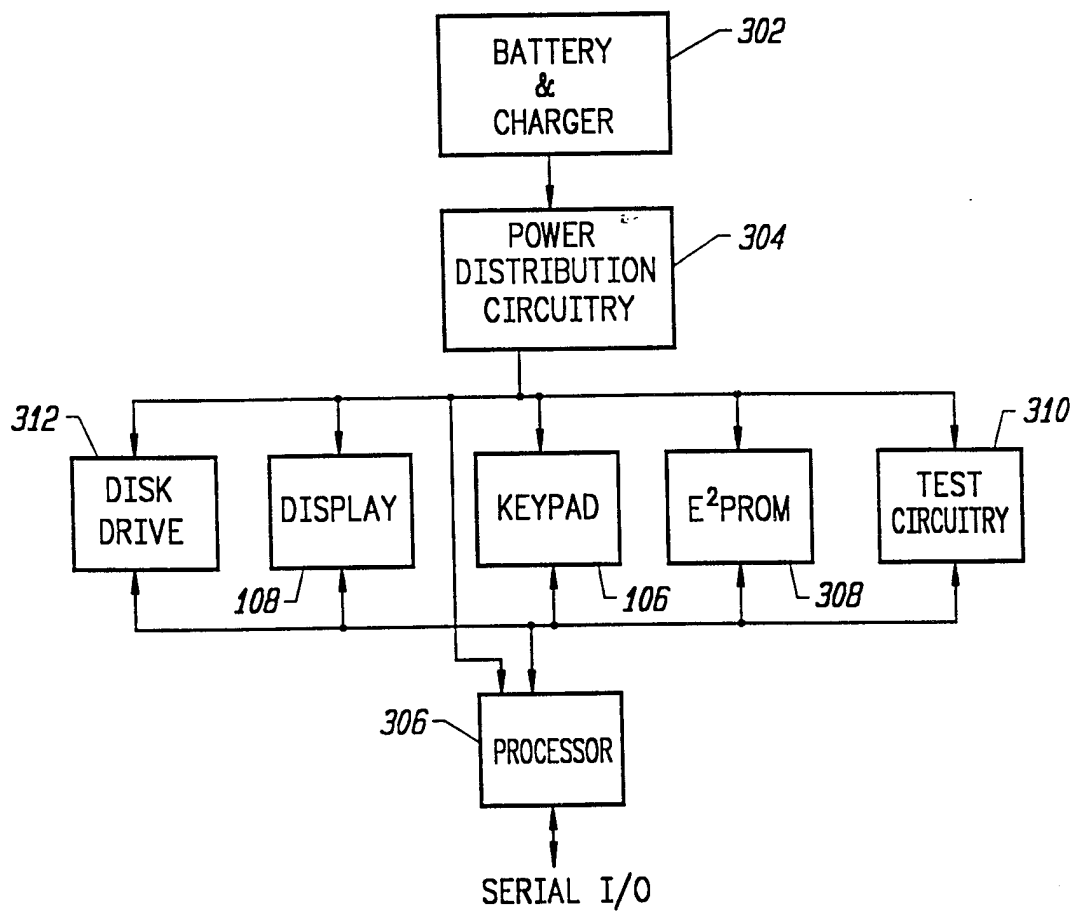
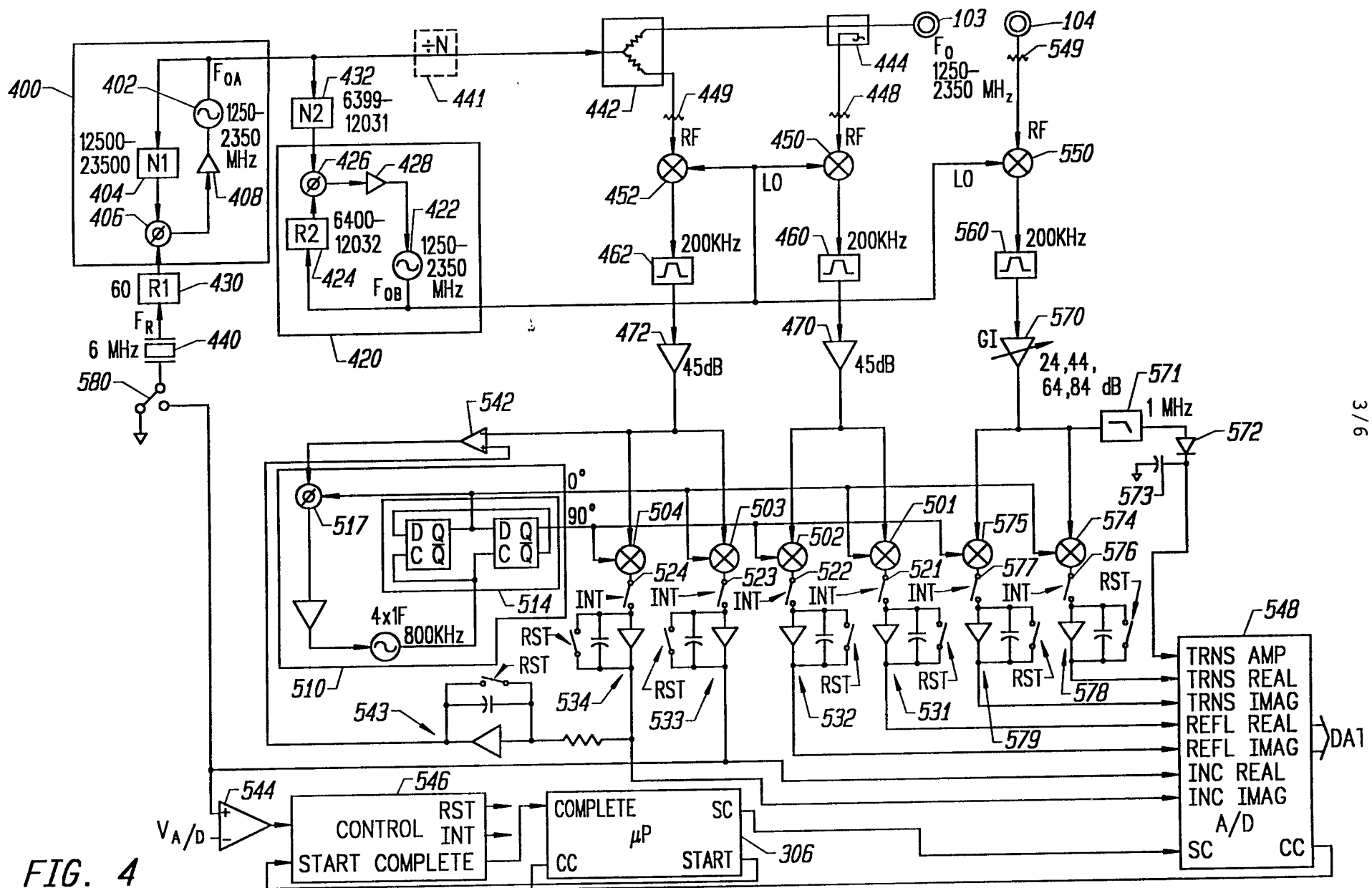


FIG. 2

*FIG. 3*

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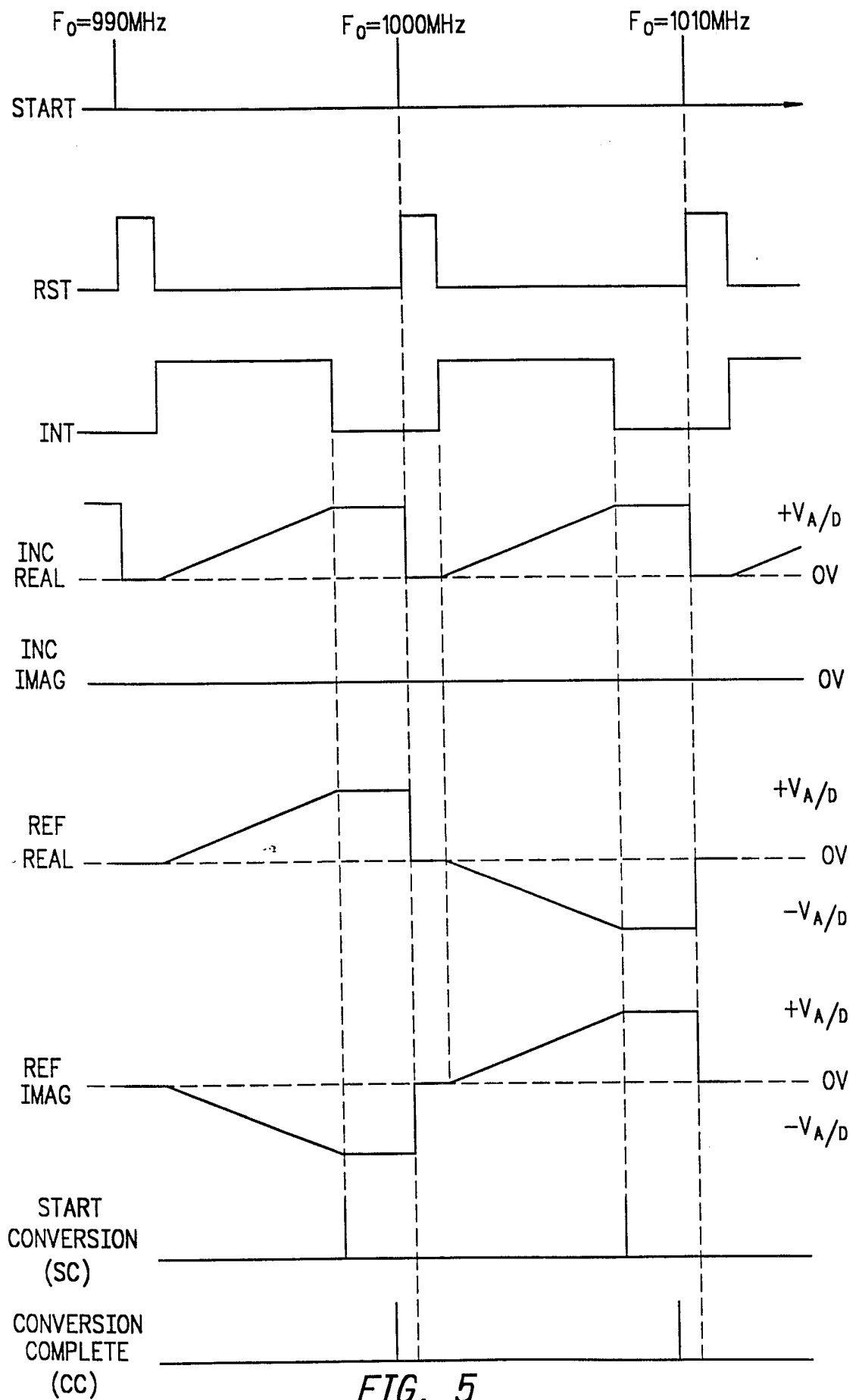
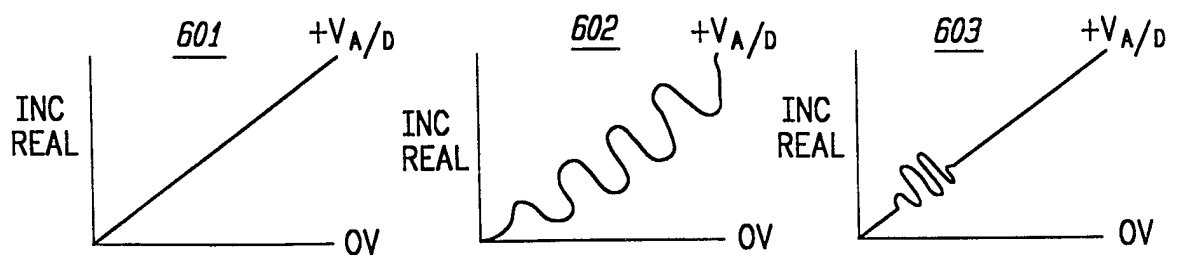
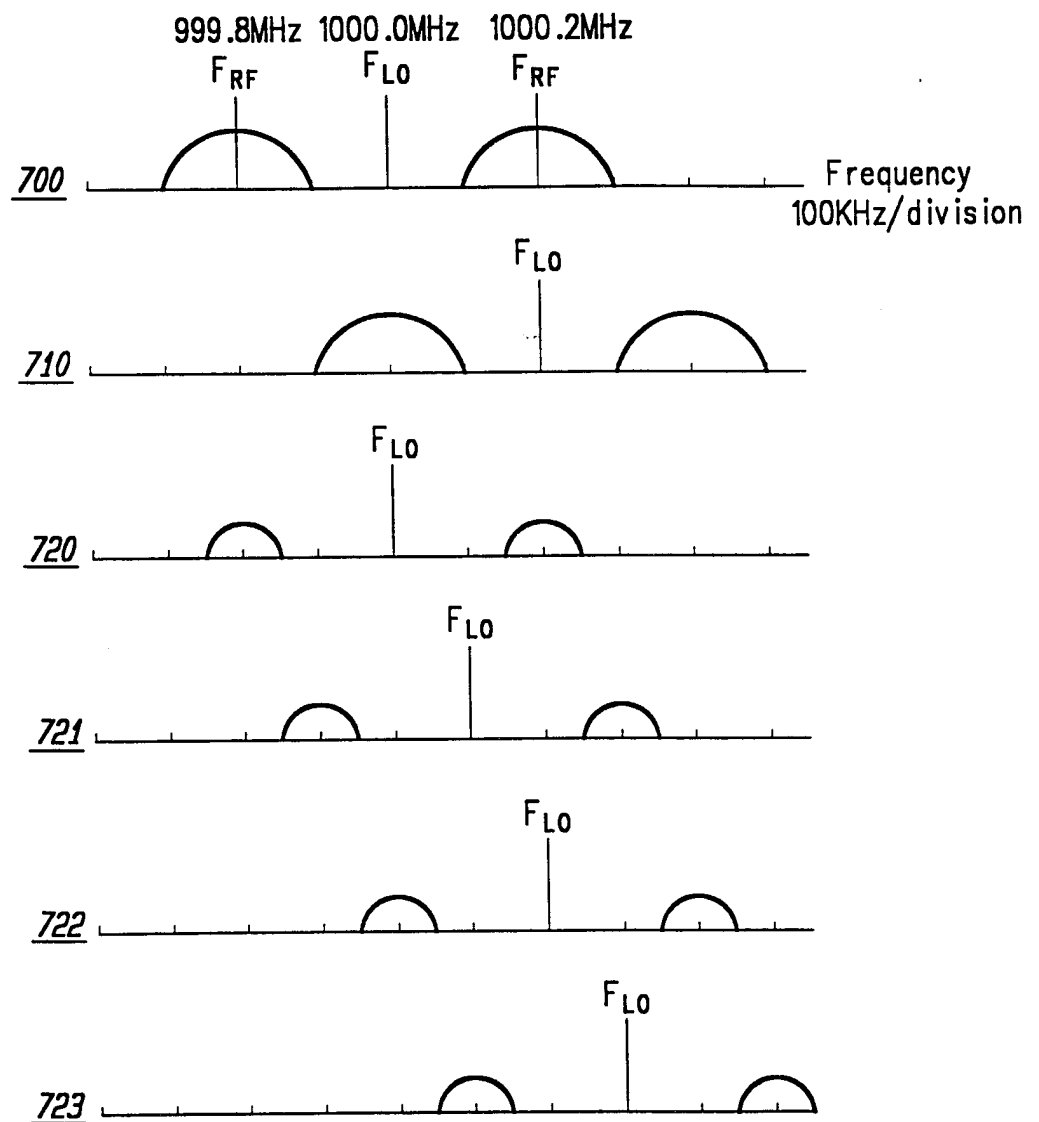


FIG. 5

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*FIG. 6*

*FIG. 7*