



(51) International Patent Classification:
G06F 1/32 (2006.01)

(21) International Application Number:
PCT/US2016/067837

(22) International Filing Date:
20 December 2016 (20.12.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/007,021 26 January 2016 (26.01.2016) US

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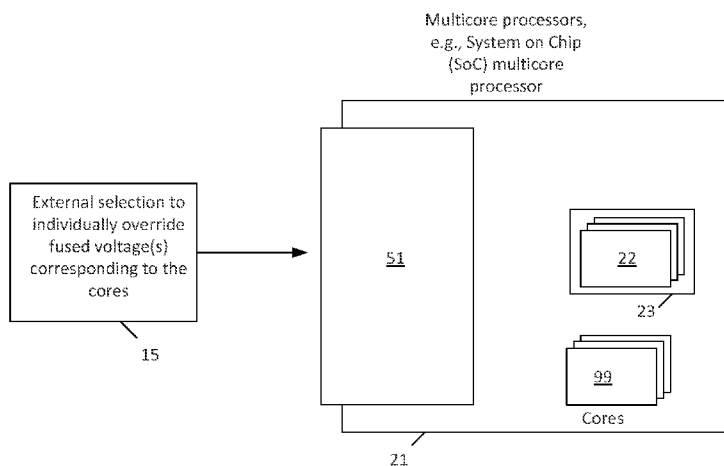
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: PROVIDING ACCESS FROM OUTSIDE A MULTICORE PROCESSOR SoC TO INDIVIDUALLY CONFIGURE VOLTAGES



(57) Abstract: Apparatuses, methods and storage medium for providing access from outside a multicore processor System on Chip (SoC) are disclosed herein. In embodiments, an SoC may include a memory to store a plurality of embedded values correspondingly associated with a plurality of architecturally identical cores. Each embedded value may indicate a default voltage for a respective one of the plurality of architecturally identical cores. In embodiments, an apparatus may include one or more processors, devices, and/or circuitry to provide access from outside the multicore processor SoC to individually configure voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages. Other embodiments may be described and/or claimed.

PROVIDING ACCESS FROM OUTSIDE A MULTICORE PROCESSOR SoC TO INDIVIDUALLY CONFIGURE VOLTAGES

Related Application

5 This application claims priority to U.S Patent Application 15/007,021, entitled “PROVIDING ACCESS FROM OUTSIDE A MULTICORE PROCESSOR SoC TO INDIVIDUALLY CONFIGURE VOLTAGES,” filed January 26, 2016.

Technical Field

10 The present disclosure relates to multicore processors, for example multicore processors of a System on Chip (SoC) architecture, and more specifically relates to access from outside a multicore processor to individually configure voltages of the processor cores.

Background

15 The background description provided herein is for the purpose of generally presenting the context of the disclosure. Unless otherwise indicated herein, the materials described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

20 In order to manage manufacturing variation during fabrication of multicore processors while maintaining quality and reliability, conservative guard bands are employed during testing, and devices are “binned” or classified based on their speed and power characteristics. Conventional speed binning treats multicore processors as single-core devices by assigning a single related speed and minimum operating voltage for the processor as a whole. The rated speed and minimum voltage typically reflects the speed of the slowest core and the minimum voltage of the core having the poorest minimum
25 voltage.

Brief Description of the Drawings

30 Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

 FIG. 1 illustrates an example system having access from outside a multicore processor to individually configure voltages of the processor cores, according to various embodiments.

 FIG. 2 illustrates example operations that may be performed by the system of FIG.

1, according to various embodiments.

FIG. 3 illustrates an example of a system that may include a Processor Control Unit (PCU) and an integrated voltage regulator, according to various embodiments.

FIG. 4 illustrates example an example process that may be used in the example
5 system of FIG. 3, according to various embodiments.

FIG. 5 illustrates an example computing device that may employ the apparatuses and/or methods described herein, according to various embodiments.

Detailed Description

Apparatuses, methods and storage medium associated with computing that
10 includes providing access from outside a multicore processor SoC to individually configure voltages of the processor cores are disclosed herein. In embodiments, an apparatus may include one or more processors, devices, and/or circuitry to provide access from outside the multicore processor SoC to individually configure voltages of the plurality of architecturally identical cores to values that are different than the values of the
15 default voltages.

In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes
20 may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments is defined by the appended claims and their equivalents.

Aspects of the disclosure are disclosed in the accompanying description. Alternate embodiments of the present disclosure and their equivalents may be devised without
25 parting from the spirit or scope of the present disclosure. It should be noted that like elements disclosed below are indicated by like reference numbers in the drawings.

Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these
30 operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

For the purposes of the present disclosure, the phrase “A and/or B” means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

The description may use the phrases “in an embodiment,” or “in embodiments,”
5 which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments of the present disclosure, are synonymous.

As used herein, the term “circuitry” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared,
10 dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

In known multicore processor SoCs, for a variety of reasons, such as manufacturing variations, all processor cores (hereinafter, simply “cores”) are not created
15 equal. While the cores may be logically identical (e.g., architecturally identical), the cores may have different physical characteristics. One core of a multicore processor SoC may be capable of operating at a higher performance level, e.g., higher frequency or lower voltage, than another core of the multicore processor SoC.

In some processors, at manufacturing time, different voltages, which may be called
20 “manufacturing fused voltages” may be associated with the different cores, reflective of their different operating capability. The manufacturing fused voltages may configure a fixed maximum voltage for each core. The manufacturing fused voltages may be stored in read only memory of the multicore processor.

Performance modification tools, sometimes referred to as “overclocking” tools,
25 may provide voltage configurability. In known performance modification tools, an operating system interface or a Basic Input Output System (BIOS) interface may communicate with a Processor Control Unit (PCU) to enable a system administrator to select an operating voltage that is different than at least some of the fused voltages of the multicore processor, by a signal to the PCU. For instance, an example six-core multicore
30 processor that is capable of operating at 1.55V (to achieve a higher frequency and/or performance level) may include a read only memory storing the voltages 1.3V, 1.35V, 1.55V, 1.35V, 1.35V, and 1.3V for core 0, core 1, core 2, core 3, core 4, and core 5, respectively. A system administrator may, accepting the associated tradeoffs, configure the multicore processor for 1.55V operation with known performance modification tools,

to attempt to operate the cores at voltages 1.55V, 1.55V, 1.55V, 1.55V, 1.55V, and 1.55V for core 0, core 1, core 2, core 3, core 4, and core 5, respectively. If the computing system using the multicore processor appears to be stable at administered multicore processor setting (e.g. 1.55V in the above example), certain tradeoffs are still realized (despite the
5 apparent stability). These tradeoffs may include accelerated reliability degradation and thermal considerations. The higher the voltage, the shorter the life of a given processor core will be. All processor cores are subjected to accelerated degradation because they all run at the voltage required by the “weakest” core. The administered multicore processor setting will also result in higher processor package temperatures. This could result in
10 throttling (lower performance) and/or may require more aggressive, such as more expensive, cooling solution.

Various embodiments disclosed herein enable the ability to externally configure voltage of each core of a multicore processor with an SoC architecture, which may be used to improve performance, power efficiency, reliability, or the like, or combinations thereof.
15 In an example, a system may support user/system/software programmability of processor core voltage for each processor core. In an example, the system may support individual processor core voltages above a respective fixed voltage maximum voltage of the manufacturing fused voltages of the multicore processor.

Various embodiments may include an externally configurable interface for per core
20 voltage settings (e.g., access from outside the multicore processor SoC to individually configure voltages to values that are different than the values of manufacturing fused voltages). In an example, a processor interface, accessible to BIOS or other software (e.g., an operating system, driver, application, etc.), may enable configuration of voltage on a per individual core basis. In an example, the interface may utilize register(s), such as
25 control register(s) (e.g., an MSR (model specific register(s))), a messaging interface, such as OC (overclocking) Mailbox, or the like, or combinations thereof. The interface may provide more than one format in which external configuration may be managed, e.g. actual voltage value per processor core, an offset from the a default such as the manufacturing fused voltages, a single voltage value and an offset from the single voltage value, or the
30 like, or combinations thereof.

Various embodiments may include an automated system, which may be internal to the processor. In an example, the automated system may include a PCU to scale and/or select voltage values for individual processor cores based on information received from the externally configurable interface, such as based on an externally requested frequency

(e.g., a user-selected frequency or a frequency selected by an external system such as an application of an operating system associated with the multicore processor). The automated system may receive an external configuration input including and/or indicating a request for individualized voltage mode. The request may be from BIOS, other software
5 (such as an operating system), a register (such as a control register), a messaging interface, or the like, or combinations thereof. The PCU may generate an estimate of how to scale an operation characteristic, e.g., scaling up voltage, and then apply the PCU generated estimate responsive to receiving the request.

Various embodiments may include a multicore processor, e.g., a multicore
10 processor of an SoC architecture, of a computing system. The multicore processor may include an interface exposed to the computing system, the exposed interface to accept and implement voltage values requested by the computing system. The computing system may include software code (of BIOS, an application, an operating system, etc.) to communicate with the exposed interface to program the multicore processor with the
15 voltage values.

Various embodiments may improve performance and/or reliability. The increased performance may be associated with a lower individual voltage for at least one core, which may create less heat. The lower heat may result in a higher “overclock” to another core, which may provide improved computing performance. The lower heat may result in
20 improved performance of automated turbo operation systems. The improved reliability may be based on reduction of the average voltage per core.

FIG. 1 illustrates an example system having access from outside a multicore processor to individually configure voltages, according to various embodiments.

The system 100 may include a multicore processor 21, e.g., an SoC multicore
25 processor. The multicore processor 21 may include a plurality of cores 99, e.g. a plurality of architecturally identical cores. A first core of the plurality of cores 99 may have a first physical characteristic, and a second core of the plurality 99 may have a second physical characteristic that is different than the first physical characteristic. The different physical characteristics may be related to process, heat, or temperature variations during
30 manufacturing, the different relative positions of the cores of the plurality 99 in the multicore processor 21, or the like, or combinations thereof.

The multicore processor 21 may include a memory 23 storing a plurality of embedded values 22 correspondingly associated with the plurality of cores 99, each embedded value to indicate a default voltage for a respective one of the plurality of cores

99.

A component 51 may provide access from outside the multicore processor 21 to individually set/program voltages of the plurality of cores 21 to values that are different than the embedded values 22. The component 51 may receive an external selection 15 to
5 individually override at least one of the embedded values 22, e.g., to override at least a subset of the values 22 and/or to override one of the values 22 differently than another one of the values. The external selection 15 may be from BIOS or other software (an application, an operating system) of a computing system in which the multicore processor 21 is resides. In various embodiments, the component 51 may include a register-based
10 interface, a message-based interface, an instruction-based interface, pins, or the like, or combinations thereof.

In an example where the multicore processor 21 utilizes a discrete voltage regulator that provides voltage to the multicore processor 21. The discrete voltage regulator may be an external voltage regulator. In such a case the component 21 may
15 include pins (e.g. input pins) that couple the multicore processor 21 to each voltage regulator of multiple individual voltage regulators or multiple individual voltage regulator components of the external voltage regulator. The external voltage regulator may be controlled by circuitry (e.g., the PCU) of the multicore processor 21 to provide, over the pins, voltages at least one of which is different than the manufacturing fused voltages.
20 The component 21 may also include the controlling circuitry, such as a PCU and code, such as microcode and/or pcode, to determine a voltage regulator setting for the external voltage regulator.

FIG. 2 illustrates example operations that may be performed by the system of FIG. 1, according to various embodiments.

25 In block 201, the system 100 may access a plurality of embedded values correspondingly associated with a plurality of cores of the multicore processor 21. The access may occur at a first time.

In block 202, the system 100 may provide the core voltages to the plurality of cores. The core voltages may correspond to the default voltages. The system 100 may
30 provide the core voltages by a control processor to read the plurality of embedded values and signal an integrated voltage regulator, such as a Fully Integrated Voltage Regulator (FIVR) to provide the core voltages. In another example, the system 100 may provide the core voltages by a component, such as BIOS, to allow an external voltage regulator to provide the core voltages.

In block 203, the system 100 may identify a new core voltage that is different than a corresponding one of the provided core voltages responsive to receiving an override selection. The override selection may be a manually determined override selection (by a system administrator), or otherwise determined override selection, for instance by
5 software such as a tuning application, BIOS, an operating system, or the like, or combinations thereof.

In block 204, the system 100 may provide the new core voltage to a corresponding one of the cores of the plurality of cores. The system 100 may provide the new core voltage at a second time that is later than the first time.

10 FIG. 3 illustrates an example of a system that may include a PCU 253 and an integrated voltage regulator (FIVR 255), according to various embodiments. In the system 200, the multicore processor 21 may include code 254, e.g., microcode and/or pcode) of a PCU 253 to control the FIVR 255 of the multicore processor 21.

The code 254 may recognize an external selection 215 to individually override
15 fused voltage(s) corresponding to the cores 99. In an example, the code 215 may utilize a protocol of a messaging interface or other interface to recognize the external selection 215.

The code 254 may be control the FIVR 255 to cause the FIVR 255 to provide Vcores 257 to the cores 99 responsive to receiving the external selection 215. For example if the FIVR 255 is already providing a voltage corresponding to a respective one
20 of a plurality of embedded values 22 of the memory 23, the FIVR 255 may change at least one of the provided voltages based on the control from the PCU 253. The respective core(s) of the cores 99 may receive the new core voltage that is different than the previously provided voltage.

FIG. 4 illustrates example an example process that may be used in the example
25 system of FIG. 3, according to various embodiments.

In block 301, the system 200 may be powered on (or cold reset). In block 302, the PCU 253 may read fuse values 22 for the core voltages of the memory 23 and may configure accordingly.

In block 303, the system 200 may be operating via BIOS/EFI (extensive firmware
30 interface) or an operating system. In block 304, a software automation or a system administer may determine a new voltage for at least one individual core. The code 254 may recognize a request for the new voltage using the protocol.

In block 305, the system 200 may override the corresponding fused voltage(s), e.g., the PCU 253 may control the FIVR 255 to cause the new core voltage(s) to be provided to

the appropriate one(s) of the cores 99. In block 306, the system 200 may output an indication to BIOS, an application, and/or the operating system, that the modification setting (e.g., a tuning or overclocking setting for the new core voltage) was granted, e.g., granted by the PCU 253. The process may be partially repeated (the control processor of
5 the multicore processor may poll for a next request) as shown by the return arrow for a next new voltage (also may be determined by a software automation or a system administer).

In an example, a six-core multicore processor that is capable of operating two of its cores at higher frequencies with 1.40V, may include a read only memory storing the
10 voltages 1.3V, 1.35V, 1.25V, 1.35V, 1.35V, and 1.25V for core 0, core 1, core 2, core 3, core 4, and core 5, respectively, is provided. A system administrator may, accepting the associated tradeoffs, configure these two cores at 1.40V operation, to attempt to operate the cores at voltages 1.3V, 1.35V, 1.40V, 1.35V, 1.35V, and 1.40V for core 0, core 1, core 2, core 3, core 4, and core 5, respectively. As such, cores 2 and 5 may be configured to a
15 higher frequency without the need of changing the voltage of other cores.

FIG. 5 illustrates an example computing device that may employ the apparatuses and/or methods described herein, according to various embodiments.

Example computing device 500 may employ the apparatuses and/or methods described herein, in accordance with various embodiments. As shown, computing device
20 500 may include a number of components, such as one or more processor(s) 504 (one shown) and at least one communication chip 506.

In various embodiments, the one or more processor(s) 504 each may include one or more processor cores. At least one of the one or more processor(s) 504 may be a multicore processor SoC of FIG. 1 or 3. In various embodiments, the at least one
25 communication chip 506 may be physically and electrically coupled to the one or more processor(s) 504. In further implementations, the communication chip 506 may be part of the one or more processor(s) 504. In various embodiments, computing device 500 may include printed circuit board (PCB) 502. For these embodiments, the one or more processor(s) 504 and communication chip 506 may be disposed thereon. In
30 alternate embodiments, the various components may be coupled without the employment of PCB 502.

Depending on its applications, computing device 500 may include other components that may or may not be physically and electrically coupled to the PCB 502. These other components include, but are not limited to, a memory controller (not

shown), volatile memory (e.g., dynamic random access memory (DRAM) 520), non-volatile memory such as read only memory (ROM) 524, flash memory 522, an I/O controller (not shown), a digital signal processor (not shown), a crypto processor (not shown), a graphics processor 530, one or more antenna 528, a display (not shown), a touch
5 screen display 532, a touch screen controller 546, a battery 536, an audio codec (not shown), a video codec (not shown), a global positioning system (GPS) device 540, a compass 542, an accelerometer (not shown), a gyroscope (not shown), a speaker 550, a camera 552, and a mass storage device (such as hard disk drive, a solid state drive, compact disk (CD), digital versatile disk (DVD)) (not shown), and so forth.

10 In some embodiments, the one or more processor(s) 504, flash memory 522, and/or a storage device (not shown) may include associated firmware (not shown) storing programming instructions configured to enable computing device 500, in response to execution of the programming instructions by one or more processor(s) 504, to practice all or selected aspects of the methods described herein. For example, the programming
15 instructions may implement the earlier control processor, e.g., PCU, with references to the respective ones of Figures 1-4. In various embodiments, these aspects may additionally or alternatively be implemented using hardware separate from the one or more processor(s) 504, flash memory 512, or storage device 511. For example, the alternate hardware may include the earlier described control processor equipped with code, e.g.,
20 microcode and/or pcode, to perform the operations earlier described with references to the respective ones of Figures 1-4.

The communication chips 506 may enable wired and/or wireless communications for the transfer of data to and from the computing device 500. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques,
25 communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 506 may implement any of a number of wireless standards or protocols, including but not limited to IEEE 702.20, Long Term Evolution (LTE), LTE
30 Advanced (LTE-A), General Packet Radio Service (GPRS), Evolution Data Optimized (Ev-DO), Evolved High Speed Packet Access (HSPA+), Evolved High Speed Downlink Packet Access (HSDPA+), Evolved High Speed Uplink Packet Access (HSUPA+), Global System for Mobile Communications (GSM), Enhanced Data rates for GSM Evolution (EDGE), Code Division Multiple Access (CDMA),

Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Worldwide Interoperability for Microwave Access (WiMAX), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 5G, 5G, and beyond. The computing device 500 may include a plurality
5 of communication chips 506. For instance, a first communication chip 506 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth, and a second communication chip 506 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

In various implementations, the computing device 500 may be a laptop, a netbook,
10 a notebook, an ultrabook, a smartphone, a computing tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit (e.g., a gaming console or automotive entertainment unit), a digital camera, an appliance, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be
15 any other electronic device that processes data.

Any combination of one or more computer usable or computer readable medium(s) may be utilized. The computer-usable or computer-readable medium may be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples
20 (a non- exhaustive list) of the computer-readable medium would include the following: an electrical connection having one or more wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), an optical fiber, a portable compact disc read-only memory (CD-ROM), an optical storage device, a transmission media such as
25 those supporting the Internet or an intranet, or a magnetic storage device. Note that the computer- usable or computer-readable medium could even be paper or another suitable medium upon which the program is printed, as the program can be electronically captured, via, for instance, optical scanning of the paper or other medium, then compiled, interpreted, or otherwise processed in a suitable manner, if necessary, and then stored in a
30 computer memory. In the context of this document, a computer-usable or computer-readable medium may be any medium that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer- usable medium may include a propagated data signal with the computer-usable program code embodied therewith, either in baseband or as part

of a carrier wave. The computer usable program code may be transmitted using any appropriate medium, including but not limited to wireless, wireline, optical fiber cable, RF, etc.

Computer program code for carrying out operations of the present disclosure may be written in any combination of one or more programming languages, including an object oriented programming language such as Java, Smalltalk, C++ or the like and conventional procedural programming languages, such as the “C” programming language or similar programming languages. The program code may execute entirely on the user's computer, partly on the user's computer, as a stand-alone software package, partly on the user's computer and partly on a remote computer or entirely on the remote computer or server. In the latter scenario, the remote computer may be connected to the user's computer through any type of network, including a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider).

Examples

Example 1 is an apparatus with per-core voltage adjustability. The apparatus may include a multicore processor SoC (system-on-chip) including: a plurality of architecturally identical cores, wherein a first core of the plurality of architecturally identical cores has a first physical characteristic and a second core of the plurality of architecturally identical cores has a second physical characteristic that is different than the first physical characteristic; and a memory to store a plurality of embedded values correspondingly associated with the plurality of architecturally identical cores, each embedded value to indicate a default voltage for a respective one of the plurality of architecturally identical cores; and a component to provide access from outside the multicore processor SoC to individually set voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages.

Example 2 includes the subject matter of example 1, and the multicore processor SoC further includes: a voltage regulator coupled to the plurality of architecturally identical cores, the voltage regulator to provide the individually set voltages to the plurality of architecturally identical cores.

Example 3 includes the subject matter of any of examples 1-2, and further comprises an external voltage regulator coupled to the multicore processor SoC.

Example 4 includes the subject matter of any of examples 1-3, and the component includes a plurality of pins each corresponding to a respective core of the plurality of

architecturally identical cores.

Example 5 includes the subject matter of any of examples 1-4, and the multicore processor SoC further includes: a power control unit (PCU); and memory having instructions stored thereon that, in response to execution by the PCU, the PCU to perform operations, to: recognize information of a signal received by the multicore processor SoC via the component; and control a voltage regulator of the multicore processor SoC based on the information of the recognition to cause the voltage regulator to provide a first voltage to a first core of the plurality of architecturally identical cores responsive to the recognition of the information, wherein a magnitude of the first voltage is different than a magnitude of a corresponding one of the default voltages.

Example 6 includes the subject matter of any of examples 1-5, and the information of the recognition includes at least one of an actual voltage value corresponding to respective one of the cores, an offset from a respective one of the default voltages, or a voltage value and an offset from the base voltage value.

Example 7 includes the subject matter of any of examples 1-6, and further comprises a module to facilitate a user to access the component to individually set voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages.

Example 8 includes the subject matter of any of examples 1-7, and the module is to message the interface in response to inputs from the user.

Example 9 includes the subject matter of any of examples 1-8, wherein the component includes a control register.

Example 10 includes the subject matter of any of examples 1-10, and further comprises a Basic Input Output System (BIOS) to facilitate a user to access the component to individually set voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages.

Example 11 is a computer-readable medium having instructions of per-core processor programming stored thereon that, in response to execution by a processing device, cause the processing device to perform operations, to: recognize information of a signal received by a multicore processor SoC (system on chip); wherein a first core of the multicore processor SoC has a first physical characteristic and a second core of the multicore processor SoC has a second physical characteristic that is different than the first physical characteristic; and control a voltage regulator of the multicore processor SoC based on the information of the recognition to cause the voltage regulator to selectively

provide a first voltage to a first core of the plurality of cores.

Example 12 includes the subject matter of example 11, wherein the operations are further to selectively provide a second voltage to a second core of the plurality of cores, said selective providing of the second voltage to the second core to be contemporaneous
5 with the selective providing of the first voltage to the first core.

Example 13 includes the subject matter of any of examples 11-12, wherein the second voltage is a default voltage corresponding to said second core.

Example 14 includes the subject matter of any of examples 11-13, wherein: the information of the recognition includes at least one of an actual voltage value
10 corresponding to respective one of the cores, an offset from a respective one of a default voltage corresponding to the first core, or a base voltage value and an offset from the base voltage value; and the first voltage corresponds to at least one of the actual voltage value, the offset from the respective one of the default voltages, or the offset from the base voltage value.

Example 15 is a method for programming a processor voltage on a per-core basis. The method may include accessing a plurality of embedded values correspondingly associated with the plurality of cores of a multicore processor, each embedded value indicating a default voltage for a respective one of the plurality of architecturally identical cores; at a first time, providing core voltages to the plurality of cores, the core voltages
20 corresponding to the default voltages; responsive to receiving an override selection, identifying a new core voltage that is different than the provided core voltages; and at a second time that is later than the first time, providing the new core voltage to one of the cores of the plurality of cores.

Example 16 includes the subject matter of example 15, and at the second time, providing a core voltage of the core voltages to a different one of the cores of the plurality of cores.
25

Example 17 includes the subject matter of any of examples 15-16, and at the second time, providing a different new core voltage to a different one of the cores of the plurality of cores.

Example 18 includes the subject matter of any of examples 15-17, and the override selection includes an overvolt command.
30

Example 19 includes the subject matter of any of examples 15-17, and wherein the override selection includes an undervolt command.

Example 20 includes the subject matter of any of examples 15-19, and the override

selection indicates a voltage range, and wherein the method further comprises: selecting the new core voltage from the voltage range.

Example 21 is an apparatus to program a processor voltage on a per-core basis. The apparatus may include means for accessing a plurality of embedded values
5 correspondingly associated with the plurality of cores of a multicore processor, each embedded value indicating a default voltage for a respective one of the plurality of architecturally identical cores; means for providing core voltages to the plurality of cores at a first time, the core voltages corresponding to the default voltages; means for identifying a new core voltage that is different than the provided core voltages responsive
10 to receiving an override selection; and means for providing the new core voltage to one of the cores of the plurality of cores at a second time that is later than the first time.

Example 22 includes the subject matter of example 21, and means for providing a core voltage of the core voltages to a different one of the cores of the plurality of cores at the second time.

15 Example 23 includes the subject matter of any of examples 21-22, and means for providing a different new core voltage to a different one of the cores of the plurality of cores at the second time.

Example 24 includes the subject matter of any of examples 21-23, and the override selection includes an overvolt command.

20 Example 25 includes the subject matter of any of examples 21-23, and the override selection includes an undervolt command.

Example 26 includes the subject matter of any of examples 21-25, and the override selection indicates a voltage range, and the apparatus may include means for selecting the new core voltage from the voltage range.

Claims

What is claimed is:

1. An apparatus with per-core voltage adjustability, the apparatus comprising:
a multicore processor SoC (system-on-chip) including:
 - 5 a plurality of architecturally identical cores, wherein a first core of the plurality of architecturally identical cores has a first physical characteristic and a second core of the plurality of architecturally identical cores has a second physical characteristic that is different than the first physical characteristic; and
 - a memory to store a plurality of embedded values correspondingly
 - 10 associated with the plurality of architecturally identical cores, each embedded value to indicate a default voltage for a respective one of the plurality of architecturally identical cores; and
 - a component to provide access from outside the multicore processor SoC to individually set voltages of the plurality of architecturally identical cores to values
 - 15 that are different than the values of the default voltages.
2. The apparatus of claim 1, wherein the multicore processor SoC further includes:
a voltage regulator coupled to the plurality of architecturally identical cores, the voltage regulator to provide the individually set voltages to the plurality of architecturally
- 20 identical cores.
3. The apparatus of claim 1, further comprising an external voltage regulator coupled to the multicore processor SoC.
4. The apparatus of claim 3, wherein the component includes a plurality of pins each corresponding to a respective core of the plurality of architecturally identical
- 25 cores.
5. The apparatus of claim 1, wherein the multicore processor SoC further includes:
a power control unit (PCU); and
memory having instructions stored thereon that, in response to execution by the
- 30 PCU, the PCU to perform operations, to:
recognize information of a signal received by the multicore processor SoC via the component; and
control a voltage regulator of the multicore processor SoC based on the information of the recognition to cause the voltage regulator to provide a first

voltage to a first core of the plurality of architecturally identical cores responsive to the recognition of the information, wherein a magnitude of the first voltage is different than a magnitude of a corresponding one of the default voltages.

6. The apparatus of claim 5, wherein the information of the recognition
5 includes at least one of an actual voltage value corresponding to respective one of the cores, an offset from a respective one of the default voltages, or a voltage value and an offset from the base voltage value.

7. The apparatus of claim 1, further comprising a module to facilitate a user to
10 access the component to individually set voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages.

8. The apparatus of claim 7, wherein the module is to message the interface in response to inputs from the user.

9. The apparatus of any of claims 1-8, wherein the component includes a control register.

15 10. The apparatus of any of claims 1-8, further comprising a Basic Input Output System (BIOS) to facilitate a user to access the component to individually set voltages of the plurality of architecturally identical cores to values that are different than the values of the default voltages.

20 11. An apparatus for programming a processor voltage on a per-core basis, the apparatus comprising:

means for recognizing information of a signal received by a multicore processor SoC (system on chip);

25 wherein a first core of the multicore processor SoC has a first physical characteristic and a second core of the multicore processor SoC has a second physical characteristic that is different than the first physical characteristic; and

means for controlling a voltage regulator of the multicore processor SoC based on the information of the recognition to cause the voltage regulator to selectively provide a first voltage to a first core of the plurality of cores.

30 12. The apparatus of claim 11, further comprising means for selectively providing a second voltage to a second core of the plurality of cores, wherein said selective providing of the second voltage to the second core is contemporaneous with the selective providing of the first voltage to the first core.

13. The apparatus of claim 12, wherein the second voltage is a default voltage corresponding to said second core.

14. The apparatus of any of claims 11-13, wherein:

the information of the recognition includes at least one of an actual voltage value corresponding to respective one of the cores, an offset from a respective one of a default voltage corresponding to the first core, or a base voltage value and an offset from the base voltage value; and

the first voltage corresponds to at least one of the actual voltage value, the offset from the respective one of the default voltages, or the offset from the base voltage value.

15. A method to program a processor voltage on a per-core basis, the method comprising:

10 accessing a plurality of embedded values correspondingly associated with the plurality of cores of a multicore processor, each embedded value indicating a default voltage for a respective one of the plurality of architecturally identical cores;

at a first time, providing core voltages to the plurality of cores, the core voltages corresponding to the default voltages;

15 responsive to receiving an override selection, identifying a new core voltage that is different than the provided core voltages; and

at a second time that is later than the first time, providing the new core voltage to one of the cores of the plurality of cores.

16. The method of claim 15, further comprising:

20 at the second time, providing a different new core voltage to a different one of the cores of the plurality of cores.

17. The method of claim 15, wherein the override selection includes an overvolt command.

25 18. The method of claim 15, wherein the override selection includes an undervolt command.

19. The method of claim 15, wherein the override selection indicates a voltage range, and wherein the method further comprises:

selecting the new core voltage from the voltage range.

20. The method of any of claims 15-19, further comprising:

30 at the second time, providing a core voltage of the core voltages to a different one of the cores of the plurality of cores.

21. An apparatus to program a processor voltage on a per-core basis, the apparatus comprising:

means for accessing a plurality of embedded values correspondingly associated

with the plurality of cores of a multicore processor, each embedded value indicating a default voltage for a respective one of the plurality of architecturally identical cores;

means for providing core voltages to the plurality of cores at a first time, the core voltages corresponding to the default voltages;

5 means for identifying a new core voltage that is different than the provided core voltages responsive to receiving an override selection; and

means for providing the new core voltage to one of the cores of the plurality of cores at a second time that is later than the first time.

22. The apparatus of claim 21, further comprising:

10 means for providing a different new core voltage to a different one of the cores of the plurality of cores at the second time.

23. The apparatus of claim 21, wherein the override selection includes an overvolt command or an undervolt command.

15 24. The apparatus of claim 21, wherein the override selection indicates a voltage range, and wherein the apparatus further comprises:

means for selecting the new core voltage from the voltage range.

25. The apparatus of any of claims 21-24, further comprising:
means for providing a core voltage of the core voltages to a different one of the cores of the plurality of cores at the second time.

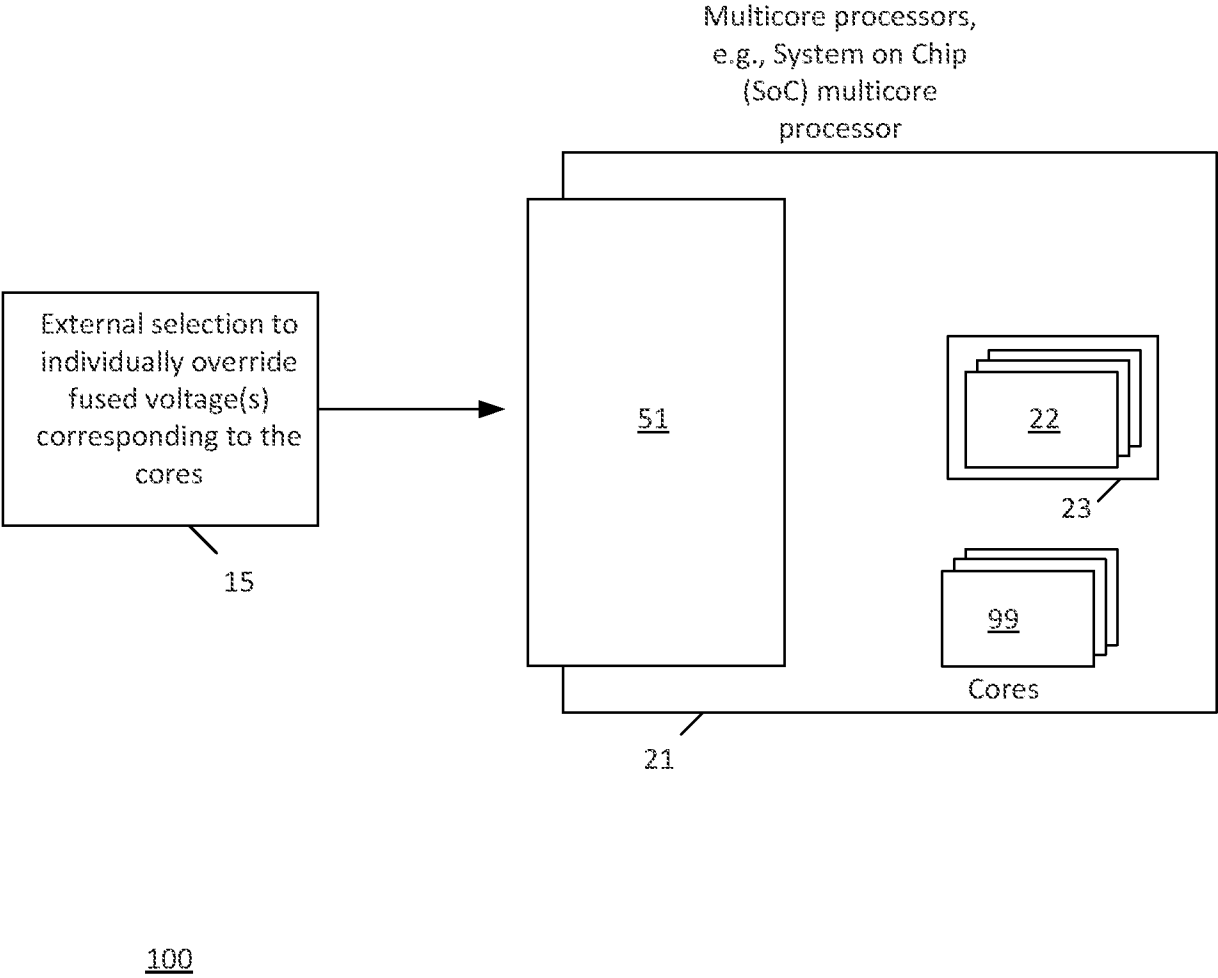


FIG. 1

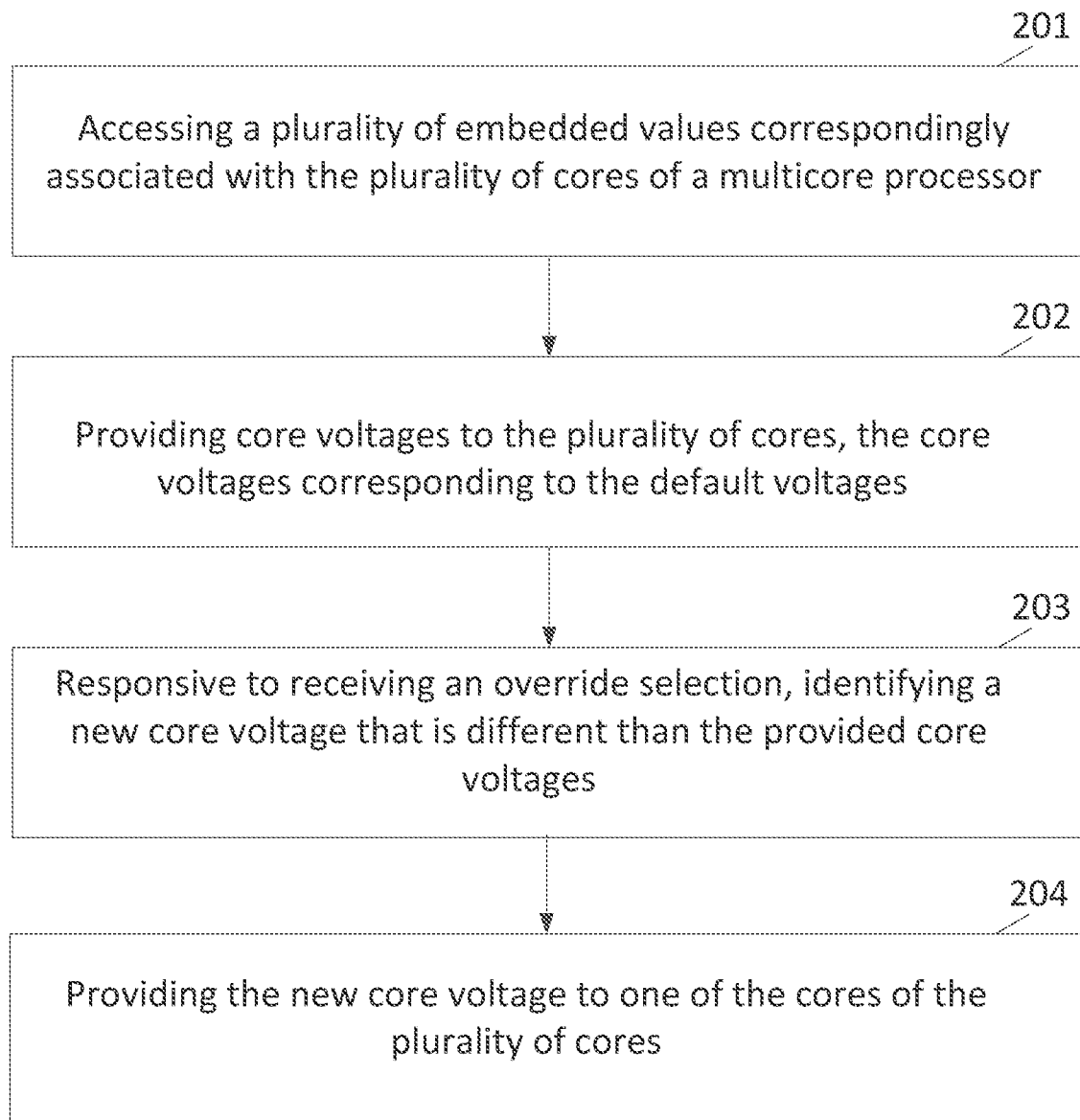


FIG. 2

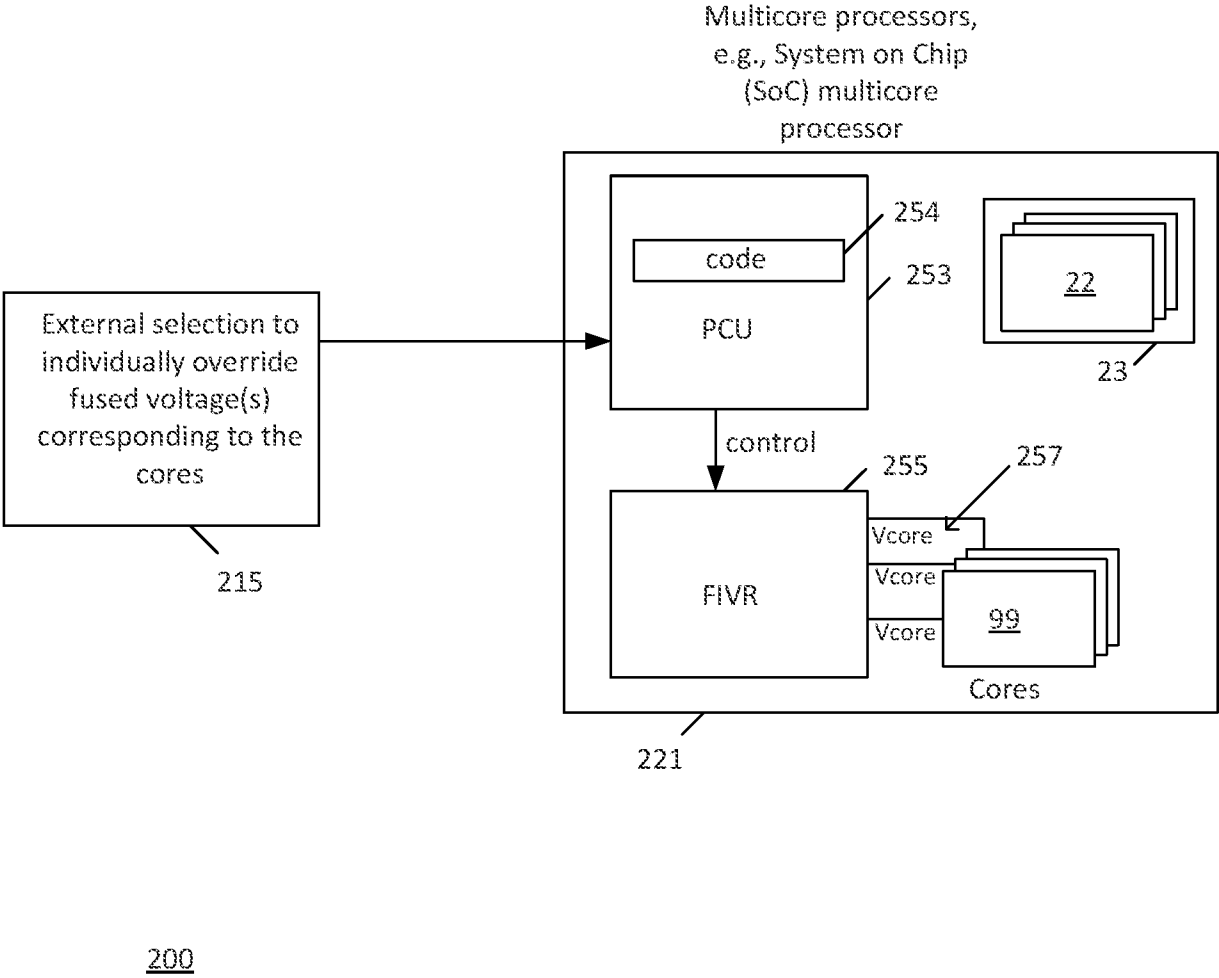


FIG. 3

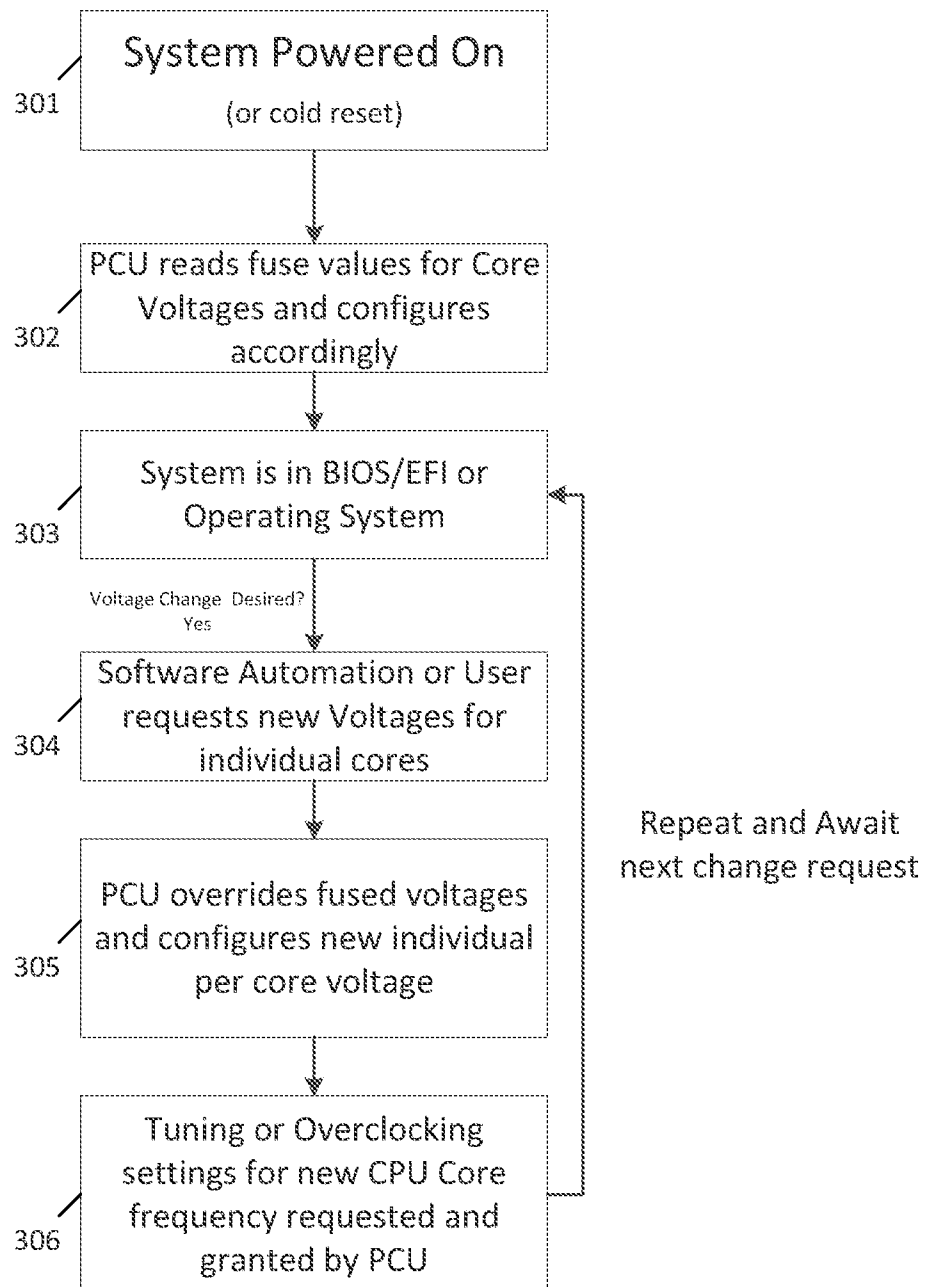


FIG. 4

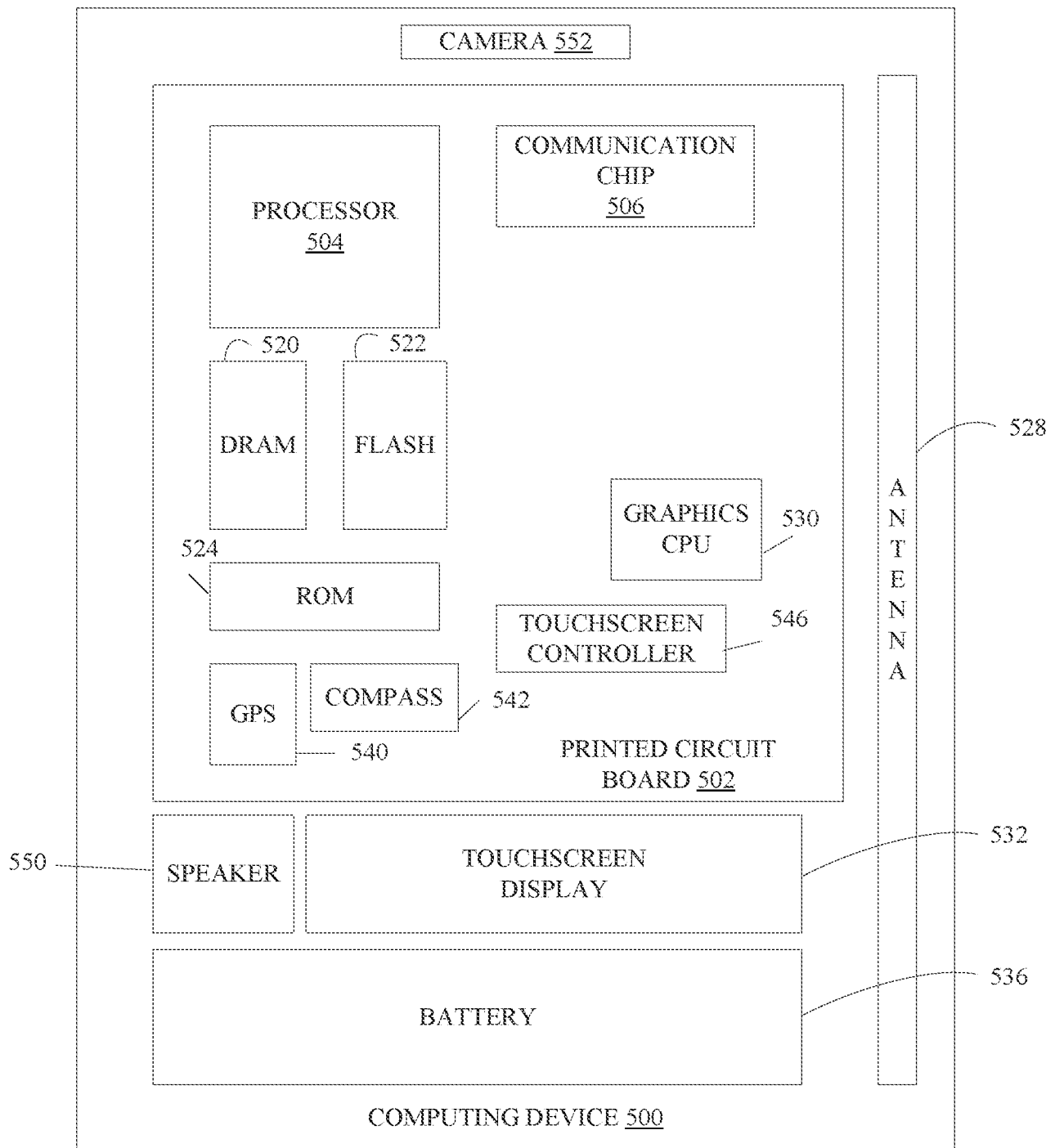


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/067837**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/32(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/32; G06F 9/02; G06F 1/20; G06F 1/00; G06F 15/177; G06F 9/318

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multicore, SoC, physical characteristic, voltage, default, individually, power control unit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009-0187777 A1 (MICHAEL T. CLARK) 23 July 2009 See paragraphs [0007]-[0009], [0013]-[0026]; claims 16-17, 20; and figures 1-2.	1-25
Y	US 2014-0136823 A1 (DANIEL J. RAGLAND et al.) 15 May 2014 See paragraphs [0017], [0022], [0038]; claims 1, 8; and figures 3-5.	1-25
A	US 2012-0166764 A1 (G. GLENN HENRY et al.) 28 June 2012 See paragraphs [0050]-[0066]; and figure 3.	1-25
A	WO 2009-114141 A1 (ADVANCED MICRO DEVICES, INC.) 17 September 2009 See paragraphs [0031]-[0036]; and figures 3-4.	1-25
A	US 2015-0286265 A1 (INTEL CORPORATION) 08 October 2015 See paragraphs [0015]-[0017]; and figure 6.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

10 April 2017 (10.04.2017)

Date of mailing of the international search report

11 April 2017 (11.04.2017)

Name and mailing address of the ISA/KR

International Application Division

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189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

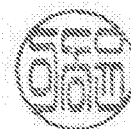


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/067837

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0187777 A1	23/07/2009	CN 101233475 A	30/07/2008
		CN 101233475 B	18/05/2011
		DE 112006002056 T5	10/07/2008
		GB 2442919 A	16/04/2008
		GB 2442919 B	10/03/2010
		JP 2009-503728 A	29/01/2009
		JP 4937260 B2	23/05/2012
		KR 10-1310044 B1	17/09/2013
		KR 10-2008-0038389 A	06/05/2008
		TW I412993 B	21/10/2013
		US 2007-0033425 A1	08/02/2007
		US 7490254 B2	10/02/2009
		WO 2007-019003 A2	15/02/2007
		WO 2007-019003 A3	18/05/2007
US 2014-0136823 A1	15/05/2014	None	
US 2012-0166764 A1	28/06/2012	CN 102520912 A	27/06/2012
		CN 102520912 B	07/01/2015
		CN 102521002 A	27/06/2012
		CN 102521002 B	28/10/2015
		CN 102521191 A	27/06/2012
		CN 102521191 B	21/01/2015
		CN 102521207 A	27/06/2012
		CN 102521207 B	30/09/2015
		CN 102541237 A	04/07/2012
		CN 102541237 B	17/09/2014
		CN 102543862 A	04/07/2012
		CN 102543862 B	10/12/2014
		CN 103955265 A	30/07/2014
		CN 104156055 A	19/11/2014
		CN 104503941 A	08/04/2015
		CN 105183134 A	23/12/2015
		EP 2469377 A2	27/06/2012
		EP 2469377 A3	02/11/2016
		TW 201234271 A	16/08/2012
		TW 201430553 A	01/08/2014
		TW I506559 B	01/11/2015
		TW I531896 B	01/05/2016
		US 2012-0161328 A1	28/06/2012
		US 2012-0166763 A1	28/06/2012
		US 2012-0166832 A1	28/06/2012
		US 2012-0166837 A1	28/06/2012
		US 2012-0166845 A1	28/06/2012
		US 2012-0239847 A1	20/09/2012
		US 2015-0046680 A1	12/02/2015
		US 2016-0179177 A1	23/06/2016
		US 2016-0209897 A1	21/07/2016
		US 2016-0209913 A1	21/07/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/067837

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 8631256 B2	14/01/2014
		US 8635476 B2	21/01/2014
		US 8637212 B2	28/01/2014
		US 8782451 B2	15/07/2014
		US 8930676 B2	06/01/2015
		US 8972707 B2	03/03/2015
		US 9367497 B2	14/06/2016
		US 9460038 B2	04/10/2016
WO 2009-114141 A1	17/09/2009	TW 200945188 A	01/11/2009
		US 2009-0235108 A1	17/09/2009
US 2015-0286265 A1	08/10/2015	CN 101403944 A	08/04/2009
		CN 101403944 B	25/04/2012
		CN 102707786 A	03/10/2012
		CN 102707786 B	20/01/2016
		DE 102007051841 A1	21/05/2008
		DE 102007051841 B4	05/09/2013
		GB 2444597 A	11/06/2008
		GB 2444597 B	22/12/2010
		JP 2008-117397 A	22/05/2008
		KR 10-0988396 B1	18/10/2010
		KR 10-1297481 B1	16/08/2013
		KR 10-2008-0039824 A	07/05/2008
		KR 10-2010-0075806 A	05/07/2010
		US 2008-0104425 A1	01/05/2008
		US 2009-0313489 A1	17/12/2009
		US 2011-0022865 A1	27/01/2011
		US 2011-0191607 A1	04/08/2011
		US 2012-0226926 A1	06/09/2012
		US 2012-0239946 A1	20/09/2012
		US 7949887 B2	24/05/2011
		US 8069358 B2	29/11/2011
		US 8856568 B2	07/10/2014
		US 8996899 B2	31/03/2015
		US 9021279 B2	28/04/2015
		US 9037885 B2	19/05/2015