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(54) **Title**: BULK FINFET WITH UNIFORM HEIGHT AND BOTTOM ISOLATION

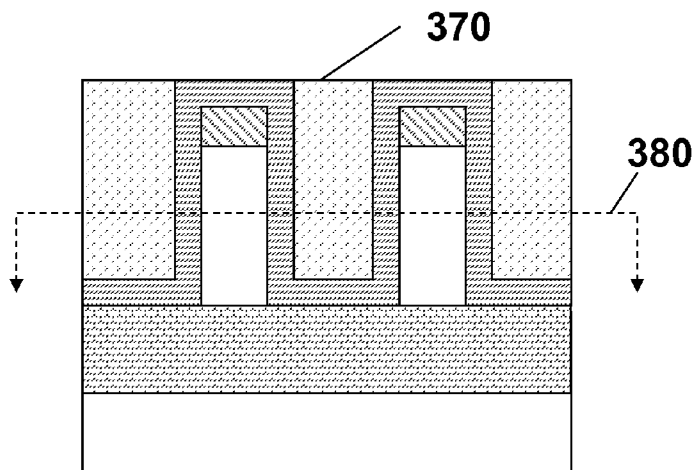

Fig. 3i

(57) **Abstract**: A fin Field Effect Transistor (finFET), an array of finFETs, and methods of production thereof. The finFETs are provided on an insulating region, which may optionally contain dopants. Further, the finFETs are optionally capped with a pad. The finFETs provided in an array are of uniform height.

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BULK FINFET WITH UNIFORM HEIGHT AND BOTTOM ISOLATION

FIELD OF THE DISCLOSURE

5 The present disclosure relates to methods of forming and substrates comprising fin Field Effect Transistors (finFETs) on semiconductor substrates. In particular, the present disclosure relates to finFETs having uniform fin height and isolation at the bottom of the fin.

10 ## BACKGROUND

In recent years, finFETs have established themselves as viable alternatives to traditional Field Effect Transistors (FETs) in semiconducting devices. A finFET is a double gate FET in which the transistor channel is a semiconducting "fin." The gate
15 dielectric and gate are positioned around the fin such that current flows down the channel on the two sides of the fin.

However, the finFETs of the related art on a bulk semiconductor substrate (referred to as "bulk finFET" hereinafter) have the disadvantage that the channel region,
20 i.e., the fin, is not electrically isolated from the rest of substrate. As a result, source/drain leakage of currents due to the channel effect may occur.

Additionally, bulk finFET arrays of the related art have to date not been provided with a uniform height. In particular, the finFETs in arrays have varying heights because
25 varying amounts of substrate are removed between adjacent finFETs within the same array at different points on the array due to variations in local etching rates. Moreover, even between two adjacent finFETS, more substrate may be etched at a position close to the first finFET and less at a position close to the second finFET, or vice versa.

30

SUMMARY OF THE DISCLOSURE

Disclosed herein are methods of forming finFETs and substrates comprising finFETs with uniform fin height and isolation at the bottom of the fin. In particular, semiconductor structures comprising a substrate and a fin Field Effect Transistor (finFET) on the substrate are disclosed, wherein the finFET is insulated from the substrate by an insulating region, and wherein the insulating region comprises a dopant selected from the group consisting of aluminum, arsenic, boron, gallium, indium, phosphorous, antimony, sulfur, selenium, germanium, carbon, argon, xenon, and fluorine, or a combination thereof.

Further disclosed is a semiconductor structure comprising a plurality of fin Field Effect Transistors (finFETs) on a substrate, wherein the plurality of finFETs are of a uniform height, and wherein the plurality of finFETs is insulated from the substrate by an insulating region, and wherein the insulating region comprises a dopant selected from the group consisting of aluminum, arsenic, boron, gallium, indium, phosphorous, antimony, sulfur, selenium, germanium, carbon, argon, xenon, and fluorine, or a combination thereof.

Moreover, a method of forming a fin Field Effect Transistor (finFET) on a substrate is disclosed, wherein the method comprises providing a substrate, forming an etch stop layer within the substrate, etching a surface of the substrate up to or into the etch stop layer to form a fin, and converting the etch stop layer into an insulating layer.

In addition, a method of forming a fin Field Effect Transistor (finFET) on a substrate is disclosed, wherein the method comprises providing a substrate, forming an etch stop layer on the substrate, forming a semiconductor layer on the etch stop layer, forming a fin by removing a portion of the semiconductor layer and a portion of the etch stop layer, and converting a remaining portion of the etch stop layer and a portion of the substrate into an insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a related art semiconductor structure of pads 110 on a semiconductor substrate 100.

5

Fig. 2 shows a related art semiconductor structure of finFETs 220 on a semiconductor substrate 200.

Figs. 3a to 3j show a first method of producing a finFET semiconductor structure.

10

Figs. 3a shows a semiconductor substrate 300.

Fig. 3b shows buried etch stop layer 310 being formed within semiconductor substrate 300.

15

Fig. 3c shows pad layer 320 on the semiconductor substrate 300.

Fig. 3d shows finFETs 330 having been formed on insulation layer 310 after removal of a portion of semiconductor substrate 300 and a portion of pad layer 320.

20

Fig. 3e shows the formation of sidewall spacer 340 on the finFETs.

Fig. 3f shows the conversion of etch stop layer 310 into insulating layer 350.

25 Fig. 3g shows the semiconductor structure after the removal of sidewall spacer 340.

Fig. 3h shows gate dielectric 360 being provided on the finFETs.

30 Fig. 3i shows gate electrodes 370 being provided on gate dielectric 360.

Fig. 3j shows a top down view of the semiconductor structure along the direction of dashed double arrow 380 depicted in Fig. 3i. Further, the semiconductor structure comprises source region 390 and drain region 395.

5 Figs. 4a to 4k show a second method of producing a finFET semiconductor structure.

Fig. 4a shows semiconductor substrate 400.

10 Fig. 4b shows etch stop layer 410 being provided on semiconductor substrate 400.

Fig. 4c shows a semiconductor layer 420 being provided on etch stop layer 410.

Fig. 4d shows pad layer 430 being provided on semiconductor layer 420.

15

Fig. 4e shows finFET 440 having been formed on insulation layer etch stop layer 420 after removal of a portion of semiconductor layer 430 and a portion of pad layer 430.

Fig. 4f shows the formation of sidewall spacer 450 on the finFET 440.

20

Fig. 4g shows the conversion of etch stop layer 410 into insulating layer 460.

Fig. 4h shows the semiconductor structure after the removal of sidewall spacer 450.

25

Fig. 4i shows gate dielectric 470 being provided on finFET 440.

Fig. 4j shows gate electrodes 480 being provided on gate dielectric 470.

Fig. 4kj shows a top down view of the semiconductor structure along the direction of dashed double arrow 485 depicted in Fig. 4j. Further, the semiconductor structure comprises source region 490 and drain region 495.

5 Figs. 5a to 5f show a third method of producing a finFET semiconductor structure.

Fig. 5a shows a semiconductor structure comprising finFET 540 with sidewall spacer 550 and pad 530 on etch stop layer 510, which, in turn, is provided on substrate 10 500. finFET 540 is composed of semiconductor 520 and pad 530. This semiconductor structure may be obtained through the steps performed in Figs. 3a to 3e or Figs. 4a to 4f.

Fig. 5b shows the removal of a portion of etch stop layer 510 by complete removal of the etch stop layer 510 between two adjacent finFETs to substrate 500.

15

Fig. 5c shows the conversion of the remaining portions of etch stop layer 510 and of a portion of substrate 500 into insulation region 570 having a non-planar interface with unconverted substrate 500.

20 Fig. 5d shows the semiconductor structure after the removal of sidewall spacer 550.

Fig. 5e shows gate dielectric 580 being provided on finFET 540.

25 Fig. 5f shows gate electrodes 590 being provided on gate dielectric 580.

DESCRIPTION OF THE BEST AND VARIOUS EMBODIMENTS

The foregoing and other objects, aspects and advantages will be better understood 30 from the following detailed description of the best and various embodiments. Throughout

the various views and illustrative embodiments of the present disclosure, like reference numbers are used to designate like elements.

It will be understood that when an element or layer is referred to as being "on" another element or layer, that the elements or layers are abutting each other. While one element or layer may be above another element or layer, "on" is not limited to an element or layer being above, but may be below or on a side to the other element or layer.

In a preferred embodiment, the fin of a finFET has a height of from about 5 nanometers to about 50 nanometers.

In another preferred embodiment, the finFET is selected from the group consisting of Si, SiGe, Ge, and GaAs. Preferably, the finFET is Si. More preferably, the Si is bulk Si.

Typically, the insulating region has a thickness of from about 5 nanometers to about 200 nanometers. Also typically, the fin has a height of from about 10 nanometers to about 50 nanometers. With particularity, the fin has a width of from about 5 nanometers to about 30 nanometers.

In a typical embodiment, the insulating region is silicon dioxide. In another typical embodiment, a bottom region of the insulating region is non-planar.

Typically, the semiconductor structure further comprises a gate dielectric on the fin and a gate conductor on the gate dielectric. Also typically, a spacer is formed on a sidewall of the fin prior to the converting the etch stop layer into an insulating layer.

With particularity, a pad layer is formed on the surface of the substrate prior to the etching the surface, and removing a portion of the pad layer during the etching the surface to form the fin and the substrate comprises performing a reactive ion etching (RIE) to form the fin. Also with particularity, the pad layer is a pad nitride or a pad oxide.

In a preferred embodiment, the spacer is a nitride spacer. Further, also in a preferred embodiment, the etch stop layer within the substrate is a buried oxide layer. In yet another preferred embodiment, the etch stop layer within the substrate is a silicon
5 germanium layer.

In a further preferred embodiment, a pad layer is formed on the semiconductor layer prior to the forming the fin; and the pad layer is patterned.

10 With particularity, a sidewall spacer is formed on the fin prior to the converting the remaining portion and the portion of the substrate and the sidewall spacer is removed after the converting the remaining portion and the portion of the substrate. Also with particularity, the semiconductor layer on the etch stop layer is grown epitaxially.

15 Turning to the drawings, Fig. 1 shows a related art semiconductor structure of pads 110 on a semiconductor substrate 100. The pads are provided using a mask with subsequent etching to form the fins of Fig. 2, which shows a related art semiconductor structure of finFETs 220 on a semiconductor substrate 200. The etching process, however, results in height variations due to a non-uniform progress of the etching
20 between fins.

Figs. 3a to 3j show a first method of producing a finFET semiconductor structure. Specifically, Fig. 3a shows a semiconductor substrate 300, which is provided as the starting point. At the onset, a buried etch stop layer 310 is being formed within
25 semiconductor substrate 300. For example, a tracer, such as aluminum, arsenic, boron, gallium, indium, phosphorous, antimony, sulfur, selenium, germanium, carbon, argon, xenon, fluorine, or any suitable combination thereof is (e.g., by ion implantation) into the substrate 300 to form the etch stop layer 310. The purpose of the tracer is either to indicate an endpoint of the etching process, typically a reactive ion etching to form the
30 find (fin RIE), or to modify the substrate properties to withstand etching to form an etch stopping layer.

Optionally, a thermal annealing process can be performed after implantation to reduce or eliminate any implantation related defects. Thus, an etch stop layer is either a layer will physically stop the etch or the tracer within the etch stop layer will provide an endpoint trace for fin RIE.

5

Fig. 3c shows pad layer 320 on the semiconductor substrate 300. Pad layer 320 is optional; however, the finFETs preferably contain a pad region derived from pad layer 320 in the subsequent etching step. Pad layer 320 is typically a dielectric material, such as, for example, silicon dioxide.

10

Fig. 3d shows finFETs 330 having been formed on insulation layer 310 after removal of a portion of semiconductor substrate 300 and a portion of pad layer 320 in an etching step. The etch stop layer 310 provides a defined endpoint for the etching process, which allows to prepare finFETs of uniform height if a plurality of finFETs is formed.

15

Fig. 3e shows the formation of optional sidewall spacer 340 on the finFETs. The sidewall spacer is provided only temporary to protect the fin during the subsequent conversion process to convert the etch stop layer 310 into an insulating layer 350, for example, by thermal oxidation, as shown in Fig. 3f. The insulating layer 350 allows to
20 electrically insulate the fins from the substrate to increase the device performance.

Subsequently, sidewall spacer 340 is removed, as can be seen in the resulting semiconductor structure of Fig. 3g. To arrive at the final semiconductor structure, gate dielectric 360 is being provided on the finFETs (Fig. 3h) and, thereafter, gate electrode
25 370 is being provided on gate dielectric 360.

Gate dielectric 360 may be selected from materials known in the art. For example, gate dielectric 360 can be chosen from SiO2, SiON, or a high k dielectric having a dielectric constant greater than 4.0, or multilayers thereof. The high k gate dielectric may
30 further include a metal oxide or a mixed metal oxide having a dielectric constant. Some examples of high k gate dielectrics that can be used in the present disclosure include, but

are not limited to: HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, CeO_2, Y_2O_3 or multilayers thereof.

The gate dielectric can be formed by a conventional deposition process such as, for example, CVD, PECVD, ALD, metalorganic chemical vapor deposition (MOCVD), evaporation, reactive sputtering, chemical solution deposition or other like deposition processes. Alternatively, the gate dielectric can be formed by a thermal process. The physical thickness of the gate dielectric may vary, but typically, the gate dielectric has a thickness from about 0.7 to about 100 nm, with a thickness from about 1 to about 7 nm being even more typical.

After forming gate dielectric 360, the gate electrode 370 is formed utilizing a conventional deposition process including, for example, CVD, PECVD, ALD, MOCVD, chemical solution deposition, reactive sputtering, platting, evaporation or other like deposition processes. The gate electrode 370 may be any suitable conductive material, such as, for example, doped polySi, doped SiGe, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multilayers thereof.

Fig. 3j shows a top down view of the semiconductor structure along the direction of dashed double arrow 380 depicted in Fig. 3i. Further, the semiconductor structure comprises source region 390 and drain region 395.

Figs. 4a to 4k show an alternative method of producing a finFET semiconductor structure. Specifically, semiconductor substrate 400 is provided as a starting point for forming a finFET semiconductor structure.

Initially, etch stop layer 410 is being provided on semiconductor substrate 400. Subsequently, a semiconductor layer 420 being provided on etch stop layer 410. Accordingly, semiconductor substrate 400 and semiconductor layer 420 may be from the same material, but may also be different. Afterwards, pad layer 430 is being provided on

semiconductor layer 420. In contrast to the method described above, this method allows to form an etch stop layer by epitaxial growth.

Thereafter, finFET 440 is formed on insulation layer etch stop layer 420 after
5 removal of a portion of semiconductor layer 430 and a portion of pad layer 430 by etching. This method also allows for the etching process to continue until a defined end point has been reached, thereby assuring that the finFETs have uniform height.

Fig. 4f shows the formation of sidewall spacer 450 on the finFET 440. In a
10 subsequent conversion step, etch stop layer 410 is converted into insulating layer 460. The presence of the sidewall spacers and the spatial distance of the fins from the resulting insulating layer avoids diffusion of impurities into the fins and, therefore, increases device performance. After the conversion, sidewall spacer 450 is removed.

15 To finish the final semiconductor structure, gate dielectric 470 is provided on finFET 440, and, thereafter, gate electrodes 480 is provided on gate dielectric 470.

Fig. 4k shows a top down view of the semiconductor structure along the direction of dashed double arrow 485 depicted in Fig. 4j. Further, the semiconductor structure
20 comprises source region 490 and drain region 495.

In Figs. 5a to 5f a third method of producing a finFET semiconductor structure is shown. The starting point is a semiconductor structure comprising finFET 540 with sidewall spacer 550 and pad 530 on etch stop layer 510, which, in turn, is provided on
25 substrate 500. finFET 540 is composed of semiconductor 520 and pad 530. This semiconductor structure may be obtained through the steps performed in Figs. 3a to 3e or Figs. 4a to 4f.

In this case, the removal of a portion of etch stop layer 510 between two adjacent
30 finFETs on substrate 500 is complete, which results in fins having a bottom portion being

made from a different material than the semiconducting channel region in the center of the fin.

Thereafter, a conversion of the remaining portions of etch stop layer 510 and of a portion of substrate 500 into insulation region 570 occurs, which results in a non-planar interface of insulation region 570 and unconverted substrate 500.

Sidewall spacer 550 is not needed in the final structure and removed prior to the provision of gate dielectric 580 being on finFET 540, and, subsequently, gate electrodes 590 on gate dielectric 580.

The embodiments described hereinabove are further intended to explain best modes known of practicing it and to enable others skilled in the art to utilize the disclosure in such, or other, embodiments and with the various modifications required by the particular applications or uses. Accordingly, the description is not intended to limit it to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.

The foregoing description of the disclosure illustrates and describes the present disclosure. Additionally, the disclosure shows and describes only the preferred embodiments but, as mentioned above, it is to be understood that the disclosure is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the concept as expressed herein, commensurate with the above teachings and/or the skill or knowledge of the relevant art.

The term “comprising” (and its grammatical variations) as used herein is used in the inclusive sense of “having” or “including” and not in the exclusive sense of “consisting only of.” The terms “a” and “the” as used herein are understood to encompass the plural as well as the singular.

All publications, patents and patent applications cited in this specification are herein incorporated by reference, and for any and all purpose, as if each individual publication, patent or patent application were specifically and individually indicated to be incorporated by reference. In the case of inconsistencies, the present disclosure will
5 prevail.

What is claimed is:

1. A semiconductor structure comprising:

a substrate, and

a fin Field Effect Transistor (finFET) on the substrate,

wherein the finFET is insulated from the substrate by an insulating region, and wherein the insulating region comprises a tracer selected from the group consisting of aluminum, arsenic, boron, gallium, indium, phosphorous, antimony, sulfur, selenium, fluorine, carbon, germanium, argon, and xenon, or a combination thereof.

2. A semiconductor structure comprising:

a plurality of fin Field Effect Transistors (finFETs) on a substrate,

wherein the plurality of finFETs are of a uniform height, and

wherein the plurality of finFETs is insulated from the substrate by an insulating region, and

wherein the insulating region comprises a tracer selected from the group consisting of aluminum, arsenic, boron, gallium, indium, phosphorous, antimony, sulfur, selenium, fluorine, carbon, germanium, argon, and xenon, or a combination thereof.

3. The semiconductor structure of claim 1, wherein the fin has a height of from about 5 nanometers to about 50 nanometers.

4. The semiconductor structure of claim 1, wherein the finFET is selected from the group consisting of Si, SiGe, Ge, and GaAs.

5. The semiconductor structure of claim 4, wherein the finFET is Si.

6. The semiconductor structure of claim 5, wherein the Si is bulk Si.

7. The semiconductor structure of claim 1, wherein the insulating region has a thickness of from about 5 nanometers to about 200 nanometers.

8. The semiconductor structure of claim 1, wherein the fin has a height of from about 10 nanometers to about 50 nanometers.

9. The semiconductor structure of claim 1, wherein the fin has a width of from about 5 nanometers to about 30 nanometers.

10. The semiconductor structure of claim 1, wherein the insulating region is silicon dioxide.

11. The semiconductor structure of claim 1, wherein a bottom region of the insulating region is non-planar.

12. The semiconductor structure of claim 1, further comprising a gate dielectric on the fin and a gate conductor on the gate dielectric.

13. A method of forming a fin Field Effect Transistor (finFET) on a substrate comprising:

providing a substrate;

forming an etch stop layer within the substrate;

etching a surface of the substrate up to or into the etch stop layer to form a fin; and

converting the etch stop layer into an insulating layer.

14. The method of claim 13, further comprising:

forming a spacer on a sidewall of the fin prior to the converting the etch stop layer into an insulating layer.

15. The method of claim 13, further comprising:

forming a pad layer on the surface of the substrate prior to the etching the surface, and removing a portion of the pad layer during the etching the surface to form the fin and the substrate comprises performing a reactive ion etching (RIE) to form the fin.

16. The method of claim 13, wherein the pad layer is a pad nitride or a pad oxide.

17. The method of claim 13, wherein the spacer is a nitride spacer.

18. The method of claim 13, wherein the etch stop layer within the substrate is a buried oxide layer.

19. The method of claim 13, wherein the etch stop layer within the substrate is a silicon germanium layer.

20. A method of forming a fin Field Effect Transistor (finFET) on a substrate comprising:

providing a substrate;

forming an etch stop layer on the substrate;

forming a semiconductor layer on the etch stop layer;

forming a fin by removing a portion of the semiconductor layer and a portion of the etch stop layer; and

converting a remaining portion of the etch stop layer and a portion of the substrate into an insulating layer.

21. The method of claim 20, further comprising:

forming a pad layer on the semiconductor layer prior to the forming the fin; and

patterning the pad layer.

22. The method of claim 20, further comprising:

forming a sidewall spacer on the fin prior to the converting the remaining portion and the portion of the substrate; and

removing the sidewall spacer after the converting the remaining portion and the portion of the substrate.

23. The method of claim 20, wherein the forming a semiconductor layer on the etch stop layer is grown epitaxially.

Related art

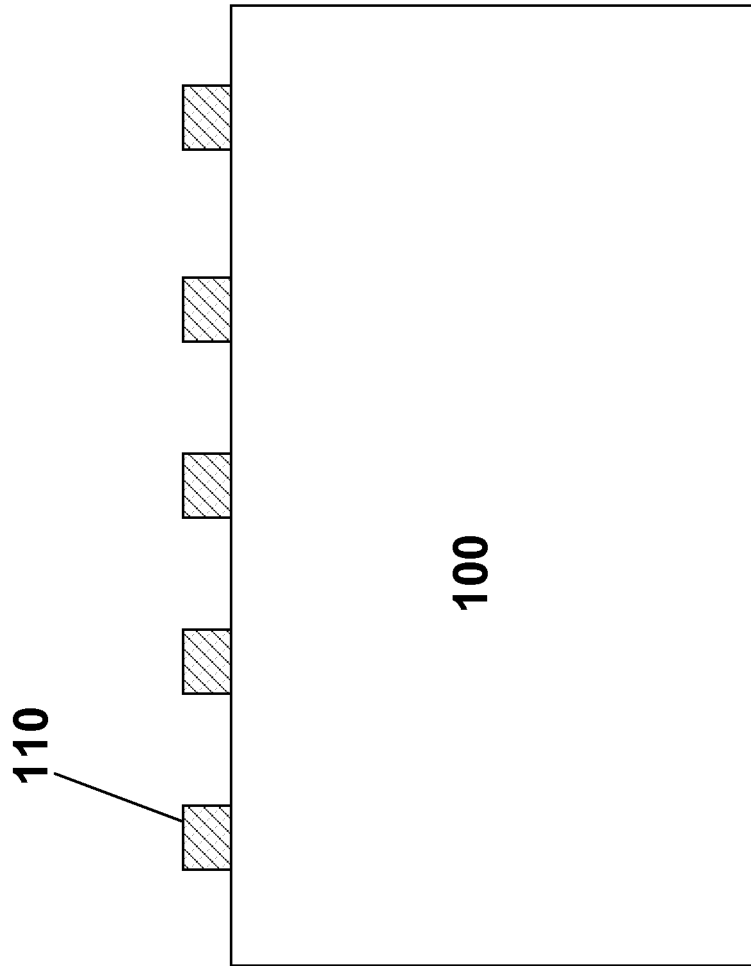

Fig. 1

Related art

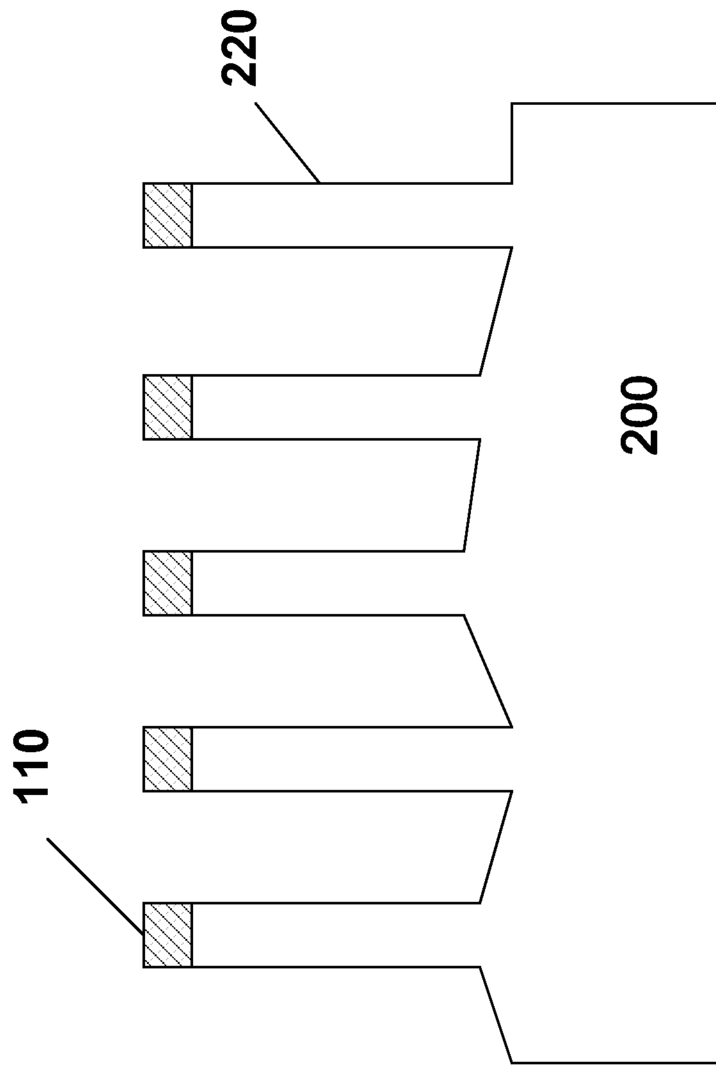

Fig. 2

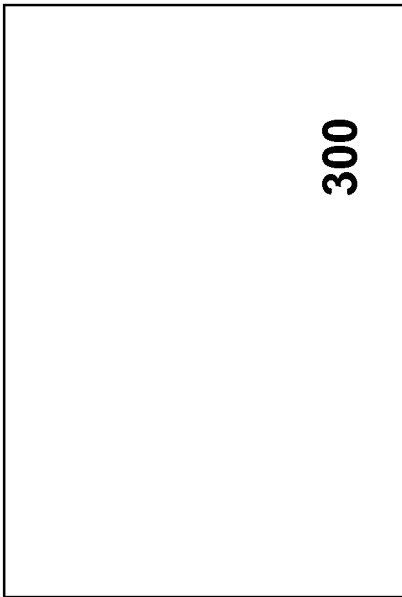

Fig. 3a

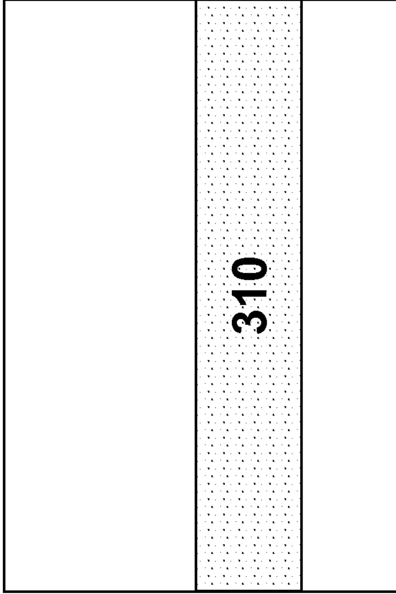

Fig. 3b

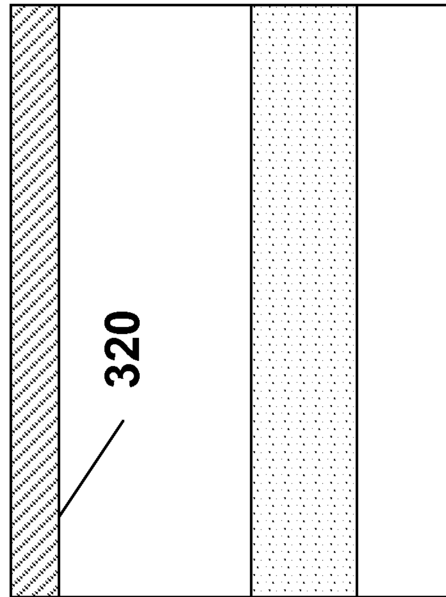

Fig. 3c

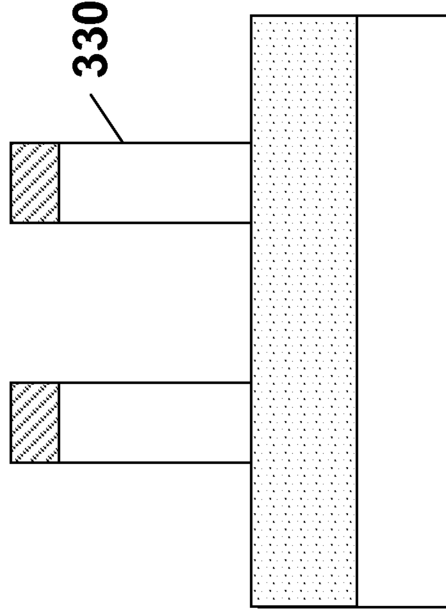

Fig. 3d

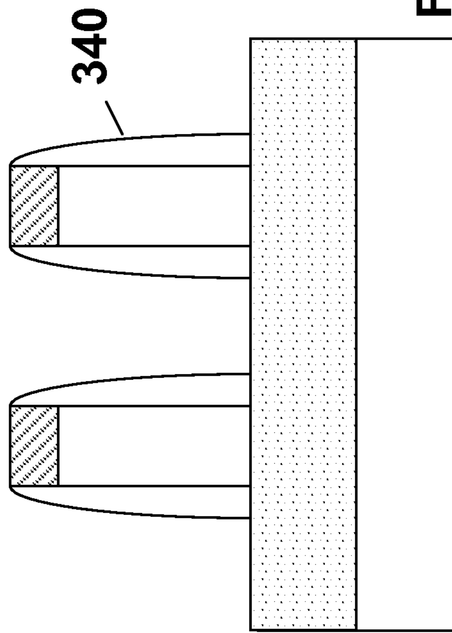

Fig. 3e

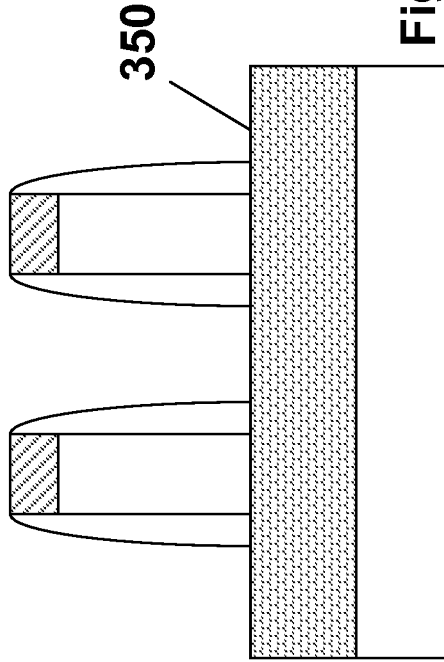

Fig. 3f

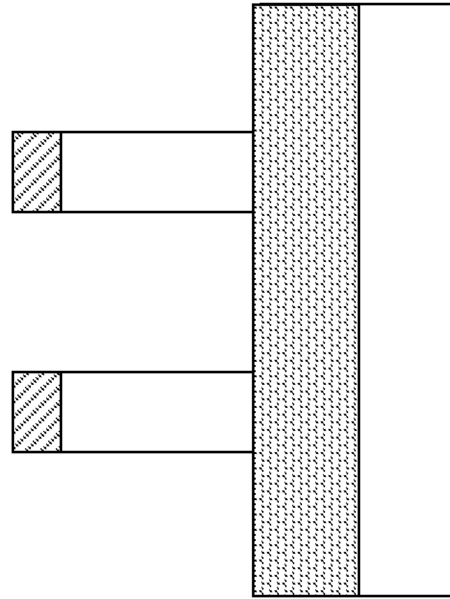

Fig. 3g

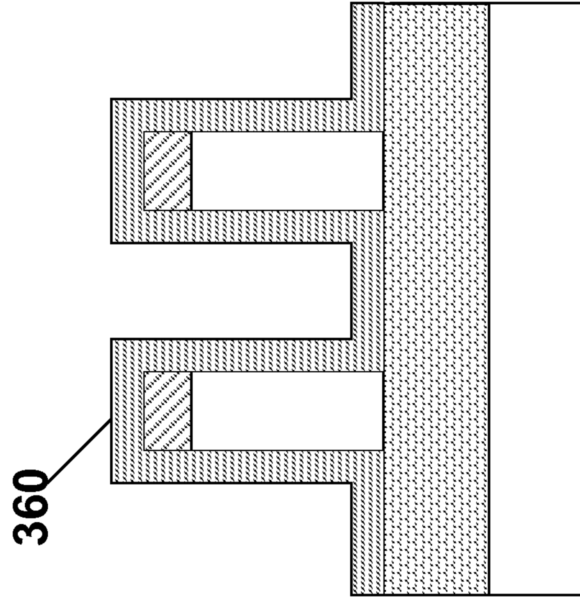

Fig. 3h

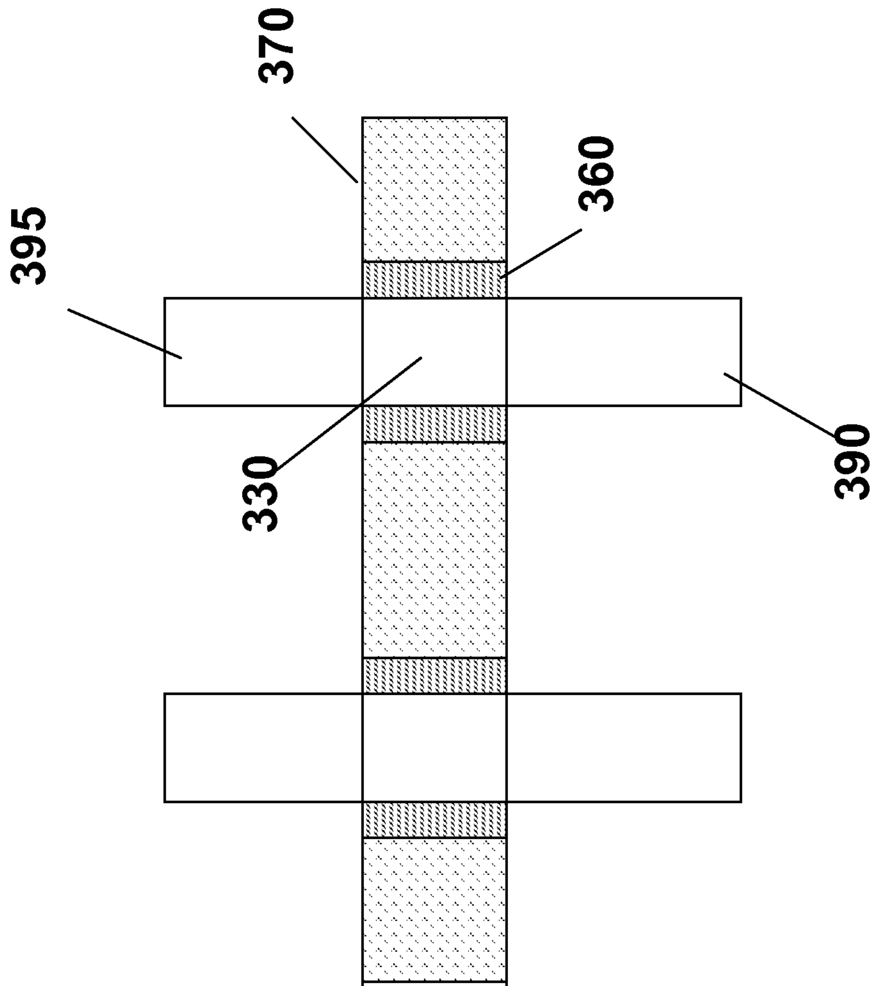

Fig. 3j

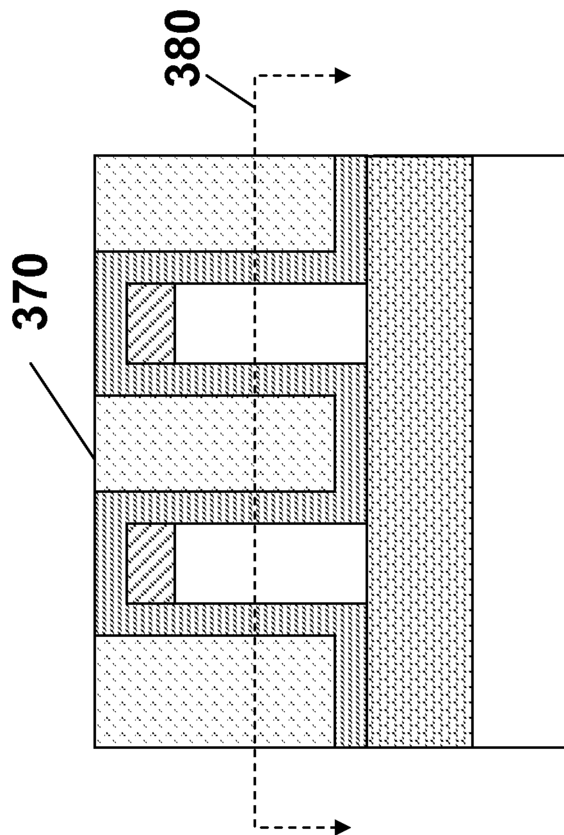

Fig. 3i

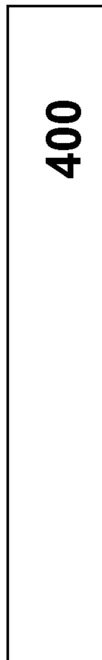

Fig. 4a

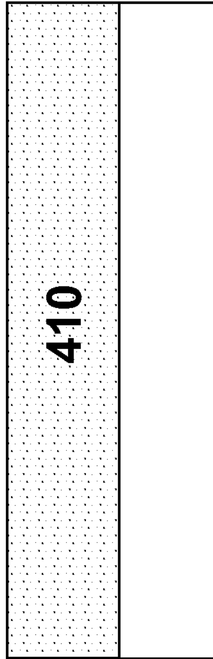

Fig. 4b

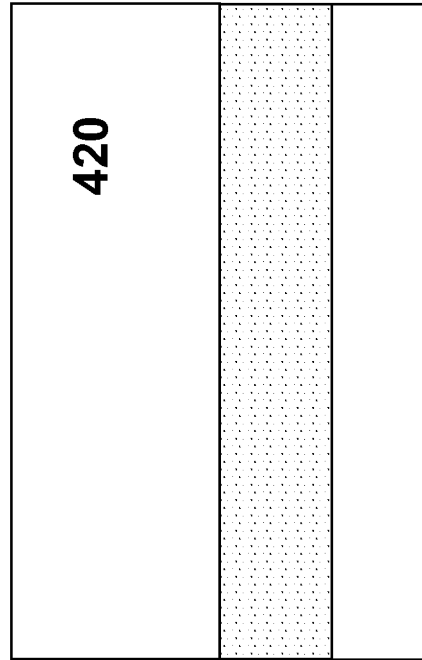

Fig. 4c

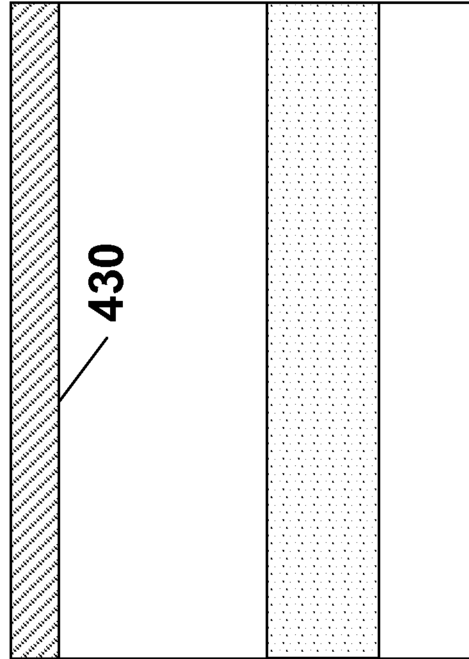

Fig. 4d

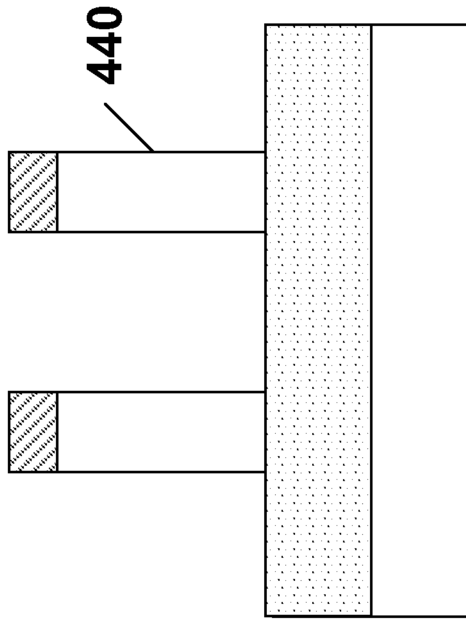

Fig. 4e

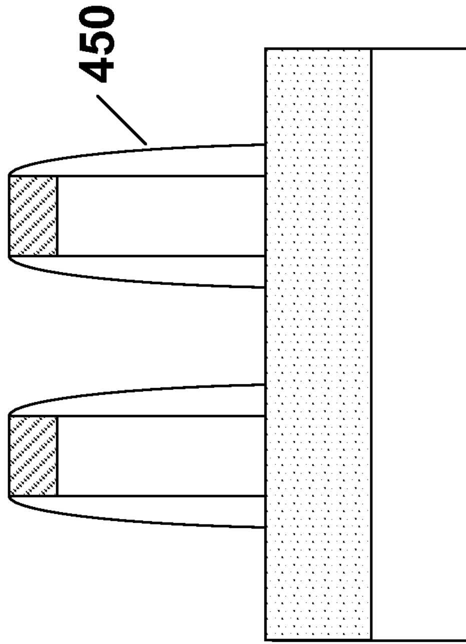

Fig. 4f

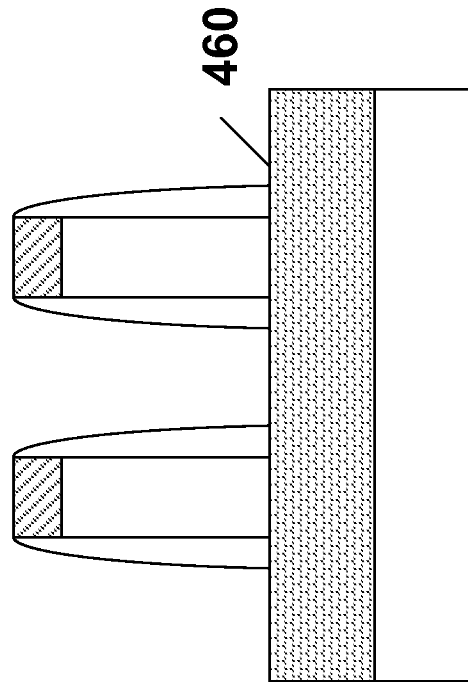

Fig. 4g

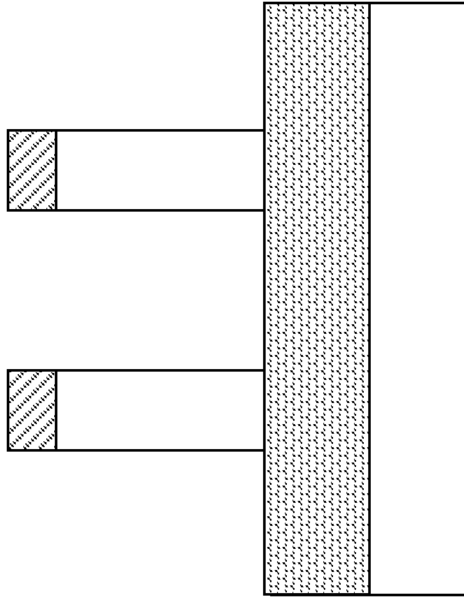
Fig. 4h

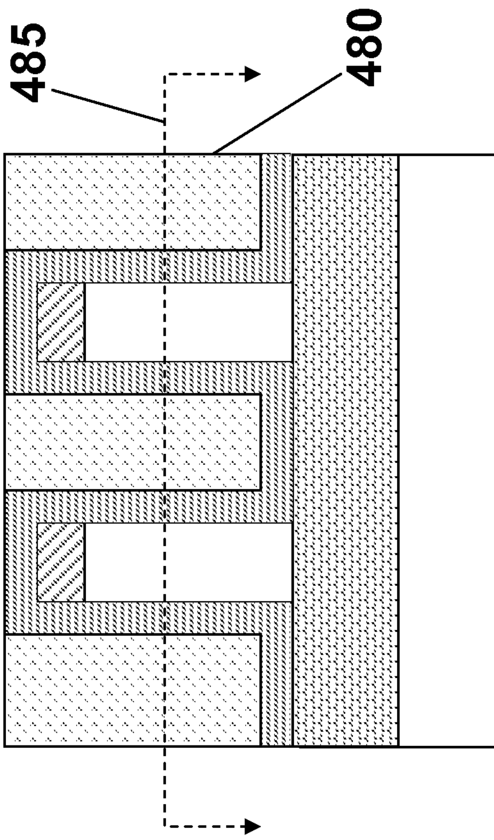

Fig. 4j

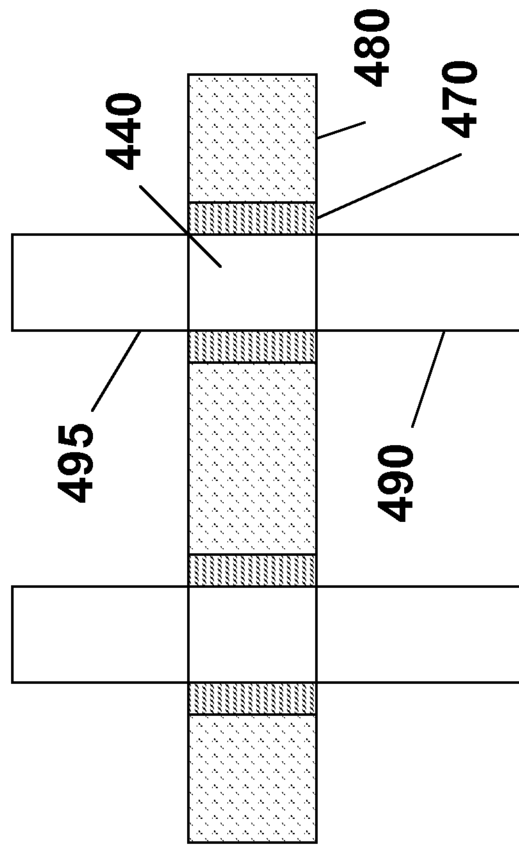

Fig. 4k

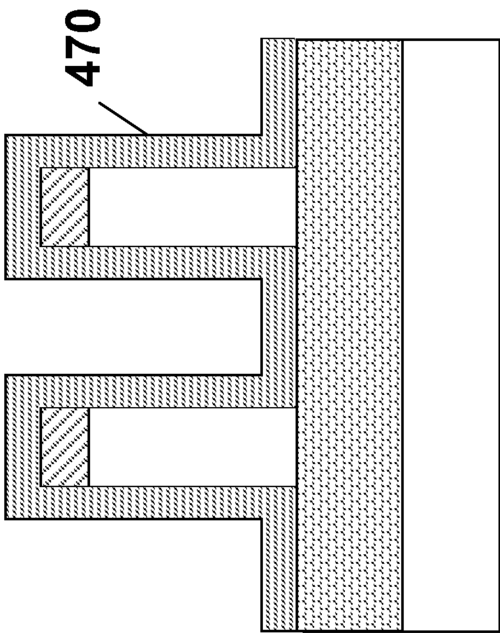

Fig. 4i

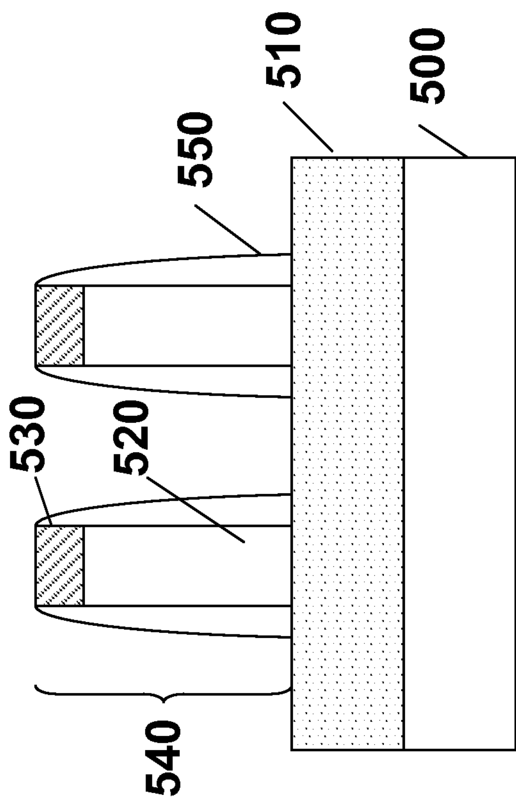

Fig. 5a

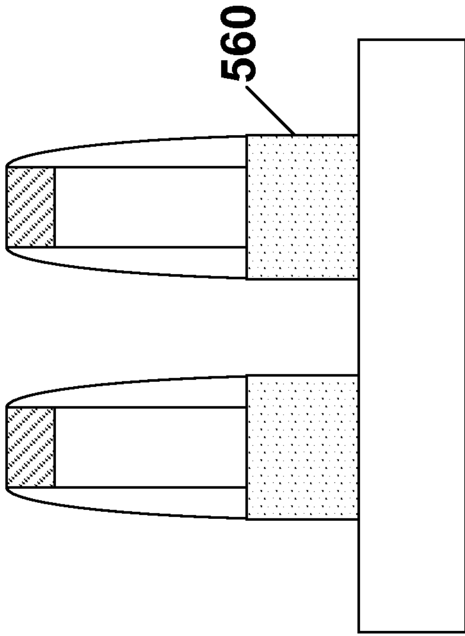

Fig. 5b

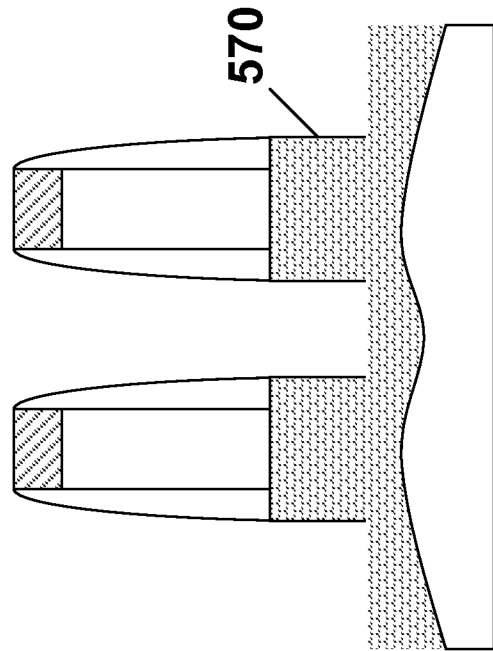

Fig. 5c

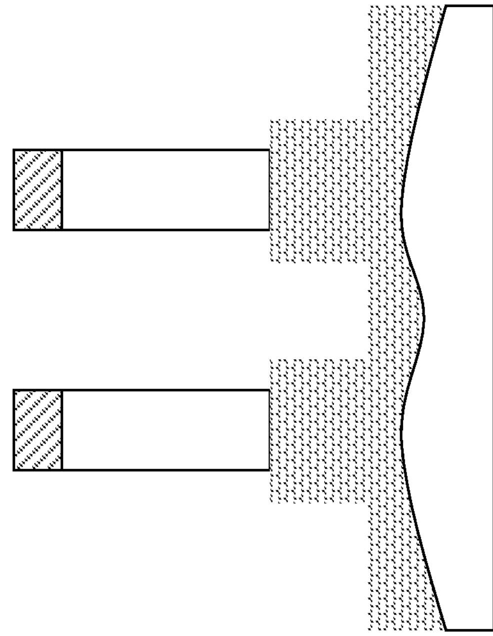

Fig. 5d

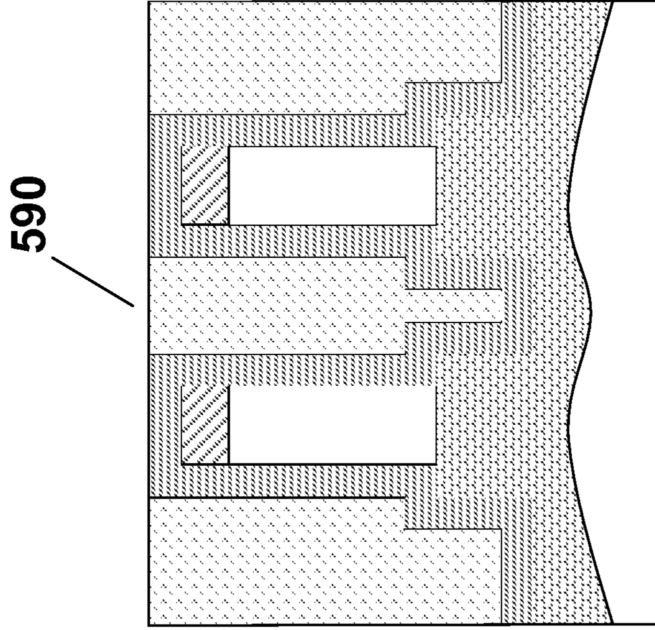

Fig. 5f

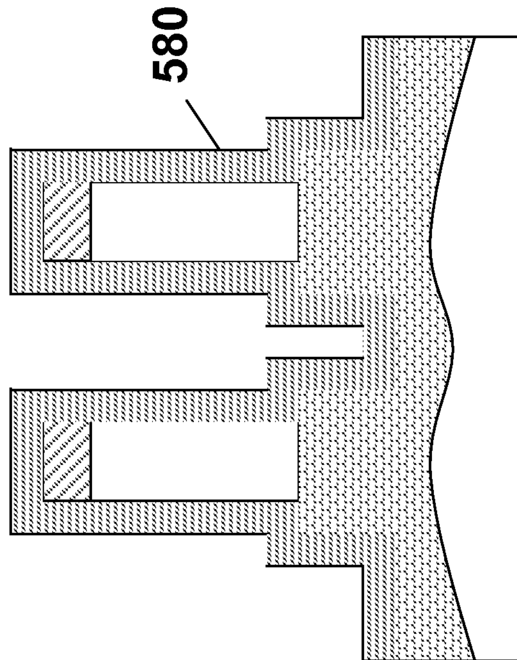

Fig. 5e

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/45389

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/732 (2013.01)
USPC - 438/206
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/3065, 29/68, 29/732 (2013.01)
USPC - 438/156, 157, 206; 257/E21.41, E21.612, E21.629

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used: FinFET, trigate OR tri-gate, field effect transistor, spacers, RIE, reactive ion etching, ion implantation, epitaxial, silicon germanium, buried oxide, carbon, bulk, wafer, silicon, Si, epi, vertical

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------ Y	WO 2010/025083 A1 (SEACRIST, M) March 4, 2010, Abstract, Figure 4, Paragraphs [0009], [0018], [0029], [0045], [0046], [0055]-[0060]	1-8 ------ 9-12
X ------ Y	US 7,871,873 B2 (MASZARA, W et al.) January 18, 2011, Figure 13, Column 1, Lines 7-12, Column 3, Lines 36-44, Column 3, Lines 47-55, Column 4, Lines 1-15, Figure 8, column 6, Lines 40-61, Figures 10 and 11, column 8, lines 4-28	20-23 ------ 10,11,13-19
Y	US 2009/0121288 A1 (PATRUNO, P) May 14, 2009, Abstract, Paragraph [0023]	9
Y	US 6,642,090 B1 (FRIED, D et al.) November 04, 2003, Abstract, Column 4, Lines 53-63, Figures 1 and 2, Column 4, Lines 16-35	12-19

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2012 (24.08.2012)	24 SEP 2012

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