CONTINUOUS DATA RETRIEVING DEVICE

A continuous data retrieving device (20) includes a data control circuit (21) adapted to receive test data from a test sample (27), a plurality of memory devices (24, 25) adapted to store test data obtained from the test sample, memory selector circuit controlled by the data control circuit to switch data storage path between the data control circuit and the memory devices for enabling received test data to be stored in a memory device in sequence and for enabling storage test data to be retrieved from the memory devices in subsequent order, and transmitted to a communication control circuit (22) where the communication control circuit (22) is controlled by the data control circuit to transmit storage test data from the memory devices to a computer connected to the analyzer for purposes of outputting the desired data signal.
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CONTINUOUS DATA RETRIEVING DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to logic analyzers and, more specifically, to a continuous data retrieving device, which enables test data received from the test sample to be stored in multiple memory devices one after another in a good order, and also enables storage test data to be retrieved from the memory devices one after another in a good order for continuously transmitting to a computer or display for display.

2. Description of the Related Art:

A logic analyzer is an instrument for examining digital circuits. FIG. 1 illustrates the arrangement of a logic data analyzer according to the prior art. The logic analyzer comprises a logic analyzer main unit 10. The logic analyzer main unit 10 comprises detection devices 11. Each detection device 11 has multiple lead-wires 111 and a clip 113 at the end of each lead-wire 111 for fastening to a respective pin of the test sample (for example, digital circuit) 13. The detection devices 11 detect high/low (1/0) potential status of every pin of the test sample 13 at a fixed time interval, and then transmit test data to a computer 16 through a transmission interface (for example, USB interface, LPT interface, or the like) 15, enabling test data to be displayed on the display screen 161 of
the computer 16. FIG. 2 is a system block diagram of the prior art logic data analyzer. The logic analyzer main unit 10 comprises a control circuit 17 and a memory (for example, SRAM) 18. When received test data from the test sample 13, the control circuit 17 stores received test data in the memory 18. When the memory space of the memory 18 used up, the control circuit 17 retrieves storage test data from the memory 18, and then transmits retrieved test data to the computer 16 through the transmission interface 15 for display on the display screen 161 of the computer 16. According to conventional logic analyzer data processing methods, test data is transmitted from the memory to the computer for analysis only when the memory capacity of the memory fully occupied with test data. Because the memory of a logic analyzer has a limited data storage space, it may not be able to store a complete series of test data. When the user debugging the digital circuit (test sample) based on an incomplete test result, the debugging work may take much time, or may be unable to proceed. In order to eliminate this problem, there are people adopting the measure of increasing the memory depth of the memory (i.e., use a relatively bigger capacity of memory for the logic analyzer) for storing more test data. However, using a big capacity memory relatively increases the cost of the logic analyzer. For example, the cost of one 256Kbytes SRAM is more than two times of the cost of a 126Kbytes SRAM.
Therefore, it is not economic to use a big capacity of memory in a logic analyzer. Therefore, it is desirable to provide a continuous data retrieving device that eliminates the aforesaid drawbacks.

**SUMMARY OF THE INVENTION**

The present invention has been accomplished under the circumstances in view. It is therefore the main object of the present invention to provide a continuous data retrieving device, which eliminates the aforesaid drawbacks.

According to one embodiment of the present invention the continuous data retrieving device has a first memory and a second memory. When received test data from the test sample, the data control circuit of the continuous data retrieving device stores received test data in the first memory. When the memory capacity of the first memory fully occupied, the data control circuit drives a memory selector circuit to shift the storage path from the first memory to the second memory for enabling received test data to be stored in the second memory, and at the same time the data control circuit transmits storage test data from the first memory through a communication control circuit and a transmission interface to an external computer. When the memory capacity of the second memory fully occupied, the data control circuit drives the memory selector circuit to shift the storage path from the second memory to the first memory for enabling received test data to be stored in the
first memory, and at the same time the data control circuit transmits storage test data from the second memory through the communication control circuit and the transmission interface to the computer. By means of alternatively storing test data from the test sample in the first memory and the second memory and alternatively transmitting storage test data from the first memory and the second memory to the computer, a complete series of test data obtained from the test sample can be fully transmitted to the computer for display.

According to an alternate form of the present invention, the continuous data retrieving device comprises a first memory and a second memory. When received test data from the test sample, the data control circuit of the continuous data retrieving device drives a compressor to compress received test data and then to store compressed test data in the first memory. When the memory capacity of the first memory fully occupied, the data control circuit drives a memory selector circuit to shift the storage path from the first memory to the second memory, and at the same time the data control circuit transmits storage test data from the first memory to the data storage device of the communication control circuit of the continuous data retrieving device. When the memory capacity of the second memory fully occupied, the data control circuit drives the memory selector circuit to shift the storage path from the
second memory to the first memory, and at the same time the data control circuit transmits storage test data from the second memory to the data storage device of the communication control circuit. This test data retrieving and storing procedure is repeated again and again for enabling the complete series of test data to be transferred to the data storage device. When the trigger condition established, the data control circuit stops receiving test data from the test sample and, transmits storage data from the data storage device to a display in the continuous data retrieving device for display. Therefore, the complete series of test data is well received from the test sample without delay, and fully displayed on the display.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 illustrates the arrangement of a logic analyzer according to the prior art.

FIG. 2 is a system block diagram of the prior art logic analyzer.

FIG. 3 is a circuit block diagram of a continuous data retrieving device according to the first embodiment of the present invention.

FIG. 4 is an operational flow chart of the communication control circuit of the continuous data retrieving device according to the first embodiment of the present invention.
FIG. 4A is an operational flow chart of the data control circuit of the continuous data retrieving device according to the first embodiment of the present invention.

FIG. 5 is a circuit block diagram of a continuous data retrieving device according to the second embodiment of the present invention.

FIG. 6 is an operational flow chart of the communication control circuit of the continuous data retrieving device according to the second embodiment of the present invention.

FIG. 7 is a circuit block diagram of a continuous data retrieving device according to the third embodiment of the present invention.

FIG. 8 is a circuit block diagram of a continuous data retrieving device according to the fourth embodiment of the present invention.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

Referring to FIG. 3, a continuous data retrieving device is shown comprising a data control circuit, a communication control circuit, a memory selector circuit, a first memory, a second memory, and a wait count. The data control circuit is connected to the sample to be tested (the test sample) through connector means (not shown), and controls the memory selector circuit to select the first memory or the second
memory 25 for storing test data from the test sample 27. The communication control circuit 22 is connected to the host computer 40 through a transmission interface (for example, an USB or LPT) 30, and communicates with the memory selector circuit 23 through a data and address bus. Therefore, the memory selector circuit 23 can transmit storage test data from the first memory 24 and the second memory 25 to the computer 40 by turn, enabling the computer 40 to display the test result.

Referring to FIG. 3 again, the continuous data retrieving device 20 has two pieces of memory, namely, the first memory 24 and the second memory 25. When received test data from the test sample 27, the data control circuit 21 stores received test data in the first memory 24. When the memory capacity of the first memory 24 used up (fully occupied), the data control circuit 21 drives the memory selector circuit 23 to shift the storage path from the first memory 24 to the second memory 25, and at the same time transmits storage test data from the first memory 24 through the communication control circuit 22 and the transmission interface 30 to the computer 40. When the memory capacity of the second memory 25 used up (fully occupied), the data control circuit 21 drives the memory selector circuit 23 to shift the storage path from the second memory 25 to the first memory 24, and at the same time transmits storage test data from the second memory 25 through the
communication control circuit 22 and the transmission interface 30 to the computer 40. By means of alternatively storing test data from the test sample 27 in the first memory 24 and the second memory 25 and alternatively transmitting storage test data from the first memory 24 and the second memory 25 to the computer 40, a complete series of test data obtained from the test sample 27 can be fully transmitted to the computer 40 for display.

Referring to FIG. 4 and FIG. 3 again, the communication control circuit 22 of the continuous data retrieving device 20 according to the first embodiment of the present invention works subject to the steps bellows:

(201) At first, determine if the data control circuit 21 has transmitted D_READY signal through a D_READY signal line or not? and then proceed to the next step. If received BUSY signal, control the wait count 26 to add 1, and then repeat step (201);

(202) Read count value of the wait count 26 and then send the data to the computer 40

(203) Data control circuit 21 starts to retrieve test data from the test sample 27 and to transmit retrieved test data to the computer 40; Send BUSY signal to the data control circuit 21 through the C_READY signal line and clear D_READY signal from the data control circuit 21;
(204) Send C READY signal to the data control circuit 21 through the C READY signal line after recognition of the transmission of the complete series of test data to the computer 40, and then return to step (201).

Referring to FIG. 4A and FIG. 3 again, the data control circuit 21 works subject to the steps bellows:

(301) At first, determine if the communication control circuit 22 has sent C READY signal through the C READY signal line or not, and then proceed to step (302) when positive, or proceed to step (305) when negative;

(302) Send first memory 24/second memory 25 switching signal through the switching control line to the communication control circuit 22 and the memory selector circuit 23;

(303) Enable the first memory 24 and the second memory 25 to alternatively receive and store test data from the test sample 27 till the saturated status;

(304) Send D READY signal through the D READY signal line to the communication control circuit 22 and zero the reading of the wait count 26, and then return to step (301);

(305) Control wait count 26 to add 1 when received BUSY signal, and then return to step (301).

Referring to FIG. 3 again, the memory selector circuit 23 is form of multiple switching circuits. Test data transmitted to the
computer 40 can be stored in the form of a file subject to a predetermined format so that the user can view the file when desired. The continuous data retrieving device 20 further comprises a data compressor 210 adapted to compress test data received from the test sample 27. Test data obtained from the test sample 27 can be compressed by the data compressor 210 to reduce the size, so that compressed test data can be stored in less space in the first memory 24 or the second memory 25. When received test data from the test sample 27, the data control circuit 21 can send received test data to the first memory 24 or the second memory 25 through the memory selector circuit 23 via the data compressor 210. After receipt of compressed test data from the communication control circuit 22 through the transmission interface 30, the computer 40 decompresses test data before displaying it.

FIG. 5 shows a continuous data retrieving device according to the second embodiment of the present invention. According to this embodiment, the continuous data retrieving device 20 comprises a data control circuit 21, a communication control circuit 22, a memory selector circuit 23, a first memory 24, a second memory 25, a wait count 26, and a display 211. The data control circuit 21 is connected to the sample to be tested (the test sample 27) through connector means (not shown), and controls the memory selector circuit 23 to select the first memory 24 or the
second memory 25 for storing test data from the test sample 27. The communication control circuit 22 comprises a data storage device 221, and communicates with the memory selector circuit 23 through a data and address bus. Therefore, the memory selector circuit 23 can alternatively transmit storage test data from the first memory 24 and the second memory 25 to the computer 40 to the data storage device 221 of the communication control circuit 22 so that when the trigger condition established, the data control circuit 21 stops receiving test data of the test sample 27 and, transmits storage data from the data storage device 221 to the display 211 for display.

Referring to FIG. 5 again, the continuous data retrieving device 20 of the second embodiment of the present invention has two pieces of memory, namely, the first memory 24 and the second memory 25. When received test data from the test sample 27, the data control circuit 21 drives the compressor 210 to compress received test data and then to store compressed test data in the first memory 24. When the memory capacity of the first memory 24 used up (fully occupied), the data control circuit 21 drives the memory selector circuit 23 to shift the storage path from the first memory 24 to the second memory 25, and at the same time transmits storage test data from the first memory 24 to the data storage device 221. When the memory capacity of the second memory 25 used up (fully
occupied), the data control circuit 21 drives the memory selector circuit 23 to shift the storage path from the second memory 25 to the first memory 24, and at the same time transmits storage test data from the second memory 25 to the data storage device 221.

This test data retrieving and storing procedure is repeated again and again for enabling the complete series of test data to be transferred to the data storage device 221. When the trigger condition established, the data control circuit 21 stops receiving test data from the test sample 27 and, transmits storage data from the data storage device 221 to the display 211 for display. Therefore, the complete series of test data is well received from the test sample 27 without delay, and fully displayed on the display 211.

Referring to FIG. 6 and FIG. 5 again, the communication control circuit 22 of the continuous data retrieving device 20 according to the second embodiment of the present invention works subject to the steps bellows:

(401) At first, determine if the data control circuit 21 has transmitted D_READY signal through a D_READY signal line or not? and then proceed to the next step. If received BUSY signal, control the wait count 26 to add 1, and then repeat step (401);

(402) Read count value of the wait count 26 and then store the data
in the data storage device 221;

(403) Data control circuit 21 starts to retrieve test data from the test sample 27 and to transmit retrieved test data to the data storage device 221; Send BUSY signal to the data control circuit 21 through the C_READY signal line and clear D_READY signal from the data control circuit 21;

(404) Send C_READY signal to the data control circuit 21 through the C_READY signal line after recognition of the transmission of the complete series of test data to the data storage device 221, and then return to step (401).

The data control circuit 21 of the continuous data retrieving device 20 according to the second embodiment of the present invention works in the same manner as the aforesaid first embodiment of the present invention, i.e., subject to the steps shown in FIG. 4A.

Referring to FIG. 5 again, the memory selector circuit 23 of the continuous data retrieving device 20 according to the second embodiment of the present invention is form of multiple switching circuits. Test data transmitted to the data storage device 221 can be stored in the form of a file subject to a predetermined format so that the user can view the file when desired. The continuous data retrieving device 20 further comprises a data compressor 210 adapted to compress test data received from the test sample 27, and
a decompressor 222 adapted to decompress compressed test data. Test data obtained from the test sample 27 can be compressed by the data compressor 210 to reduce the size, so that compressed test data can be stored in less space in the first memory 24 or the second memory 25. When received test data from the test sample 27, the data control circuit 21 can send received test data to the first memory 24 or the second memory 25 through the memory selector circuit 23 via the data compressor 210. After receipt of the complete series of compressed test data from the first memory 24 and the second memory 25, the decompressor 222 of the communication control circuit 22 decompress compressed test data from the data storage device 221 and then sends decompressed test data to the display 21 for display.

FIG. 7 shows a continuous data retrieving device 20 according to the third embodiment of the present invention. This embodiment is similar to the aforesaid first embodiment of the present invention with the exception of the arrangement of the data compressor 210. According to this embodiment, the data compressor 210 is connected between the memory selector circuit 23 and the communication control circuit 22. The data compressor 210 compresses test data retrieved from the first embodiment 24 or the second memory 25, and then sends compressed test data to the communication control circuit 22, which in turns transmits
compressed test data to the computer 40 through the transmission interface 30. After receipt of compressed test data from the communication control circuit 22, the computer decompresses received compressed test data for display.

FIG. 8 shows a continuous data retrieving device 20 according to the fourth embodiment of the present invention. This embodiment is similar to the aforesaid second embodiment of the present invention with the exception of the arrangement of the data compressor 210. According to this embodiment, the data compressor 210 is connected between the memory selector circuit 23 and the data storage device 221 of the communication control circuit 22. The data compressor 210 compresses test data retrieved from the first embodiment 24 or the second memory 25, and then sends compressed test data to the data storage device 221, and then the data decompressor 222 of the communication control circuit 22 decompresses compressed test data before sending it to the display 211 for display.

In the aforesaid embodiments, the data retrieving device 20 is a logic analyzer. In case the data retrieving device 20 is a wave monitor, an analog/digital converter 28 must be used and connected between the control circuit 21 and the test sample 27 to convert analog test signal into digital test signal for further processing.

In the aforesaid embodiments where a data compressor 210
is used, the data transmission speed is greatly accelerated. For example, the data transmission speed is accelerated by 10 times if the compression ratio is 10:1. Assume the frequency of sampling test data from the test sample 27 is 100MHz and the compression ratio is 10:1, the speed at the transmitting side requires only 10MHz to match the data sampling speed of 100MHz.

A prototype of continuous data retrieving device has been constructed with the features of the annexed drawings of FIGS. 3~8. The continuous data retrieving device functions smoothly to provide all of the features discussed earlier.

Although particular embodiments of the invention have been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.
What the invention claimed is:

1. A continuous data retrieving device comprising:
   a data control circuit adapted to receive test data from a test sample connected thereto;
   a plurality of memory devices adapted to store test data obtained from said test sample;
   a memory selector circuit controlled by said data control circuit to switch data storage path between said data control circuit and said memory devices for enabling test data received from said test sample to be stored in said memory devices one after another in an order and for enabling storage test data to be retrieved from said memory devices one after another in an order for transmission to a communication control circuit; and
   a communication control circuit controlled by said data control circuit to transmit storage test data from said memory devices one after another in an order to a computer connected thereto.

2. The continuous data retrieving device as claimed in claim 1, wherein said memory selector switch is formed of a plurality of switching circuits.

3. The continuous data retrieving device as claimed in claim 1, wherein the storage test data being transmitted by said communication control circuit to said computer is converted into
the form of a computer readable file subject to a predetermined format.

4. The continuous data retrieving device as claimed in claim 1, wherein said data control circuit comprises a data compressor adapted to compress test data received from said test sample and then to send compressed test data to said memory devices; said computer decompresses compressed test data received from said memory devices through said communication control circuit.

5. The continuous data retrieving device as claimed in claim 1, further comprising a data compressor connected between said memory selector circuit and said communication control circuit and adapted to compress storage test data to be sent from said memory devices to said communication control circuit.

6. The continuous data retrieving device as claimed in claim 1, which is a logic analyzer.

7. The continuous data retrieving device as claimed in claim 1, which is a wave monitor, which further comprises an analog/digital converter connected between said control circuit and said test sample and adapted to convert analog signal obtained from said test sample into digital signal for said control circuit.

8. A logic analyzer data circuit arrangement comprising:

  a data control circuit adapted to receive test data from a test
sample connected thereto;

a plurality of memory devices adapted to store test data obtained from said test sample;

a memory selector circuit controlled by said data control circuit to switch data storage path between said data control circuit and said memory devices for enabling test data received from said test sample to be stored in said memory devices one after another in an order and for enabling storage test data to be retrieved from said memory devices one after another in an order for transmission to a communication control circuit;

a communication control circuit, said communication control circuit having a data storage device controlled by said data control circuit to store storage test data retrieved from said memory devices; and

display means adapted to display test data from the data storage device of said communication control circuit.

9. The continuous data retrieving device as claimed in claim 8, wherein said memory selector switch is formed of a plurality of switching circuits.

10. The continuous data retrieving device as claimed in claim 8, wherein the storage test data being retrieved from said memory devices is stored in the data storage device of said communication control circuit in the form of a computer readable
file subject to a predetermined format; said data control circuit
comprises a data compressor adapted to compress test data received
from said test sample and then to send compressed test data to said
memory devices.

11. The continuous data retrieving device as claimed in
claim 10, wherein said communication control device further
comprises a data decompressor adapted to decompress compressed
test data before sending from said data storage device to said
display means.

12. The continuous data retrieving device as claimed in
claim 8, further comprising a data compressor connected between
said memory selector circuit and said communication control
circuit and adapted to compress storage test data to be sent from
said memory devices to said communication control circuit.

13. The continuous data retrieving device as claimed in
claim 8, which is a logic analyzer.

14. The continuous data retrieving device as claimed in
claim 8, which is a wave monitor, which further comprises an
analog/digital converter connected between said control circuit and
said test sample and adapted to convert analog signal obtained from
said test sample into digital signal for said control circuit.
Start or trigger

Data control circuit sent D_Ready signal?

D_Ready

Read count value of wait count and send the data to computer

Busy

Retrieve test data and send test data to computer; send Busy signal to data control circuit and clear D_Ready signal from data control circuit

Send C_Ready signal to data control circuit when complete series of test data transmitted to computer

FIG. 4
Start or trigger

Communication control circuit sent out C_Ready signal?

301

Busy

C_Ready

Switching control line sends first/second memory switching signal to communication control circuit and memory selector circuit

302

Retrieve test data and store retrieved test data in first/second memory till the saturated status

303

Send D_Ready signal to communication control circuit, and zero the reading of wait count

304

Wait count plus 1

305

FIG. 4A
FIG. 5
Start or trigger

Data control circuit sent D_Ready signal?

D_Ready → Read count value of wait count and store the data in data storage device

Busy → Retrieve test data and store test data in data storage device; send Busy signal to data control circuit and clear D_Ready signal from data control circuit

Send C_Ready signal to data control circuit when complete series of test data transmitted to data storage device

FIG. 6
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 19/00, 13/28
US CL : 702/80; 710/23
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : Please See Continuation Sheet

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
General online articles, IEEE Journal & Articles, Textbook, and U.S. Patents and Publications

Electronic database consulted during the international search (name of data base and, where practical, search terms used)
EAST (Examiners' Automated Search Tool), Internet Search Engines (Yahoo and Google), and IEEE Explore

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category *</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 4,688,168 A (GUDAITIS et al.) 18 August 1987 (18.08.1987), Figs. 1 and 2, column 2, lines 10-66 and column 5, line 51 to column 6, line 67.</td>
<td>1-3, 4-14</td>
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Further documents are listed in the continuation of Box C.
See patent family annex.

Date of the actual completion of the international search

Date of mailing of the international search report
02 SEP 2003

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703)305-3230

Authorized Officer
Marc S Hoff
Telephone No. (703)-308-1782

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Continuation of B. FIELDS SEARCHED Item 1: