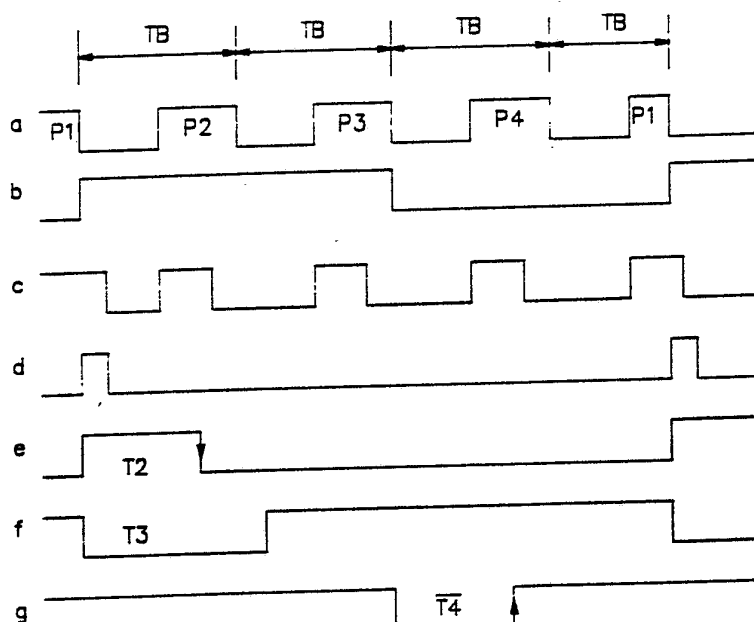




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(54) Title: OPTICAL COMMUNICATIONS TRANSMITTER AND RECEIVER

**(57) Abstract**

An improved digital communications system in which synchronization information is transmitted with the data. A start pulse (P1), having a duration different than the other pulses in the transmitted digital data signal is used to mark the beginning of the frame of digital data. Preferably, a midpoint pulse (P3) is also transmitted with the start pulse to mark the midpoint of the frame to facilitate the generation of a local clock signal. Bit positions within the transmitted signal are sampled by sampling pulses which are generated by digital timers (34) having time intervals keyed to the start and midpoint pulses.

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Optical Communications Transmitter and Receiver

BACKGROUND OF THE INVENTIONField of the Invention

The invention relates to digital data transmission systems in which clock information, data and other information is transmitted within a single baud and, more particularly, to the aforementioned systems used with optical communication mediums.

Description of the Prior Art

Digital data transmitting systems, used, for example, with telephone communication links, are known in which two or more bits are transmitted per baud. These systems are known as synchronous modems. See Understanding Data Communications, George E. Friend, John L. Fike, H. Charles Baker and John C. Bellamy, Chap. 5, "Synchronous Modems and Digital Transmission", p. 5-2, copyright Texas Instruments, Inc. 1984 published by Radio Shack.

Summary of the Invention:

The present invention provides a system for the synchronous data transmission of multiple bits per baud in which a start signal and an optional midpoint signal is used to encode the clock signal used for sampling data transmitted within the baud at the receiver having a plurality of bit positions which may assume a zero or one level. The bit

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positions may be used to encode diverse signals such as, but not limited to, the address of the receiver which is to receive the frames of transmitted data, priority information, general control and command information, basic data to be
5 processed by the receiver and a RTS signal which is transmitted by the transmitter to inform the receiver of the operational state of the transmitter. The invention utilizes a start pulse, having a duration different than all of the other pulses including the optional midpoint pulse and the
10 bits to be transmitted to mark the beginning of a frame which is required to provide correct processing of data at the receiver in accordance with the basic frame rate. The preferred embodiment of the present invention is a system used with a fiber optic transmission medium which contains both
15 transmitting and receiving circuitry for full duplex communications.

In the preferred embodiment, the receiver precisely generates a derived synchronizing clock signal occurring at the basic baud rate by the control of a bistable element with
20 the start pulse and midpoint pulse. The resultant generated clock signal from the output of the bistable element in practice has proved to be highly stable and meets the V.35 specification.

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The invention has the advantage that the system will process information at different baud rates simply by the change of the frequency of the master clock signal throughout the system.

5 A method of transmitting a data signal comprised of a plurality of bits per frame of a predetermined duration in accordance with the preferred embodiment of the invention includes the steps of providing a digital data signal to be transmitted having a series of bit positions having a first
10 level or a second level; providing a train of pulses comprising a start pulse which marks the beginning of a frame and a midpoint pulse which marks the midpoint of the frame; and combining the digital data signal with the train of pulses to form the frame of the data signal, the frame having an even
15 number of bit positions within the frame for transmitting the digital data signal in the form of bits, each of the bits which occur at the bit positions and the midpoint pulse having a duration which is different from the duration of the start pulse.

20 A method of transmitting a digital signal having a plurality of bits occurring in a frame with successive frames occurring at a frame rate in accordance with the invention includes the steps providing a basic data signal having a
basic frequency equal to the basic frame rate; sampling the
25 basic data signal at a predetermined time within the frame to form one of the bits of the frame; providing other signals to

be encoded as the other bits within the frame; sampling the other signals which are to be encoded as the remaining bits of the frame at predetermined times within the frame with each other signal and the basic data signal being sampled at a separate time within the frame; combining the sampled signals to form the frame; and transmitting the frame. The other signals may be used for diverse purposes including but not limited to control, priority and addressing.

A receiver for receiving a transmitted data signal comprised of one or more frames of binary data which occur at a frame rate with each frame having a start pulse of a first time duration which marks the beginning of the frame, a midpoint pulse which marks the midpoint of the frame and a plurality of bit positions within the frame for transmitting digital data with the midpoint pulse and each bit having a second time duration different than the first time duration in accordance with the preferred embodiment includes a signal receiver for receiving the frames of transmitted data; a detector coupled to the receiver for detecting the start pulse having an output on which the set pulse is produced; a detector coupled to the receiver for detecting the midpoint pulse and having an output on which the reset pulse is produced; a bistable circuit having a set input for causing an output signal to assume a set level, a reset input for causing the output signal to assume a reset level different than the set level with the output of the detector for the

start pulse being coupled to the set input and the output of the detector for detecting the midpoint pulse being coupled to the reset input and an output for producing a clock signal of the same frequency as the frame rate; a sampler for sampling the bit positions, coupled to the detector for detecting the start pulse and the detector for detecting the midpoint pulse, which samples the bit positions at fixed time intervals keyed to the start and midpoint pulses; and a storage coupled to the sampler and the output of the bistable circuit for processing the bit positions at the frame rate.

The storage includes a plurality of keyed storage circuits each coupled to the receiver with each keyed storage sampling a different one of the bit positions, half of the keyed storage circuits being coupled to the detector for detecting the start pulse and keyed to sample bit positions at time intervals measured from the occurrence of the start pulse and half of the keyed storage circuits being coupled to the detector for detecting the midpoint pulse to sample bit positions at time intervals measured from the occurrence of the midpoint pulse. Each keyed storage includes a timing circuit coupled to the detector for detecting the start pulse or the detector of the midpoint pulse for producing a sampling pulse at a time interval during the time of occurrence of bits at the bit position which is to be sampled and a triggered storage having a trigger input coupled to an output of the

sampler and an input coupled to the receiver for storing the level of the bit position at the bit position.

The bit positions may be used to encode a plurality of types of information including a control signal for controlling the activation of the receiver, the address of the receiver which is to receive the one or more frames of the transmitted data signal, the priority of the transmitted data signal, a control signal for the receiver, and data to be processed by the receiver. Any type of data may be encoded on the bit positions without limitation to the above examples.

Furthermore, a circuit is provided for signalling when there has been a failure of the receiver to receive a plurality of successively transmitted frames. The circuit for detecting failure includes a restartable one-shot multivibrator which produces an output signal of one level when the successive frames are being received and another level when they are not being received.

Preferably, the timing circuit is a digital counter which counts a predetermined number of pulses derived from a clock signal, counted from the occurrence of the start pulse, which is produced by a clock signal coupled to the digital counter.

The detector of the start pulse includes a circuit, coupled to the signal receiver, for producing a pulse on an output of a predetermined duration which is longer than the duration of the start pulse in response to each of the

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received pulses or bits in the received data signal, an
EXCLUSIVE OR gate having inputs coupled respectively to the
receiver and an output of the circuit for producing a pulse of
a predetermined duration and an output and an AND gate having
5 inputs coupled respectively to the output of the EXCLUSIVE OR
gate and the output of the circuit for producing a pulse.

Brief Description of the Drawings

Fig. 1 illustrates a transmitter of a digital signal
in accordance with the present invention.

10 Fig. 2 illustrates a first embodiment of a receiver
in accordance with the present invention.

Figs. 3a-g illustrate oscillograms of various
signals within the receiver of Fig. 2.

15 Fig. 4 illustrates another embodiment of a receiver
in accordance with the present invention.

Figs. 5a-h illustrate oscillograms of various
signals within the receiver of Fig. 4.

20 Fig. 6 illustrates a preferred embodiment of a
combined transmitter and receiver in accordance with Figs. 1
and 2.

Description of the Preferred Embodiments

Fig. 1 illustrates a transmitter 10 in accordance with the present invention. The transmitter generates a composite digital signal in accordance with Fig. 3a which is discussed below. The composite signal with reference to Fig. 3a has four pulses identified by the legends "P1-P4" which constitute a frame of the digital signal to be transmitted. Pulse P1 has a time duration less than that of the remaining pulses P2-P4. Pulse P1 is a start pulse which is used for marking the beginning of a frame as described below. Signals P2 and P4 are actual high level bits which occur at a series of bit positions within the frame which are used for transmitting any type of information other than information for controlling the clock of the receiver. Preferably, the bit are integer numbers of pairs of bits positions. The basic time rate of the transmitter 10 is derived from a clock signal CK2 which is derived from the main clock of the system as illustrated in Figs. 2, 4 and 6. The clock signal is coupled to a division circuit 12 which produces output pulses occurring respectively at $1/4$, $1/8$, $1/16$ and $1/32$ of the basic CK2, respectively, on lines C2, C3, C4 and C5. It should be noted that the C5 output signal is sent to an external cable driving circuit of conventional construction. C5 is the synchronizing clock for the transmitter. The division circuit 12 outputs C2-C5 are respectively coupled to a circuit 14 for creating the SRTS

signal and a TMES signal generator 16. An inverter 17 is coupled between the divide by 16 output C4 of the division circuit 12 and the SRTS creation circuit 14. The SRTS output signal is defined by a Boolean operator equal to $C2 \cdot C3 \cdot \overline{C4} \cdot C5$.

5 A storage register 18 is provided for storing the RTS control signal provided by the transmitter which is the signal specified by the BELL SYSTEM technical reference publication 41450, published Nov. 1981, for controlling the turning off of a receiver section 14 frames after the RTS signal is no longer
10 being received by the receiver. The storage register 18 latches the RTS control signal in response to the presence of the SRTS signal produced by the SRTS creation circuit 14 described above. A storage register 20 latches the data signal which is to be sent a bit at a time with each frame in
15 response to the generation of the S DATA signal which is produced by the output of inverting amplifier 22 having an input which is the C5 output from the division circuit 12. The BASIC DATA SIGNAL has a basic frequency equal to the frame rate. The frame rate is equal to one over the BASIC DATA
20 SIGNAL baud rate of the synchronous system. The function of the storage register 20 is to produce the DATA FF1 signal which is sampled once per frame at the center of the frame. The DATA FF1 signal is illustrated as the P4 pulse in Fig. 3a. The TMES signal is defined by the following Boolean operator:

$$25 \quad \text{TMES} = [(\overline{C3} \cdot \overline{C4}) \cdot (C2 \cdot C5)] + [(\overline{C3} \cdot C4) \cdot \overline{C5}] + [\overline{C3} \cdot C4 \cdot [(RTSFF1 \cdot C5) + (DATAFF1 \cdot C5)]]$$

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The SRTS and TMES signal generators may be implemented by conventional combinatorial logic. The output of the TMES signal generator 16 is coupled to a light emitting diode which generates a modulated light beam which is coupled to a fiber optic transmission medium in a conventional manner.

Fig. 2 illustrates a first embodiment of a receiver 24 in accordance with the invention. The receiver has a receiving section 26 which is coupling to a fiber optic transmission medium, not illustrated, over which the digital signal is transmitted. The received signal is designated by the term MES. The received signal is illustrated in Fig. 3a. The start pulse is identified by P1 and the midpoint pulse is identified by P3. The additional bit positions, which are illustrated with bits present, are identified by P2 and P4. Signal P1 is equal to $.25 T_B$ as illustrated in Fig. 3. A starting pulse detector is provided which is comprised of a digital one shot 28, EXCLUSIVE OR gate 30, and AND gate 32. The digital one shot 28 is driven by a main clock 34 which corresponds to the system clock for both the transmitter and receiver sections. The main clock 34 may have a selectable frequency as described below with reference to Fig. 4. The output of the main clock 34 CK1 drives the digital one shot 28 which functions to count a predetermined number of pulses of the signal CK1 when a pulse is present in the MES signal applied to the receiving section 26. The rising edge of the pulses within the MES signal keys the digital one shot 28 into

counting. The digital one shot 28 produces an output signal T1 of a high level until the predetermined count is reached at which point the signal goes to the low level. The output of the digital one shot 28 is illustrated in Fig. 3c.

5 EXCLUSIVE OR gate 30 produces a high level signal when the respective input signals are of a different level. A high level signal occurs on the output of EXCLUSIVE OR gate 30 only when there is a difference between the levels of the pulses in the MES signal as illustrated in Fig. 3a and the output pulses
10 from the digital one shot 28 as illustrated in Figs. 3c which occurs only in the time interval measured between the falling edge of signal P1 and the falling edge of the output pulse T1 produced by the digital one shot. AND gate 32 logically ands the output signal T1 of the digital one shot 28 and the output
15 of the EXCLUSIVE OR gate 30 to produce the STRT output signal as illustrated in Fig. 3d. The STRT signal produces a triggering signal for the digital one shot 36 which produces an output signal T3, as illustrated in Fig. 3f and to digital one shot 38 which produces output signal T2, as illustrated in
20 Fig. 3e. The digital one shots 36 and 38 each count a different predetermined number of pulses produced by the output of dividing circuit 40 which divides the main clock rate by two. The predetermined number of pulses which are respectively counted by the digital one shot 36 and digital
25 one shot 38 are different. AND gate 40 functions as a midpulse detector for marking the falling edge of the

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signal P3 of Fig. 3a. The inputs to the AND gate 40 are respectively the output of the digital one shot 36, the MES signal, and the output of the clock signal producing flip/flop 42 which produces the output clock signal DCLK. The delay in the response of the output of the clock signal producing flip/flop 42 is used to feed back that signal to the input of the AND gate 40 to permit the correct logic condition to be present at the input of the AND gate. The output signal DCLK of the flip/flop 42 is the clock signal for controlling the processing of the additional bit positions represented by pulses P2 and P4 of Fig. 3a by the RTS signal processing circuitry 44 and the data signal flip/flop 46 in a manner described below. The MP output signal from AND gate 40 is inverted by inverter 48 to produce a rising edge pulse which occurs during the time interval of the falling edge of the pulse P3 to initiate the counting of the digital one shot 50. The output signal T4 is illustrated in Fig. 3g. RTS signal processing circuitry 52 processes the RTS signal present at the bit position which is occupied by bit P2 of Fig. 3a at the falling edge of signal T2 as illustrated in Fig. 3e. This circuitry is illustrated in detail in Fig. 6. Data storage register 54 latches the data bit present at the bit position illustrated by bit P4 of Fig. 3a upon the rising edge of signal T4 of Fig. 3g. The data latched into the data signal storage register 54 is latched into the data storage register 46 upon the occurrence of the DCLK signal produced by

the clock signal producing flip/flop 42. The DCLK signal is the derived synchronizing signal for the receiver. The output of the data signal 46 is coupled to the data signal processing circuitry which is not described herein in detail but which is illustrated in detail in Fig. 6. A start pulse detector 56 is coupled to the output of the digital one shot 38 for producing a high level signal to activate a light emitting diode when successive frames each containing the start pulse are being received. When successive frames are not being received, the level of the output signal from the start pulse detector changes which indicates that there is a transmission fault or that the frames of digital information are no longer being sent by the transmitter. A light emitting diode 58 or other indicator is coupled to the output of the start pulse detector for producing a signal indicating the receipt of information by the receiver from the transmitter.

Fig. 4 illustrates an alternative embodiment of a receiver in accordance with the present invention. The receiver of Fig. 4 differs principally from the receiver of Fig. 2 in its processing of more bit positions than Fig. 2. Like reference numerals identify like parts in Figs. 2 and 4. In the embodiment of Fig. 4, a plurality of digital timers 58 initiate storage of the bit level present at the bit positions of the MES signal present at the receiver 26 prior to the midpulse in associated edge triggered registers 60.

Similarly, a plurality of digital timers 62 initiate storage of the bits present at the bit positions after the midpulse in a plurality of associated edge triggered registers 64. It should be understood that in this embodiment equal numbers of digital timers 58 and 62 are provided as a consequence of the symmetry in the duty cycles of the high and low levels of the clock signal. The master clock 66 permits different clock frequencies to be chosen by the positioning of a multiple pole switch 68 in any one of three positions to select the clock frequency as the output of oscillator 70, divide by two circuit 72 or divide by integer P circuit 74 which may be any integer number. The present invention has the advantage that the digital timers automatically proportionally time their respective time intervals as a function of the frequency of the output from the master clock 66 which is applied by the switch 68 to the start pulse detector 72 without requiring the digital timers to be programmed for each different driving frequency. The start pulse detector 72 is identical to that described above with reference to Fig. 2. The midpulse detector 40 produces the midpulse in response to the output of digital timer number k and the MES signal in the same manner as the midpulse detector in Fig. 2. The clock signal producing flip/flop 42 functions in the same manner as that illustrated in Fig. 2. The restartable one shot 56 functions in the same manner as the start pulse detector of Fig. 2. An address decoder 74 is coupled to the output of the edge

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triggered storage register 60 which samples the additional bit position which contains addressing information. The address decoder 74 is a conventional address decoder which responds to a signal comprised of one or more bits to detect if the received signal is addressed to the particular receiver. A priority detector 76 is coupled to the output of the edge triggered storage register 60 which samples the additional bit position containing priority information. The priority decoder may be any conventional priority detection circuit. A control/command decoder 78 is coupled to the output of the edge triggered storage register 64 which samples the bit position encoding command information for the receiver. The control/command decoder may be any conventional decoder for decoding encoded digital commands to control the operation of the receiver. One example of such a command is the RTS signal described above with reference to the embodiment of Fig. 2. Data is outputted from the edge triggered storage register 64. The embodiment of Fig. 4 does not illustrate the application of the driven clock signal produced by the clock signal producing flip/flop 42 to an additional flip/flop such as 46 illustrated in Fig. 2.

The operation of the embodiment of Fig. 4 is described above with reference to Fig. 5. The input signal MES on the receiver section 26 is illustrated in Fig. 5a. The time duration between successive additional bit positions represented by DCA1-DCAn is equal to T_B which is

equal to $T_A + n$ wherein n is an integer which is equal to the number of bit positions plus pulse positions and T_A is the length of the derived clock signal, as illustrated in Figs. 5b and 5c. Figs. 5d-h illustrate the outputs of the respective digital timers 58 and 62 which sample the additional bit positions illustrated in Fig. 5a by DC1-DCAn. The arrows identifying the falling edge and the rising edge of the outputs of the timers identify the actual sampling point for the additional bit positions identified by DCAl-DCAn.

Fig. 6 illustrates a wiring schematic of an actual transmitter and receiver in accordance with the present invention. Part numbers are identified by their industry known part identification number or their logic function identification.

Numerous modifications may be made to the present invention without departing from the spirit and scope thereof. For example, while the preferred embodiment utilizes both a start pulse and a midpoint pulse to precisely synchronize the generation of the clock signal by the controlling of the states of a bistable circuit for generating the clock signal, it is within the scope of the present invention to omit the transmission of the midpoint pulse. When the midpoint pulse is omitted, an additional digital timer may be provided which counts a number of pulses produced by the clock which is substantially equal to half of the desired clock interval to thus ensure that the clock signal

maintains a square wave configuration. For example, the V.35 specification permits the clock signal to have plus or minus 5% jitter in the transition point which permits it to occur within the range of 45-55% of the midpoint measured from the start of the clock pulse signal. Therefore, a locally generated midpulse is acceptable for producing proper system operation in many configurations.

CLAIMS:

1 1. A method of transmitting a digital signal
2 comprised of a plurality of bits per frame of a predetermined
3 duration comprising:
4 providing a digital data signal to be
5 transmitted having a series of bit positions having a first
6 level or a second level;
7 providing a train of pulses comprising a start
8 pulse which marks the beginning of a frame, and a midpoint
9 pulse which marks the midpoint of the frame; and
10 combining the digital data signal with the
11 train of pulses to form the frame of the data signal, the
12 frame having an even number of bit positions within the frame
13 for transmitting the digital data signal in the form of bits,
14 each of the bits which occur at the bit positions and the
15 midpoint pulse having a duration which is different from the
16 duration of the start pulse.

1 2. A receiver for receiving a transmitted data
2 signal comprised of one or more frames of binary data which
3 occur at a frame rate with each frame having a start pulse of
4 a first time duration which marks the beginning of the frame,
5 a midpoint pulse which marks the midpoint of the frame and
6 plurality of bit positions within the frame for transmitting
7 digital data with the midpoint pulse and each bit having a

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8 second time duration different than the first time duration
9 comprising:

10 means for receiving the frames of the
11 transmitted data signal;

12 means, coupled to the means for receiving the
13 transmitted frames of the data signal, for detecting the start
14 pulse and having an output on which the start pulse is
15 produced;

16 means, coupled to the means for receiving the
17 frames of the transmitted data signal, for detecting the
18 midpoint pulse and having an output on which the midpoint
19 pulse is produced;

20 a bistable means having a set input for causing
21 an output signal to assume a set level, a reset input for
22 causing the output signal to assume a reset level different
23 than the set level with the output of the means for detecting
24 the start pulse being coupled to the set input and the output
25 of the means for detecting the midpoint pulse being coupled to
26 reset input and an output for producing a clock signal of the
27 same frequency as the frame rate;

28 means for sampling the bit positions, coupled
29 to the means for detecting the start pulse and the means for
30 detecting the midpoint pulse which samples the bit positions
31 at fixed time intervals keyed to the start and midpoint
32 pulses; and

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33 storage means coupled to the means for sampling
34 the bit positions and the output of bistable means for
35 processing the additional bit positions at the frame rate.

1 3. A receiver in accordance with claim 2 wherein
2 the means for sampling is comprised of a keyed storage means
3 coupled to the means for receiving for sampling each
4 additional bit position.

1 4. A receiver in accordance with claim 3 wherein
2 the keyed storage means comprises a plurality of keyed storage
3 means each coupled to the means for receiving with each keyed
4 storage means sampling a different one of the bit positions,
5 half of the keyed storage means being coupled to the means for
6 detecting the start pulse and to sample bit positions at time
7 intervals measured from the occurrence of the start pulse and
8 half of the keyed storage means being coupled to the means for
9 detecting the midpoint pulse and to sample bit positions at
10 time intervals measured from the occurrence of the midpoint
11 pulse.

1 5. A receiver in accordance with claim 4 wherein
2 each keyed storage means comprises a timing means coupled to
3 the means for detecting the start pulse or means for detecting
4 the midpoint pulse for producing a sampling pulse at a time
5 interval during the time of occurrence of bits at the bit
6 position which is to be sampled and a triggered storage
7 means having a trigger input coupled to an output of the means

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8 for producing a sampling pulse and an input coupled to the
9 means for receiving for storing the level of the bit position
10 occurring at the bit position.

1 6. A receiver in accordance with claim 5 wherein
2 one of the bit positions encode data to be processed by the
3 receiver and another of the bit positions encodes a control
4 signal for controlling the activation of the receiver.

1 7. A receiver in accordance with claim 5 wherein
2 one of the bit positions encodes the address of the receiver
3 which is to receive the transmitted data signal.

1 8. A receiver in accordance with claim 5 wherein
2 one of the bit positions encodes the priority of the
3 transmitted data signal.

1 9. A receiver in accordance with claim 5 wherein
2 one of the bit positions encodes a control signal for the
3 receiver.

1 10. A receiver in accordance with claim 5 wherein
2 one of the bit positions encodes data to be processed by the
3 receiver.

1 11. A receiver in accordance with claim 4
2 comprising means coupled to the means for detecting the start
3 pulse for signalling when there has been a failure of the
4 receiver to receive a plurality of successively transmitted
5 frames.

1 12. A receiver in accordance with claim 11 wherein
2 the means for detecting when there has been a failure of the
3 receiver to receive a plurality of successively transmitted
4 frames comprises a restartable one-shot multivibrator means
5 which produces an output signal of one level when successive
6 frames are being received and another level when successive
7 frames are not being received.

1 13. A receiver in accordance with claim 5 wherein
2 the timing means is a digital counting means which counts a
3 predetermined number of pulses derived from a clock signal
4 counted from the occurrence of the start pulse or the midpoint
5 pulse to produce the sampling pulse and further comprising
6 means for producing a clock signal coupled to the digital
7 counting means.

1 14. A receiver in accordance with claim 2 wherein
2 the means for detecting the start pulse comprises means,
3 coupled to the means for receiving, for producing a pulse on
4 an output of a predetermined duration which is longer than the
5 duration of the start pulse in response to each of the
6 received pulses or bits in the received digital signal,

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7 an EXCLUSIVE OR gate having inputs coupled respectively
8 to the means for receiving and the output of the means for
9 producing a pulse of predetermined duration and an output and
10 an AND gate having inputs respectively coupled to the output
11 of the EXCLUSIVE OR gate and the output of the means for
12 producing a pulse.

1 15. A method of transmitting a data signal
2 comprised of a plurality of bits occurring during a frame of a
3 predetermined time duration comprising:

4 providing a digital data signal to be
5 transmitted having a series of bit positions having a first
6 level or a second level;

7 providing a train of pulses comprised of a
8 start pulse which marks the beginning of a frame; and

9 combining the digital data signal with the
10 train of pulses to form the frame of the data signal, the
11 frame having a plurality of bit positions within the frame for
12 transmitting the digital data signal in the form of bits, each
13 of the bits having a duration which is different from the
14 duration of the start pulse.

1 16. A receiver for receiving a transmitted data
2 signal comprised of one or more frames of binary data which
3 occur at a frame rate with each frame having a start pulse of
4 a first time duration which marks the beginning of the frame,
5 and a plurality of bit positions within the frame for

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6 transmitting digital data and each bit having a second time
7 duration different than the first time duration comprising:

8 means for receiving the transmitted frames of
9 the data signal;

10 means coupled to the means for receiving the
11 transmitted frames of data for detecting the start pulse
12 within the frames of the transmitted data signal having an
13 output on which the start pulse is produced; and

14 means for sampling the bit positions, coupled
15 to the means for detecting the start pulse, which samples the
16 bit positions at fixed time intervals keyed to the start
17 pulse.

1 17. A receiver in accordance with claim 16 further
2 comprising:

3 storage means coupled to the means for sampling
4 a bit position for processing the bit position at the frame
5 rate.

1 18. A receiver in accordance with claim 17 wherein
2 the means for sampling is comprised of a keyed storage means
3 coupled to the means for receiving for sampling the bit
4 position.

1 19. A receiver in accordance with claim 18 wherein
2 the keyed storage means comprises a plurality of keyed storage
3 means each coupled to the means for receiving with each keyed
4 storage means sampling a different one of the bit positions,

5 half of the keyed storage means being coupled to the means for
6 detecting the start pulse and to sample additional bit
7 positions at time intervals measured from the occurrence of
8 the start pulse and half of the keyed storage means sampling
9 bit positions at time intervals measured as a function the
10 occurrence of the start pulse.

1 20. A receiver in accordance with claim 19 wherein
2 each keyed storage means comprises a timing means producing a
3 sampling pulse at a time interval during the time of
4 occurrence of bits at the bit position which is to be sampled
5 and a triggered storage means having a trigger input coupled
6 to an output of the means for producing a sampling pulse and
7 an input coupled to the means for receiving for storing the
8 level of the bit position occurring at the bit position.

1 21. A method of transmitting a digital signal
2 having a plurality of bits occurring in a frame with
3 successive frames occurring at a frame rate comprising:
4 providing a basic data signal having a basic
5 frequency equal to the basic frame rate;
6 sampling the basic data signal at a
7 predetermined time within the frame to form one of the bits of
8 the frame;
9 providing other signals to be encoded as the
10 other bits within the frame;

11 sampling the other signals which are to be
12 encoded as the remaining bits of the frame at predetermined
13 times within the frame with each other signal and the basic
14 data signal being sampled at a separate time within the frame;
15 combining the sampled signals to form the
16 frame; and
17 transmitting the frame.

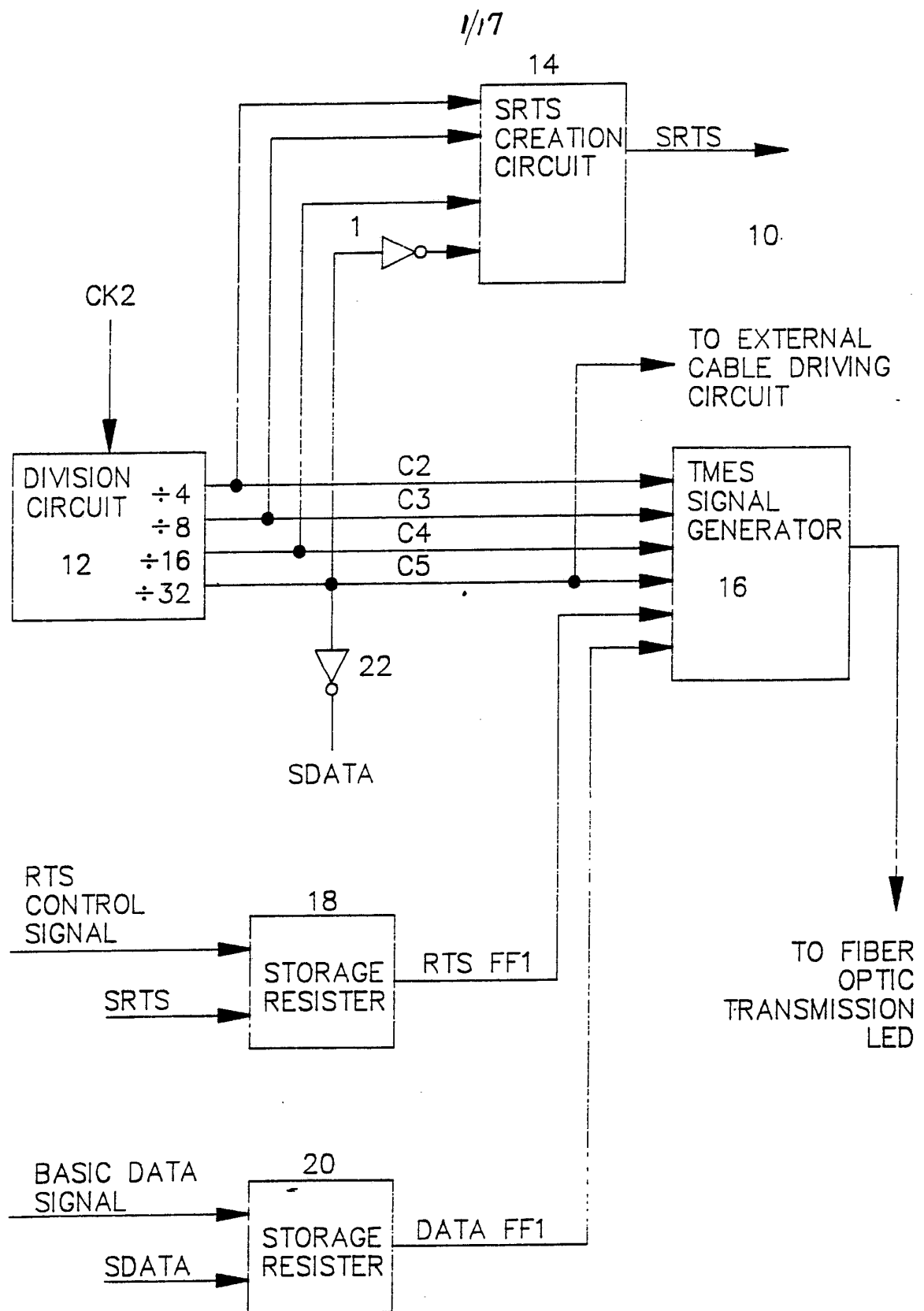


FIGURE 1

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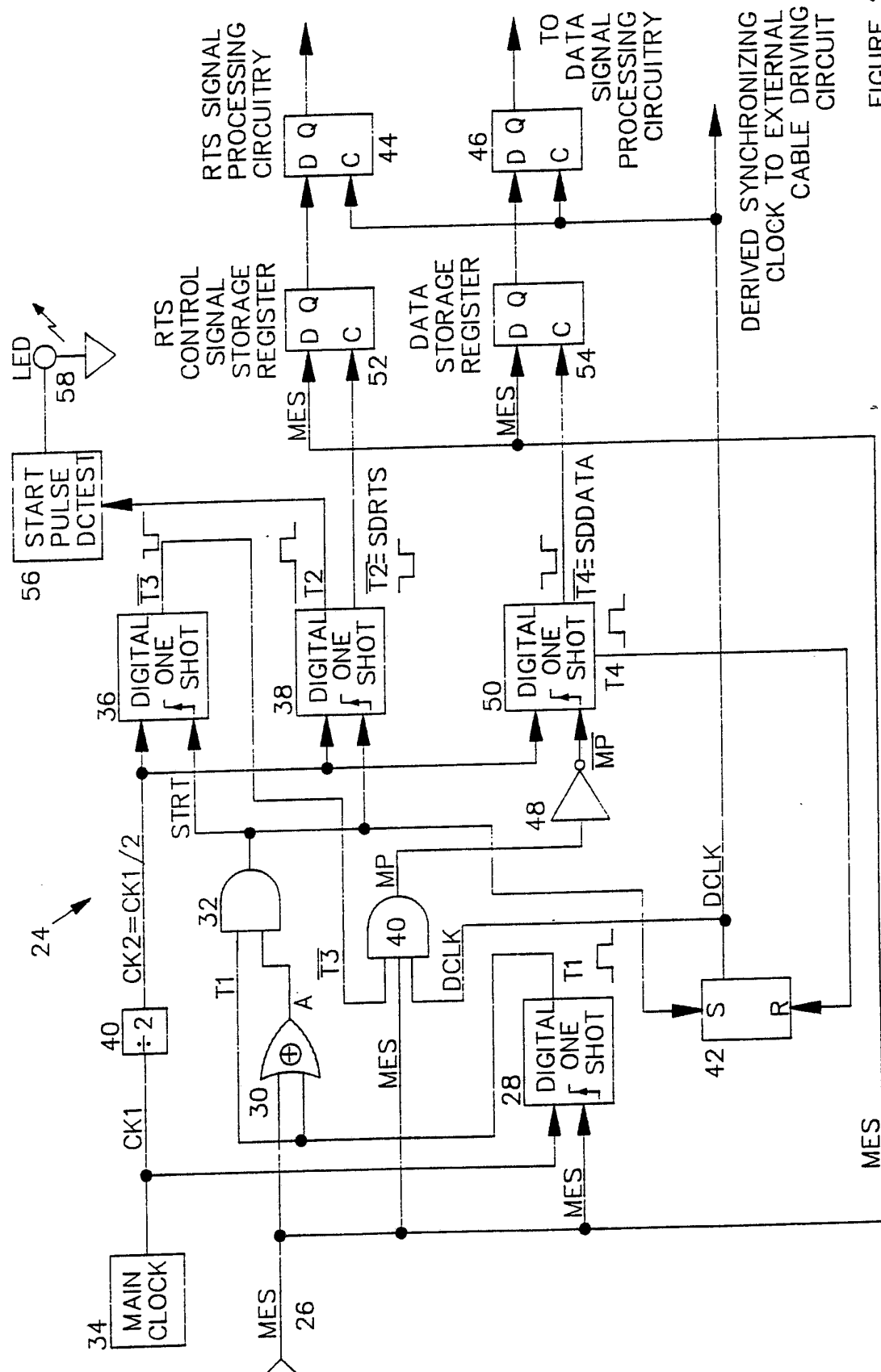


FIGURE 2

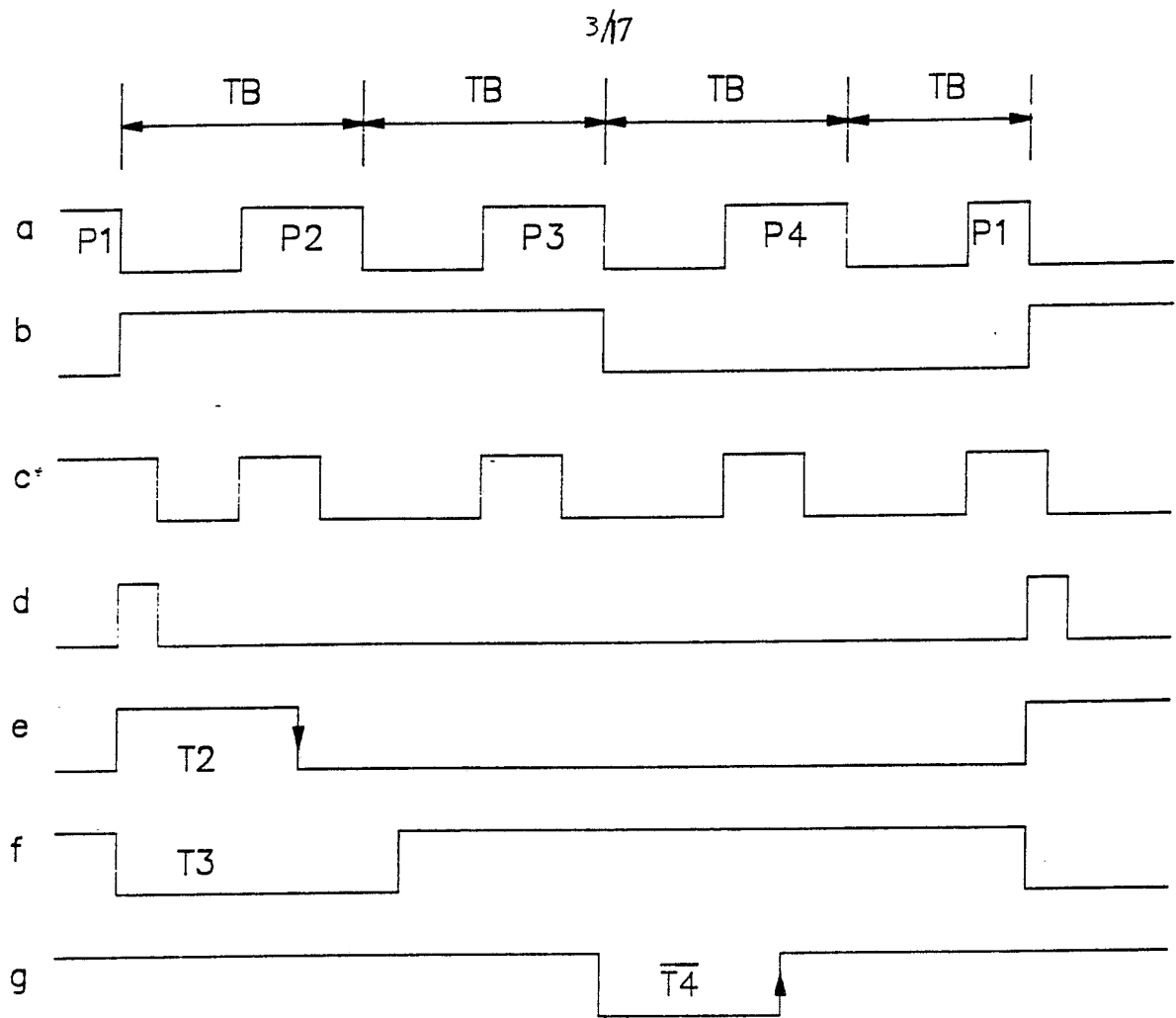


FIGURE 3

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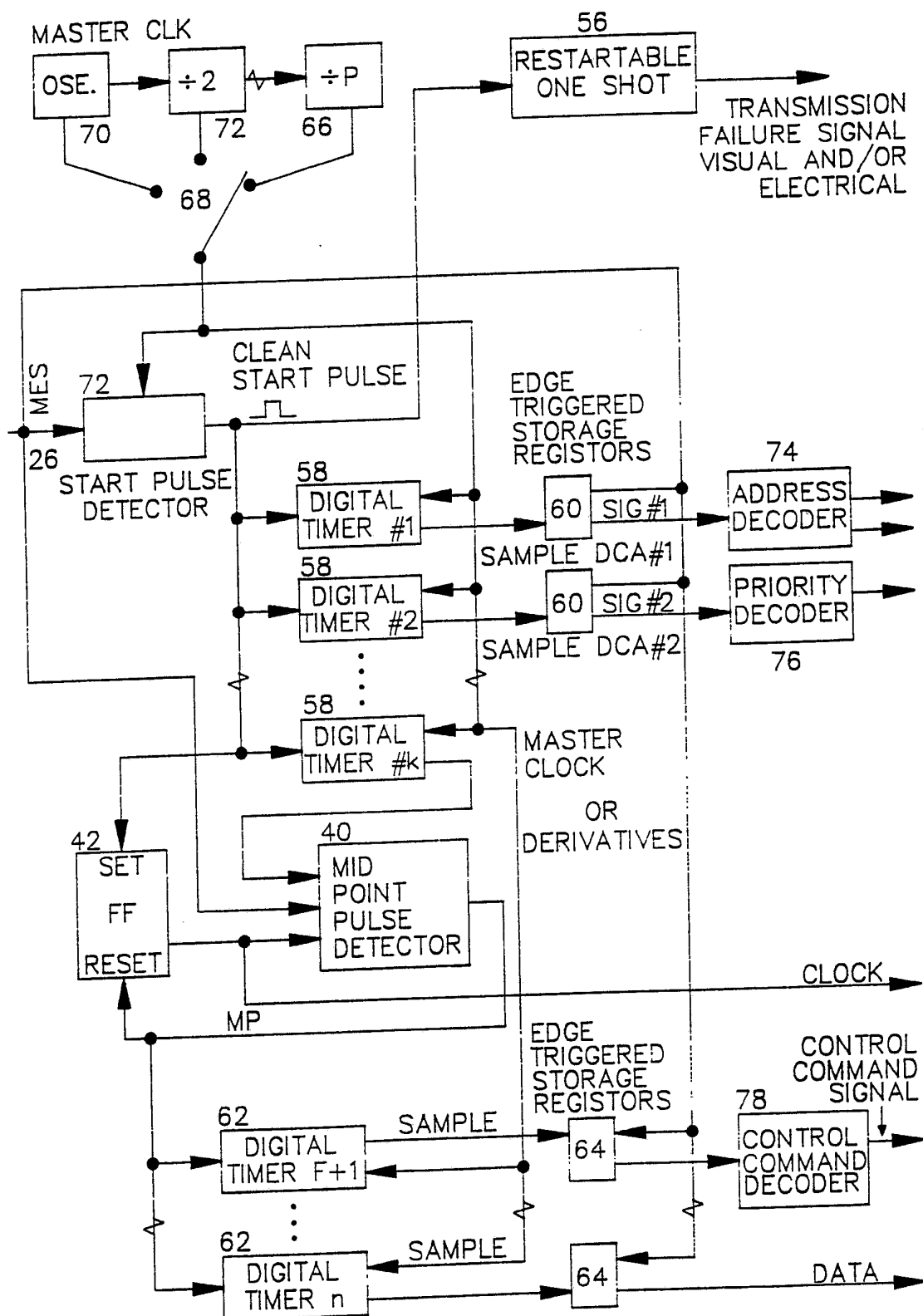


FIGURE 4

SUBSTITUTE SHEET

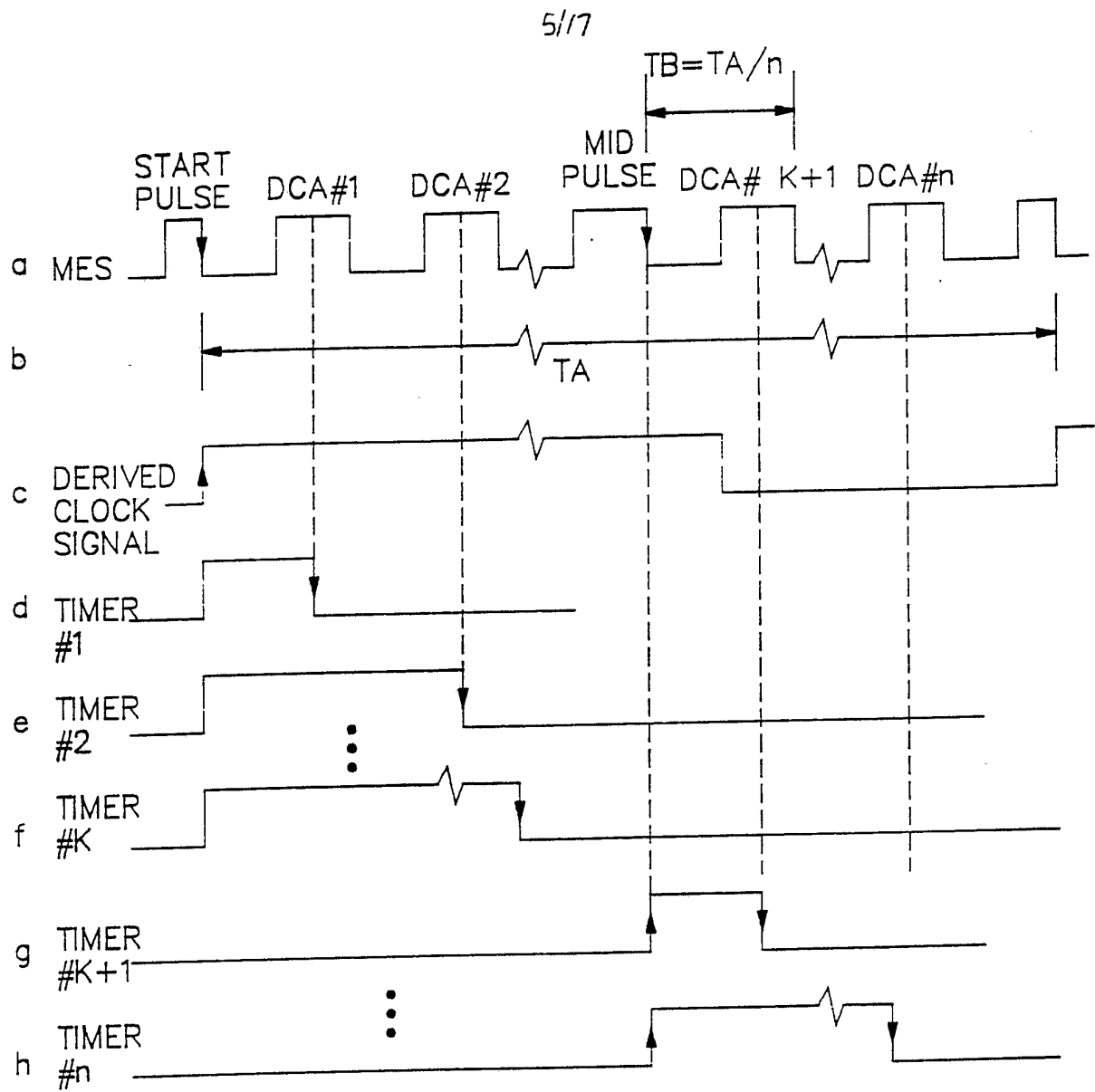


FIGURE 5

SUBSTITUTE SHEET

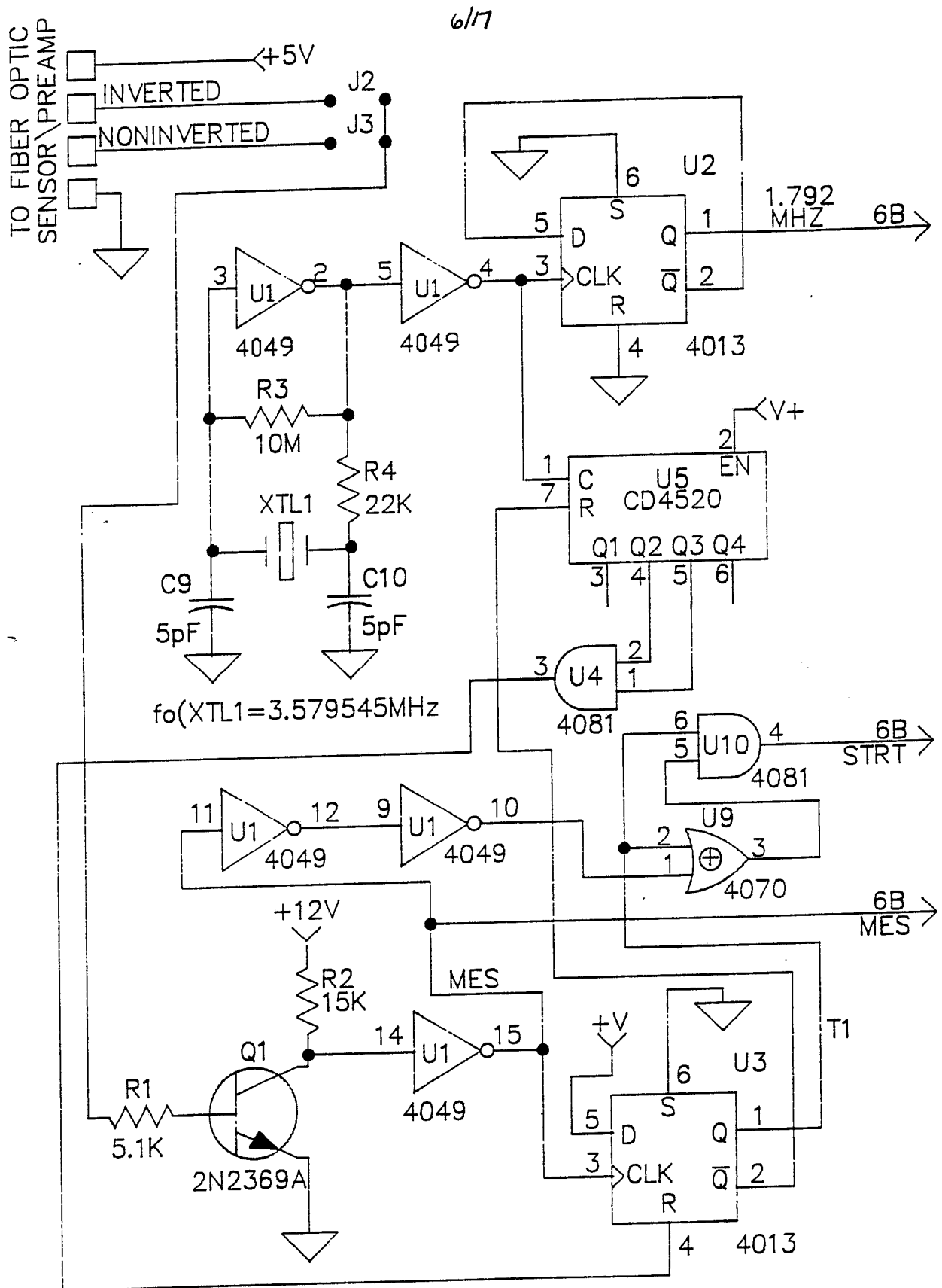


FIGURE 6A

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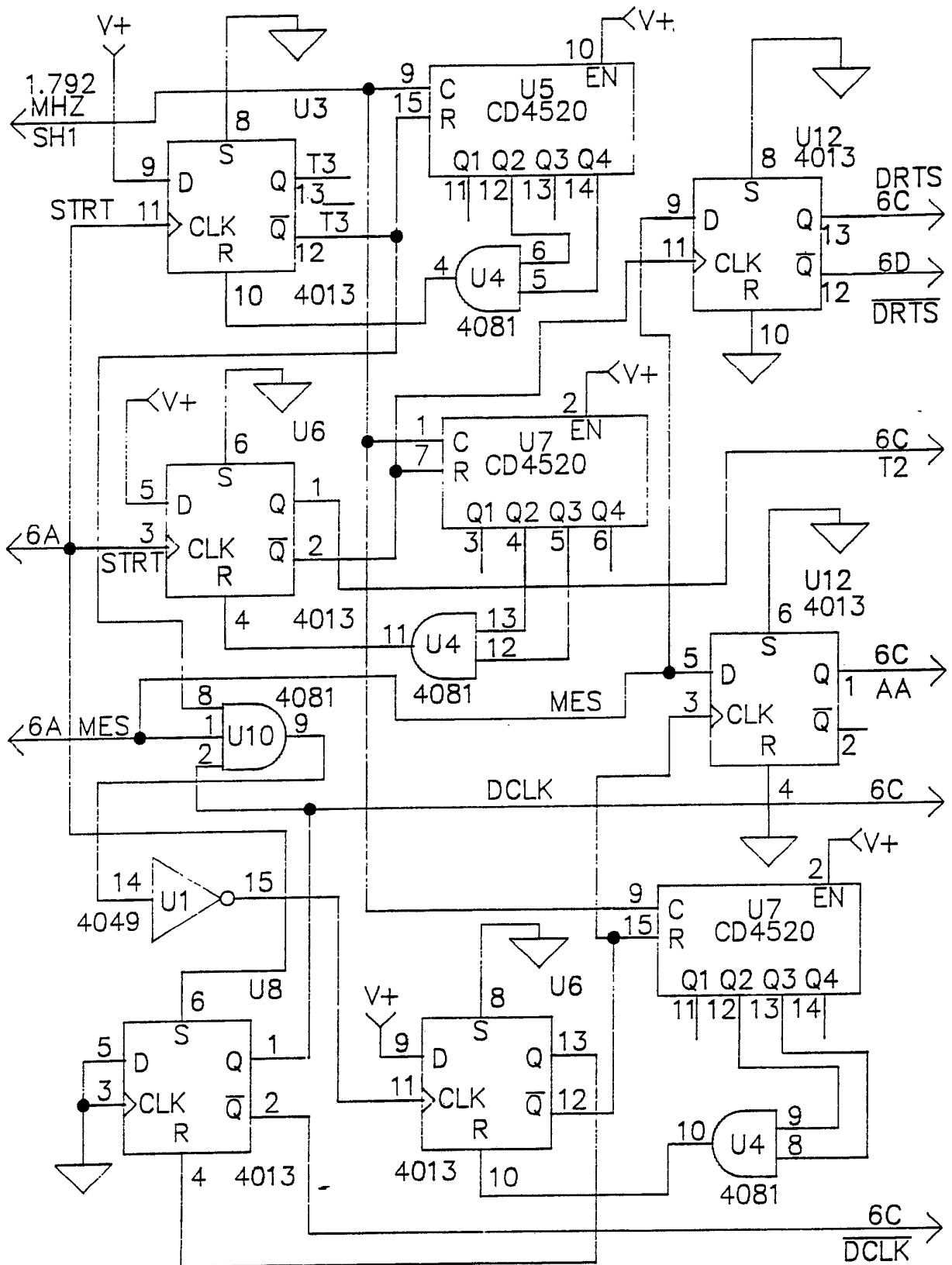


FIGURE 6B

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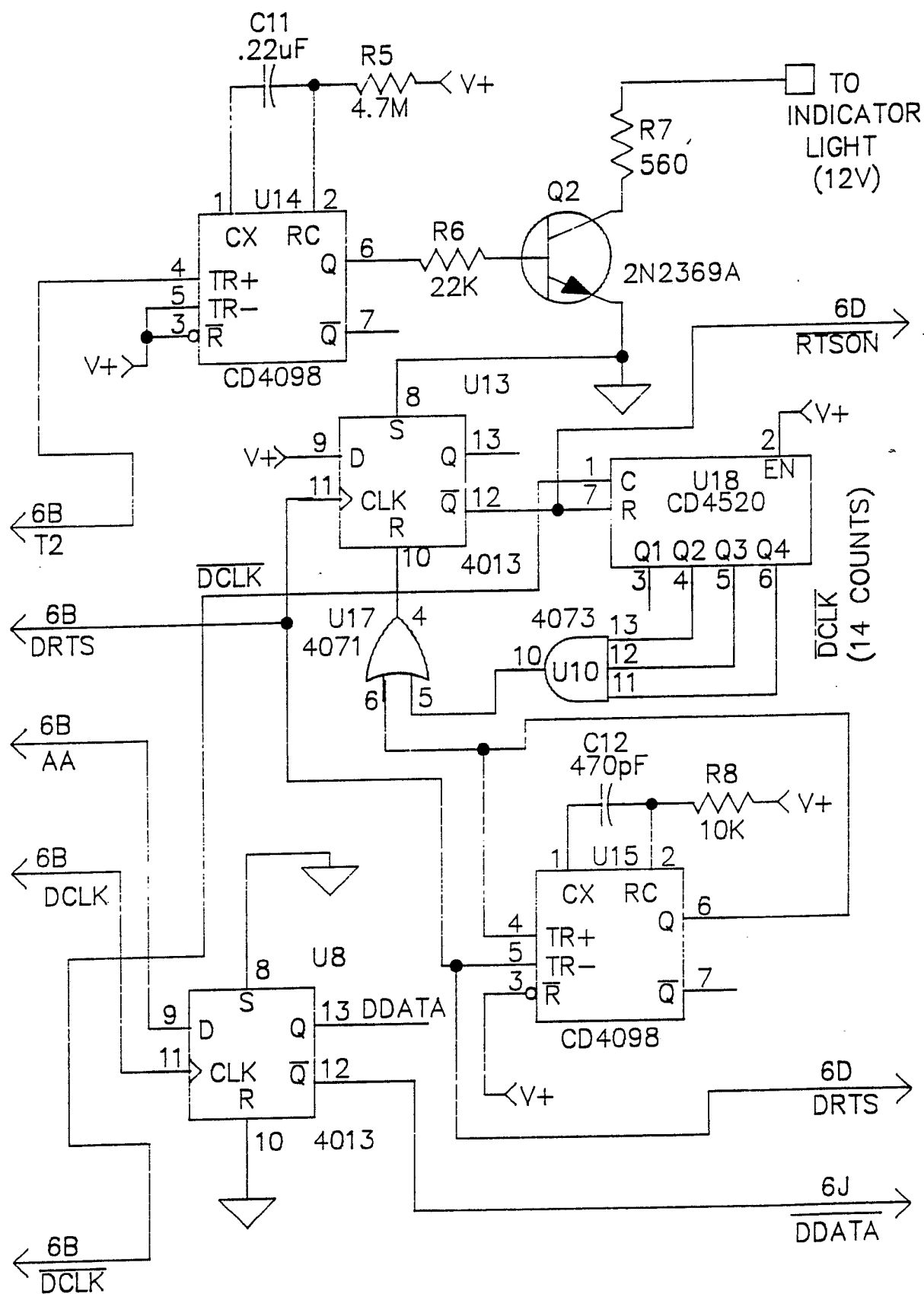
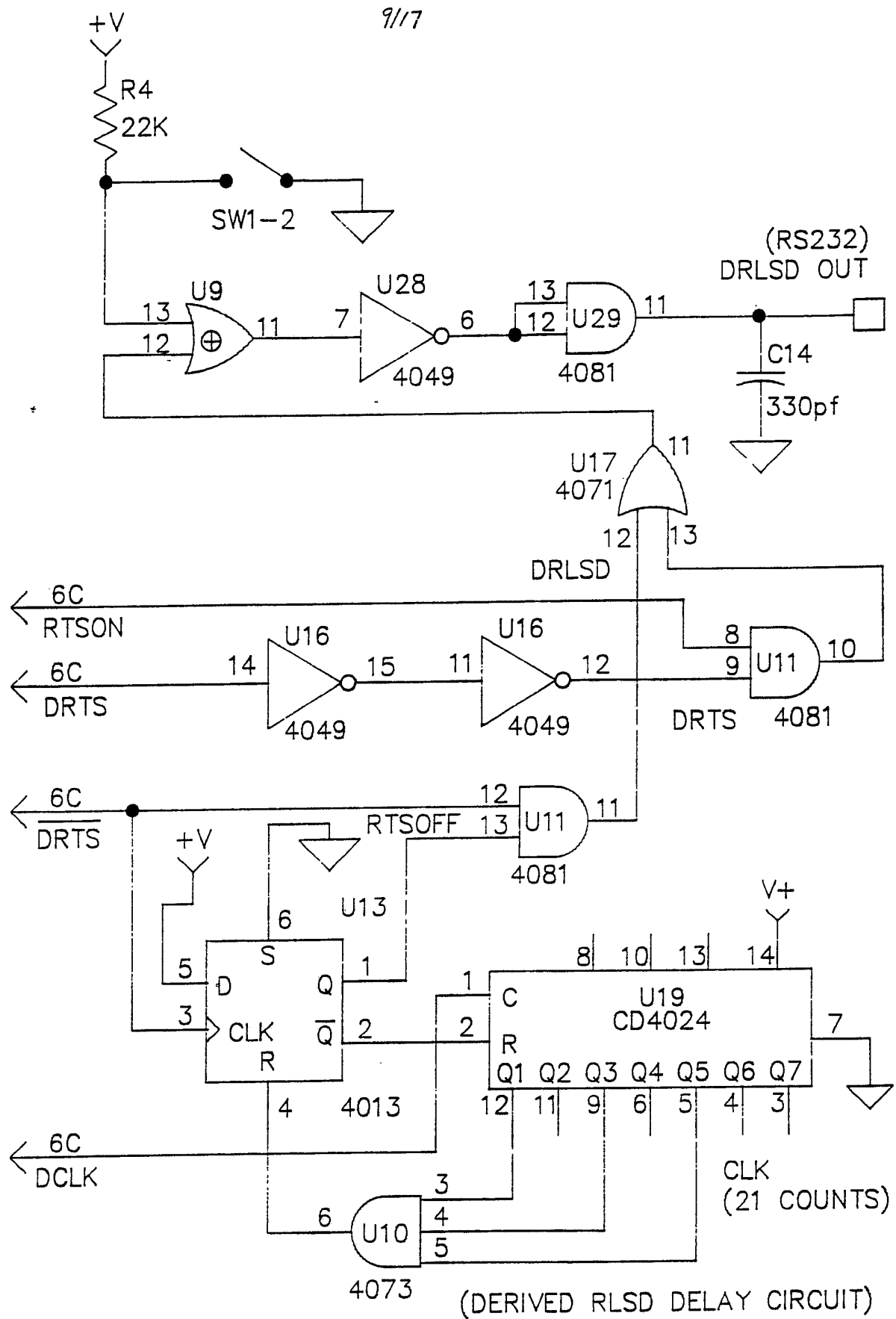


FIGURE 6C

SUBSTITUTE SHEET



SUBSTITUTE SHEET

FIGURE 6D

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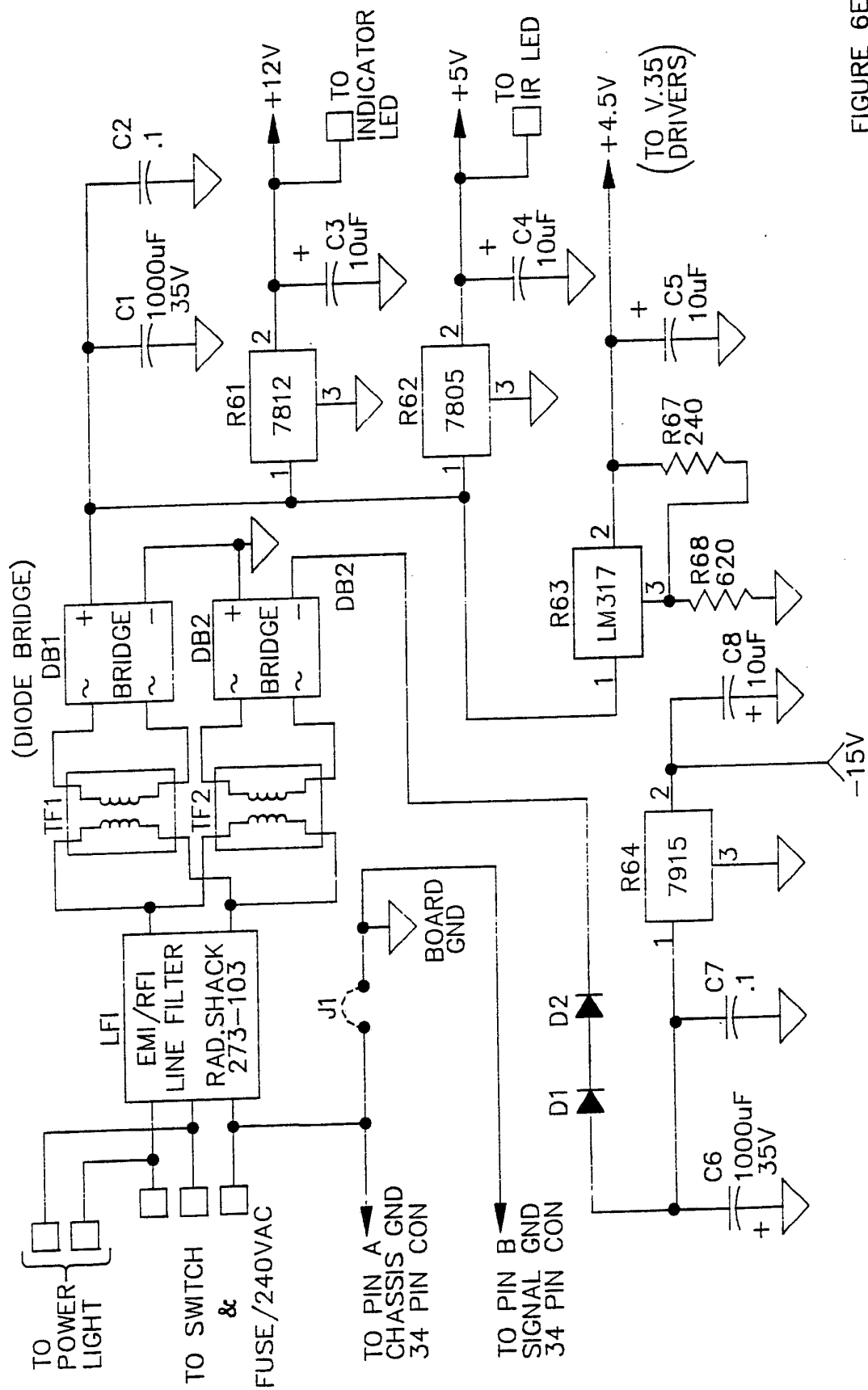


FIGURE 6E

SUBSTITUTE SHEET

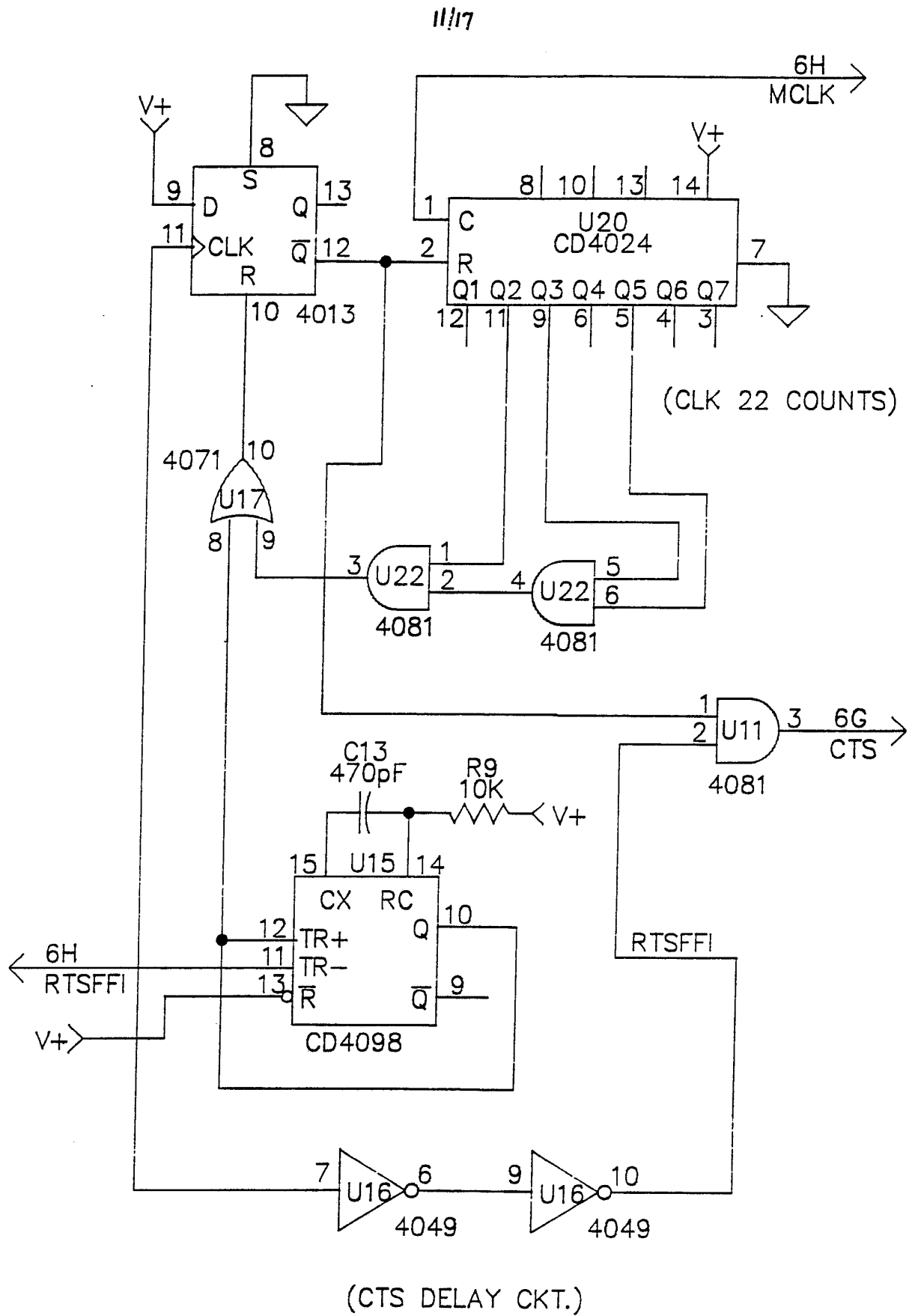


FIGURE 6F

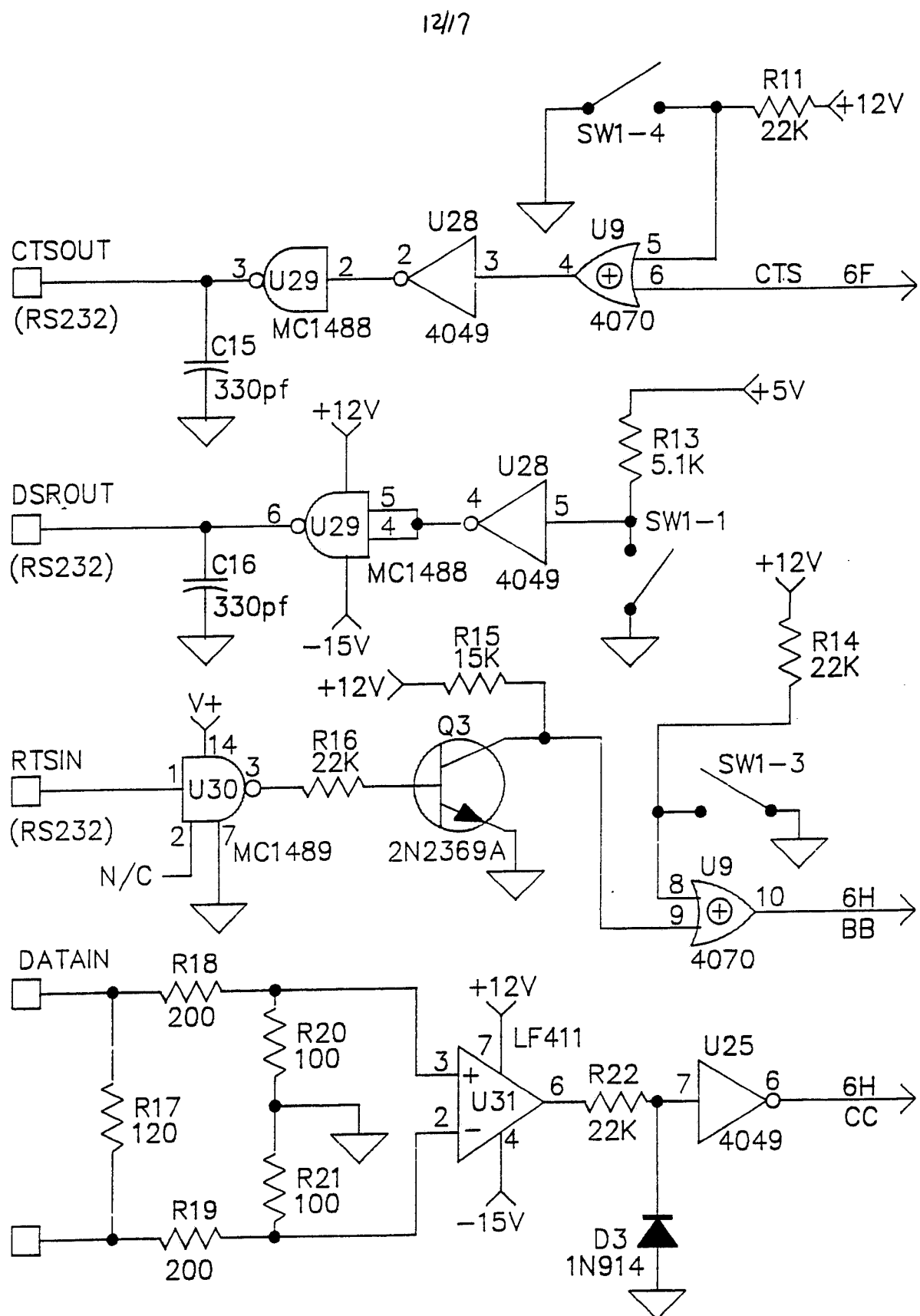


FIGURE 6G

SUBSTITUTE SHEET

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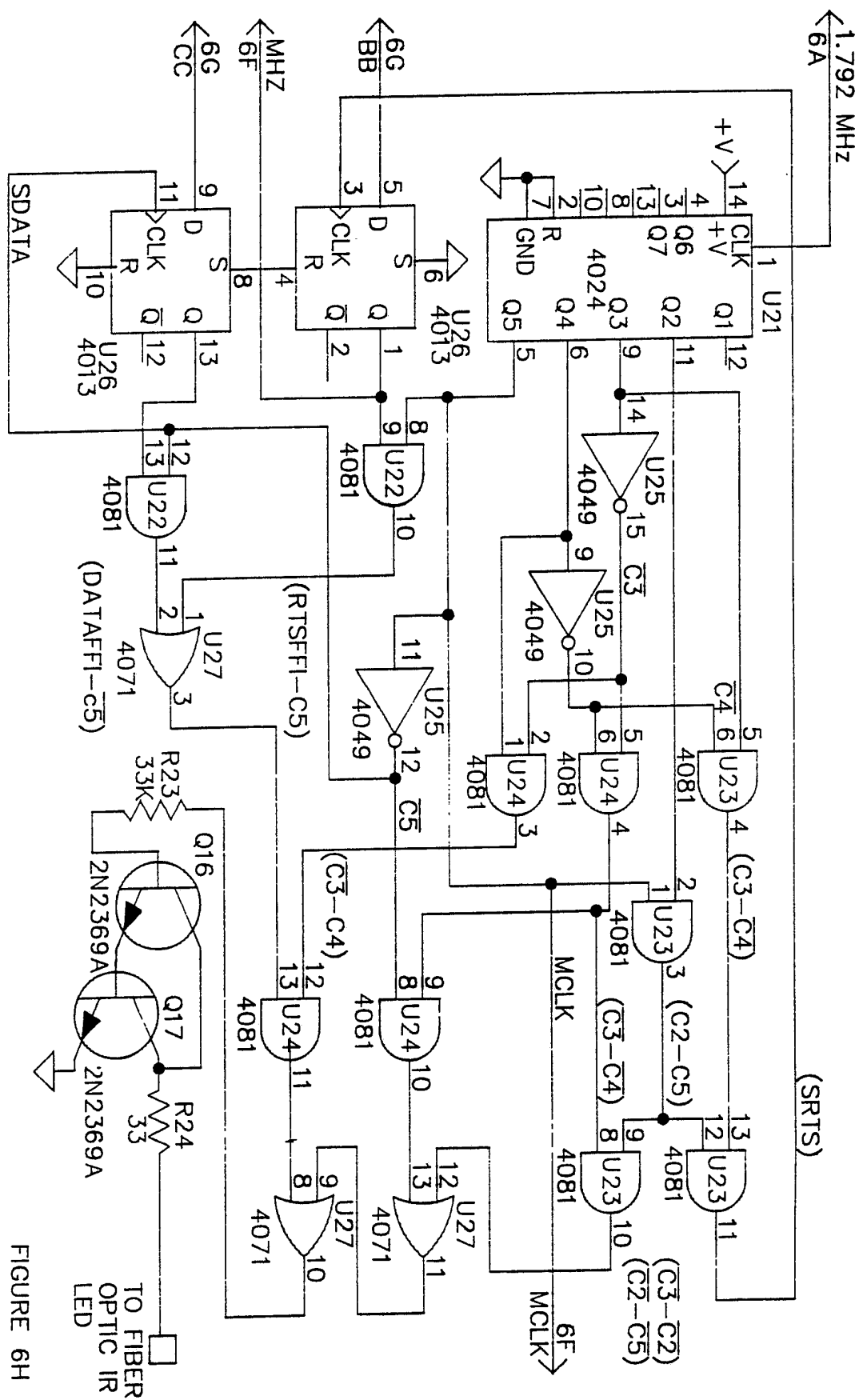


FIGURE 6H

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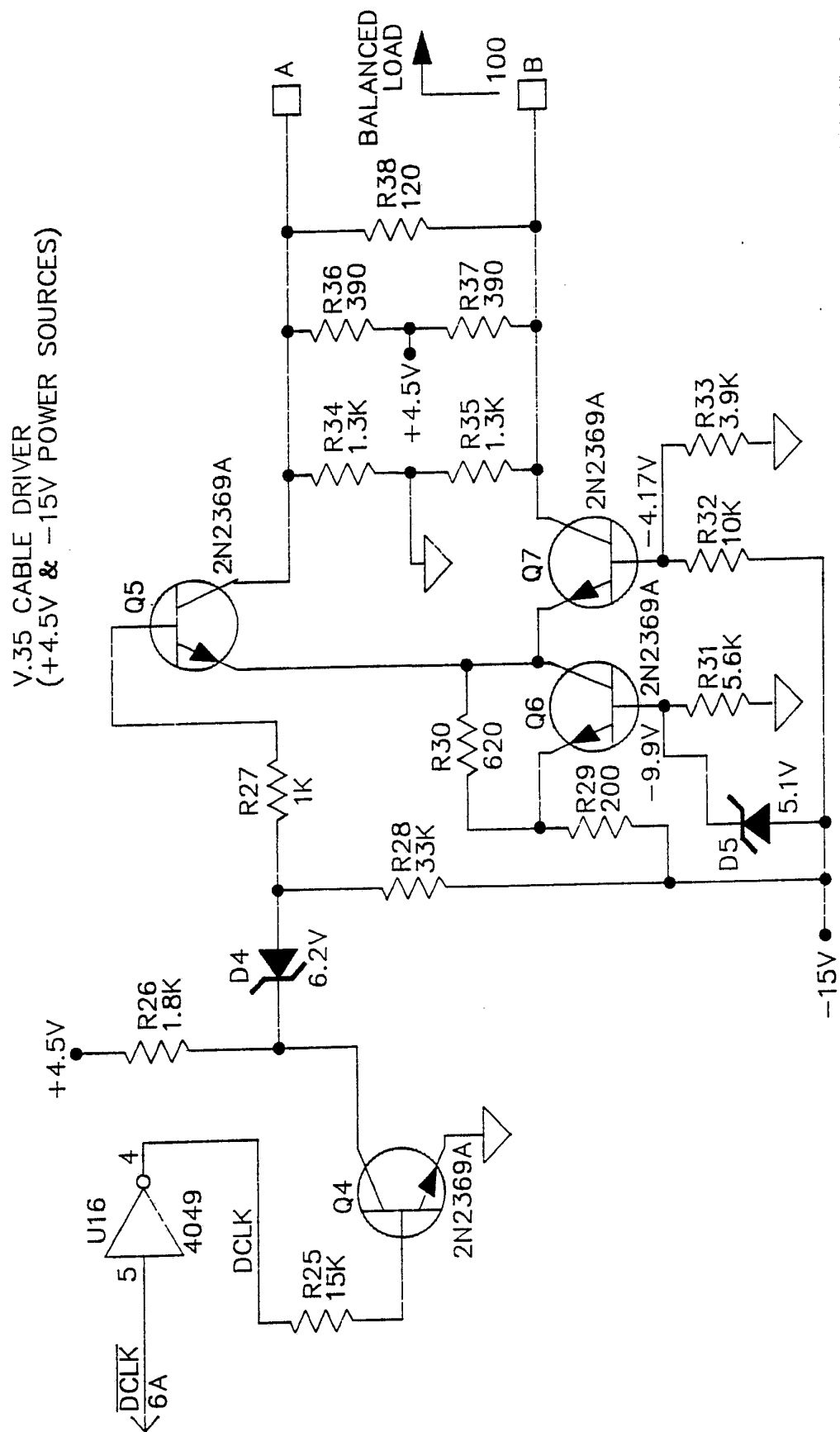


FIGURE 61

SUBSTITUTE SHEET

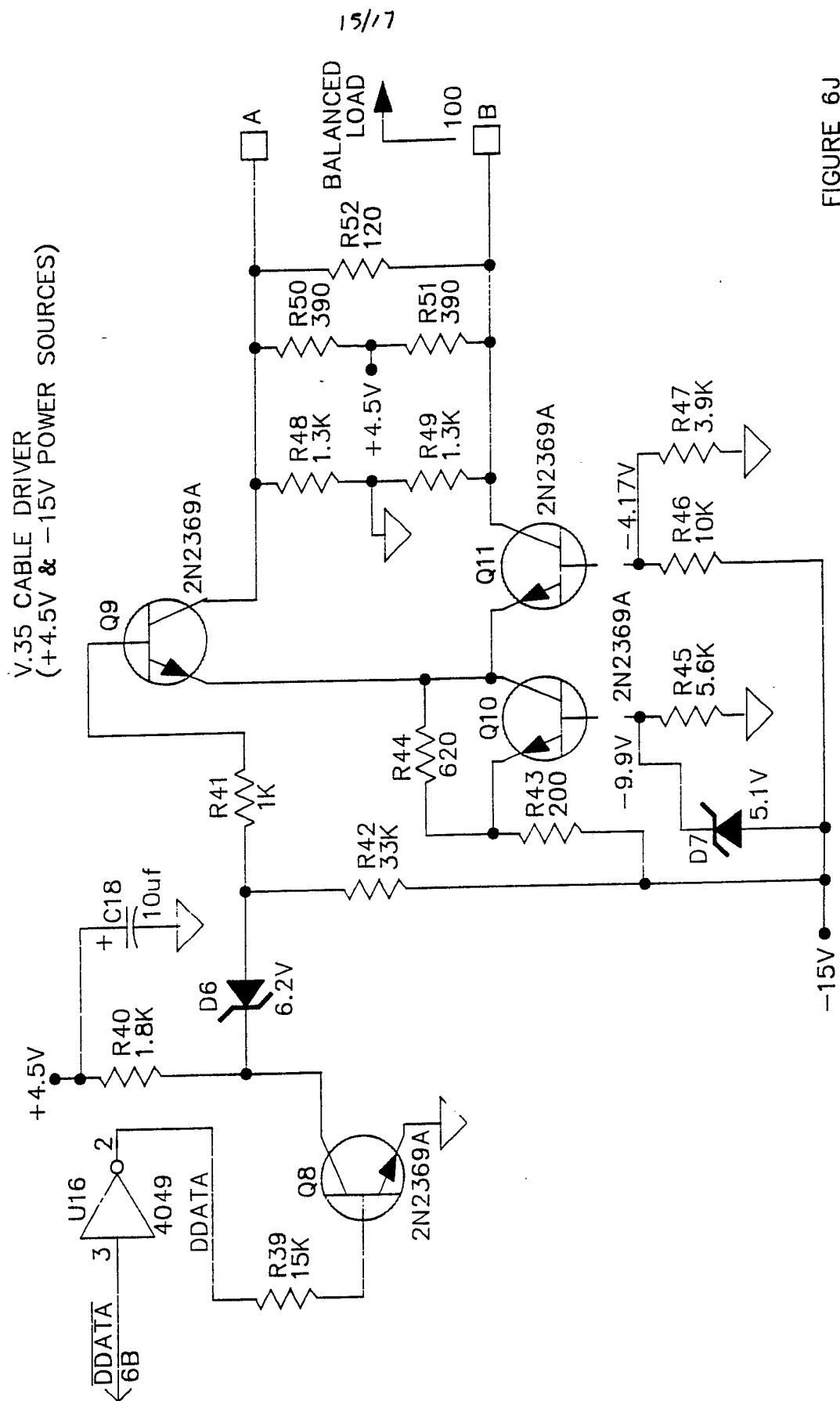


FIGURE 6J

SUBSTITUTE SHEET

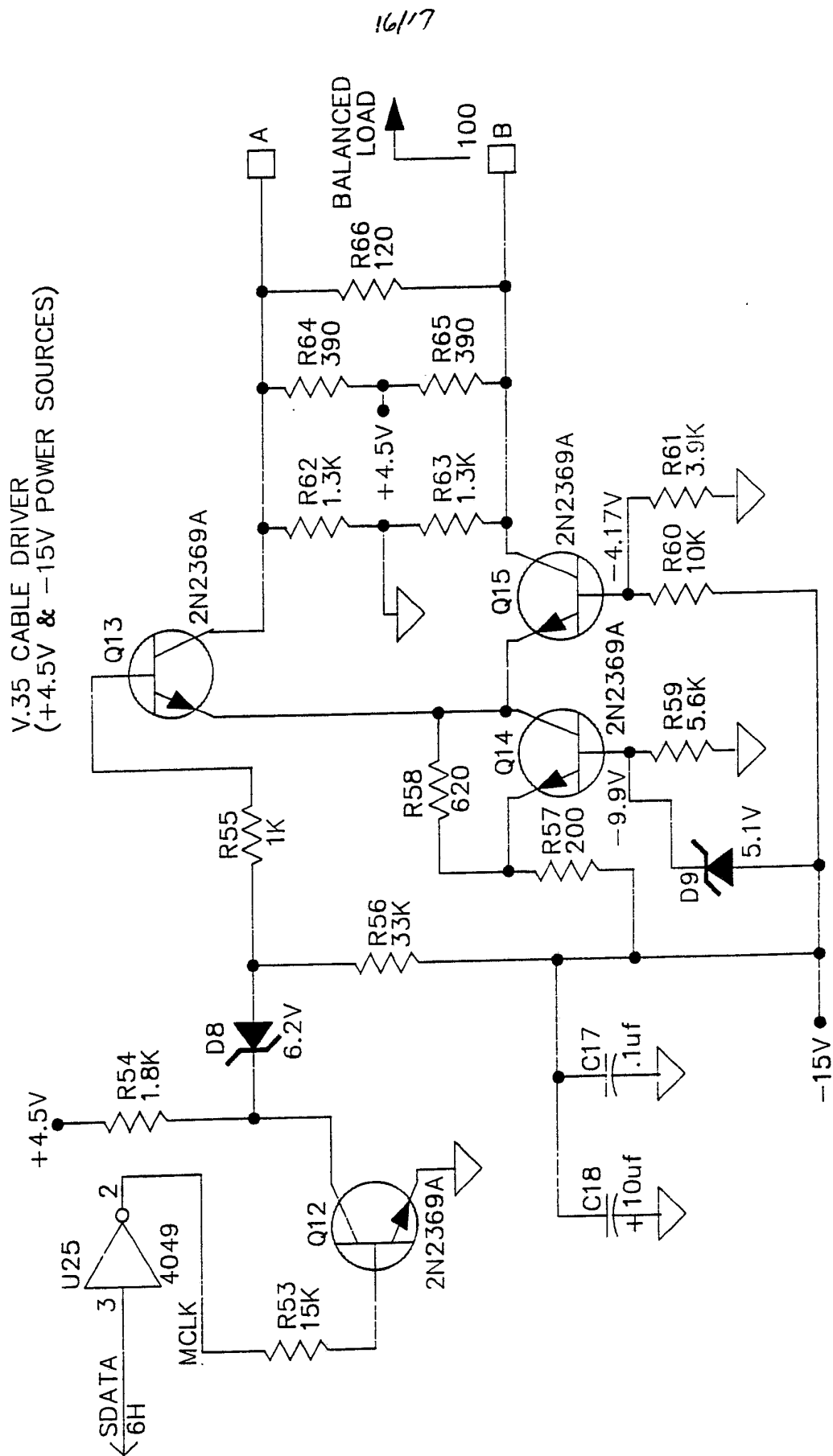


FIGURE 6K

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UNUSED

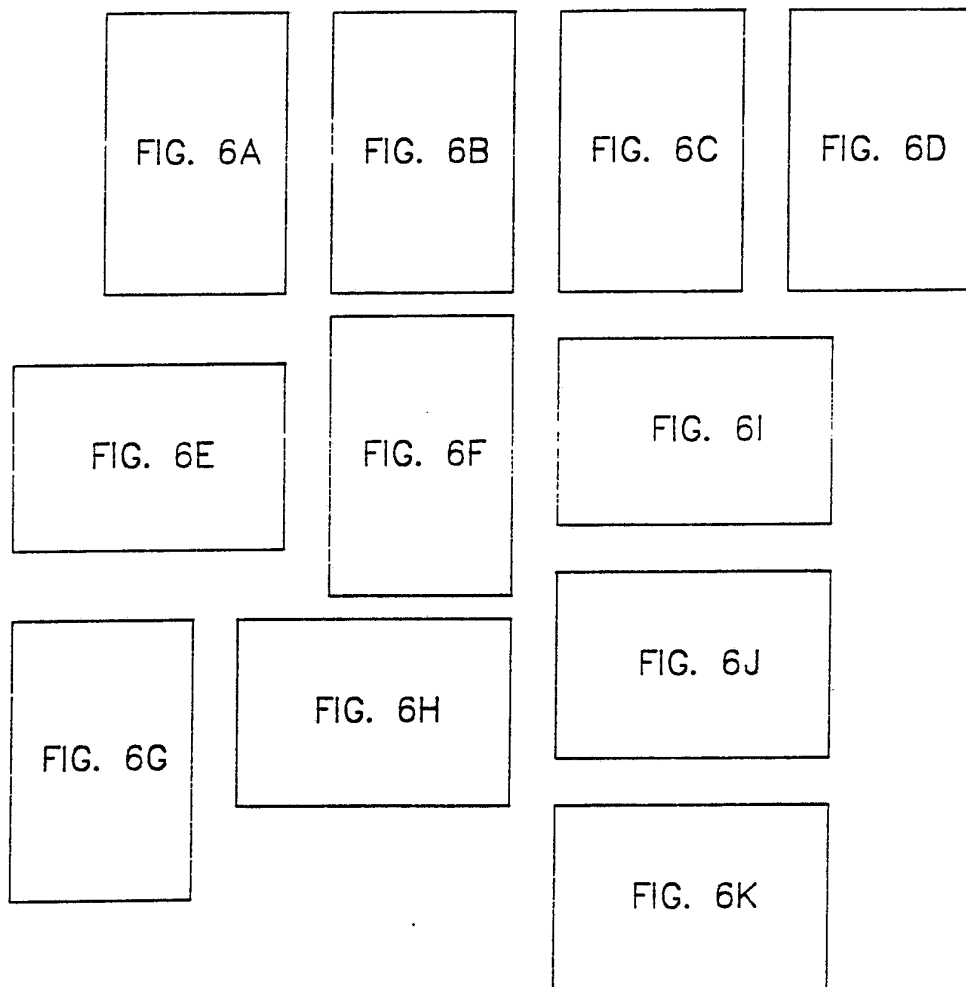
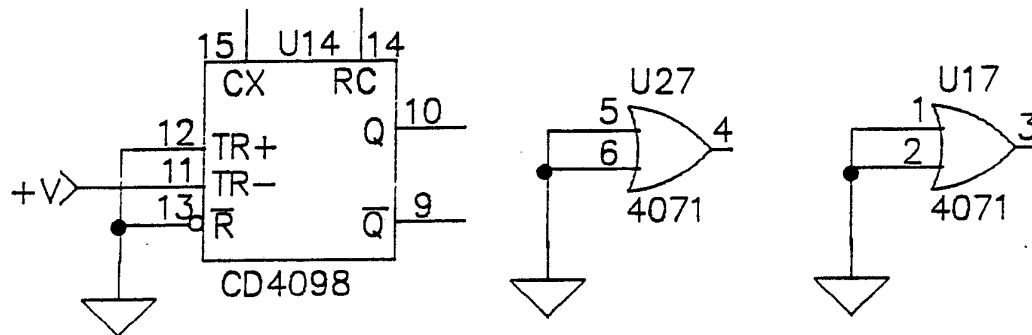


FIGURE 6L

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/01714

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
Int. CL. ⁴ H04L 25/38, 7/06; H04L 5/24, H04J 3/06; H04L 9/00		
U.S. CL. 375/117, 113; 370/48, 106; 380/48		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S. C.L.	375/117,113; 370/48,106; 380/48	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category [*]	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
Y	US, A 3,430,204 Published 25 February 1969 Milford (col. #2, lines 51-72; col. #14, lines 72-75)	1, 15-21
A	US, A 3,662,114 Published 09 May 1972 Clark	1-21
A	US, A 3,742,145 Published 26 June 1973 Clark et al.	1-21
A	US, A 3,798,378 Published 19 March 1974 Epstein	1-21
Y	US, A 3,961,137 Published 01 June 1976 Hutt et al.	1, 15-21
A	US, A 4, 101,732 Published 18 July 1978 Suzuki	1 - 21
A	US, A 4,562,581 Published 31 December 1985 Tanaka et al.	1 - 21
<p>[*] Special categories of cited documents: ¹⁵</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"Δ" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ²	Date of Mailing of this International Search Report ²	
27 September 1987	16 NOV 1987	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	Aaron J. Lewis	