(54) Title: MECHANISM FOR PROVIDING PROGRAM BREAKPOINTS IN A MICROCONTROLLER WITH FLASH PROGRAM MEMORY
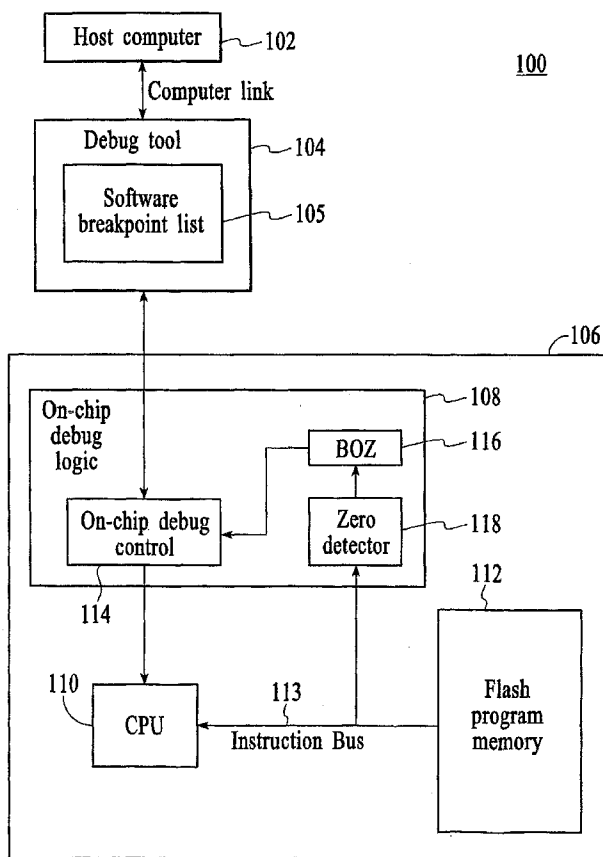
(57) Abstract: A microcontroller is disclosed. The microcontroller includes a central processor unit (CPU) and a Flash program memory in communication with the CPU via an instruction bus. The microcontroller includes an on-chip debug (OCD) logic coupled to the CPU. The OCD logic containing logic that detects a zero opcode on an instruction bus between the CPU and the Flash program memory to provide a program breakpoint. This is an advantage over prior art in that any number of such breakpoints can be inserted into the Flash program memory, without requiring the memory to be erased. A system and method in accordance with the present invention provides a vastly improved support for program breakpoints in Flash program memory-based microcontrollers with a minimum increase in on-chip debug logic and complexity.

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
21 December 2007

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8): G06F 11/00 (2007.01)
USPC: 714/35
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): G06F 11/00 (2007.01)
USPC: 714/35

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): G06F 9/44, G11C 8/00, H02H 3/05, H04L 1/22
USPC: 365/238.5, 365/230.03, 365/185.11, 717/129, 717/130

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWest (USPB, USPT, USOC, EPAB, JPAB), DialogPro, GoogleScholar; software breakpoint debug debugging microcontroller non-volatile flash memory processor CPU opcode zero flag list instruction bus module method system

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,798,713 B1 (Yearsley et al.), 28 September 2004 (28.09.2004), Figs. 1-3	1-3, 6-7, 10-12 ------- 4, 5, 8, 9, 13, 14
Y	US 2004/0168155 A1 (O'Farrell et al.), 26 August 2004 (26.08.2004), Figs. 7-8	4, 8, 13
Y	US 2004/0059961 A1 (Jentsch et al.), 25 March 2004 (25.03.2004), Figs. 1-2	5, 9, 14

☐ Further documents are listed in the continuation of Box C. ☐

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
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"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 July 2007 (05.07.2007)	**2 9 OCT 2007**

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